

MPSW05, MPSW06

One Watt Amplifier Transistors

NPN Silicon

Features

- Pb-Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit	
Collector - Emitter Voltage	MPSW05 MPSW06	V_{CEO}	60 80	Vdc
Collector - Base Voltage	MPSW05 MPSW06	V_{CBO}	60 80	Vdc
Emitter - Base Voltage		V_{EBO}	4.0	Vdc
Collector Current - Continuous		I_C	500	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C		P_D	1.0 8.0	W mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C		P_D	2.5 20	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range		T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	125	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	50	$^\circ\text{C}/\text{W}$

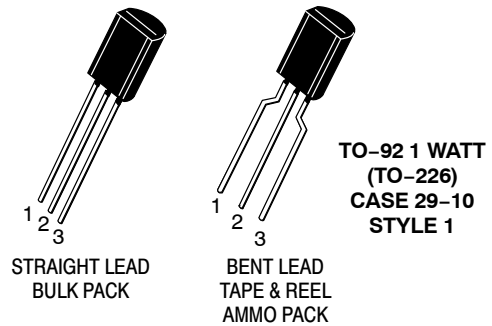
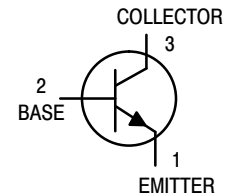
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

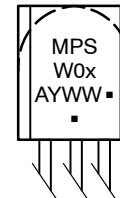


ON Semiconductor®

<http://onsemi.com>



MARKING DIAGRAM



- x = 5 or 6
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MPSW05G	TO-92 (Pb-Free)	5000 Units/Bulk
MPSW06G	TO-92 (Pb-Free)	5000 Units/Bulk
MPSW06RLRA	TO-92	2000/Tape & Reel
MPSW06RLRAG	TO-92 (Pb-Free)	2000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MPSW05, MPSW06

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector - Emitter Breakdown Voltage (Note 1) ($I_C = 1.0\text{ mAdc}$, $I_B = 0$)	$V_{(BR)CEO}$	60 80	- -	Vdc
Emitter - Base Breakdown Voltage ($I_E = 100\ \mu\text{Adc}$, $I_C = 0$)	$V_{(BR)EBO}$	4.0	-	Vdc
Collector Cutoff Current ($V_{CE} = 40\text{ Vdc}$, $I_B = 0$) ($V_{CE} = 60\text{ Vdc}$, $I_B = 0$)	I_{CES}	- -	0.5 0.5	μAdc
Collector Cutoff Current ($V_{CB} = 40\text{ Vdc}$, $I_E = 0$) ($V_{CB} = 60\text{ Vdc}$, $I_E = 0$)	I_{CBO}	- -	0.1 0.1	μAdc
Emitter Cutoff Current ($V_{EB} = 3.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	-	0.1	μAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain ($I_C = 50\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 250\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	80 60	- -	-
Collector - Emitter Saturation Voltage ($I_C = 250\text{ mAdc}$, $I_B = 10\text{ mAdc}$)	$V_{CE(sat)}$	-	0.4	Vdc
Base - Emitter Saturation Voltage ($I_C = 250\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$)	$V_{BE(sat)}$	-	1.2	Vdc
SMALL - SIGNAL CHARACTERISTICS				
Current - Gain - Bandwidth Product ($I_C = 200\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$, $f = 20\text{ MHz}$)	f_T	50	-	MHz
Output Capacitance ($V_{CB} = 10\text{ V}$, $f = 1.0\text{ MHz}$)	C_{obo}	-	12	pF

1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

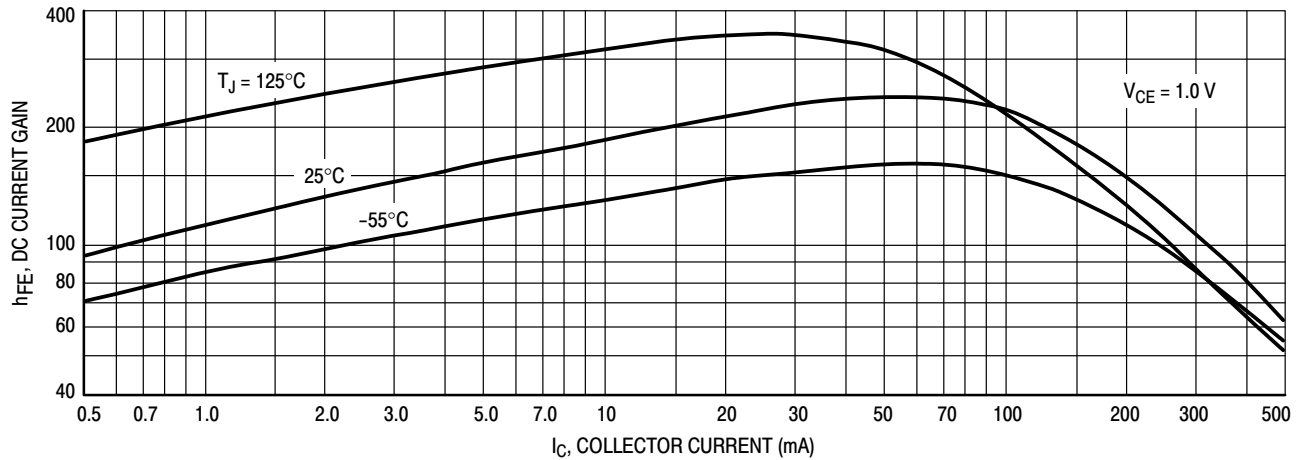


Figure 1. DC Current Gain

MPSW05, MPSW06

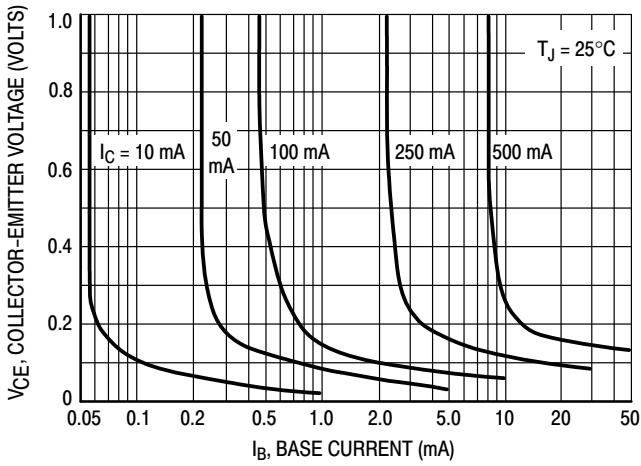


Figure 2. Collector Saturation Region

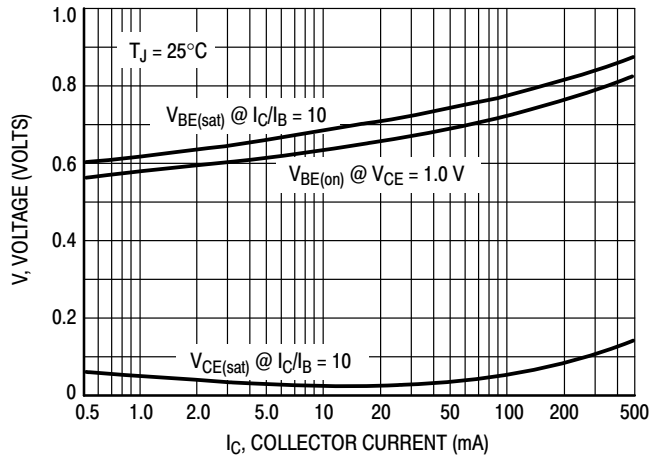


Figure 3. "On" Voltages

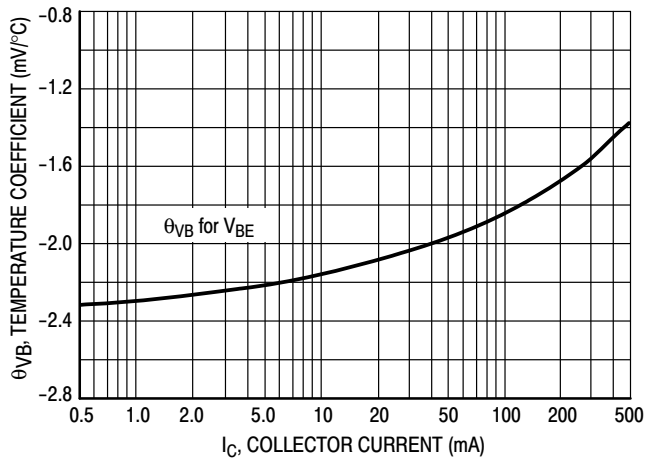


Figure 4. Base-Emitter Temperature Coefficient

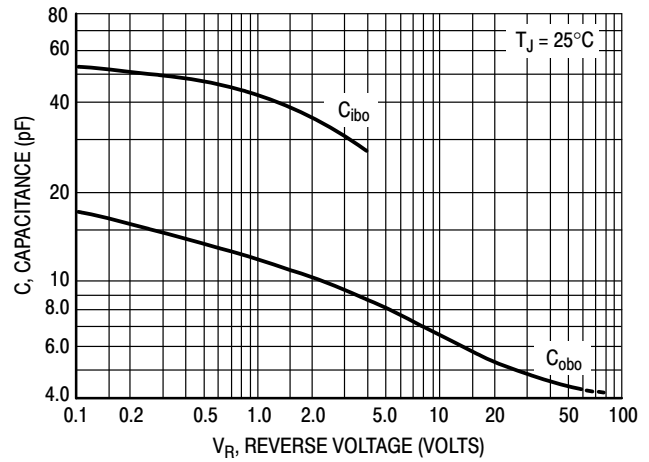


Figure 5. Capacitance

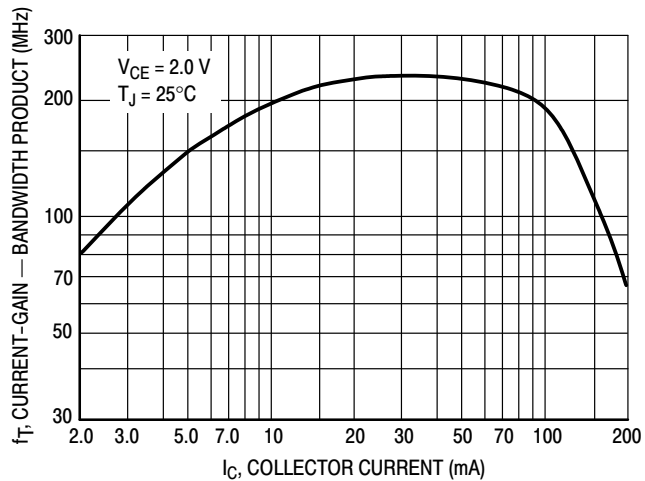


Figure 6. Current-Gain - Bandwidth Product

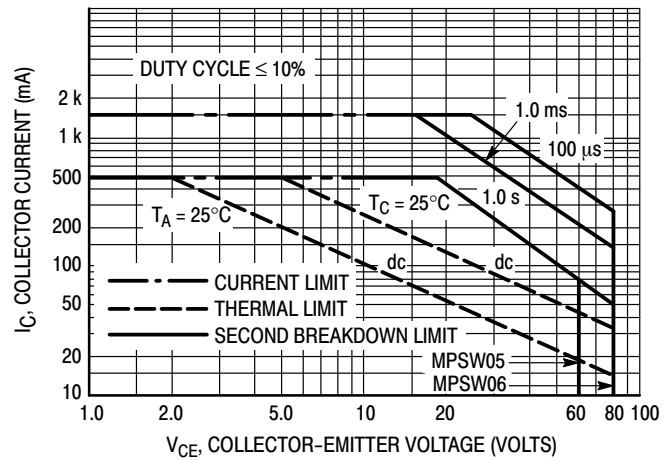
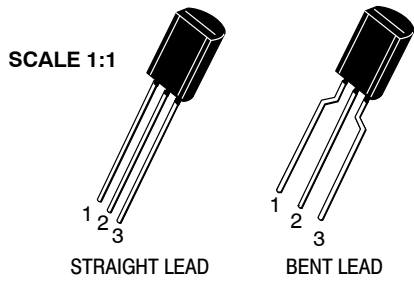


Figure 7. Active Region - Safe Operating Area

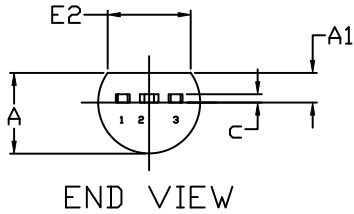
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-92 (TO-226) 1 WATT	PAGE 1 OF 3

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

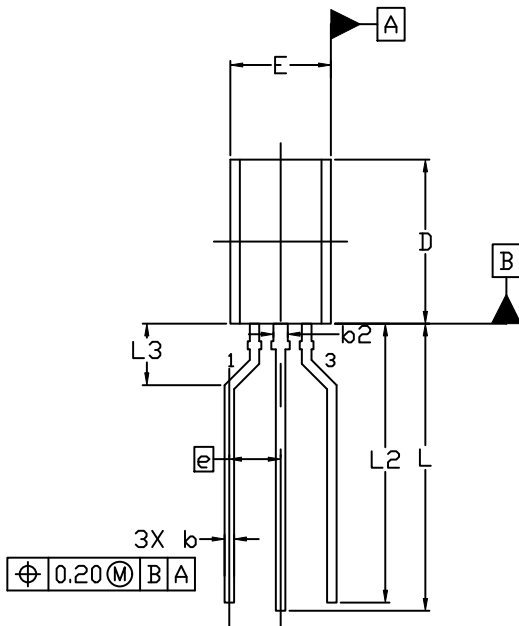
TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD



END VIEW



TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-92 (TO-226) 1 WATT	PAGE 2 OF 3

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

**TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D**

DATE 05 MAR 2021

- | | | | | |
|---|--|--|---|---|
| STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR | STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE | STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE | STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE |
| STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN | STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE | STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE | STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2 | STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE |
| STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE | STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2 | STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2 | STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE | STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2 |
| STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE | STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER | STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED | STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE | STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE |
| STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE | STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN | STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN | STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE | STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2 |
| STYLE 26:
PIN 1. V _{CC}
2. GROUND 2
3. OUTPUT | STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT | STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE | STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE | STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE |
| STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE | STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER | STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT | STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC | STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER |

**GENERIC
MARKING DIAGRAM***



- XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON52857E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-92 (TO-226) 1 WATT	PAGE 3 OF 3

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales