

NVD5484NL

Power MOSFET

60 V, 17 mΩ, 54 A, Single N-Channel
Logic Level, DPAK

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | Symbol | Value | Unit | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|---------------------------|------------------|---|
| Drain-to-Source Voltage | V_{DSS} | 60 | V | |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3) | Steady State | $T_C = 25^\circ\text{C}$ | 54 | A |
| | | $T_C = 100^\circ\text{C}$ | 38 | |
| Power Dissipation $R_{\theta JC}$ (Note 1) | Steady State | $T_C = 25^\circ\text{C}$ | 100 | W |
| | | $T_C = 100^\circ\text{C}$ | 50 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3) | Steady State | $T_A = 25^\circ\text{C}$ | 10.7 | A |
| | | $T_A = 100^\circ\text{C}$ | 7.6 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1 & 2) | Steady State | $T_A = 25^\circ\text{C}$ | 3.9 | W |
| | | $T_A = 100^\circ\text{C}$ | 2.0 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} | 305 | A |
| Current Limited by Package (Note 3) | $T_A = 25^\circ\text{C}$ | $I_{Dmaxpkg}$ | 60 | A |
| Operating Junction and Storage Temperature | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | I_S | 83 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, V_{DD} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{L(pk)} = 50 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$) | E_{AS} | 125 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---------------------------------------------|-----------------|-------|---------------------------|
| Junction-to-Case - Steady State (Drain) | $R_{\theta JC}$ | 1.5 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient - Steady State (Note 2) | $R_{\theta JA}$ | 38 | |

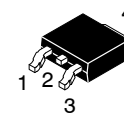
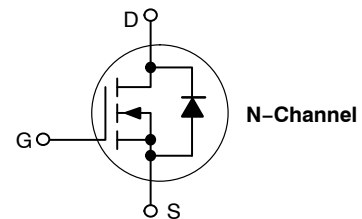
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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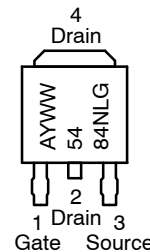
www.onsemi.com

| $V_{(BR)DSS}$ | $R_{DS(on)}$ | I_D |
|---------------|---------------|-------|
| 60 V | 17 mΩ @ 10 V | 54 A |
| | 23 mΩ @ 4.5 V | |



DPAK
CASE 369AA
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENT



- A = Assembly Location*
- Y = Year
- WW = Work Week
- 5484NL = Device Code
- G = Pb-Free Package

* The Assembly Location Code (A) is front side optional. In cases where the Assembly Location is stamped in the package bottom (molding ejector pin), the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NVD5484NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|-----------------------------------|----------------------|--------------------------------------------------|------------------------|--|------|----|
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 60 | | | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 60 V | T _J = 25°C | | 1.0 | μA |
| | | | T _J = 125°C | | 10 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = ±20 V | | | ±100 | nA |

ON CHARACTERISTICS (Note 4)

| | | | | | | |
|-------------------------------|---------------------|-------------------------------------------------------------|-----|------|-----|----|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 250 μA | 1.5 | 1.9 | 2.5 | V |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V, I _D = 25 A | | 13.5 | 17 | mΩ |
| | | V _{GS} = 4.5 V, I _D = 25 A | | 18 | 23 | |
| Forward Transconductance | g _{FS} | V _{DS} = 15 V, I _D = 20 A | | 41 | | S |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|---------------------|--------------------------------------------------------------------------|-------------------------|------|--|----|
| Input Capacitance | C _{iss} | V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V | | 1410 | | pF |
| Output Capacitance | C _{oss} | | | 315 | | |
| Reverse Transfer Capacitance | C _{rss} | | | 135 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{DS} = 48 V, I _D = 23 A | V _{GS} = 4.5 V | 27 | | nC |
| | | | V _{GS} = 10 V | 48 | | |
| Threshold Gate Charge | Q _{G(TH)} | V _{GS} = 10 V, V _{DS} = 48 V, I _D = 23 A | | 0.9 | | |
| Gate-to-Source Charge | Q _{GS} | | | 4.4 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 19 | | |
| Gate Resistance | R _G | | | 8.5 | | |

SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---------------------|---------------------|--------------------------------------------------------------------------------------------------|--|-----|--|----|
| Turn-On Delay Time | t _{d(on)} | V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 23 A, R _G = 10 Ω | | 18 | | ns |
| Rise Time | t _r | | | 160 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 100 | | |
| Fall Time | t _f | | | 110 | | |
| Turn-On Delay Time | t _{d(on)} | V _{GS} = 10 V, V _{DS} = 48 V, I _D = 23 A, R _G = 10 Ω | | 7.8 | | |
| Rise Time | t _r | | | 45 | | |
| Turn-Off Delay Time | t _{d(off)} | | | 152 | | |
| Fall Time | t _f | | | 113 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | |
|-------------------------|-----------------|---------------------------------------------------------------------------------|------------------------|-----|-----|----|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 25 A | T _J = 25°C | 0.9 | 1.2 | V |
| | | | T _J = 125°C | 0.8 | | |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 23 A | | 64 | | ns |
| Charge Time | t _a | | | 33 | | |
| Discharge Time | t _b | | | 31 | | |
| Reverse Recovery Charge | Q _{RR} | | | 118 | | |

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

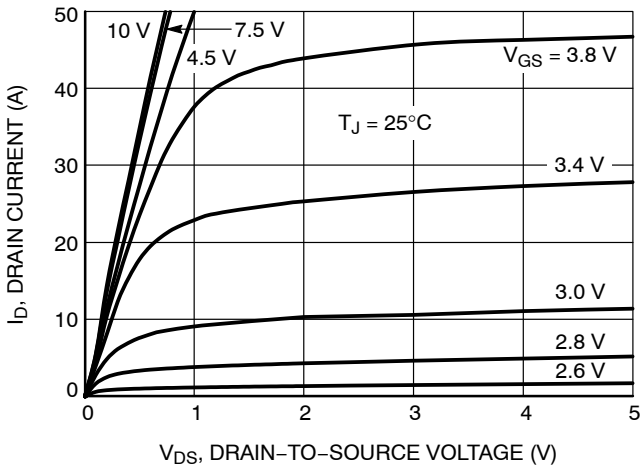


Figure 1. On-Region Characteristics

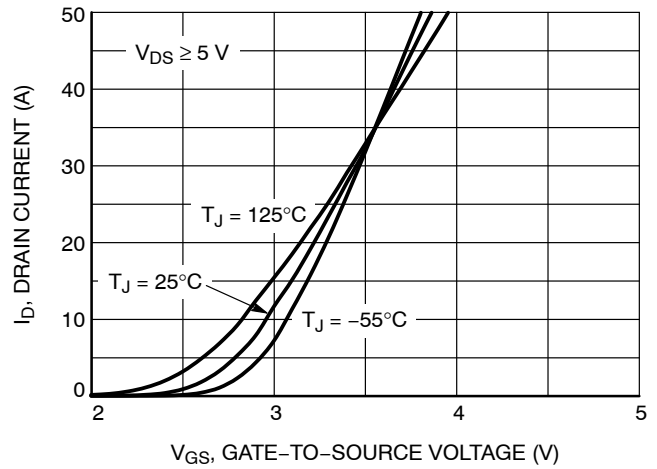


Figure 2. Transfer Characteristics

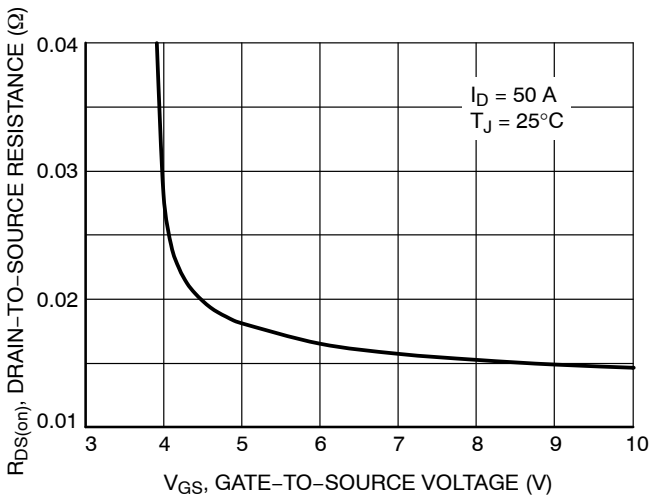


Figure 3. On-Resistance vs. Gate-to-Source Voltage

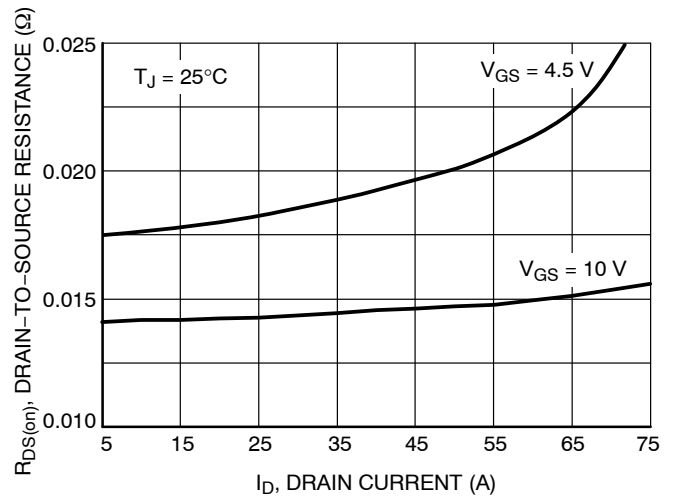


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

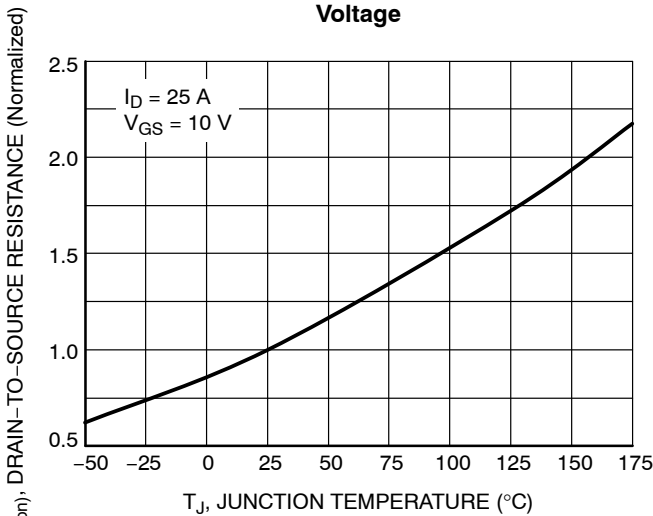


Figure 5. On-Resistance Variation with Temperature

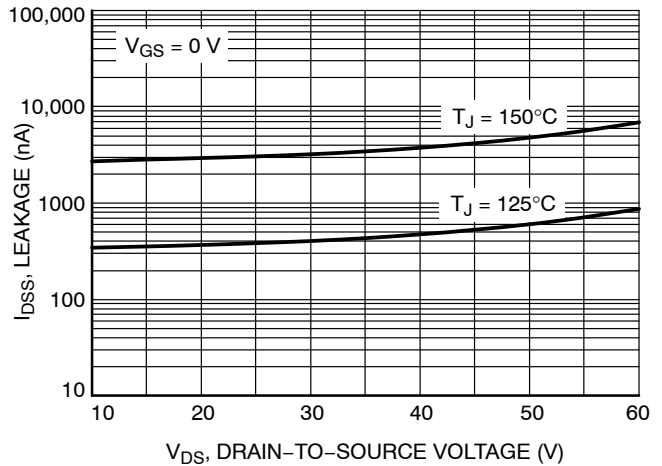


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

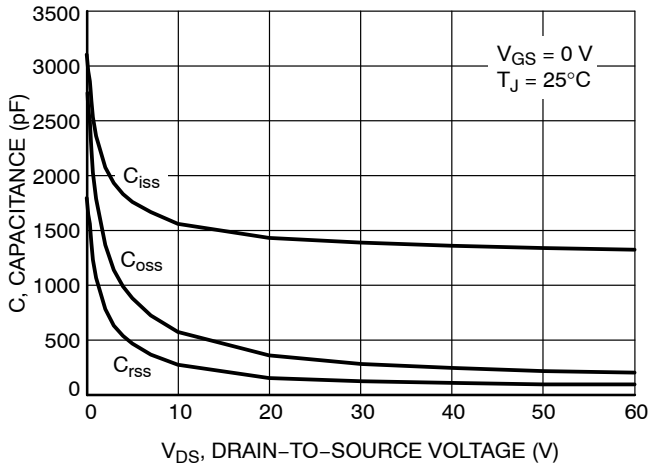


Figure 7. Capacitance Variation

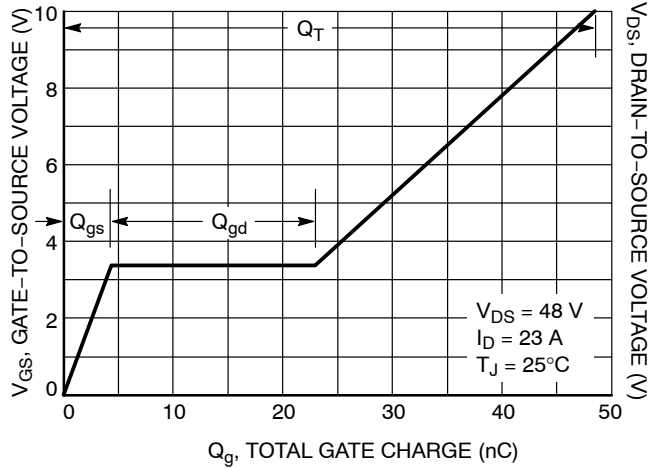


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

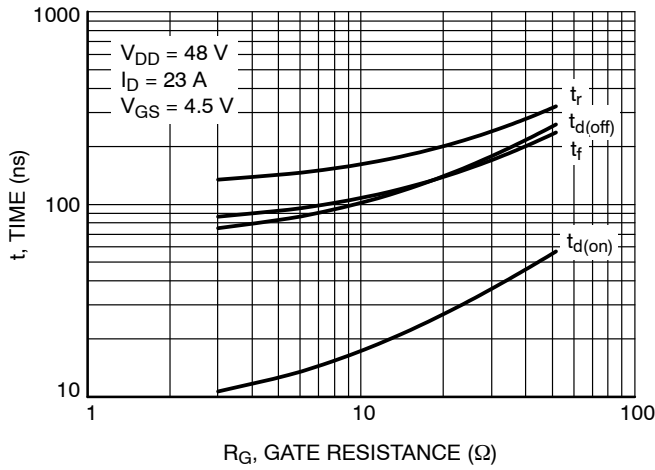


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

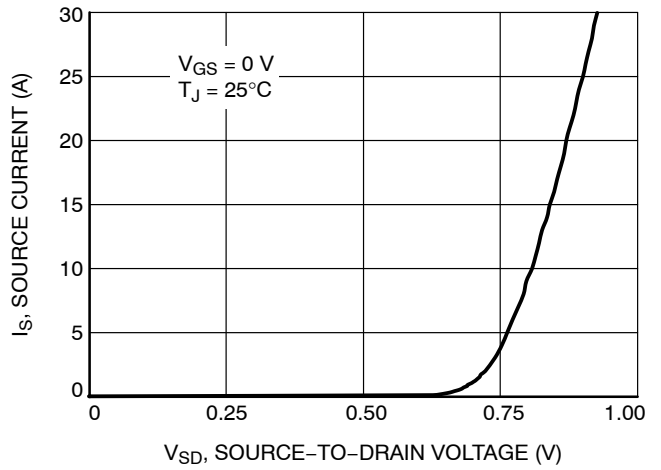


Figure 10. Diode Forward Voltage vs. Current

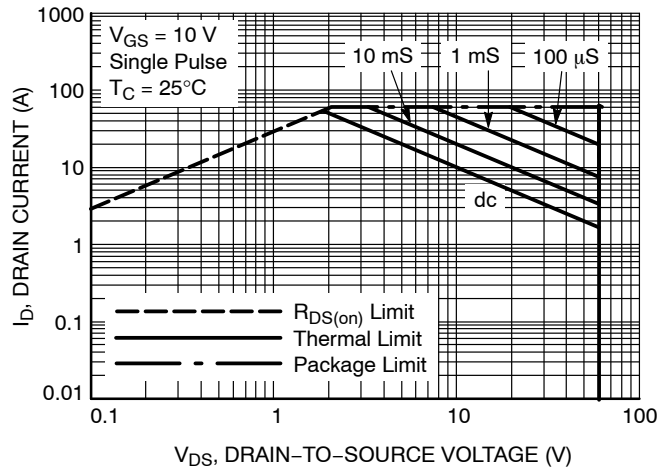


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NVD5484NL

TYPICAL CHARACTERISTICS

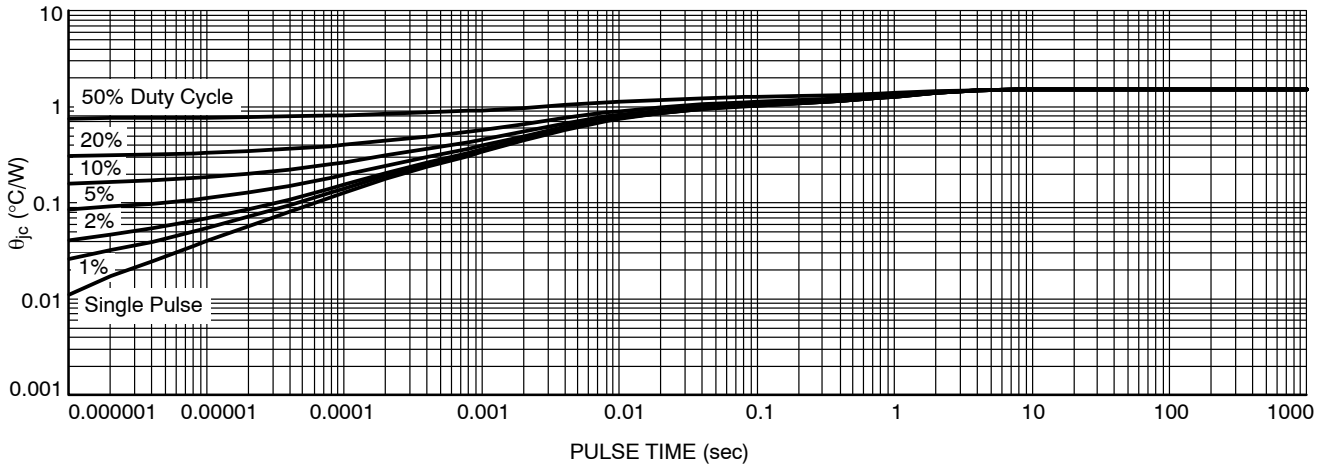


Figure 12. Thermal Response

ORDERING INFORMATION

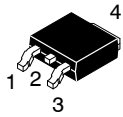
| Order Number | Package | Shipping [†] |
|-------------------|-------------------|-----------------------|
| NVD5484NLT4G | DPAK (Pb-Free) | 2500 / Tape & Reel |
| NVD5484NLT4G-VF01 | DPAK (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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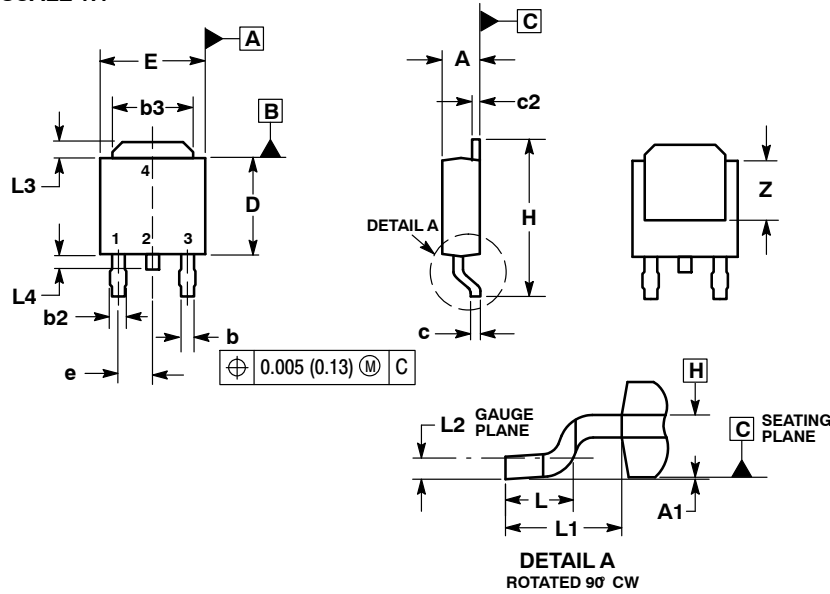
SCALE 1:1

DPAK (SINGLE GAUGE)

CASE 369AA-01

ISSUE B

DATE 03 JUN 2010



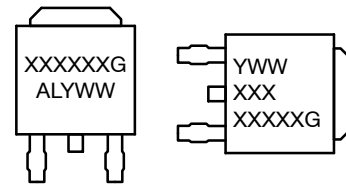
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

- | | | | |
|----------------------------------------------------------------------------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------|--------------------------------------------------------------------------|
| <p>STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR</p> | <p>STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN</p> | <p>STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE</p> | <p>STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE</p> |
| <p>STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE</p> | <p>STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2</p> | <p>STYLE 7: PIN 1. GATE 2. ANODE 3. EMITTER 4. COLLECTOR</p> | |

GENERIC MARKING DIAGRAM*

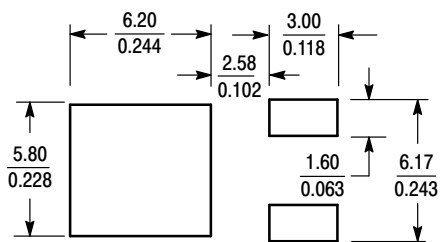


IC Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
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