



74HC3G14; HCT3G14

Triple inverting Schmitt trigger

Rev. 7 — 18 December 2023

Product data sheet

1. General description

The 74HC3G14; 74HCT3G14 is a triple inverter with Schmitt-trigger inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} . Schmitt trigger inputs transform slowly changing input signals into sharply defined jitter-free output signals.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - For 74HC3G14: CMOS level
 - For 74HCT3G14: TTL level
- CMOS low power dissipation
- High noise immunity
- Unlimited input rise and fall times
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Wave and pulse shaper for highly noisy environments
- Astable multivibrators
- Monostable multivibrators

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC3G14DP 74HCT3G14DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HC3G14DC 74HCT3G14DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

5. Marking

Table 2. Marking

Type number	Marking code [1]
74HC3G14DP	H14
74HCT3G14DP	T14
74HC3G14DC	H14
74HCT3G14DC	T14

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

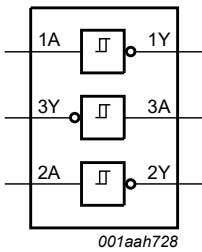


Fig. 1. Logic symbol

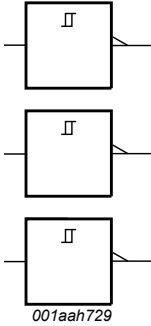


Fig. 2. IEC logic symbol

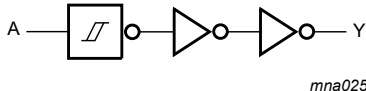
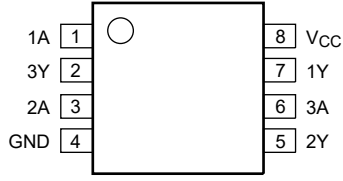


Fig. 3. Logic diagram (one Schmitt trigger)

7. Pinning information

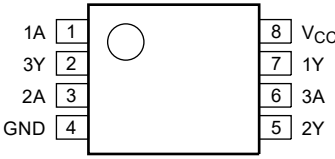
7.1. Pinning

**DP package
SOT505-2 (TSSOP8)**



aaa-035929

**DC package
SOT765-1 (VSSOP8)**



aaa-037225

7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V _{CC}	8	supply voltage

8. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input	Output
nA	nY
L	H
H	L

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $V_{CC} + 0.5\text{ V}$ [1]	-	± 25	mA
I_{CC}	supply current	[1]	-	+50	mA
I_{GND}	ground current	[1]	-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

10. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC3G14			74HCT3G14			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C

11. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at $T_{amb} = 25\text{ °C}$.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC3G14										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_O = -4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	4.18	4.32	-	4.13	-	3.7	-	V
		$I_O = -5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$	5.68	5.81	-	5.63	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{CC}	supply current	per input pin; $V_{CC} = 6.0\text{ V}$; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	-	1.0	-	10	-	20	μA
C_I	input capacitance		-	2.0	-	-	-	-	-	pF
74HCT3G14										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	4.18	4.32	-	4.13	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5\text{ V}$	-	-	± 0.1	-	± 1.0	-	± 1.0	μA
I_{CC}	supply current	per input pin; $V_{CC} = 5.5\text{ V}$; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	-	1.0	-	10	-	20	μA
ΔI_{CC}	additional supply current	per input; $V_{CC} = 4.5\text{ V}$ to 5.5 V ; $V_I = V_{CC} - 2.1\text{ V}$; $I_O = 0\text{ A}$	-	-	300	-	375	-	410	μA
C_I	input capacitance		-	2.0	-	-	-	-	-	pF

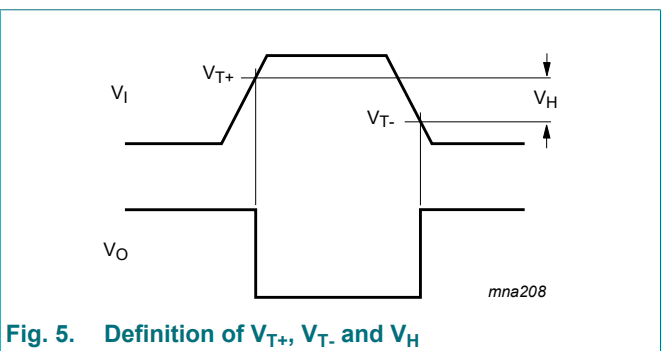
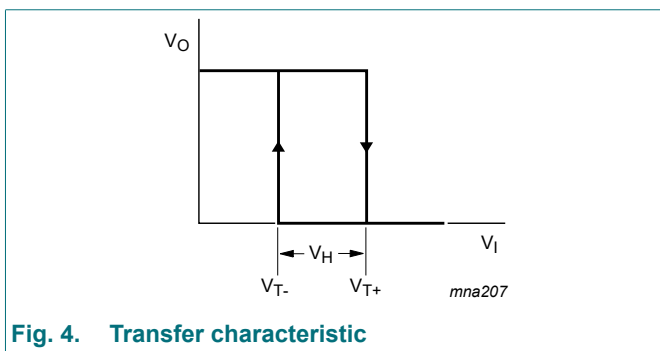
11.1. Transfer characteristics

Table 8. Transfer characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC3G14										
V _{T+}	positive-going threshold voltage	see Fig. 4, Fig. 5								
		V _{CC} = 2.0 V	1.00	1.18	1.50	1.00	1.50	1.00	1.50	V
		V _{CC} = 4.5 V	2.30	2.60	3.15	2.30	3.15	2.30	3.15	V
		V _{CC} = 6.0 V	3.00	3.46	4.20	3.00	4.20	3.00	4.20	V
V _{T-}	negative-going threshold voltage	see Fig. 4, Fig. 5								
		V _{CC} = 2.0 V	0.30	0.60	0.90	0.30	0.90	0.30	0.90	V
		V _{CC} = 4.5 V	1.13	1.47	2.00	1.13	2.00	1.13	2.00	V
		V _{CC} = 6.0 V	1.50	2.06	2.60	1.50	2.60	1.50	2.60	V
V _H	hysteresis voltage	(V _{T+} - V _{T-}); see Fig. 4, Fig. 5 and Fig. 6								
		V _{CC} = 2.0 V	0.30	0.60	1.00	0.30	1.00	0.30	1.00	V
		V _{CC} = 4.5 V	0.60	1.13	1.40	0.60	1.40	0.60	1.40	V
		V _{CC} = 6.0 V	0.80	1.40	1.70	0.80	1.70	0.80	1.70	V
74HCT3G14										
V _{T+}	positive-going threshold voltage	see Fig. 4, Fig. 5								
		V _{CC} = 4.5 V	1.20	1.58	1.90	1.20	1.90	1.20	1.90	V
		V _{CC} = 5.5 V	1.40	1.78	2.10	1.40	2.10	1.40	2.10	V
V _{T-}	negative-going threshold voltage	see Fig. 4, Fig. 5								
		V _{CC} = 4.5 V	0.50	0.87	1.20	0.50	1.20	0.50	1.20	V
		V _{CC} = 5.5 V	0.60	1.11	1.40	0.60	1.40	0.60	1.40	V
V _H	hysteresis voltage	(V _{T+} - V _{T-}); see Fig. 4, Fig. 5 and Fig. 7								
		V _{CC} = 4.5 V	0.40	0.71	-	0.40	-	0.40	-	V
		V _{CC} = 5.5 V	0.40	0.67	-	0.40	-	0.40	-	V

11.2. Transfer characteristics waveforms



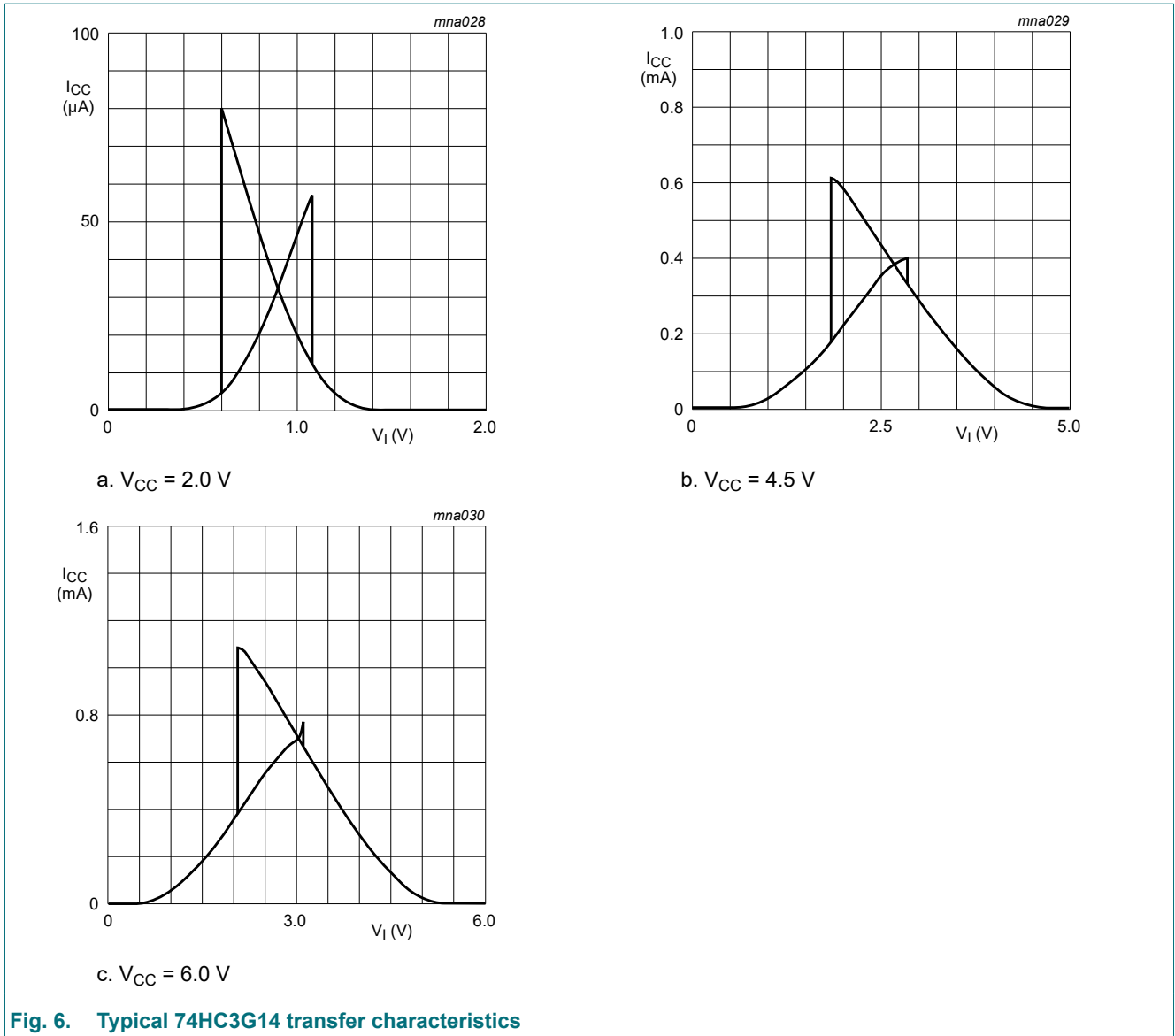


Fig. 6. Typical 74HC3G14 transfer characteristics

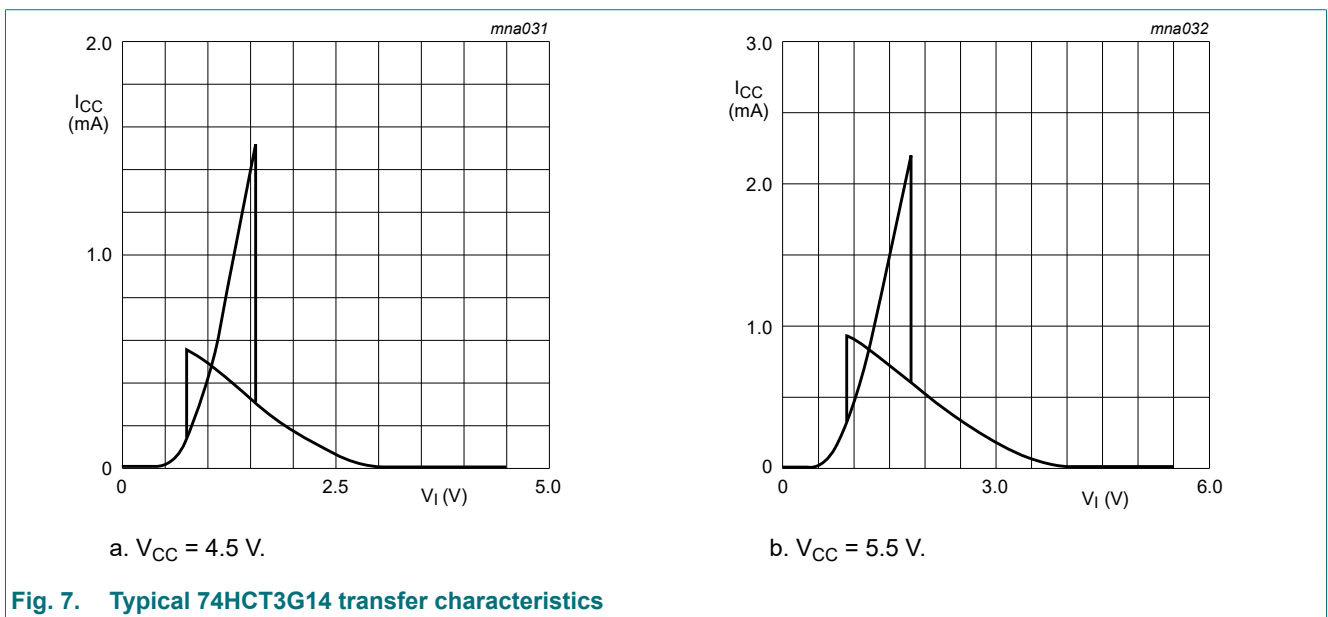


Fig. 7. Typical 74HCT3G14 transfer characteristics

12. Dynamic characteristics

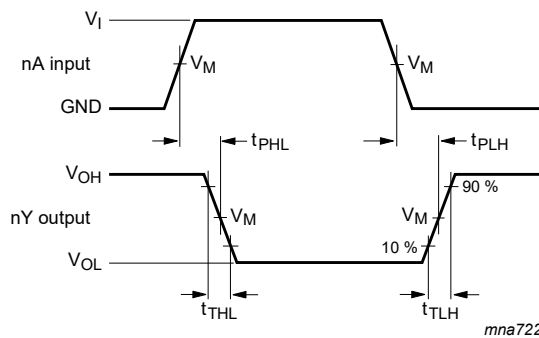
Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC3G14										
t _{pd}	propagation delay	nA to nY; see Fig. 8 [1]								
		V _{CC} = 2.0 V	-	53	125	-	155	-	190	ns
		V _{CC} = 4.5 V	-	16	25	-	31	-	38	ns
		V _{CC} = 6.0 V	-	13	21	-	26	-	32	ns
t _t	transition time	nY; see Fig. 8 [2]								
		V _{CC} = 2.0 V	-	20	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	5	13	-	16	-	19	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} [3]	-	10	-	-	-	-	-	pF
74HCT3G14										
t _{pd}	propagation delay	nA to nY; V _{CC} = 4.5 V; see Fig. 8 [1]	-	21	32	-	40	-	48	ns
t _t	transition time	nY; V _{CC} = 4.5 V; see Fig. 8 [2]	-	6	15	-	19	-	22	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} - 1.5 V [3]	-	10	-	-	-	-	-	pF

- [1] t_{pd} is the same as t_{PLH} and t_{PHL}
- [2] t_t is the same as t_{TLH} and t_{THL}
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12.1. Waveforms and test circuit



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. The data input (nA) to output (nY) propagation delays and output transition times

Table 10. Measurement points

Type	Input	Output
	V_M	V_M
74HC3G14	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT3G14	1.3 V	1.3 V

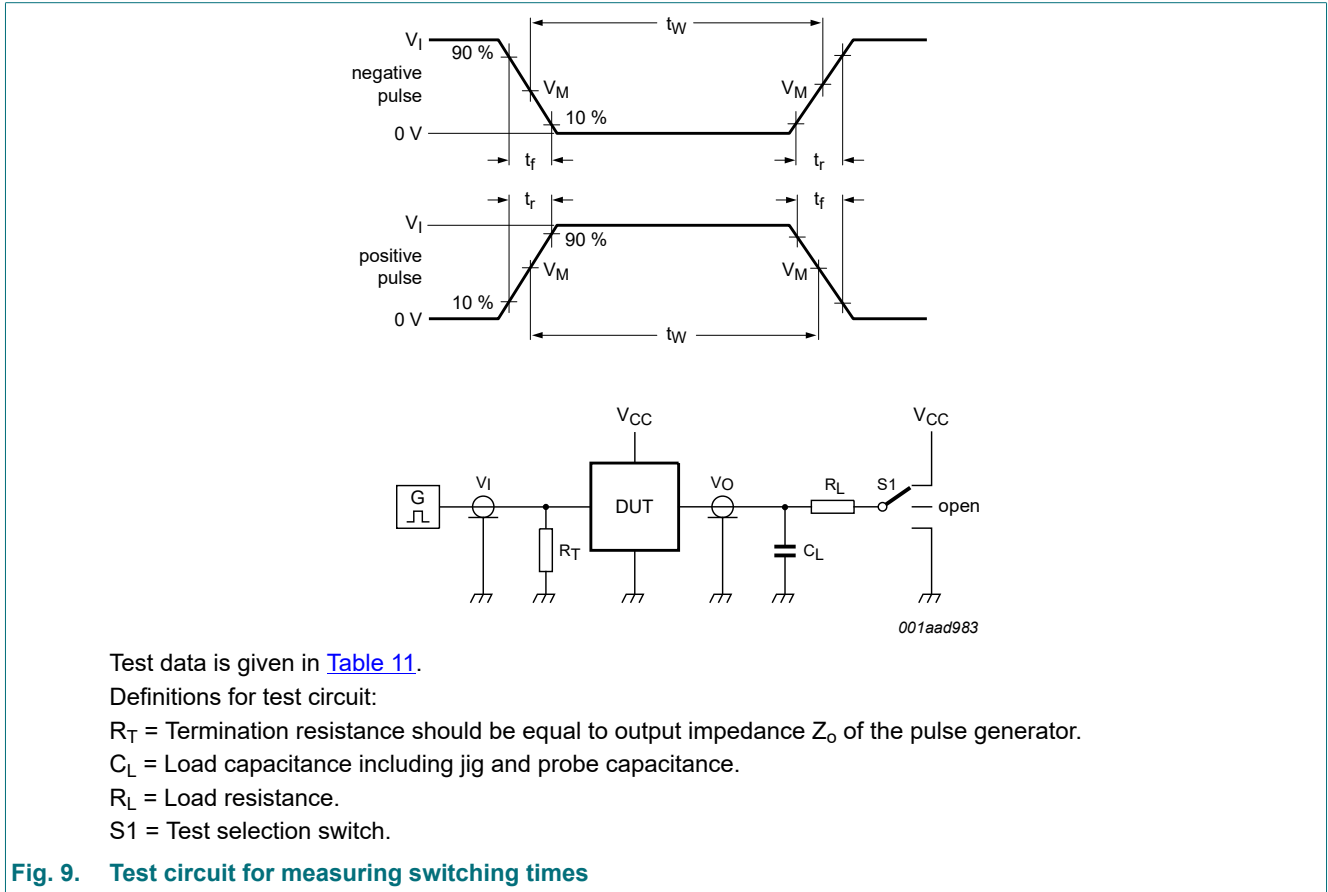


Fig. 9. Test circuit for measuring switching times

Table 11. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC3G14	GND to V_{CC}	≤ 6 ns	50 pF	1 k Ω	open
74HCT3G14	GND to 3.0 V	≤ 6 ns	50 pF	1 k Ω	open

13. Application information

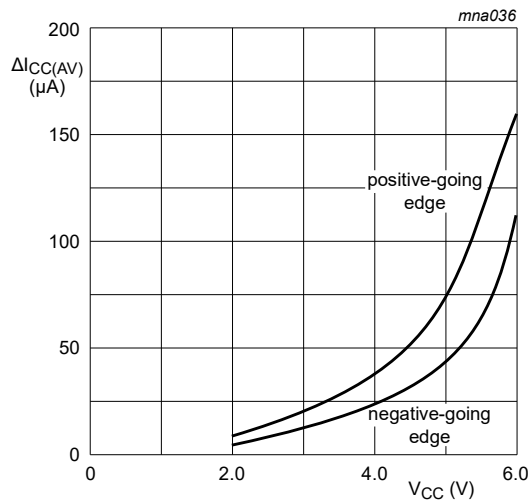
The slow input rise and fall times cause additional power dissipation, which can be calculated using the following formula:

$$P_{add} = f_i \times (t_r \times \Delta I_{CC(AV)} + t_f \times \Delta I_{CC(AV)}) \times V_{CC} \text{ where:}$$

- P_{add} = additional power dissipation (μW);
- f_i = input frequency (MHz);
- t_r = input rise time (ns); 10 % to 90 %;
- t_f = input fall time (ns); 90 % to 10 %;
- $\Delta I_{CC(AV)}$ = average additional supply current (μA).

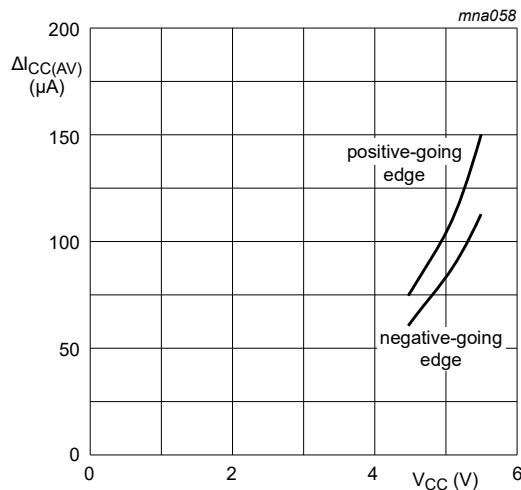
$\Delta I_{CC(AV)}$ differs with positive or negative input transitions, as shown in Fig. 10 and Fig. 11.

An example of a relaxation circuit using the 74HC3G14/74HCT3G14 is shown in Fig. 12.



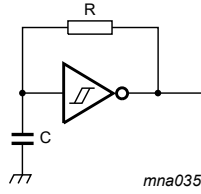
Linear change of V_I between $0.1 \times V_{CC}$ to $0.9 \times V_{CC}$.

Fig. 10. $\Delta I_{CC(AV)}$ as a function of V_{CC} for 74HC3G14



Linear change of V_I between $0.1 \times V_{CC}$ to $0.9 \times V_{CC}$.

Fig. 11. $\Delta I_{CC(AV)}$ as a function of V_{CC} for 74HCT3G14

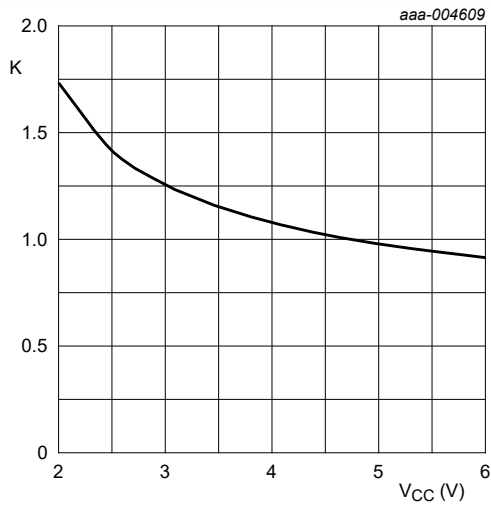


For 74HC3G14: $f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$

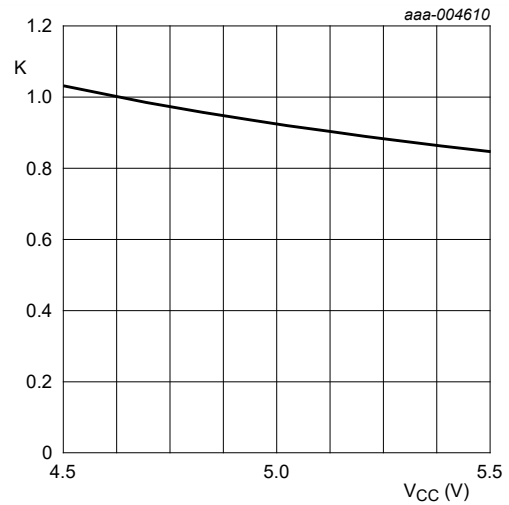
For 74HCT3G14: $f = \frac{1}{T} \approx \frac{1}{0.67 \times RC}$

For K-factor, see [Fig. 13](#)

Fig. 12. Relaxation oscillator



a. K-factor for 74HC3G14



b. K-factor for 74HCT3G14

Fig. 13. Typical K-factor for relaxation oscillator

14. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

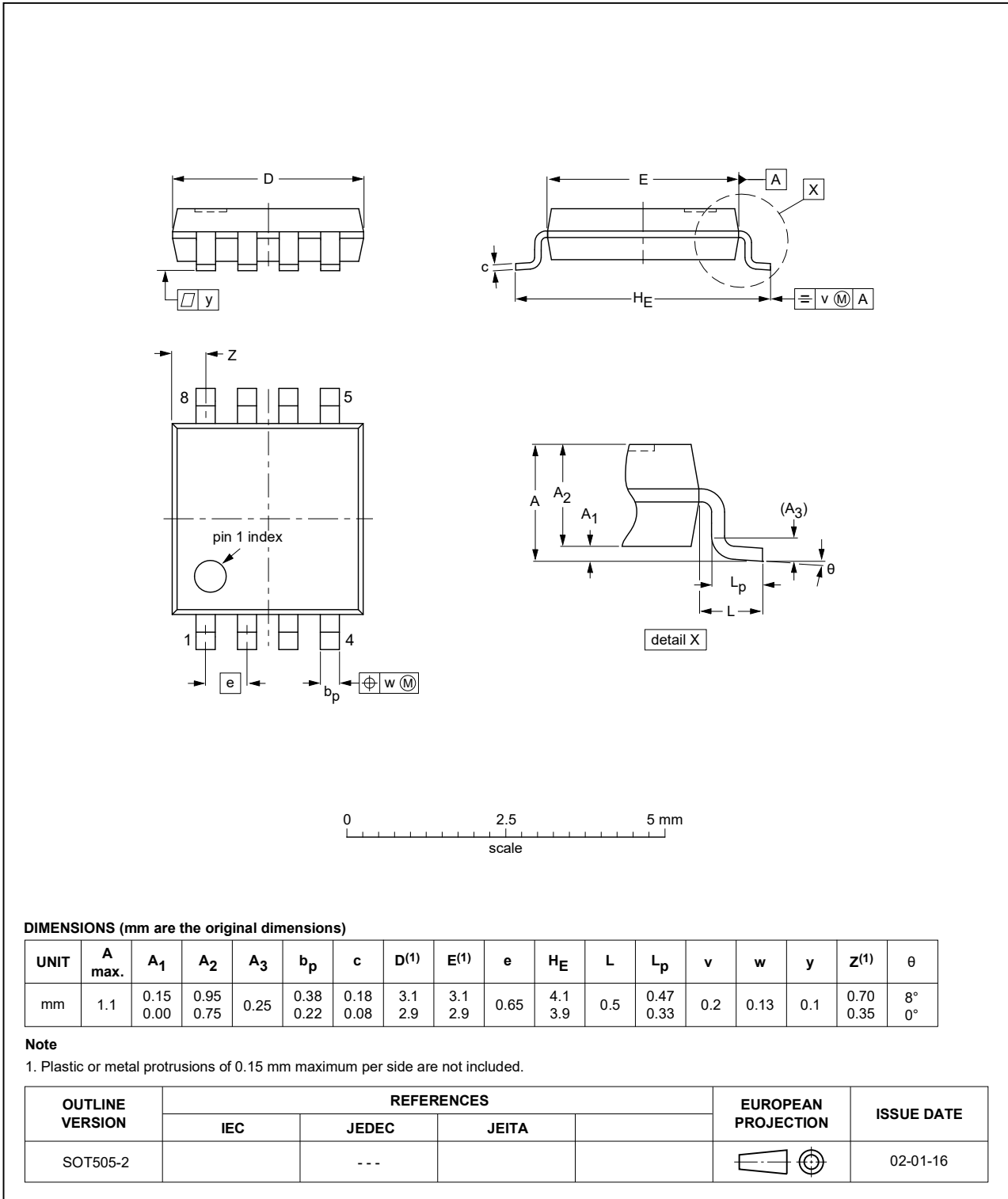


Fig. 14. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

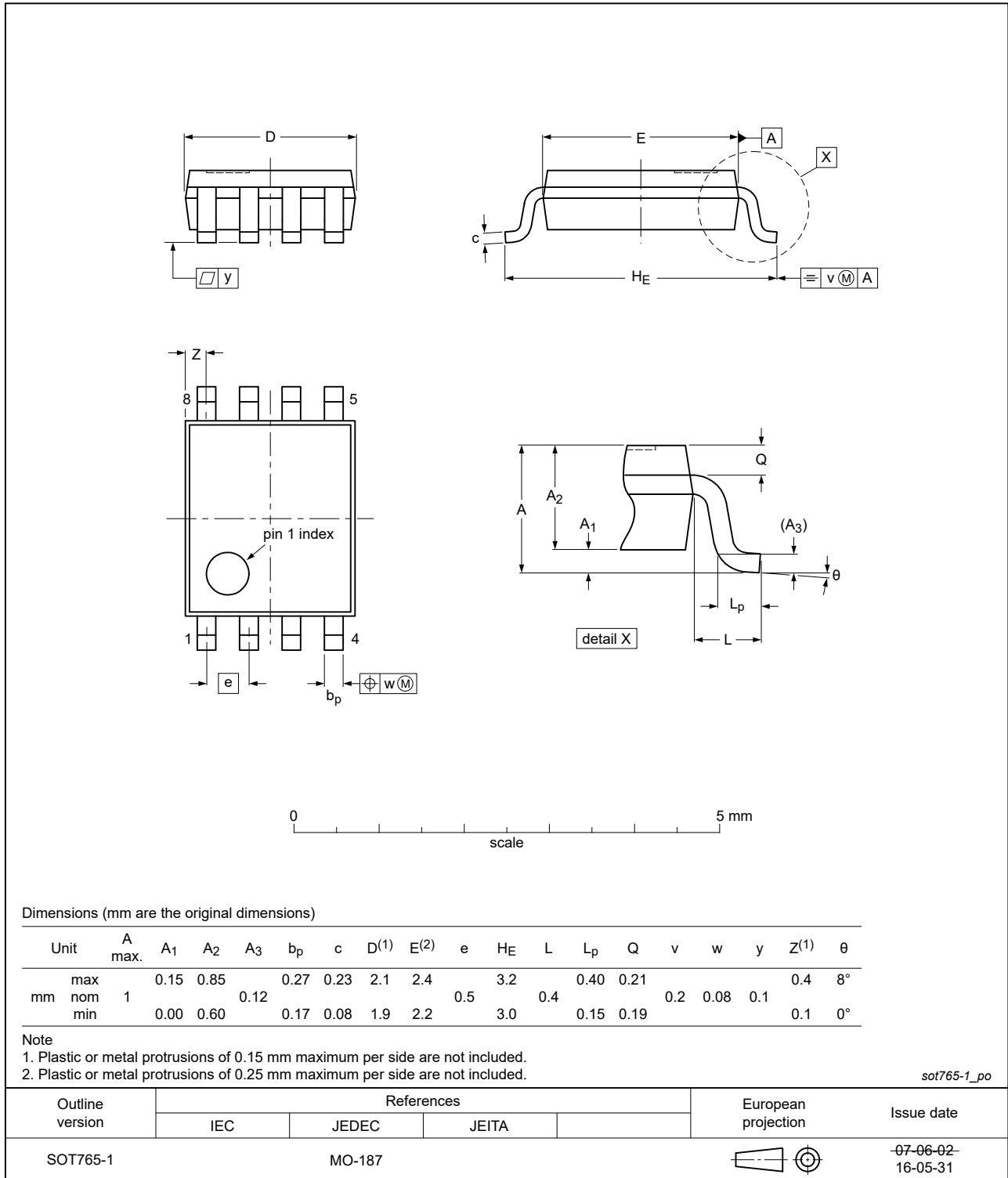


Fig. 15. Package outline SOT765-1 (VSSOP8)

15. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT3G14 v.7	20231218	Product data sheet	-	74HC_HCT3G14 v.6
Modifications:	<ul style="list-style-type: none"> • Section 2 updated. • Section 2: ESD specification updated according to the latest JEDEC standard. • Section 9: P_{tot} and derating values for P_{tot} total power dissipation updated. 			
74HC_HCT3G14 v.6	20190201	Product data sheet	-	74HC_HCT3G14 v.5
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC3G14GD and 74HCT3G14GD (SOT996-2) removed. • Package outline drawing SOT765-1 (VSSOP8) updated. 			
74HC_HCT3G14 v.5	20131209	Product data sheet	-	74HC_HCT3G14 v.4
Modifications:	<ul style="list-style-type: none"> • Fig. 13 added (typical K-factor for relaxation oscillator). 			
74HC_HCT3G14 v.4	20131003	Product data sheet	-	74HC_HCT3G14 v.3
Modifications:	<ul style="list-style-type: none"> • For type numbers 74HC3G14GD and 74HCT3G14GD XSON8U has changed to XSON8. 			
74HC_HCT3G14 v.3	20090508	Product data sheet	-	74HC_HCT3G14 v.2
74HC_HCT3G14 v.2	20031104	Product specification	-	74HC_HCT3G14 v.1
74HC_HCT3G14 v.1	20020723	Product specification	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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