# Quad D-Type Flip-Flop With Clear

## MM74HC175

### Description

The MM74HC175 high speed D−type flip−flop with complementary outputs utilizes advanced silicon−gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS−TTL loads. Information at the D inputs of the MM74HC175 is transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse. Both true and complement outputs from each flip flop are externally available. All four flip−flops are controlled by a common clock and a common CLEAR. Clearing is accomplished by a negative pulse at the CLEAR input. All four Q outputs are cleared to a logical "0" and all four $\overline{Q}$ outputs to a logical "1." The 74HC logic family is functionally as well as pin−out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{CC}$ and ground.

### Features

- Typical Propagation Delay: 15 ns
- Wide Operating Supply Voltage Range: 2–6 V
- Low Input Current: 1 μA Maximum
- Low Quiescent Supply Current: 160 μA Maximum (74HC)
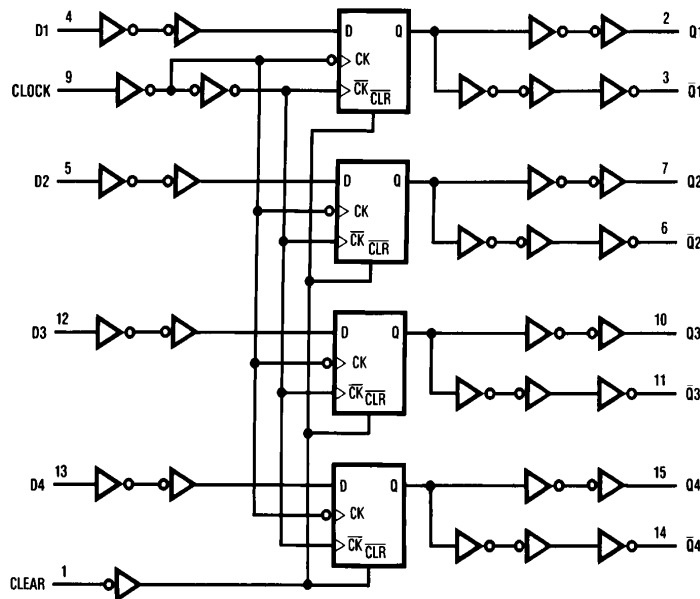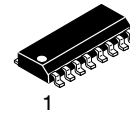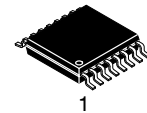- High Output Drive Current: 4 mA Minimum (74HC)
- These are Pb−Free Devices



**SOIC−16**
**CASE 751B**

**TSSOP−16**
**CASE 948F**

### MARKING DIAGRAMS



HC175A
AWLYWW

HC
175A
ALYW
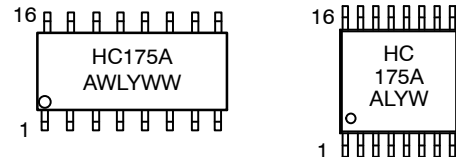
| HC175A | = Specific Device Code |
|---|---|
| A | = Assembly Location |
| L/WL | = Wafer Lot |
| Y/YY | = Year of Production, Last Number |
| W/WW | = Work Week Number |

### CONNECTION DIAGRAM



(Top View)
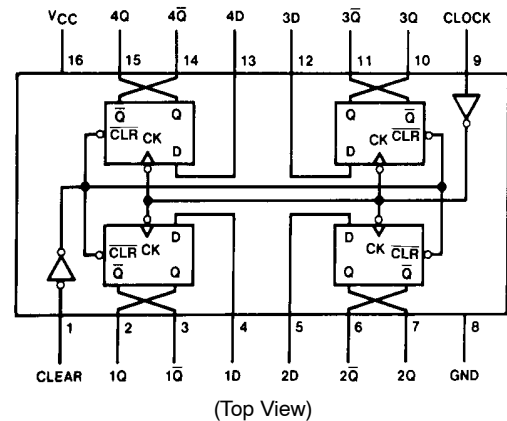
### TRUTH TABLE
(Each Flip Flop)

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **Clear** | **Clock** | **D** | **Q** | **$\overline{Q}$** |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | $Q_0$ | $\overline{Q_0}$ |

H = HIGH Level (steady state)
L = LOW Level (steady state)
X = Irrelevant
↑ = Transition from LOW−to−HIGH level
$Q_0$ = The level of Q before the indicated steady−state input conditions were established



**Figure 1. Logic Diagram**

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

November, 2022 – Rev. 1

Publication Order Number:
**MM74HC175/D**

# MM74HC175

## ABSOLUTE MAXIMUM RATINGS (Note 1)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | −0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage | −0.5 to $V_{CC}$ + 0.5 | V |
| $V_{OUT}$ | DC Output Voltage | −0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$, $I_{OK}$ | Clamp Diode Current | ±20 | mA |
| $I_{OUT}$ | DC Output Current, per Pin | ±25 | mA |
| $I_{CC}$ | DC $V_{CC}$ or GND Current, per Pin | ±50 | mA |
| $T_{STG}$ | Storage Temperature Range | −65 to +150 | °C |
| $P_D$ | Power Dissipation<br>(Note 2)<br>S. O. Package Only | 600<br>500 | mW |
| $T_L$ | Lead Temperature (Soldering 10 seconds) | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating – plastic "N" package: 12 mW/°C from 65°C to 85°C.

## RECOMMENDED OPERATIONG CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2 | 6 | V |
| $V_{IN}$, $V_{OUT}$ | DC Input or Output Voltage | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Times<br>$V_{CC}$ = 2.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | −<br>−<br>− | 1000<br>500<br>400 | ns |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Note 3)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C Typ | $T_A$ = 25°C Guaranteed Limits | $T_A$ −40°C to 85°C | $T_A$ = −55°C to 125°C | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum HIGH Level Input Voltage | | 2.0<br>4.5<br>6.0 | −<br>−<br>− | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V |
| $V_{IL}$ | Maximum LOW Level Input Voltage | | 2.0<br>4.5<br>6.0 | −<br>−<br>− | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | 0.5<br>1.35<br>1.8 | V |
| $V_{OH}$ | Minimum HIGH Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ ≤ 20 μA | 2.0<br>4.5<br>6.0 | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ ≤ 4.0 mA<br>$\|I_{OUT}\|$ ≤ 5.2 mA | 4.5<br>6.0 | 4.2<br>5.7 | 3.98<br>5.48 | 3.84<br>5.34 | 3.7<br>5.2 | V |
| $V_{OL}$ | Maximum LOW Level Output Voltage | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ ≤ 20 μA | 2.0<br>4.5<br>6.0 | 0<br>0<br>0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$\|I_{OUT}\|$ ≤ 4.0 mA<br>$\|I_{OUT}\|$ ≤ 5.2 mA | 4.5<br>6.0 | 0.2<br>0.2 | 0.26<br>0.26 | 0.33<br>0.33 | 0.4<br>0.4 | V |

**DC ELECTRICAL CHARACTERISTICS** (Note 3) (continued)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = 25°C$ | | $T_A -40°C$ to $85°C$ | $T_A = -55°C$ to $125°C$ | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | | |
| $I_{IN}$ | Maximum Input Current | $V_{IN} = V_{CC}$ or GND | 6.0 | – | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$ μA | 6.0 | – | 8 | 80 | 160 | μA |

3. For a power supply of 5 V ±10% the worst case output voltages ($V_{OH}$, and $V_{OL}$) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case $V_{IH}$ and $V_{IL}$ occur at $V_{CC}$ = 5.5 V and 4.5 V respectively. (The $V_{IH}$ value at 5.5 V is 3.85 V.) The worst case leakage current ($I_{IN}$, $I_{CC}$, and $I_{OZ}$) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5 V, $T_A$ = 25°C, CL = 15 pF, $t_r = t_f$ = 6 ns)

| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Unit |
|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Operating Frequency | | 60 | 35 | MHz |
| $t_{PHL}, t_{PLH}$ | Maximum Propagation Delay, Clock to Q or $\overline{Q}$ | | 15 | 25 | ns |
| $t_{PHL}, t_{PLH}$ | Maximum Propagation Delay, Reset to Q or $\overline{Q}$ | | 13 | 21 | ns |
| $t_{REC}$ | Minimum Removal Time, Clear to Clock | | – | 20 | ns |
| $t_S$ | Minimum Setup Time, Data to Clock | | – | 20 | ns |
| $t_H$ | Minimum Hold Time, Data from Clock | | – | 0 | ns |
| $t_W$ | Minimum Pulse Width, Clock or Clear | | 10 | 16 | ns |

**AC ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 2.0 V to 6.0 V, $C_L$ = 50 pF, $t_r = t_f$ = 6 ns unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A = 25°C$ | | $T_A -40°C$ to $85°C$ | $T_A = -55°C$ to $125°C$ | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Typ | Guaranteed Limits | | | |
| $f_{MAX}$ | Maximum Operating Frequency | | 2.0<br>4.5<br>6.0 | 12<br>60<br>70 | 6<br>30<br>35 | 5<br>24<br>28 | 4<br>20<br>24 | MHz |
| $t_{PHL}, t_{PLH}$ | Maximum Propagation Delay, Clock to Q or $\overline{Q}$ | | 2.0<br>4.5<br>6.0 | 80<br>15<br>13 | 150<br>30<br>26 | 190<br>38<br>32 | 225<br>45<br>38 | ns |
| $t_{PHL}, t_{PLH}$ | Maximum Propagation Delay, Reset to Q or $\overline{Q}$ | | 2.0<br>4.5<br>6.0 | 64<br>14<br>12 | 125<br>25<br>21 | 158<br>32<br>27 | 186<br>37<br>32 | ns |
| $t_{REM}$ | Minimum Removal Time, Clear to Clock | | 2.0<br>4.5<br>6.0 | –<br>–<br>– | 100<br>20<br>17 | 125<br>25<br>21 | 150<br>30<br>25 | ns |
| $t_S$ | Minimum Setup Time, Data to Clock | | 2.0<br>4.5<br>6.0 | –<br>–<br>– | 100<br>20<br>17 | 125<br>25<br>21 | 150<br>30<br>25 | ns |
| $t_H$ | Minimum Hold Time, Data from Clock | | 2.0<br>4.5<br>6.0 | –<br>–<br>– | 0<br>0<br>0 | 0<br>0<br>0 | 0<br>0<br>0 | ns |
| $t_W$ | Minimum Pulse Width, Clock or Clear | | 2.0<br>4.5<br>6.0 | 30<br>9<br>8 | 80<br>16<br>14 | 100<br>20<br>17 | 120<br>24<br>20 | ns |
| $t_r, t_f$ | Maximum Input Rise and Fall Time | | 2.0<br>4.5<br>6.0 | –<br>–<br>– | 1000<br>500<br>400 | 1000<br>500<br>400 | 1000<br>500<br>400 | ns |
| $t_{TLH}, t_{THL}$ | Maximum Output Rise and Fall Time | | 2.0<br>4.5<br>6.0 | 30<br>9<br>8 | 75<br>15<br>13 | 95<br>19<br>16 | 110<br>22<br>19 | ns |

# MM74HC175

## AC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 2.0 V to 6.0 V, $C_L$ = 50 pF, $t_r = t_f$ = 6 ns unless otherwise specified)

| Symbol | Parameter | Conditions | $V_{CC}$ (V) | $T_A$ = 25°C Typ | $T_A$ = 25°C | $T_A$ −40°C to 85°C | $T_A$ = −55°C to 125°C | Unit |
|--------|-----------|-----------|--------------|------------------|--------------|---------------------|------------------------|------|
| | | | | | Guaranteed Limits | | | |
| $C_{PD}$ | Power Dissipation Capacitance (Note 4) | (per package) | − − − | 150 − − | − − | − − | − − | pF |
| $C_{IN}$ | Maximum Input Capacitance | | − | 5 | 10 | 10 | 10 | pF |

4. $C_{PD}$ determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

## ORDERING INFORMATION

| Device | Package | Shipping[†] |
|--------|---------|-------------|
| MM74HC175M | SOIC−16 (Pb−Free) | 48 Units / Tube |
| MM74HC175MX | SOIC−16 (Pb−Free) | 2500 / Tape & Reel |
| MM74HC175MTCX | TSSOP−16 (Pb−Free) | 2500 Units / Tube |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**onsemi**
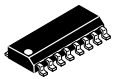
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CASE 751B−05
ISSUE K
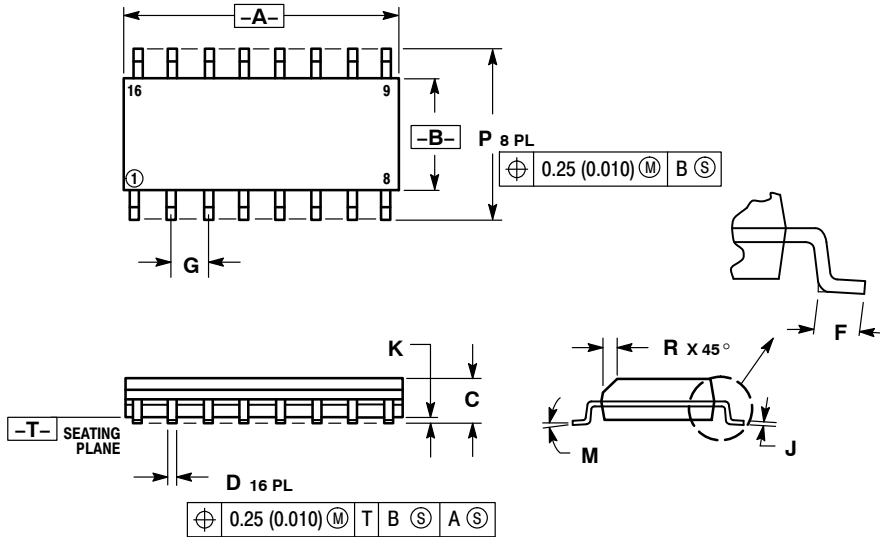
**SCALE 1:1**

DATE 29 DEC 2006

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

P 8 PL

⊕ | 0.25 (0.010) Ⓜ | B Ⓢ

G

K

C

−T− SEATING PLANE

R X 45°

F

M

J

D 16 PL

⊕ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
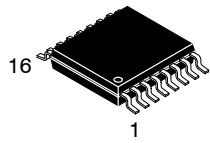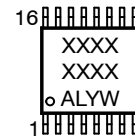16. SOURCE N-CH

## RECOMMENDED SOLDERING FOOTPRINT*

8X
6.40

16X 1.12

16X
0.58

1.27 PITCH
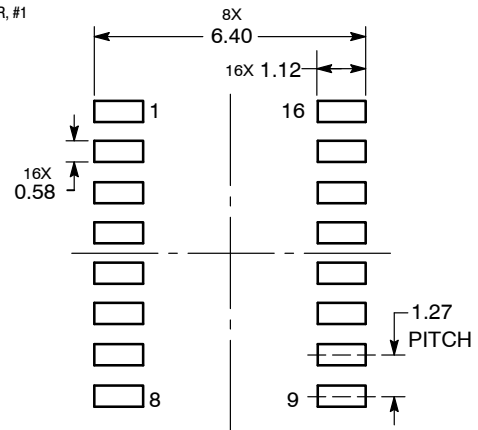
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DOCUMENT NUMBER: | 98ASB42566B | | |
|---|---|---|---|
| DESCRIPTION: | SOIC−16 | | PAGE 1 OF 1 |

**onsemi**

**TSSOP−16 WB**
CASE 948F
ISSUE B

DATE 19 OCT 2006
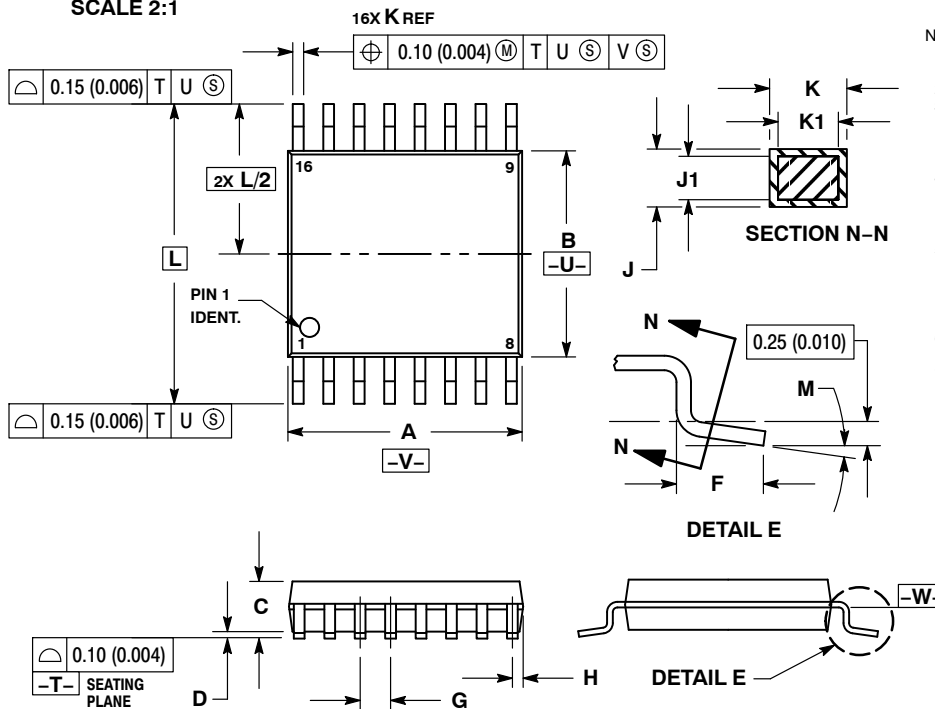
16

1

**SCALE 2:1**

**16X K** REF

$\oplus$ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

⌴ | 0.15 (0.006) | T U Ⓢ

**2X L/2**

L

PIN 1
IDENT.

16   9

B
−U−

1   8

⌴ | 0.15 (0.006) | T U Ⓢ

A
−V−

C

⌴ | 0.10 (0.004)

−T− SEATING
PLANE

D   G

K
K1

J1

J

**SECTION N−N**

N

0.25 (0.010)

M

N

F

**DETAIL E**

H   **DETAIL E**   −W−

**NOTES:**
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
|-----|------|------|-------|-------|
| | **MIN** | **MAX** | **MIN** | **MAX** |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

**RECOMMENDED
SOLDERING FOOTPRINT\***

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS
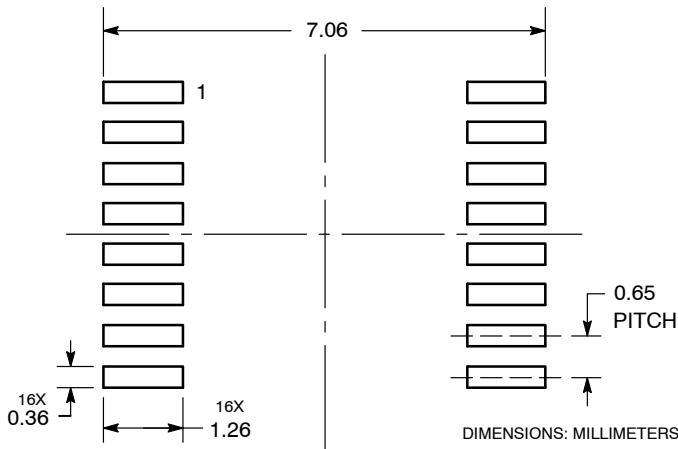
**GENERIC
MARKING DIAGRAM\***

16

XXXX
XXXX
ALYW

1

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ▪ = Pb−Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪ ", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| **DOCUMENT NUMBER:** | **98ASH70247A** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| **DESCRIPTION:** | **TSSOP−16** | | **PAGE 1 OF 1** |

**ADDITIONAL INFORMATION**

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