# 74AHC594; 74AHCT594

## 8-bit shift register with output register

Rev. 5 — 9 October 2023 Product data sheet

## 1. General description

The 74AHC594; 74AHCT594 is a high-speed Si-gate CMOS device and is pin compatible with Low-Power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC594; 74AHCT594 is an 8-bit, non-inverting, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (SHCP and STCP) and direct overriding clears ($\overline{SHR}$ and $\overline{STR}$) are provided on both the shift and storage registers. A serial output (Q7S) is provided for cascading purposes.

Both the shift and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one count pulse ahead of the storage register.

## 2. Features and benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Balanced propagation delays
- All inputs have Schmitt-trigger action
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- 8-bit serial-in, parallel-out shift register with storage
- Independent direct overriding clears on shift and storage registers
- Independent clocks for shift and storage registers
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Input levels:
  - For 74AHC594: CMOS level
  - For 74AHCT594: TTL level
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Applications

- Serial-to parallel data conversion
- Remote control holding register

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74AHC594D<br>74AHCT594D | -40 °C to +125 °C | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |
| 74AHC594PW<br>74AHCT594PW | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| 74AHC594BQ<br>74AHCT594BQ | -40 °C to +125 °C | DHVQFN16 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm | SOT763-1 |

## 5. Functional diagram

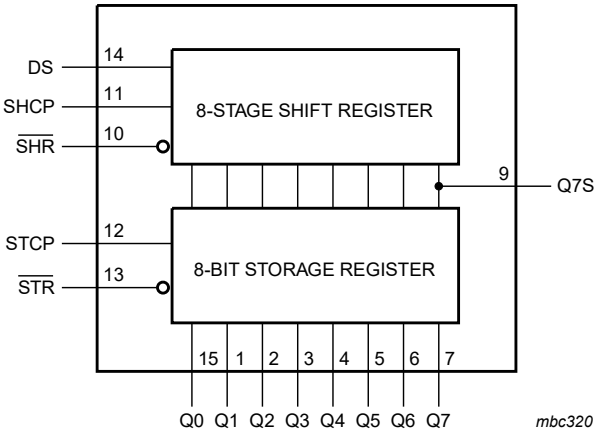


**Fig. 1. Functional diagram**

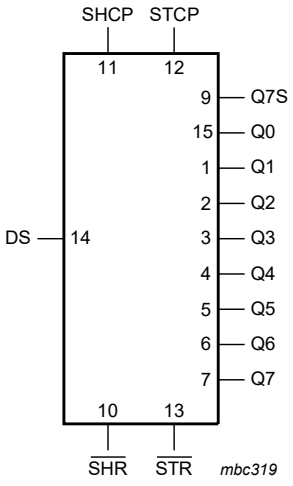


**Fig. 2. Logic symbol**

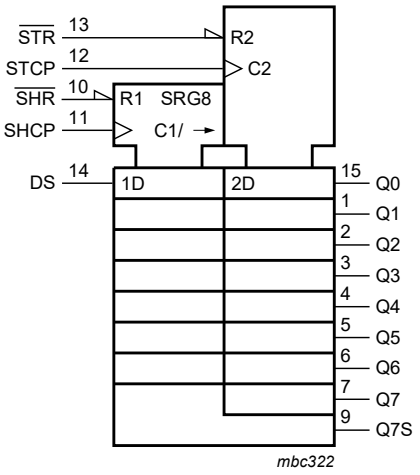


**Fig. 3. IEC logic symbol**


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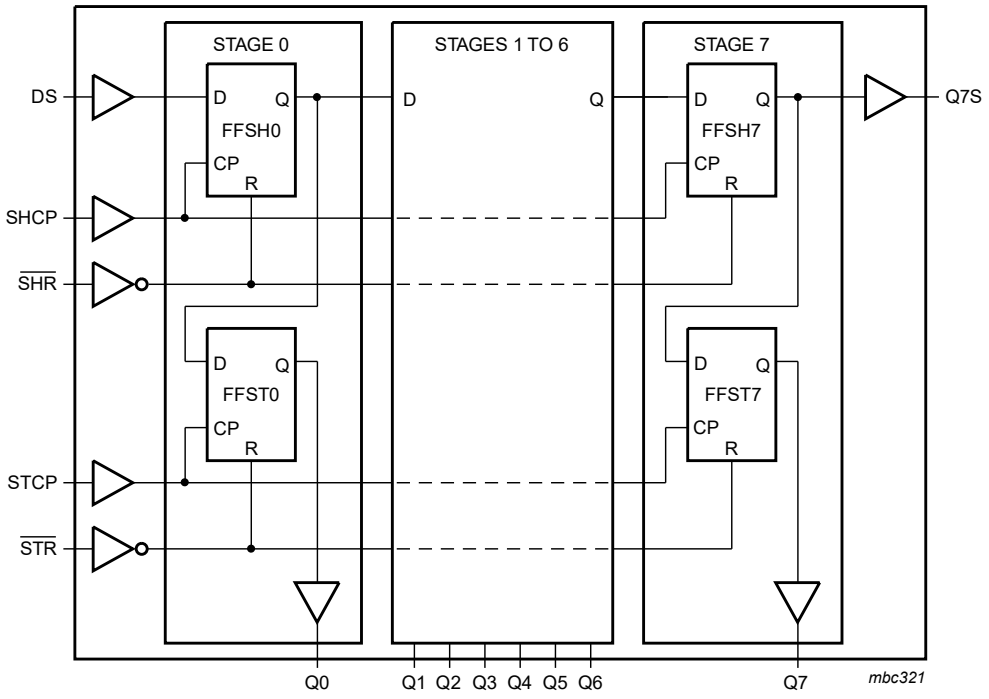
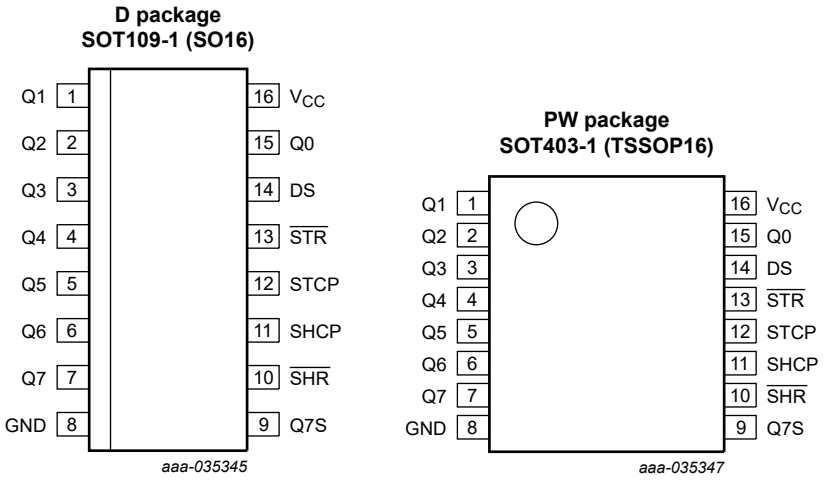



**Fig. 4. Logic diagram**

# 6. Pinning information

## 6.1. Pinning





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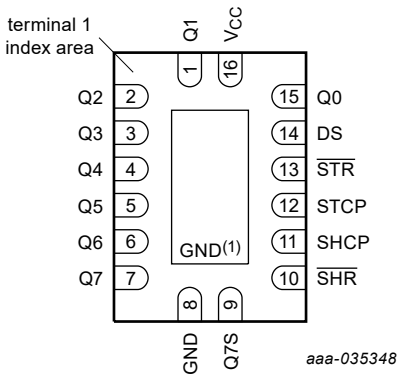
**BQ package**
**SOT763-1 (DHVQFN16)**




Transparent top view

(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

## 6.2. Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | 15, 1, 2, 3, 4, 5, 6, 7 | parallel data output |
| GND | 8 | ground (0 V) |
| Q7S | 9 | serial data output |
| $\overline{SHR}$ | 10 | shift register reset input (active LOW) |
| SHCP | 11 | shift register clock input |
| STCP | 12 | storage register clock input |
| $\overline{STR}$ | 13 | storage register reset input (active LOW) |
| DS | 14 | serial data input |
| $V_{CC}$ | 16 | supply voltage |

# 7. Functional description

**Table 3. Function table**

*H = HIGH voltage state; L = LOW voltage state; ↑ = LOW to HIGH transition; X = don't care; NC = no change.*

| Input | | | | | Output | | Function |
|---|---|---|---|---|---|---|---|
| SHCP | STCP | $\overline{SHR}$ | $\overline{STR}$ | DS | Q7S | Qn | |
| X | X | L | X | X | L | NC | a LOW-state on $\overline{SHR}$ only affects the shift register |
| X | X | X | L | X | NC | L | a LOW-state on $\overline{STR}$ only affects the storage register |
| X | ↑ | L | H | X | L | L | empty shift register loaded into storage register |
| ↑ | X | H | X | H | Q6S | NC | logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S). |
| X | ↑ | H | H | X | NC | QnS | contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages |
| ↑ | ↑ | H | H | X | Q6S | QnS | contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages |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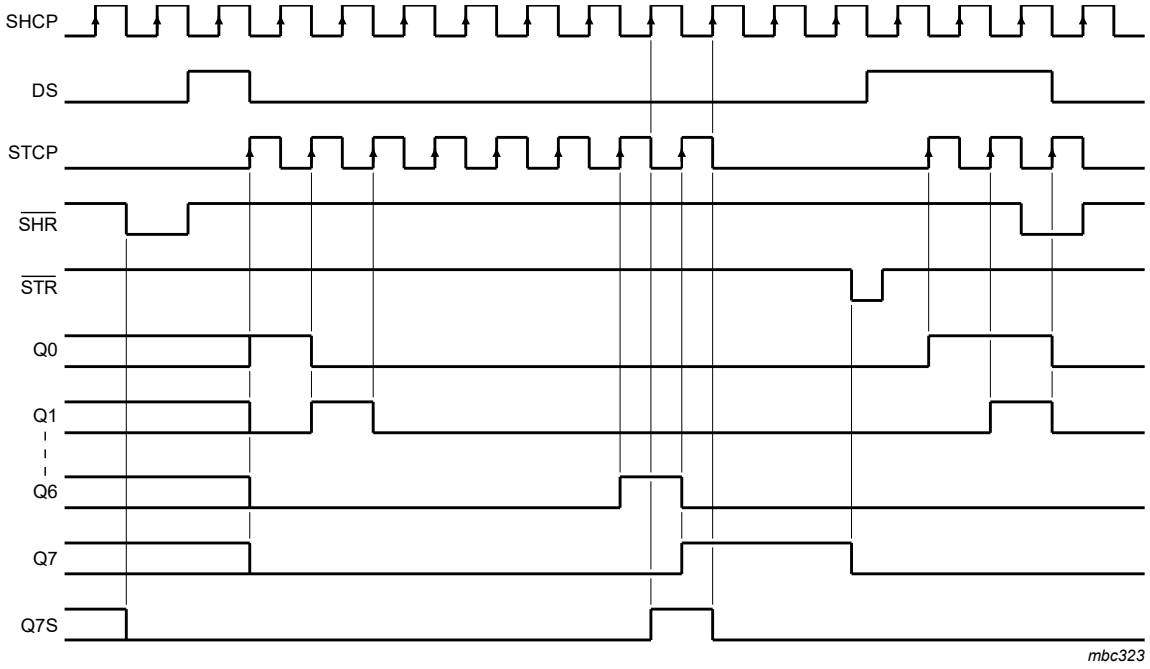


**Fig. 5. Timing diagram**

## 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | -0.5 | +7.0 | V |
| $V_I$ | input voltage | | | -0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I$ < -0.5 V | [1] | -20 | - | mA |
| $I_{OK}$ | output clamping current | $V_O$ < -0.5 V or $V_O$ > $V_{CC}$ + 0.5 V | [1] | -20 | +20 | mA |
| $I_O$ | output current | $V_O$ = -0.5 V to ($V_{CC}$ + 0.5 V) | | -25 | +25 | mA |
| $I_{CC}$ | supply current | | | - | +75 | mA |
| $I_{GND}$ | ground current | | | -75 | - | mA |
| $T_{stg}$ | storage temperature | | | -65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +125 °C | [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT109-1 (SO16) package: $P_{tot}$ derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: $P_{tot}$ derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: $P_{tot}$ derates linearly with 11.2 mW/K above 106 °C.


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# 9. Recommended operating conditions

**Table 5. Operating conditions**

| Symbol | Parameter | Conditions | 74AHC594 | | | 74AHCT594 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | 5.5 | 0 | - | 5.5 | V |
| $V_O$ | output voltage | | 0 | - | $V_{CC}$ | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 3.0 V to 3.6 V | - | - | 100 | - | - | - | ns/V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 20 | - | - | 20 | ns/V |

# 10. Static characteristics

**Table 6. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74AHC594** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC}$ = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | $V_{CC}$ = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC}$ = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | $V_{CC}$ = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = -50 µA; $V_{CC}$ = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O$ = -50 µA; $V_{CC}$ = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | $I_O$ = -50 µA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = -4.0 mA; $V_{CC}$ = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | | $I_O$ = -8.0 mA; $V_{CC}$ = 4.5 V | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 50 µA; $V_{CC}$ = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 µA; $V_{CC}$ = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 50 µA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 4 mA; $V_{CC}$ = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | $I_O$ = 8 mA; $V_{CC}$ = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | µA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | µA |
| $C_I$ | input capacitance | $V_I$ = $V_{CC}$ or GND | - | 3 | 10 | - | 10 | - | 10 | pF |


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| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| **74AHCT594** | | | | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = -50 μA; $V_{CC}$ = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O$ = -8.0 mA; $V_{CC}$ = 4.5 V | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | | | |
| | | $I_O$ = 50 μA; $V_{CC}$ = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O$ = 8 mA; $V_{CC}$ = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| $I_{CC}$ | supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 5.5 V | - | - | 4.0 | - | 40 | - | 80 | μA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_I$ = $V_{CC}$ - 2.1 V; other pins at $V_{CC}$ or GND; $I_O$ = 0 A; $V_{CC}$ = 4.5 V to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| $C_I$ | input capacitance | $V_I$ = $V_{CC}$ or GND | - | 3 | 10 | - | 10 | - | 10 | pF |

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 12.*

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| **74AHC594** | | | | | | | | | | |
| $t_{PLH}$ | LOW to HIGH propagation delay | SHCP to Q7S; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 5.2 | 8.5 | 2.2 | 9.7 | 2.2 | 10.6 | ns |
| | | $C_L$ = 50 pF | - | 7.4 | 11.5 | 3.0 | 13.2 | 3.0 | 14.3 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 3.8 | 6.3 | 1.7 | 7.2 | 1.7 | 7.8 | ns |
| | | $C_L$ = 50 pF | - | 4.8 | 8.0 | 2.4 | 9.1 | 2.4 | 10.0 | ns |
| | | STCP to Qn; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 5.1 | 8.3 | 2.3 | 9.5 | 2.3 | 10.6 | ns |
| | | $C_L$ = 50 pF | - | 7.3 | 11.9 | 3.3 | 13.6 | 3.3 | 14.7 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 3.5 | 5.7 | 1.8 | 6.5 | 1.8 | 7.1 | ns |
| | | $C_L$ = 50 pF | - | 4.8 | 7.8 | 2.6 | 9.0 | 2.6 | 9.8 | ns |


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| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| $t_{PHL}$ | HIGH to LOW propagation delay | SHCP to Q7S; see Fig. 6 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 5.5 | 8.9 | 2.3 | 10.2 | 2.3 | 11.0 | ns |
| | | $C_L$ = 50 pF | - | 7.4 | 12.1 | 3.0 | 13.9 | 3.0 | 15.1 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 4.1 | 6.7 | 1.9 | 7.6 | 1.9 | 8.2 | ns |
| | | $C_L$ = 50 pF | - | 5.4 | 8.8 | 2.5 | 10.1 | 2.5 | 11.0 | ns |
| | | STCP to Qn; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 5.5 | 9.1 | 2.4 | 10.4 | 2.4 | 11.3 | ns |
| | | $C_L$ = 50 pF | - | 7.3 | 12.0 | 3.2 | 13.8 | 3.2 | 15.0 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 3.7 | 6.0 | 1.9 | 6.9 | 1.9 | 7.5 | ns |
| | | $C_L$ = 50 pF | - | 5.2 | 8.5 | 2.6 | 9.7 | 2.6 | 10.5 | ns |
| | | $\overline{SHR}$ to Q7S; see Fig. 10 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 5.7 | 9.5 | 2.3 | 10.8 | 2.3 | 11.7 | ns |
| | | $C_L$ = 50 pF | - | 7.5 | 12.2 | 3.6 | 14.0 | 3.6 | 15.2 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 4.1 | 6.7 | 2.0 | 7.6 | 2.0 | 8.2 | ns |
| | | $C_L$ = 50 pF | - | 5.4 | 8.8 | 2.8 | 10.1 | 2.8 | 11.0 | ns |
| | | $\overline{STR}$ to Qn; see Fig. 9 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 5.8 | 9.6 | 2.8 | 11.0 | 2.8 | 12.0 | ns |
| | | $C_L$ = 50 pF | - | 7.7 | 12.5 | 3.8 | 14.4 | 3.8 | 15.6 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | | | | | | | |
| | | $C_L$ = 15 pF | - | 4.1 | 7.2 | 2.2 | 8.2 | 2.2 | 8.9 | ns |
| | | $C_L$ = 50 pF | - | 5.4 | 9.4 | 3.0 | 10.7 | 3.0 | 11.6 | ns |
| $f_{max}$ | maximum frequency | SHCP or STCP; see Fig. 6 and Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 80 | 125 | - | 70 | - | 65 | - | MHz |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 90 | 170 | - | 80 | - | 70 | - | MHz |
| $t_W$ | pulse width | SHCP and STCP HIGH or LOW; see Fig. 6 and Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 6.0 | - | - | 6.5 | - | 7.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 5.5 | - | - | 6.0 | - | 6.5 | - | ns |
| | | $\overline{SHR}$ and $\overline{STR}$ HIGH or LOW; see Fig. 10 and Fig. 9 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 5.0 | - | - | 5.0 | - | 5.5 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 5.0 | - | - | 5.2 | - | 5.7 | - | ns |


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| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| $t_{su}$ | set-up time | DS to SHCP; see Fig. 8 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 3.5 | - | - | 3.5 | - | 4.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 3.0 | - | - | 3.0 | - | 3.5 | - | ns |
| | | $\overline{SHR}$ to STCP; see Fig. 11 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 8.0 | - | - | 9.0 | - | 9.5 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 5.0 | - | - | 5.0 | - | 5.5 | - | ns |
| | | SHCP to STCP; see Fig. 7 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 8.0 | - | - | 8.5 | - | 9.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 5.0 | - | - | 5.0 | - | 5.5 | - | ns |
| $t_h$ | hold time | DS to SHCP; see Fig. 8 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.5 | - | - | 1.5 | - | 2.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.5 | - | ns |
| $t_{rec}$ | recovery time | $\overline{SHR}$ to SHCP; see Fig. 10 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 4.2 | - | - | 4.8 | - | 5.3 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 2.9 | - | - | 3.3 | - | 3.8 | - | ns |
| | | $\overline{STR}$ to STCP; see Fig. 9 | | | | | | | | |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 4.6 | - | - | 5.3 | - | 5.8 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 3.2 | - | - | 3.7 | - | 4.3 | - | ns |
| $C_{PD}$ | power dissipation capacitance | $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ [2] | - | 55 | - | - | - | - | - | pF |
| **74AHCT594; $V_{CC}$ = 4.5 V to 5.5 V** | | | | | | | | | | |
| $t_{PLH}$ | LOW to HIGH propagation delay | SHCP to Q7S; see Fig. 6 | | | | | | | | |
| | | $C_L$ = 15 pF | - | 3.8 | 6.3 | 1.7 | 7.2 | 1.7 | 7.8 | ns |
| | | $C_L$ = 50 pF | - | 4.8 | 8.0 | 2.2 | 9.1 | 2.2 | 9.9 | ns |
| | | STCP to Qn; see Fig. 7 | | | | | | | | |
| | | $C_L$ = 15 pF | - | 3.5 | 5.7 | 1.8 | 6.5 | 1.8 | 7.1 | ns |
| | | $C_L$ = 50 pF | - | 4.6 | 7.7 | 2.6 | 8.8 | 2.6 | 9.6 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | SHCP to Q7S; see Fig. 6 | | | | | | | | |
| | | $C_L$ = 15 pF | - | 4.1 | 6.7 | 1.8 | 7.6 | 1.8 | 8.3 | ns |
| | | $C_L$ = 50 pF | - | 5.4 | 8.8 | 2.4 | 10.1 | 2.4 | 11.0 | ns |
| | | STCP to Qn; see Fig. 7 | | | | | | | | |
| | | $C_L$ = 15 pF | - | 3.7 | 6.1 | 1.9 | 6.9 | 1.9 | 7.2 | ns |
| | | $C_L$ = 50 pF | - | 5.2 | 8.5 | 2.6 | 9.7 | 2.6 | 10.5 | ns |
| | | $\overline{SHR}$ to Q7S; see Fig. 10 | | | | | | | | |
| | | $C_L$ = 15 pF | - | 4.3 | 7.0 | 2.4 | 8.0 | 2.4 | 8.7 | ns |
| | | $C_L$ = 50 pF | - | 5.4 | 8.8 | 2.7 | 10.1 | 2.7 | 11.0 | ns |
| | | $\overline{STR}$ to Qn; see Fig. 9 | | | | | | | | |
| | | $C_L$ = 15 pF | - | 4.5 | 7.4 | 2.3 | 8.4 | 2.3 | 9.2 | ns |
| | | $C_L$ = 50 pF | - | 5.7 | 9.4 | 3.1 | 10.7 | 3.1 | 11.7 | ns |
| $f_{max}$ | maximum frequency | SHCP or STCP; see Fig. 6 and Fig. 7 | 90 | 160 | - | 80 | - | 70 | - | MHz |


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| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| $t_W$ | pulse width | SHCP and STCP HIGH or LOW; see Fig. 6 and Fig. 7 | 5.5 | - | - | 6.0 | - | 6.5 | - | ns |
| | | $\overline{SHR}$ and $\overline{STR}$ HIGH or LOW; see Fig. 10 and Fig. 9 | 5.2 | - | - | 5.5 | - | 6.0 | - | ns |
| $t_{su}$ | set-up time | DS to SHCP; see Fig. 8 | 3.0 | - | - | 3.0 | - | 3.5 | - | ns |
| | | $\overline{SHR}$ to STCP; see Fig. 11 | 5.0 | - | - | 5.0 | - | 5.5 | - | ns |
| | | SHCP to STCP; see Fig. 7 | 5.0 | - | - | 5.0 | - | 5.5 | - | ns |
| $t_h$ | hold time | DS to SHCP; see Fig. 8 | 2.0 | - | - | 2.0 | - | 2.5 | - | ns |
| $t_{rec}$ | recovery time | $\overline{SHR}$ to SHCP; see Fig. 10 | 2.9 | - | - | 3.3 | - | 3.8 | - | ns |
| | | $\overline{STR}$ to STCP; see Fig. 9 | 3.4 | - | - | 3.8 | - | 4.3 | - | ns |
| $C_{PD}$ | power dissipation capacitance | $f_i$ = 1 MHz; $V_I$ = GND to $V_{CC}$ [2] | - | 55 | - | - | - | - | - | pF |

[1] Typical values are measured at nominal supply voltage ($V_{CC}$ = 3.3 V and $V_{CC}$ = 5.0 V).

[2] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

$f_i$ = input frequency in MHz;

$f_o$ = output frequency in MHz;

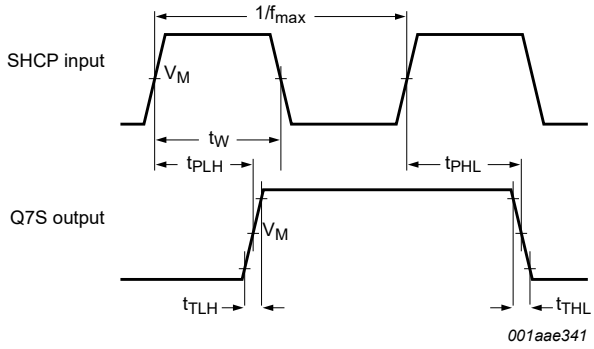
$C_L$ = output load capacitance in pF;

$V_{CC}$ = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

## 11.1. Waveforms and test circuit




Measurement points are given in Table 8.

**Fig. 6. Shift register clock pulse width, maximum frequency and input to output propagation delays**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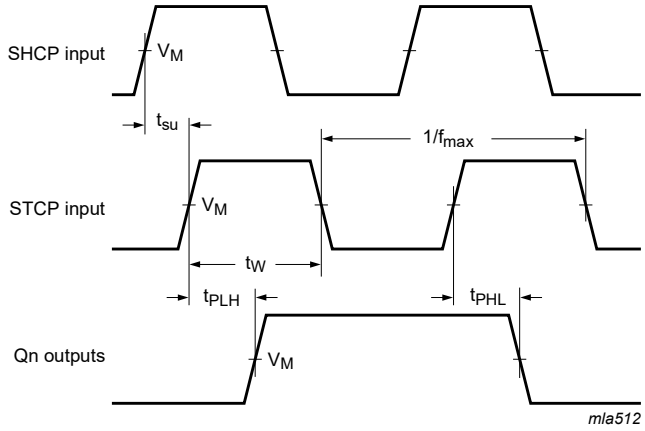
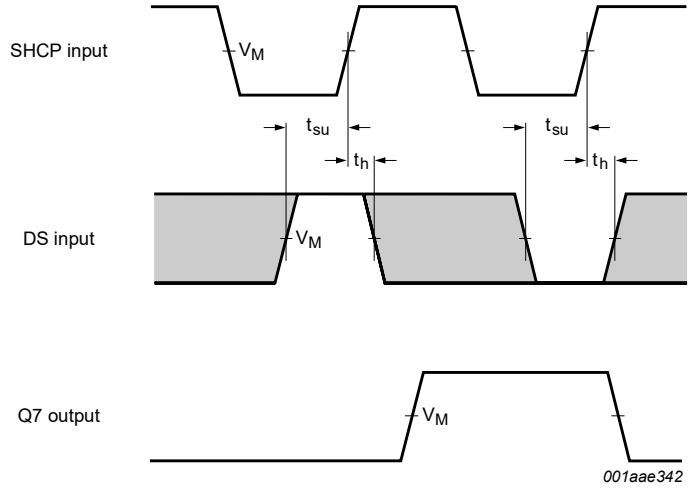



Measurement points are given in Table 8.

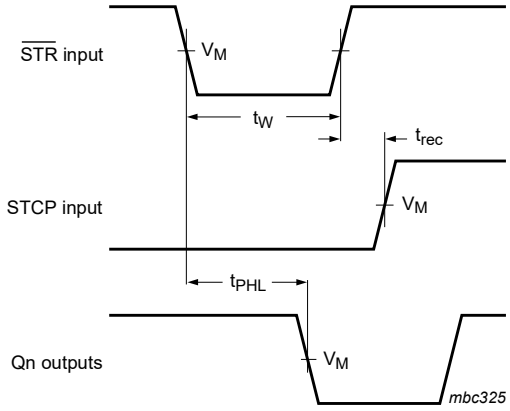
**Fig. 7. Shift register clock to storage register clock set-up time and storage clock pulse width, maximum frequency and input to output propagation delays**




Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig. 8. Shift register clock to data input set-up and hold times**




Measurement points are given in Table 8.

**Fig. 9. Storage register reset pulse width, input to output propagation delay and recovery time**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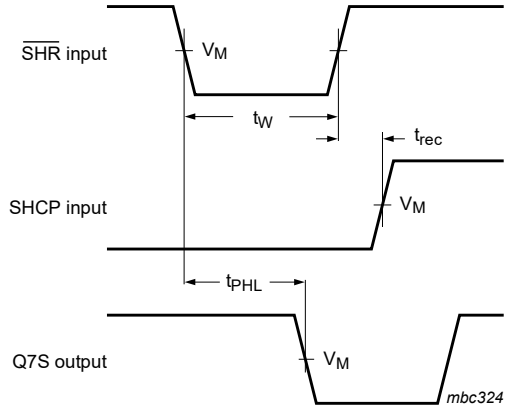
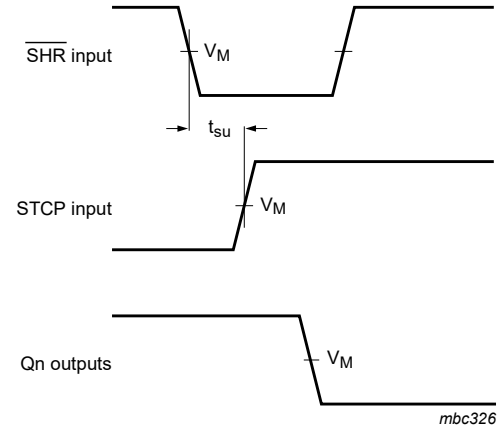



Measurement points are given in Table 8.

**Fig. 10. Shift register reset pulse width, input to output propagation delay and recovery time**




Measurement points are given in Table 8.

**Fig. 11. Shift register reset to storage register clock set-up time**

**Table 8. Measurement points**

| Type | Input | Output |
|---|---|---|
| | $V_M$ | $V_M$ |
| 74AHC594 | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ |
| 74AHCT594 | 1.5 V | 0.5 × $V_{CC}$ |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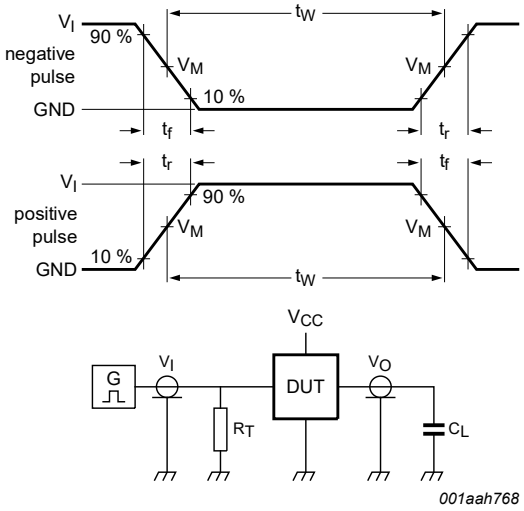


For test data see Table 9.

Definitions for test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator;

$C_L$ = Load capacitance including jig and probe capacitance.

**Fig. 12. Test circuit for measuring switching times**

**Table 9. Test data**

| Type | Input | | Load | Test |
|---|---|---|---|---|
| | $V_I$ | $t_r$, $t_f$ | $C_L$ | |
| 74AHC594 | $V_{CC}$ | ≤ 3.0 ns | 15 pF, 50 pF | $t_{PLH}$, $t_{PHL}$ |
| 74AHCT594 | 3.0 V | ≤ 3.0 ns | 15 pF, 50 pF | $t_{PLH}$, $t_{PHL}$ |


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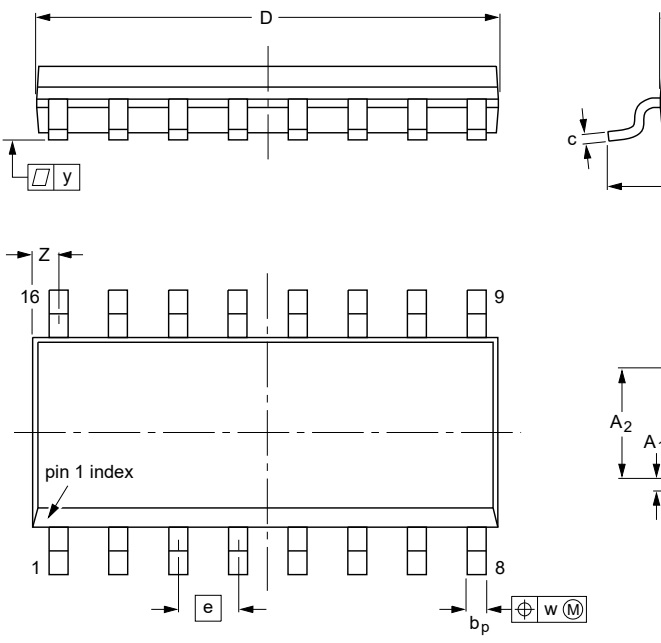
## 12. Package outline

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig. 13. Package outline SOT109-1 (SO16)**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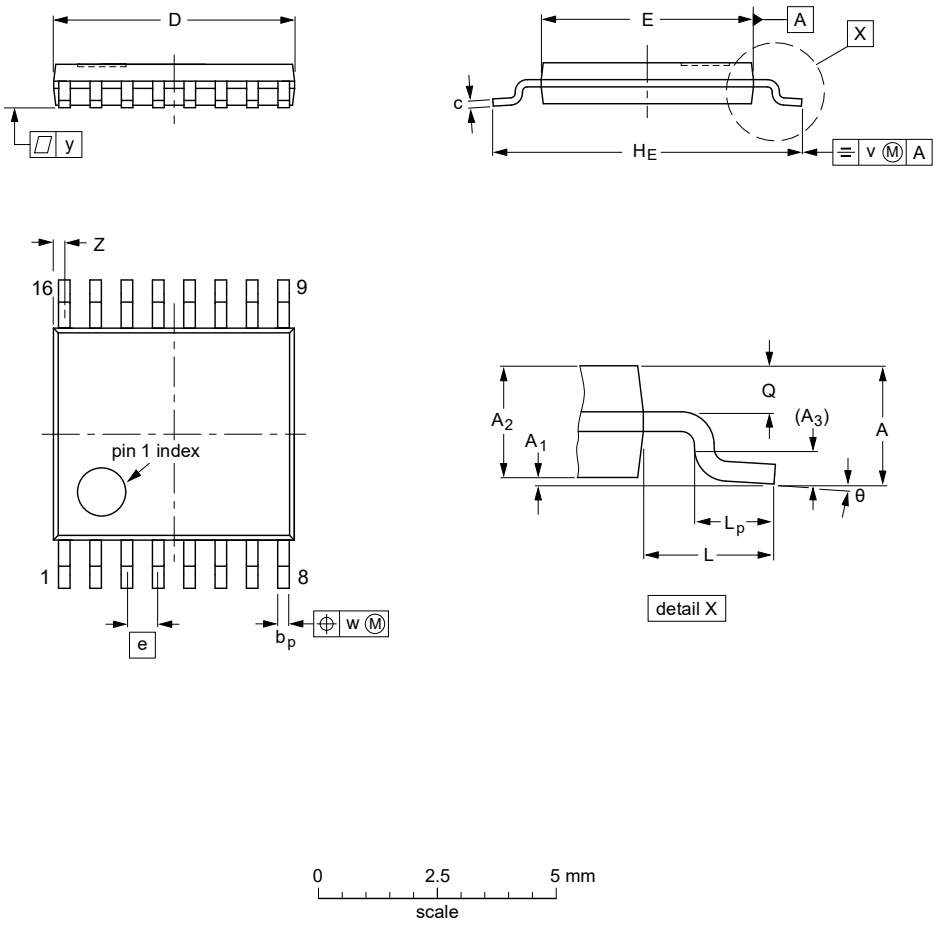
**TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm** **SOT403-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.80 | 0.25 | 0.30<br>0.19 | 0.2<br>0.1 | 5.1<br>4.9 | 4.5<br>4.3 | 0.65 | 6.6<br>6.2 | 1 | 0.75<br>0.50 | 0.4<br>0.3 | 0.2 | 0.13 | 0.1 | 0.40<br>0.06 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT403-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-18 |

**Fig. 14. Package outline SOT403-1 (TSSOP16)**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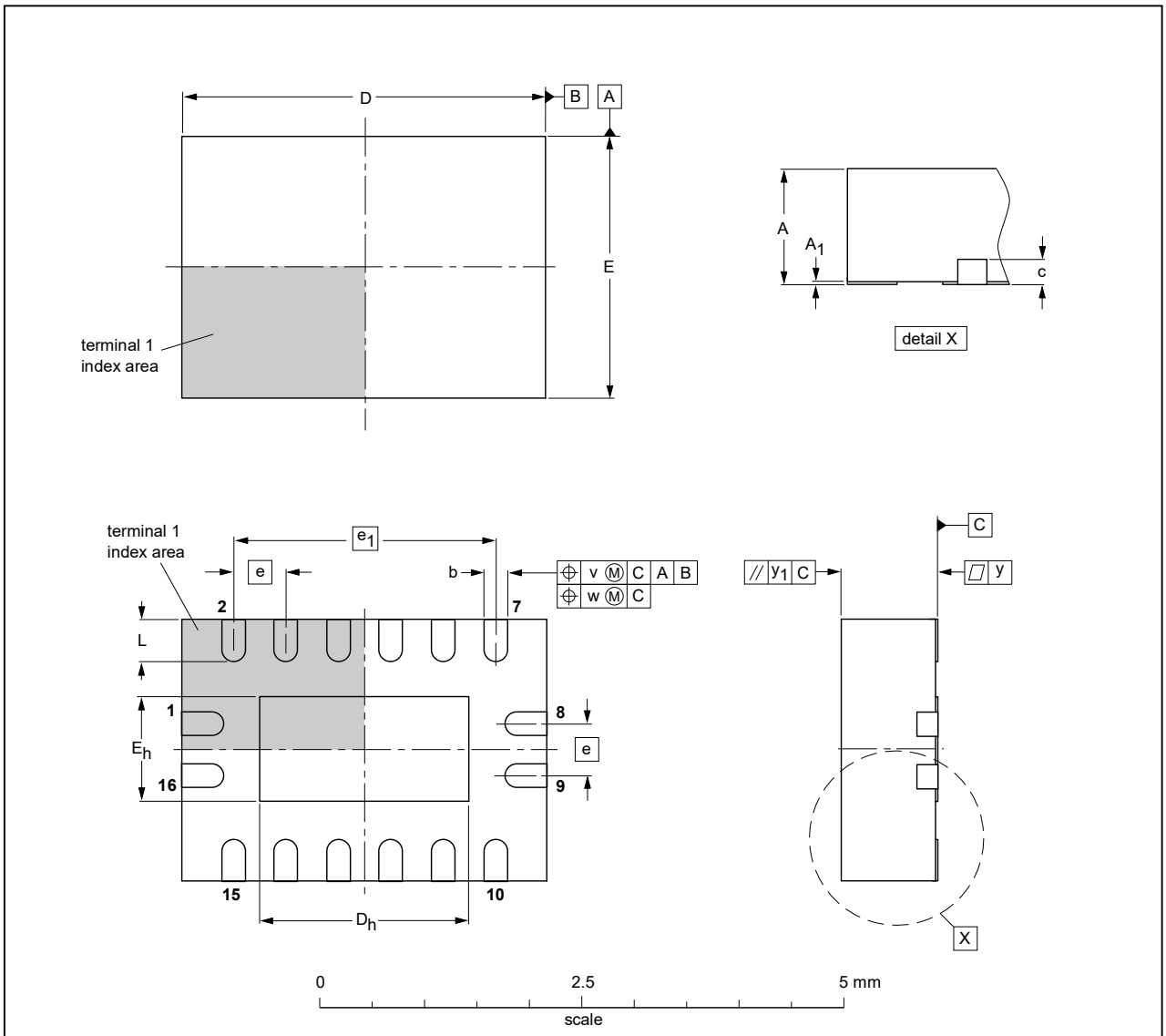
**DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm** **SOT763-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | $A^{(1)}$ max. | $A_1$ | b | c | $D^{(1)}$ | $D_h$ | $E^{(1)}$ | $E_h$ | e | $e_1$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1 | 0.05<br>0.00 | 0.30<br>0.18 | 0.2 | 3.6<br>3.4 | 2.15<br>1.85 | 2.6<br>2.4 | 1.15<br>0.85 | 0.5 | 2.5 | 0.5<br>0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT763-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~<br>03-01-27 |

**Fig. 15. Package outline SOT763-1 (DHVQFN16)**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## 13. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |
| TTL | Transistor-Transistor Logic |

## 14. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74AHC_AHCT594 v.5 | 20231009 | Product data sheet | - | 74AHC_AHCT594 v.4 |
| Modifications: | • Section 2: ESD specification updated according to the latest JEDEC standard. | | | |
| 74AHC_AHCT594 v.4 | 20210707 | Product data sheet | - | 74AHC_AHCT594 v.3 |
| Modifications: | • Type numbers 74AHC594DB and 74AHCT594DB (SOT338-1/SSOP16) removed. | | | |
| 74AHC_AHCT594 v.3 | 20200625 | Product data sheet | - | 74AHC_AHCT594 v.2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Section 2 updated.<br>• Table 4: Derating values for $P_{tot}$ total power dissipation updated. | | | |
| 74AHC_AHCT594 v.2 | 20080609 | Product data sheet | - | 74AHC_AHCT594 v.1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Table 6: the conditions for input leakage current have been changed. | | | |
| 74AHC_AHCT594 v.1 | 20060704 | Product data sheet | - | - |


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## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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**Date of release: 9 October 2023**