Wideband, Low-Distortion Fully Differential Amplifiers

Check for Samples: THS4502, THS4503

FEATURES

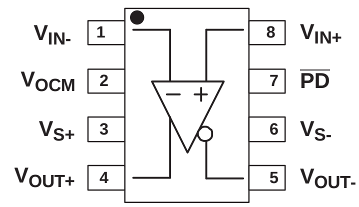
- **Fully Differential Architecture**
- **Bandwidth: 370 MHz**
- **Slew Rate: 2800 V/μs**
- **IMD_3: -95 dBc at 30 MHz**
- **OIP_3: 51 dBm at 30 MHz**
- **Output Common-Mode Control**
- **Wide Power Supply Voltage Range: 5 V, ±5 V, 12 V, 15 V**
- **Centered Input Common-Mode Range**
- **Power-Down Capability (THS4502)**
- **Evaluation Module Available**

APPLICATIONS

- **High Linearity Analog-to-Digital Converter Preamplifier**
- **Wireless Communication Receiver Chains**
- **Single-Ended to Differential Conversion**
- **Differential Line Driver**
- **Active Filtering of Differential Signals**

DESCRIPTION

The THS4502 and THS4503 are high-performance fully differential amplifiers from Texas Instruments. The THS4502, featuring power-down capability, and the THS4503, without power-down capability, set new performance standards for fully differential amplifiers with unsurpassed linearity, supporting 14-bit operation through 40 MHz. Package options include the 8-pin SOIC and the 8-pin MSOP with PowerPAD™ for a smaller footprint, enhanced ac performance, and improved thermal dissipation capability.



RELATED DEVICES

DEVICE (1)	DESCRIPTION
THS4500/1	370 MHz, 2800 V/μs, V_{ICR} Includes V_{S-}
THS4502/3	370 MHz, 2800 V/μs, Centered V_{ICR}
THS4120/1	3.3 V, 100 MHz, 43 V/μs, 3.7 nV√Hz
THS4130/1	±15 V, 150 MHz, 51 V/μs, 1.3 nV√Hz
THS4140/1	±15 V, 160 MHz, 450 V/μs, 6.5 nV√Hz
THS4150/1	±15 V, 150 MHz, 650 V/μs, 7.6 nV√Hz

(1) Even numbered devices feature power-down capability.

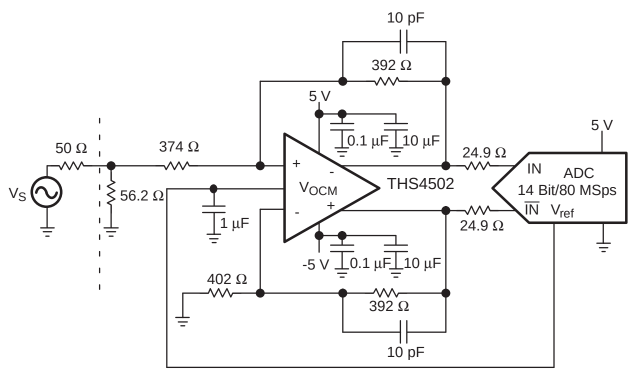
WARNING

The THS4502 and THS4503 may have low-level oscillation when the die temperature (also known as the junction temperature) exceeds +60°C. These devices are not recommended for new designs where the die temperature is expected to exceed +60°C. For more information, see Maximum Die Temperature to Prevent Oscillation section.

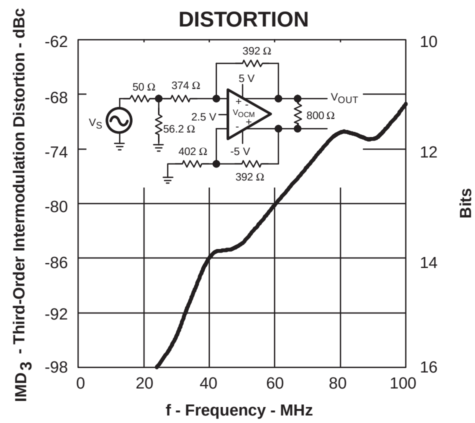
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

APPLICATION CIRCUIT DIAGRAM



THIRD-ORDER INTERMODULATION DISTORTION

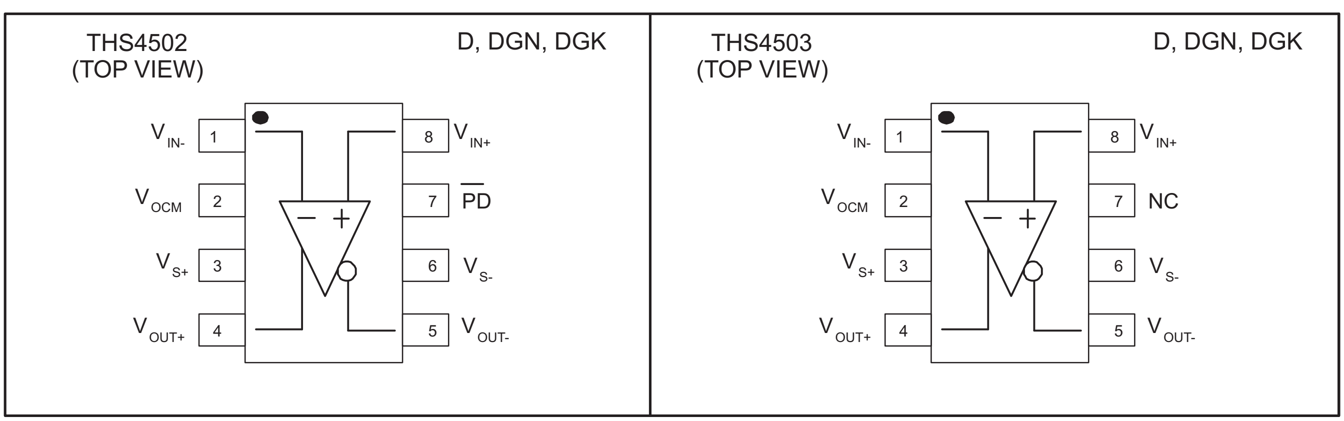


PACKAGE/ORDERING INFORMATION

TEMPERATURE	ORDERABLE PACKAGE AND NUMBER				
	PLASTIC SMALL OUTLINE	PLASTIC MSOP(1) PowerPAD		PLASTIC MSOP	
	(D)	(DGN)	SYMBOL	(DGK)	SYMBOL
0°C to 70°C	THS4502CD	THS4502CDGN	BCG	THS4502CDGK	ATX
	THS4503CD	THS4503CDGN	BCK	THS4503CDGK	ATY
-40°C to 85°C	THS4502ID	THS4502IDGN	BCI	THS4502IDGK	ASX
	THS4503ID	THS4503IDGN	BCL	THS4503IDGK	ASY

(1) All packages are available taped and reeled. The R suffix standard quatity is 2500. The T suffix standard quantity is 250 (e.g., THS4502DT).

PIN ASSIGNMENTS



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted (1)

		UNIT
Supply voltage, V_S		16.5 V
Input voltage, V_I		$\pm V_S$
Output current, I_O (2)		150 mA
Differential input voltage, V_{ID}		4 V
Continuous power dissipation		See Dissipation Rating Table
Maximum junction temperature, T_J (3)		150°C
Maximum junction temperature, continuous operation, long term reliability, T_J (4)		125°C
Maximum junction temperature to prevent oscillation, T_J (5)		60°C
Operating free-air temperature range, T_A	C suffix	0°C to 70°C
	I suffix	-40°C to 85°C
Storage temperature range, T_{stg}		-65°C to 150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The THS450x may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.
(3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.
(5) See Maximum Die Temperature to Prevent Oscillation section in the Application Information of this data sheet.

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (1) (°C/W)
D (8 pin)	38.3	97.5
DGN (8 pin)	4.7	58.4
DGK (8 pin)	54.2	260

(1) This data was taken using the JEDEC standard High-K test PCB.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage	Dual supply		±5	±7.5	V
	Single supply	4.5	5	15	
Operating free- air temperature, T_A	C suffix	0		70	°C
	I suffix	-40		85	

ELECTRICAL CHARACTERISTICS V_S = ±5 V

R_f = R_g = 499Ω , R_L = 800 Ω, G = +1, Single-ended input unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS4502 AND THS4503					
		TYP	OVER TEMPERATURE(1)				MIN/ TYP/ MAX
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	
AC PERFORMANCE							
Small-signal bandwidth	G = +1, P_{IN} = -20 dBm, R_f = 392 Ω	370				MHz	Typ
	G = +2, P_{IN} = -30 dBm, R_f = 1 kΩ	175				MHz	Typ
	G = +5, P_{IN} = -30 dBm, R_f = 1.3 kΩ	70				MHz	Typ
	G = +10, P_{IN} = -30 dBm, R_f = 1.3 kΩ	30				MHz	Typ
Gain-bandwidth product	G > +10	300				MHz	Typ
Bandwidth for 0.1 dB flatness	P_{IN} = -20 dBm	150				MHz	Typ
Large-signal bandwidth	V_P = 2 V	220				MHz	Typ
Slew rate	4 V_{PP} Step	2800				V/μs	Typ
Rise time	2 V_{PP} Step	0.8				ns	Typ
Fall time	2 V_{PP} Step	0.6				ns	Typ
Settling time to 0.01%	V_O = 4 V_{PP}	8.3				ns	Typ
Settling time to 0.1%	V_O = 4 V_{PP}	6.3				ns	Typ
Harmonic distortion	G = +1, V_O = 2 V_{PP}						Typ
2^{nd} harmonic	f = 8 MHz	-83				dBc	Typ
	f = 30 MHz	-74				dBc	Typ
3^{rd} harmonic	f = 8 MHz	-97				dBc	Typ
	f = 30 MHz	-78				dBc	Typ
Third-order intermodulation distortion	V_O = 2V_{PP}, f_c= 30 MHz, R_f = 392 Ω, 200 kHz tone spacing	-94				dBc	Typ
Third-order output intercept point	f_c = 30 MHz, R_f = 392 Ω, Referenced to 50 Ω	52				dBm	Typ
Input voltage noise	f > 1 MHz	6.8				$nV/\sqrt{Hz}$	Typ
Input current noise	f > 100 kHz	1.7				$pA/\sqrt{Hz}$	Typ
Overdrive recovery time	Overdrive = 5.5 V	75				ns	Typ
DC PERFORMANCE							
Open-loop voltage gain		55	52	50	50	dB	Min
Input offset voltage		-1	-4/+2	-5/+3	-6/+4	mV	Max
Average offset voltage drift				±10	±10	μV/°C	Typ
Input bias current		4	4.6	5	5.2	μA	Max
Average bias current drift				±10	±10	nA/°C	Typ
Input offset current		0.5	1	2	2	μA	Max
Average offset current drift				±40	±40	nA/°C	Typ
INPUT							
Common-mode input range		±4.0	±3.7	±3.4	±3.4	V	Min
Common-mode rejection ratio		80	74	70	70	dB	Min
Input impedance		10^7 || 1				Ω || pF	Typ
OUTPUT							
Differential output voltage swing	R_L = 1 kΩ	±8	±7.6	±7.4	±7.4	V	Min
Differential output current drive	R_L = 20Ω	120	110	100	100	mA	Min
Output balance error	P_{IN} = -20 dBm, f = 100 kHz	-58				dB	Typ
Closed-loop output impedance (single-ended)	f = 1 MHz	0.1				Ω	Typ

(1) See Maximum Die Temperature to Prevent Oscillation section in the Application Information of this data sheet.

ELECTRICAL CHARACTERISTICS V_S = ±5 V (continued)

$R_f = R_g$ = 499Ω , R_L = 800 Ω, G = +1, Single-ended input unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS4502 AND THS4503					
		TYP	OVER TEMPERATURE (1)				MIN/TYP/MAX
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-signal bandwidth	R_L = 400Ω	180				MHz	Typ
Slew rate	2 V_{PP} step	87				V/μs	Typ
Minimum gain		1	0.98	0.98	0.98	V/V	Min
Maximum gain		1	1.02	1.02	1.02	V/V	Max
Common-mode offset voltage		+2	-1.6/+6.8	-3.6/+8.8	-4.6/+9.8	mV	Max
Input bias current	V_{OCM} = 2.5 V	100	150	170	170	μA	Max
Input voltage range		±4	±3.7	±3.4	±3.4	V	Min
Input impedance		25 || 1				kΩ || pF	Typ
Maximum default voltage	V_{OCM} left floating	0	0.05	0.10	0.10	V	Max
Minimum default voltage	V_{OCM} left floating	0	-0.05	-0.10	-0.10	V	Min
POWER SUPPLY							
Specified operating voltage		±5	±8.25	±8.25	±8.25	V	Max
Maximum quiescent current		23	28	32	34	mA	Max
Minimum quiescent current		23	18	14	12	mA	Min
Power supply rejection (±PSRR)		80	76	73	70	dB	Min
POWER DOWN (THS4502 ONLY)							
Enable voltage threshold	Device enabled *ON* above -2.9 V		-2.9			V	Min
Disable voltage threshold	Device disabled *OFF* below -4.3 V		-4.3			V	Max
Power-down quiescent current		800	1000	1200	1200	μA	Max
Input bias current		200	240	260	260	μA	Max
Input impedance		50 || 1				kΩ || pF	Typ
Turnon time delay		1000				ns	Typ
Turnoff time delay		800				ns	Typ

ELECTRICAL CHARACTERISTICS V_S = 5 V

$R_f = R_g$ = 499 Ω, R_L = 800 Ω, G = +1, Single-ended input unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS4502 AND THS4503					
		TYP	OVER TEMPERATURE (1)				MIN/TYP/MAX
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	
AC PERFORMANCE							
Small-signal bandwidth	G = +1, P_{IN} = -20 dBm, R_f = 392 Ω	320				MHz	Typ
	G = +2, P_{IN} = -30 dBm, R_f = 1 kΩ	160				MHz	Typ
	G = +5, P_{IN} = -30 dBm, R_f = 1.3 kΩ	60				MHz	Typ
	G = +10, P_{IN} = -30 dBm, R_f = 1.3 kΩ	30				MHz	Typ
Gain-bandwidth product	G > +10	300				MHz	Typ
Bandwidth for 0.1 dB flatness	P_{IN} = -20 dBm	180				MHz	Typ
Large-signal bandwidth	V_P = 1 V	200				MHz	Typ
Slew rate	2 V_{PP} Step	1300				V/μs	Typ
Rise time	2 V_{PP} Step	0.6				ns	Typ
Fall time	2 V_{PP} Step	0.8				ns	Typ
Settling time to 0.01%	V_O = 2 V Step	13.1				ns	Typ

(1) See Maximum Die Temperature to Prevent Oscillation section in the Application Information of this data sheet.

ELECTRICAL CHARACTERISTICS V_S = 5 V (continued)

R_f = R_g = 499 Ω, R_L = 800 Ω, G = +1, Single-ended input unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS4502 AND THS4503					
		TYP	OVER TEMPERATURE (1)				MIN/TYP/MAX
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	
Settling time to 0.1%	V_O = 2 V Step	8.3				ns	Typ
Harmonic distortion	V_O = 2 V_{PP}						Typ
2nd harmonic	f = 8 MHz,	-81				dBc	Typ
	f = 30 MHz	-60				dBc	Typ
3rd harmonic	f = 8 MHz	-74				dBc	Typ
	f = 30 MHz	-62				dBc	Typ
Input voltage noise	f > 1 MHz	6.8				nV/√Hz	Typ
Input current noise	f > 100 kHz	1.6				pA/√Hz	Typ
Overdrive recovery time	Overdrive = 5.5 V	75				ns	Typ
DC PERFORMANCE							
Open-loop voltage gain		54	51	49	49	dB	Min
Input offset voltage		-0.6	-3.6/+2.4	-4.6/+3.4	-5.6/+4.4	mV	Max
Average offset voltage drift				±10	±10	μV/°C	Typ
Input bias current		4	4.6	5	5.2	μA	Max
Average bias current drift				±10	±10	nA/°C	Typ
Input offset current		0.5	0.7	1.2	1.2	μA	Max
Average offset current drift				±20	±20	nA/°C	Typ
INPUT							
Common-mode input range		1 / 4	1.3 / 3.7	1.6 / 3.4	1.6 / 3.4	V	Min
Common-mode rejection ratio		80	74	70	70	dB	Min
Input Impedance		10^7 || 1				Ω || pF	Typ
OUTPUT							
Differential output voltage swing	R_L = 1 kΩ, Referenced to 2.5 V	±3.3	±2.8	±2.6	±2.6	V	Min
Output current drive	R_L = 20Ω	100	90	80	80	mA	Min
Output balance error	P_{IN} = -20 dBm, f = 100 kHz	-58				dB	Typ
Closed-loop output impedance (single-ended)	f = 1 MHz	0.1				Ω	Typ
OUTPUT COMMON-MODE VOLTAGE CONTROL							
Small-signal bandwidth	R_L = 400 Ω	180				MHz	Typ
Slew rate	2 V_{PP} Step	80				V/μs	Typ
Minimum gain		1	0.98	0.98	0.98	V/V	Min
Maximum gain		1	1.02	1.02	1.02	V/V	Max
Common-mode offset voltage		2	-2.2/6.2	-4.2/8.2	-5.2/9.2	mV	Max
Input bias current	V_{OCM} = 2.5 V	1	2	3	3	μA	Max
Input voltage range		1/4	1.2/3.8	1.3/3.7	1.3/3.7	V	Min
Input impedance		25 || 1				kΩ || pF	Typ
Maximum default voltage	V_{OCM} left floating	2.5	2.55	2.6	2.6	V	Max
Minimum default voltage	V_{OCM} left floating	2.5	2.45	2.4	2.4	V	Min
POWER SUPPLY							
Specified operating voltage		5	16.5	16.5	16.5	V	Max
Maximum quiescent current		20	25	29	31	mA	Max
Minimum quiescent current		20	16	12	10	mA	Min
Power supply rejection (+PSRR)		75	72	69	66	dB	Min

ELECTRICAL CHARACTERISTICS V_S = 5 V (continued)

R_f = R_g = 499 Ω, R_L = 800 Ω, G = +1, Single-ended input unless otherwise noted.

PARAMETER	TEST CONDITIONS	THS4502 AND THS4503					
		TYP	OVER TEMPERATURE (1)				MIN/TYP/MAX
		25°C	25°C	0°C to 70°C	-40°C to 85°C	UNITS	
POWER DOWN (THS4502 ONLY)							
Enable voltage threshold	Device enabled *ON* above 2.1 V		2.1			V	Min
Disable voltage threshold	Device disabled *OFF* below 0.7 V		0.7			V	Max
Power-down quiescent current		600	800	1200	1200	µA	Max
Input bias current		100	125	140	140	µA	Max
Input impedance		50 || 1				kΩ || pF	Typ
Turnon time delay		1000				ns	Typ
Turnoff time delay		800				ns	Typ

TYPICAL CHARACTERISTICS

Table of Graphs (±5 V)

	FIGURE
Small signal unity gain frequency response	1
Small signal frequency response	2
0.1 dB gain flatness frequency response	3
Harmonic distortion (single-ended input to differential output) vs Frequency	4, 6, 12, 14
Harmonic distortion (differential input to differential output) vs Frequency	5, 7, 13, 15
Harmonic distortion (single-ended input to differential output) vs Output voltage swing	8, 10, 16, 18
Harmonic distortion (differential input to differential output) vs Output voltage swing	9, 11, 17, 19
Harmonic distortion (single-ended input to differential output) vs Load resistance	20
Harmonic distortion (differential input to differential output) vs Load resistance	21
Third order intermodulation distortion (single-ended input to differential output) vs Frequency	22
Third order output intercept point vs Frequency	23
Slew rate vs Differential output voltage step	24
Settling time	25, 26
Large-signal transient response	27
Small-signal transient response	28
Overdrive recovery	29, 30
Voltage and current noise vs Frequency	31
Rejection ratios vs Frequency	32
Rejection ratios vs Case temperature	33
Output balance error vs Frequency	34
Open-loop gain and phase vs Frequency	35
Open-loop gain vs Case temperature	36
Input bias and offset current vs Case temperature	37
Quiescent current vs Supply voltage	38
Input offset voltage vs Case temperature	39
Common-mode rejection ratio vs Input common-mode range	40
Differential output current drive vs Case temperature	41
Harmonic distortion (single-ended and differential input to differential output) vs Output common-mode voltage	42
Small signal frequency response at V_{OCM}	43
Output offset voltage at V_{OCM} vs Output common-mode voltage	44
Quiescent current vs Power-down voltage	45
Turnon and turnoff delay times	46
Single-ended output impedance in power down vs Frequency	47
Power-down quiescent current vs Case temperature	48
Power-down quiescent current vs Supply voltage	49

Table of Graphs (5 V)

	FIGURE
Small signal unity gain frequency response	50
Small signal frequency response	51
0.1 dB gain flatness frequency response	52
Harmonic distortion (single-ended input to differential output) vs Frequency	53, 54, 61, 63
Harmonic distortion (differential input to differential output) vs Frequency	55, 56, 62, 64
Harmonic distortion (single-ended input to differential output) vs Output voltage swing	57, 58, 65, 67
Harmonic distortion (differential input to differential output) vs Output voltage swing	59, 60, 66, 68
Harmonic distortion (single-ended input to differential output) vs Load resistance	69
Harmonic distortion (differential input to differential output) vs Load resistance	70
Slew rate vs Differential output voltage step	71
Large-signal transient response	72
Small-signal transient response	73
Voltage and current noise vs Frequency	74
Rejection ratios vs Frequency	75
Rejection ratios vs Case temperature	76
Output balance error vs Frequency	77
Open-loop gain and phase vs Frequency	78
Open-loop gain vs Case temperature	79
Input bias and offset current vs Case temperature	80
Quiescent current vs Supply voltage	81
Input offset voltage vs Case temperature	82
Common-mode rejection ratio vs Input common-mode range	83
Output drive vs Case temperature	84
Harmonic distortion (single-ended and differential input) vs Output common-mode range	85
Small signal frequency response at V_{OCM}	86
Output offset voltage vs Output common-mode voltage	87
Quiescent current vs Power-down voltage	88
Turnon and turnoff delay times	89
Single-ended output impedance in power down vs Frequency	90
Power-down quiescent current vs Case temperature	91
Power-down quiescent current vs Supply voltage	92

TYPICAL CHARACTERISTICS (±5 V Graphs)

SMALL SIGNAL UNITY GAIN FREQUENCY RESPONSE

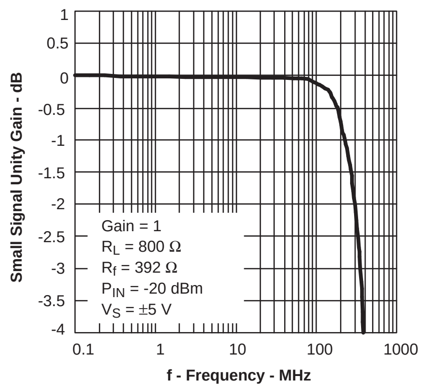


Figure 1.

SMALL SIGNAL FREQUENCY RESPONSE

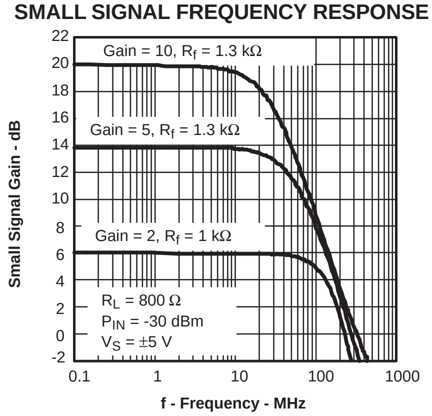


Figure 2.

0.1 dB GAIN FLATNESS FREQUENCY RESPONSE

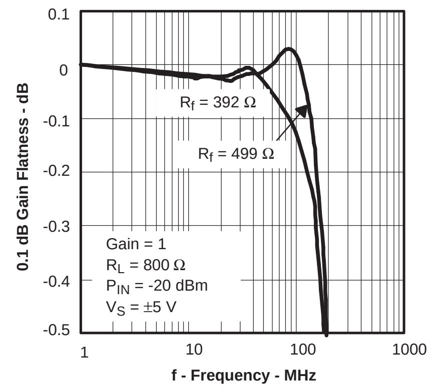


Figure 3.

HARMONIC DISTORTION vs FREQUENCY

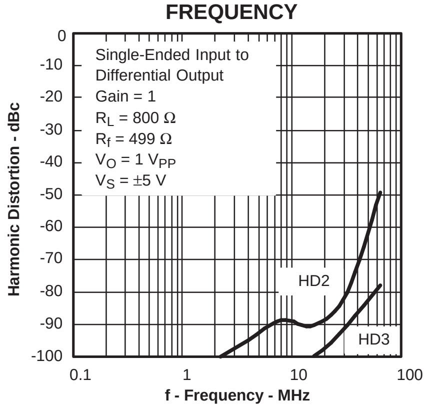


Figure 4.

HARMONIC DISTORTION vs FREQUENCY

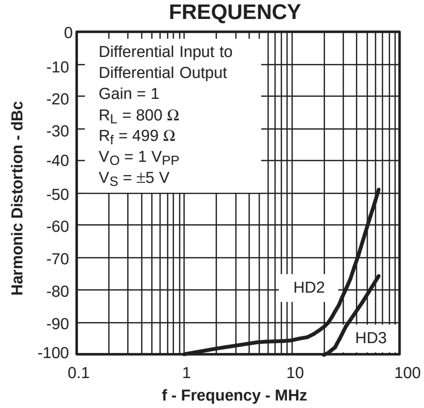


Figure 5.

HARMONIC DISTORTION vs FREQUENCY

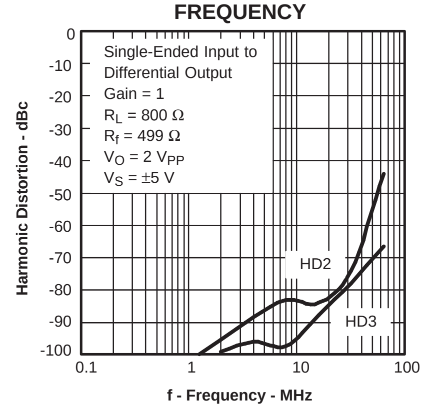


Figure 6.

HARMONIC DISTORTION vs FREQUENCY

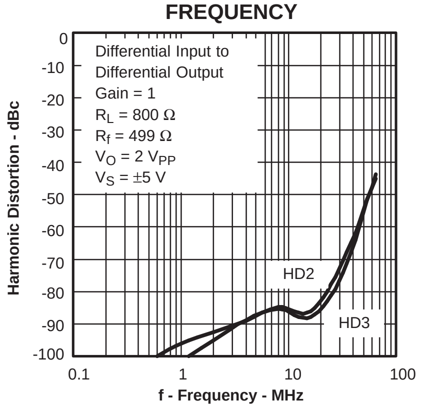


Figure 7.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

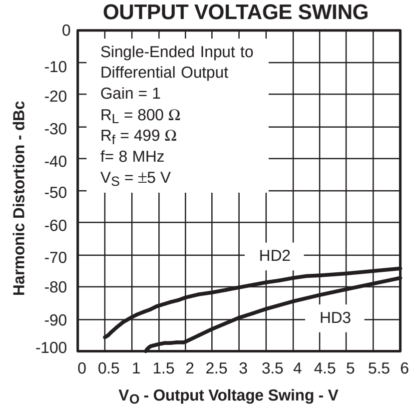


Figure 8.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

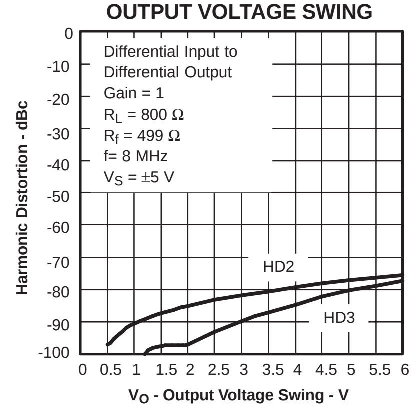


Figure 9.

TYPICAL CHARACTERISTICS (±5 V Graphs) (continued)

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

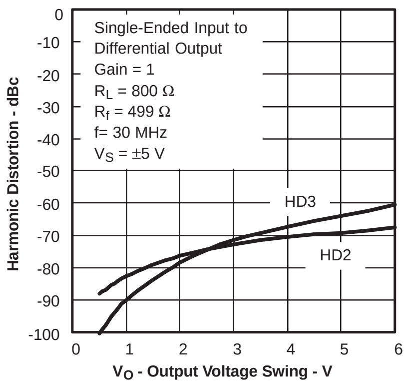


Figure 10.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

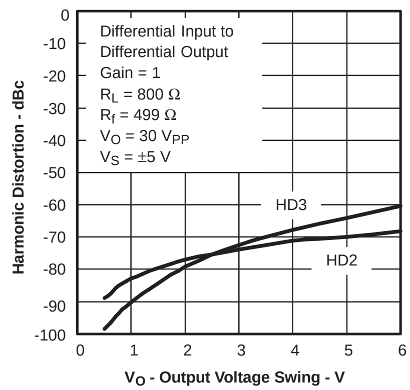


Figure 11.

HARMONIC DISTORTION vs FREQUENCY

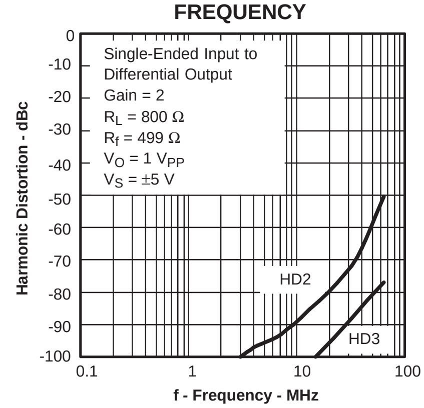


Figure 12.

HARMONIC DISTORTION vs FREQUENCY

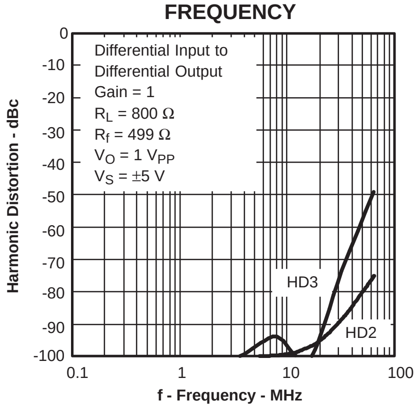


Figure 13.

HARMONIC DISTORTION vs FREQUENCY

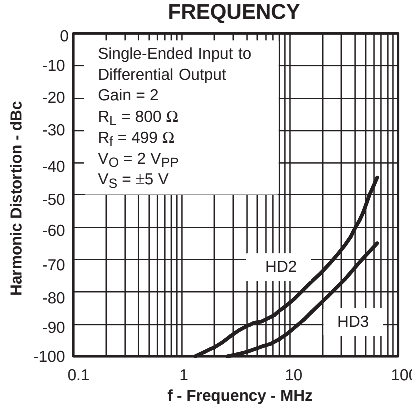


Figure 14.

HARMONIC DISTORTION vs FREQUENCY

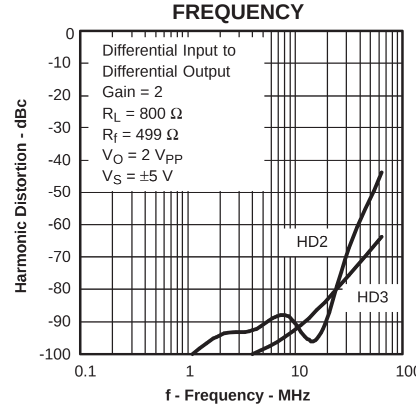


Figure 15.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

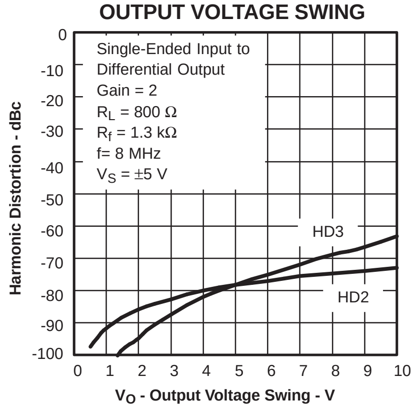


Figure 16.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

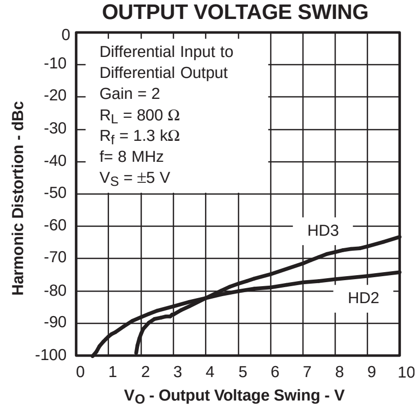


Figure 17.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

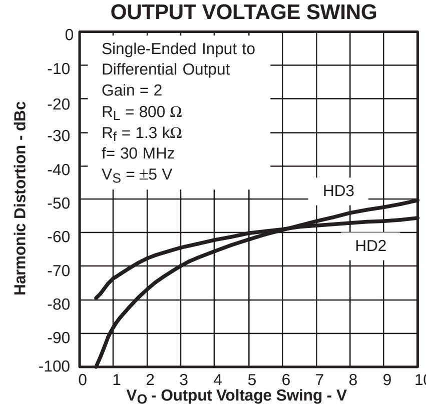


Figure 18.

TYPICAL CHARACTERISTICS (±5 V Graphs) (continued)

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

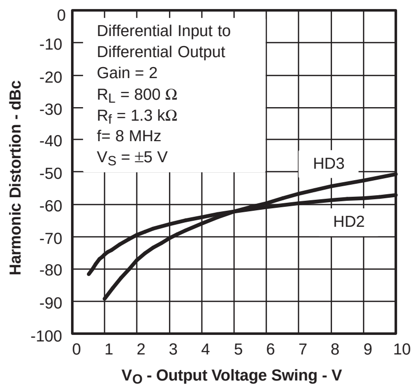


Figure 19.

HARMONIC DISTORTION vs LOAD RESISTANCE

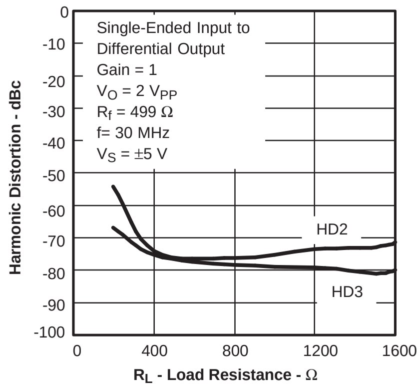


Figure 20.

HARMONIC DISTORTION vs LOAD RESISTANCE

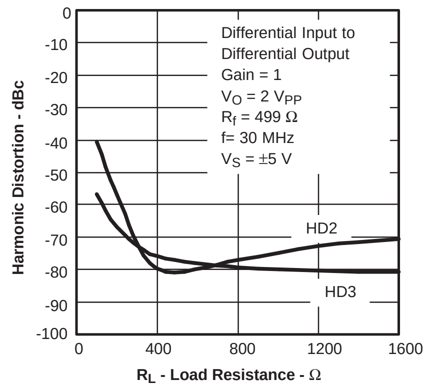


Figure 21.

THIRD-ORDER INTERMODULATION DISTORTION vs FREQUENCY

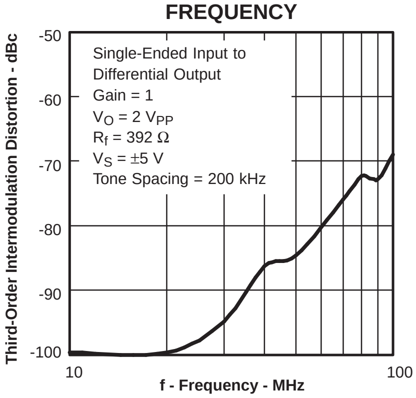


Figure 22.

THIRD-ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

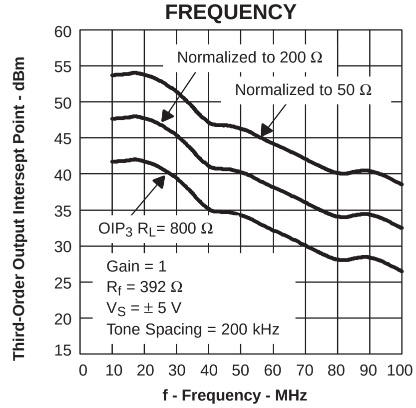


Figure 23.

SLEW RATE vs DIFFERENTIAL OUTPUT VOLTAGE STEP

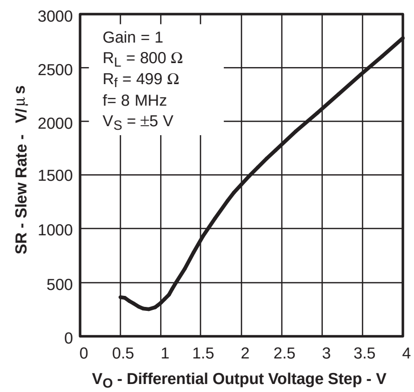


Figure 24.

SETTLING TIME

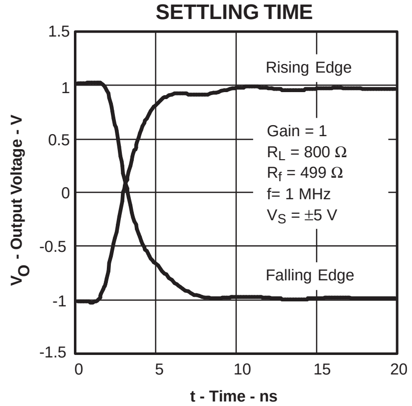


Figure 25.

SETTLING TIME

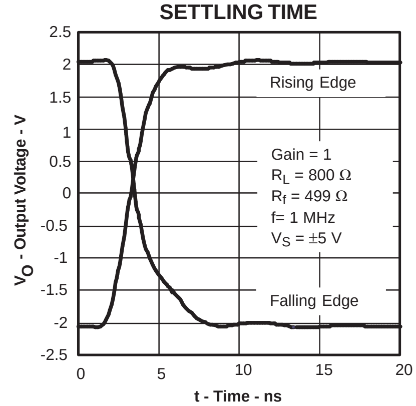


Figure 26.

LARGE-SIGNAL TRANSIENT RESPONSE

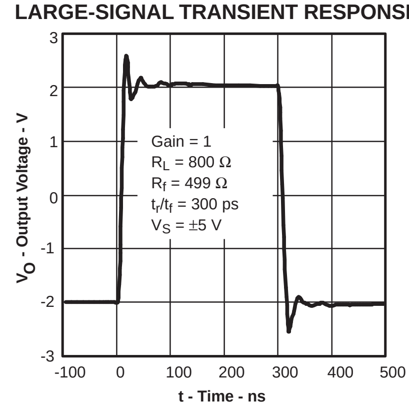


Figure 27.

TYPICAL CHARACTERISTICS (±5 V Graphs) (continued)

SMALL-SIGNAL TRANSIENT RESPONSE

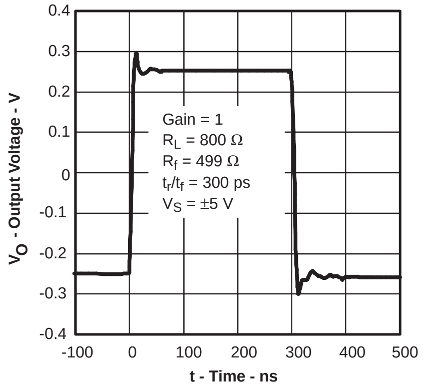


Figure 28.

OVERDRIVE RECOVERY

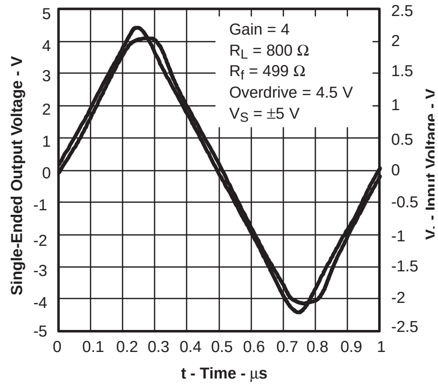


Figure 29.

OVERDRIVE RECOVERY

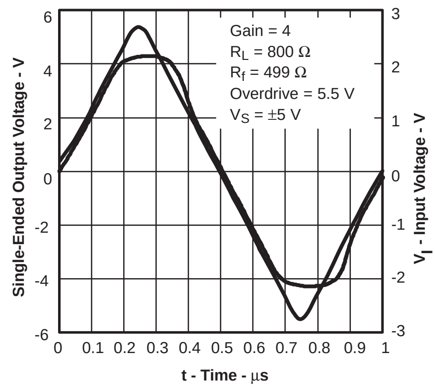


Figure 30.

VOLTAGE AND CURRENT NOISE vs FREQUENCY

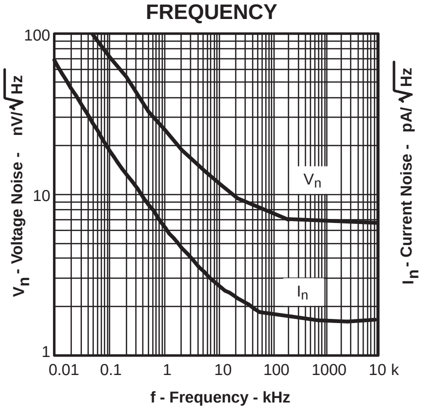


Figure 31.

REJECTION RATIOS vs FREQUENCY

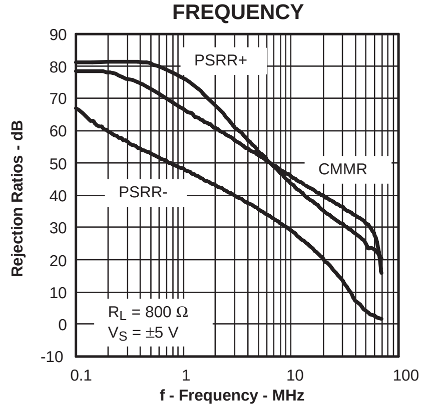


Figure 32.

REJECTION RATIOS vs CASE TEMPERATURE

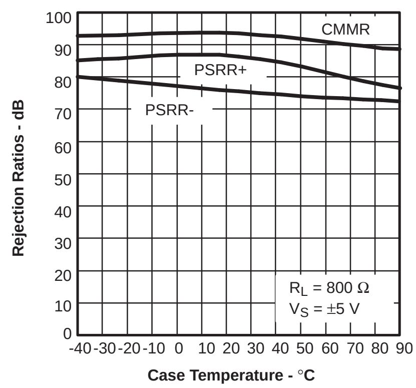


Figure 33.

OUTPUT BALANCE ERROR vs FREQUENCY

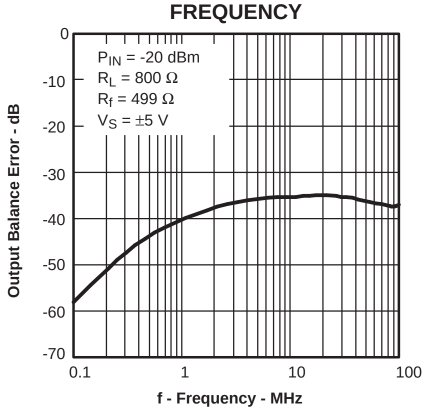


Figure 34.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

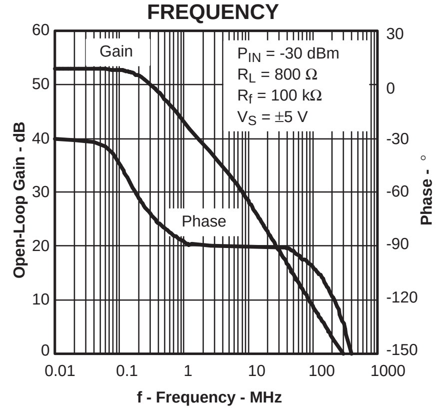


Figure 35.

OPEN-LOOP GAIN vs CASE TEMPERATURE

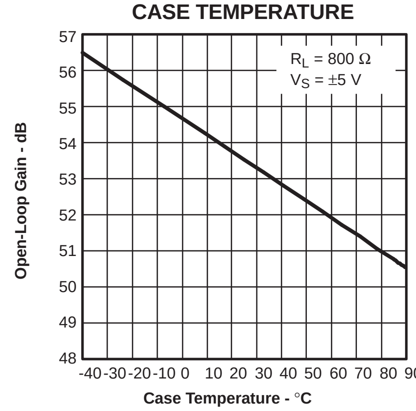


Figure 36.

TYPICAL CHARACTERISTICS (±5 V Graphs) (continued)

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

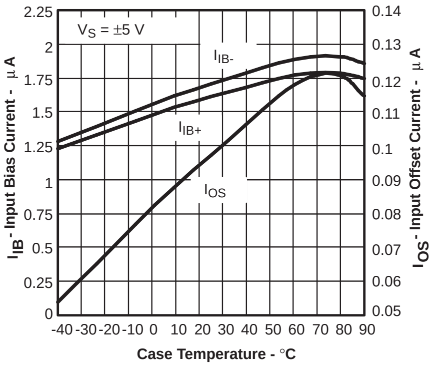


Figure 37.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

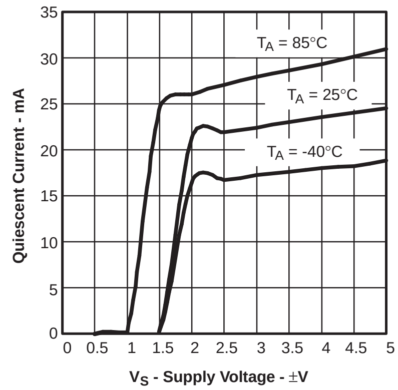


Figure 38.

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

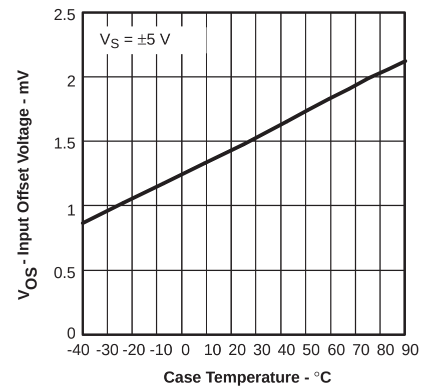


Figure 39.

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

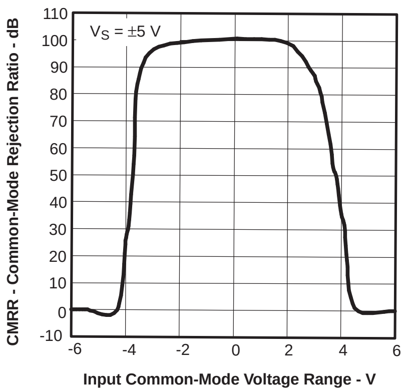


Figure 40.

DIFFERENTIAL OUTPUT CURRENT DRIVE vs CASE TEMPERATURE

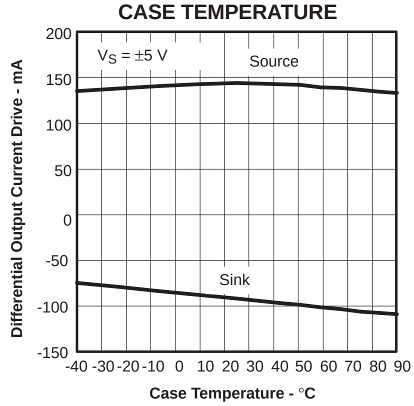


Figure 41.

HARMONIC DISTORTION vs OUTPUT COMMON-MODE VOLTAGE

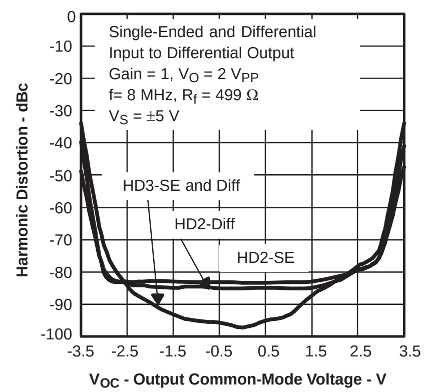


Figure 42.

SMALL SIGNAL FREQUENCY RESPONSE AT V_{OCM}

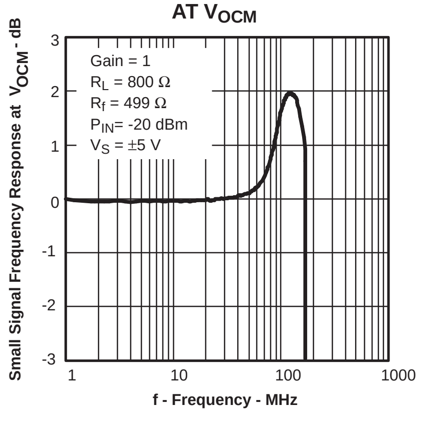


Figure 43.

OUTPUT OFFSET VOLTAGE AT V_{OCM} vs OUTPUT COMMON-MODE VOLTAGE

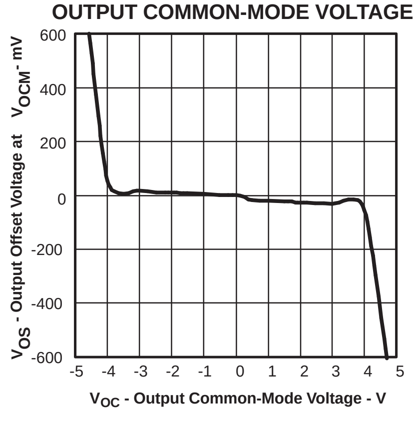


Figure 44.

QUIESCENT CURRENT vs POWER-DOWN VOLTAGE

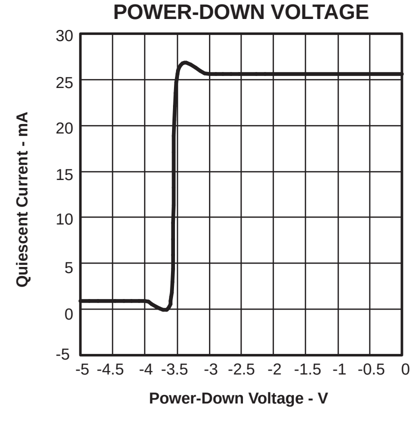


Figure 45.

TYPICAL CHARACTERISTICS (±5 V Graphs) (continued)

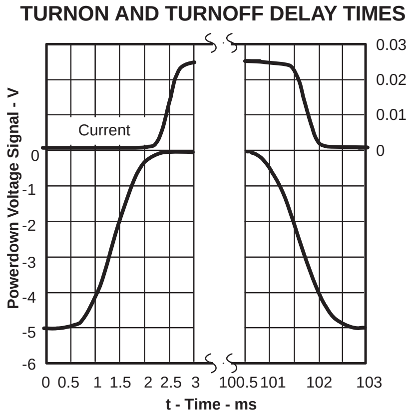


Figure 46.

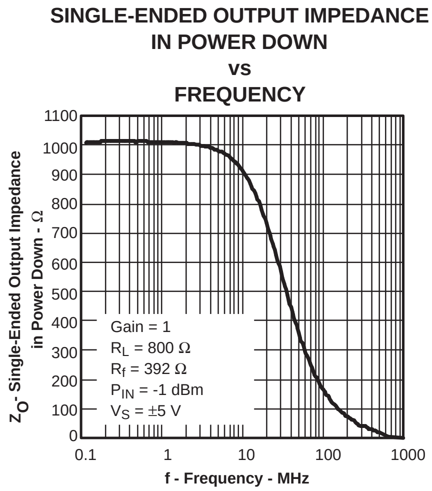


Figure 47.

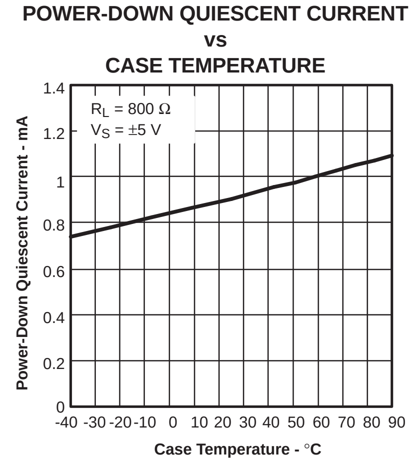


Figure 48.

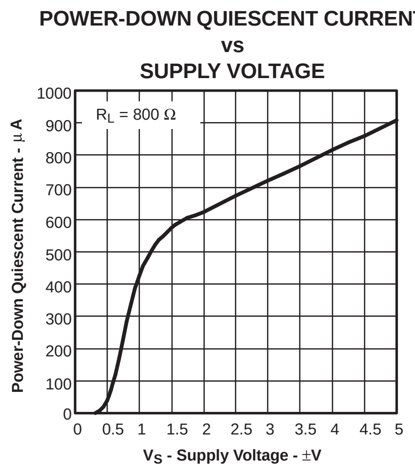


Figure 49.

TYPICAL CHARACTERISTICS (5 V GRAPHS)

SMALL SIGNAL UNITY GAIN FREQUENCY RESPONSE

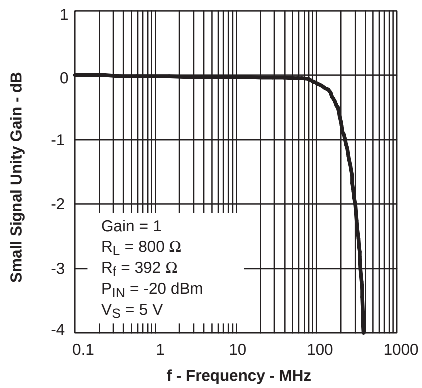


Figure 50.

SMALL SIGNAL FREQUENCY RESPONSE

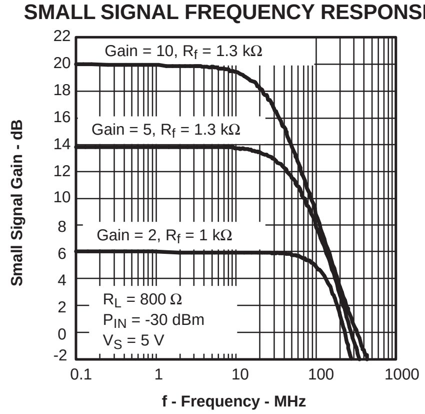


Figure 51.

0.1 dB GAIN FLATNESS FREQUENCY RESPONSE

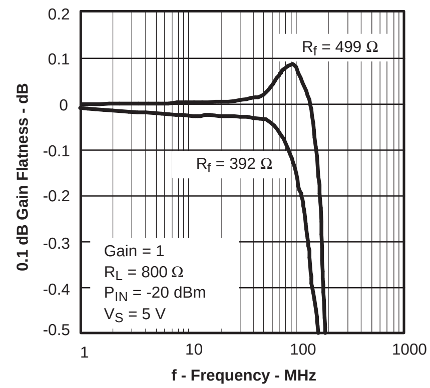


Figure 52.

HARMONIC DISTORTION vs FREQUENCY

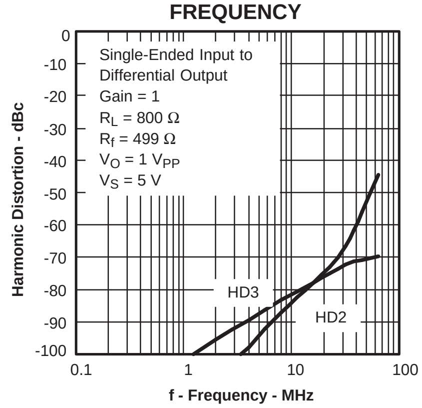


Figure 53.

HARMONIC DISTORTION vs FREQUENCY

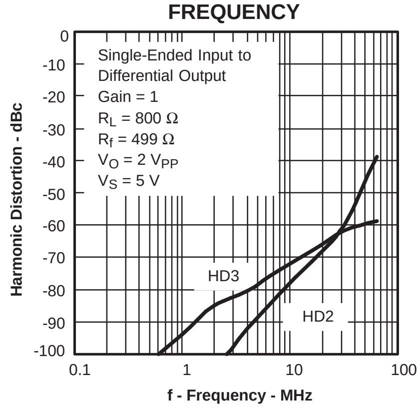


Figure 54.

HARMONIC DISTORTION vs FREQUENCY

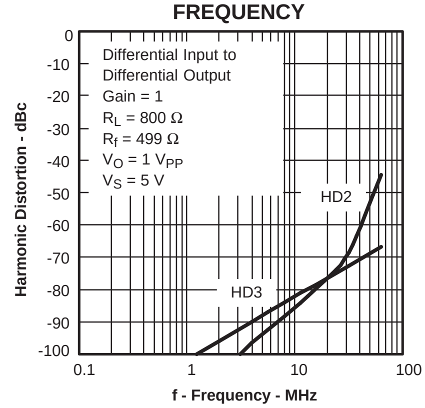


Figure 55.

HARMONIC DISTORTION vs FREQUENCY

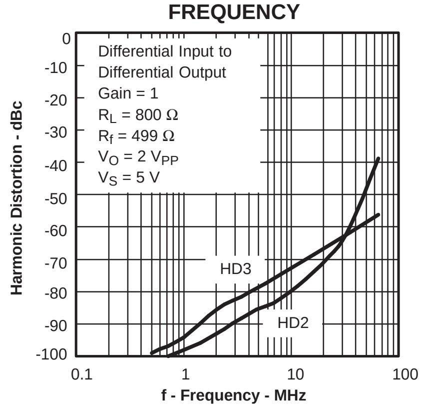


Figure 56.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

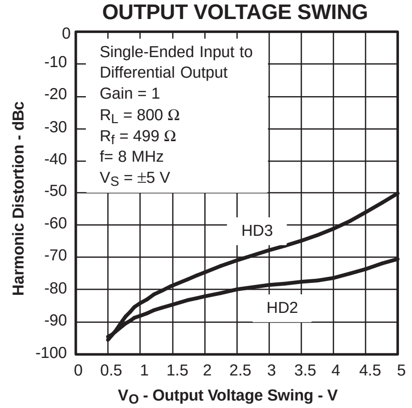


Figure 57.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

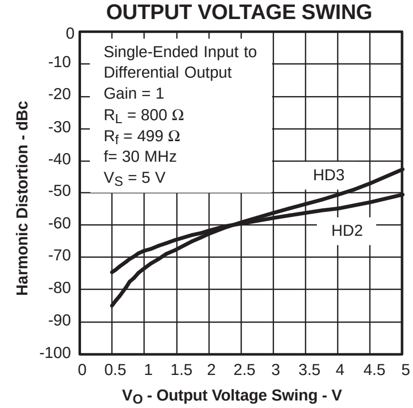


Figure 58.

TYPICAL CHARACTERISTICS (5 V GRAPHS) (continued)

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

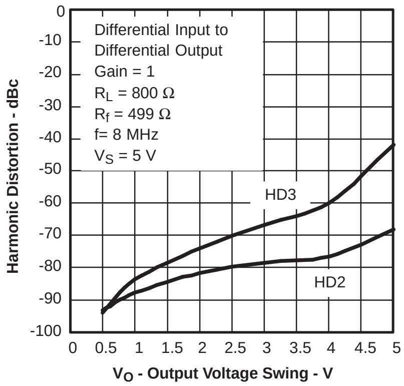


Figure 59.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

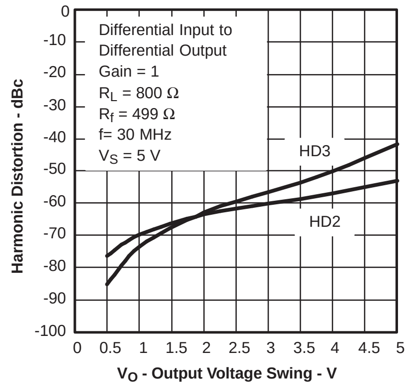


Figure 60.

HARMONIC DISTORTION vs FREQUENCY

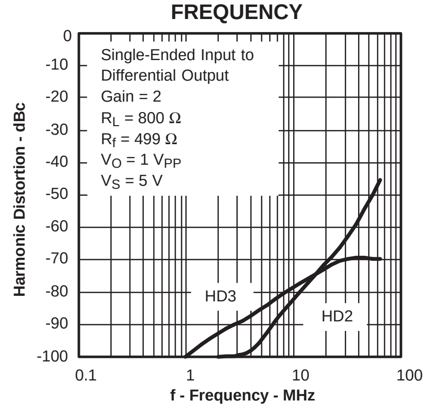


Figure 61.

HARMONIC DISTORTION vs FREQUENCY

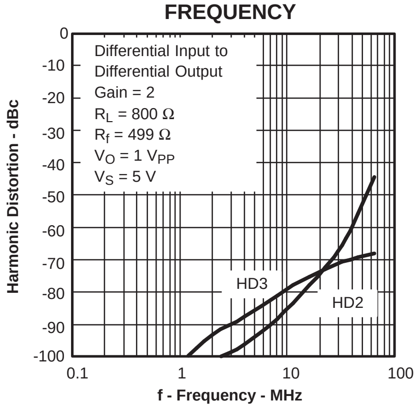


Figure 62.

HARMONIC DISTORTION vs FREQUENCY

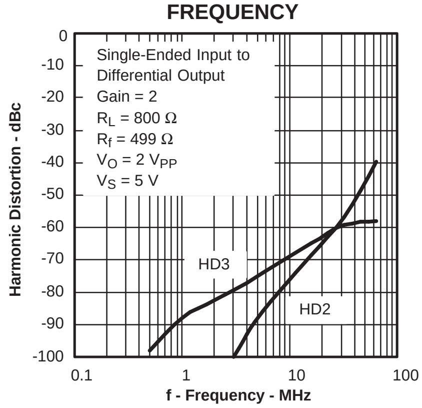


Figure 63.

HARMONIC DISTORTION vs FREQUENCY

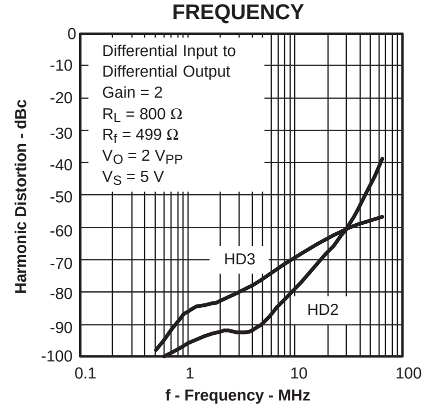


Figure 64.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

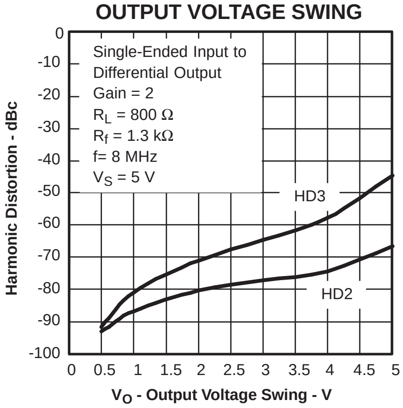


Figure 65.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

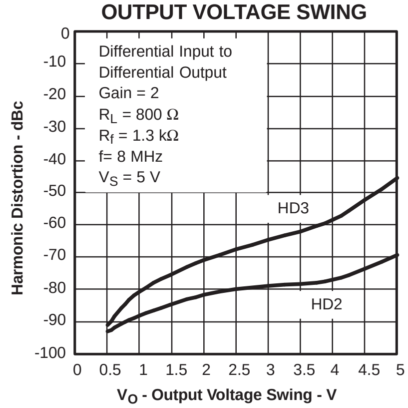


Figure 66.

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

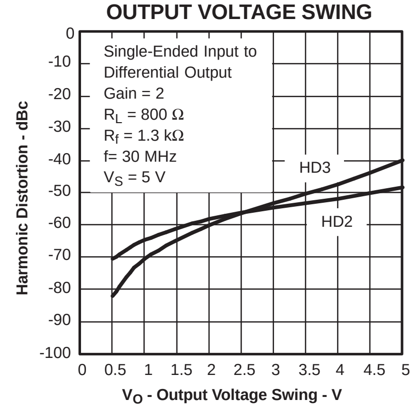


Figure 67.

TYPICAL CHARACTERISTICS (5 V GRAPHS) (continued)

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

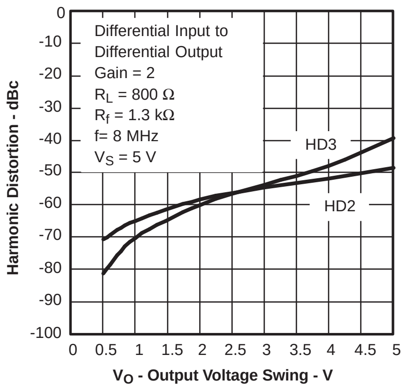


Figure 68.

HARMONIC DISTORTION vs LOAD RESISTANCE

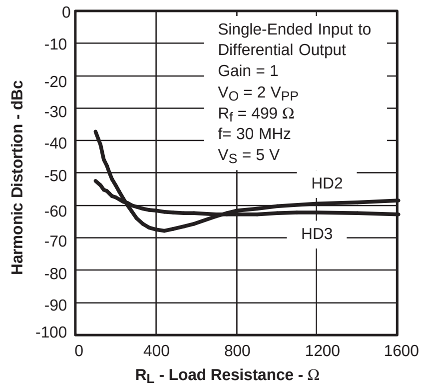


Figure 69.

HARMONIC DISTORTION vs LOAD RESISTANCE

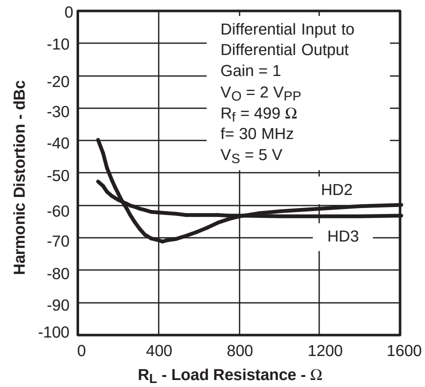


Figure 70.

SLEW RATE vs DIFFERENTIAL OUTPUT VOLTAGE STEP

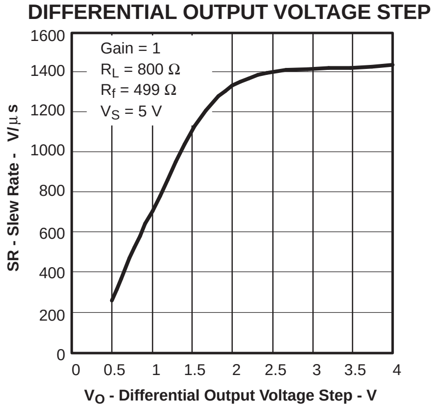


Figure 71.

LARGE-SIGNAL TRANSIENT RESPONSE

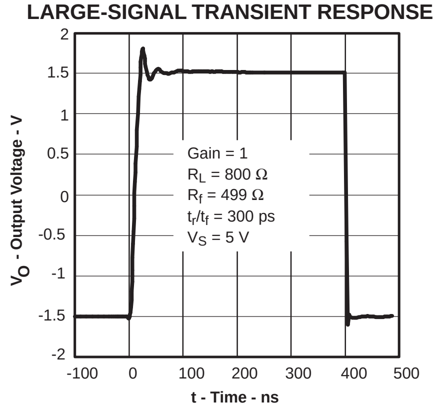


Figure 72.

SMALL-SIGNAL TRANSIENT RESPONSE

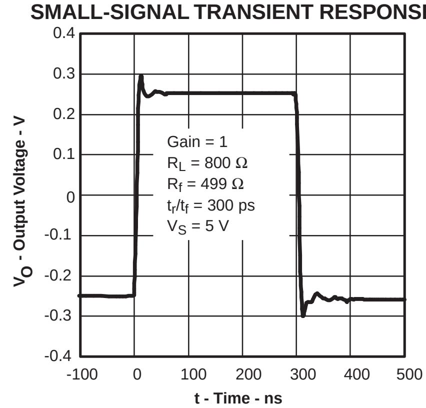


Figure 73.

VOLTAGE AND CURRENT NOISE vs FREQUENCY

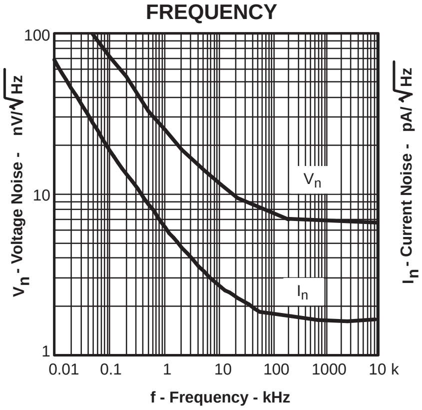


Figure 74.

REJECTION RATIOS vs FREQUENCY

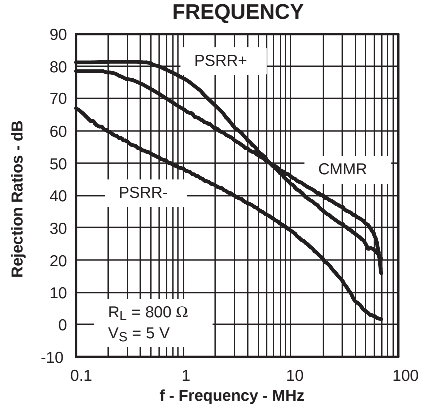


Figure 75.

REJECTION RATIOS vs CASE TEMPERATURE

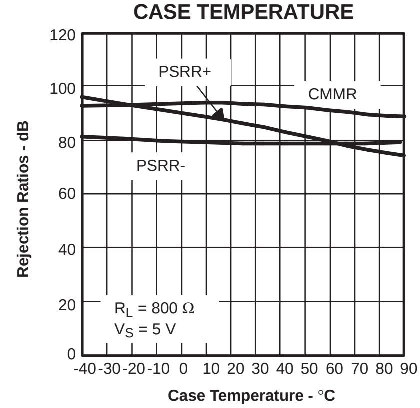


Figure 76.

TYPICAL CHARACTERISTICS (5 V GRAPHS) (continued)

OUTPUT BALANCE ERROR vs FREQUENCY

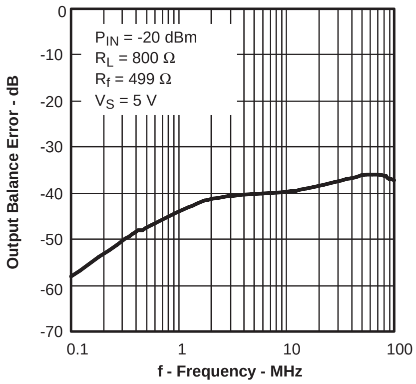


Figure 77.

OPEN-LOOP GAIN AND PHASE vs FREQUENCY

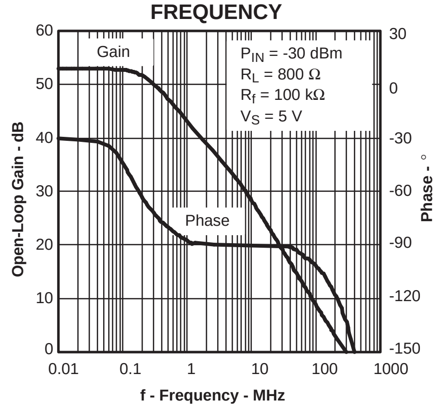


Figure 78.

OPEN-LOOP GAIN vs CASE TEMPERATURE

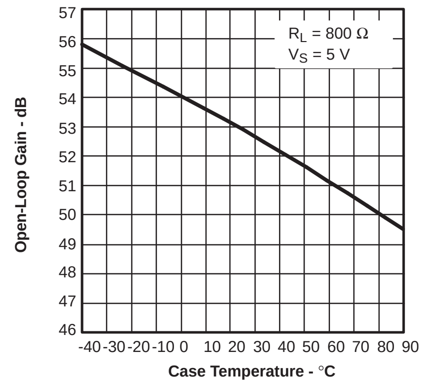


Figure 79.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

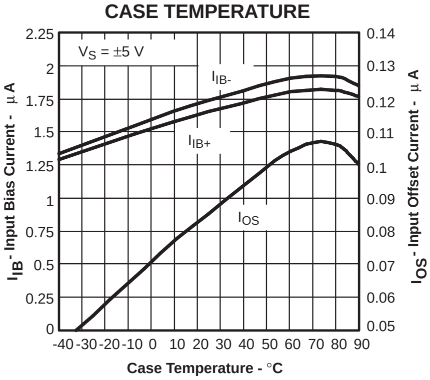


Figure 80.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

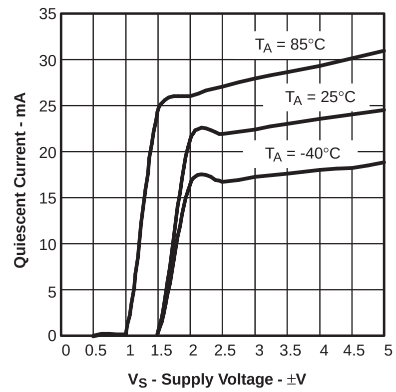


Figure 81.

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

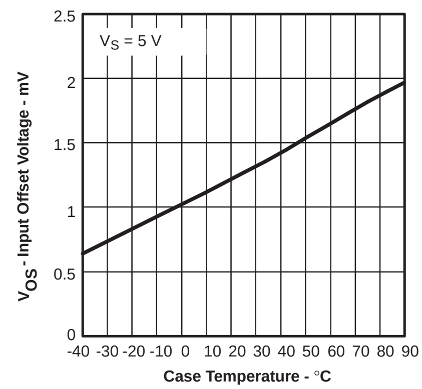


Figure 82.

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

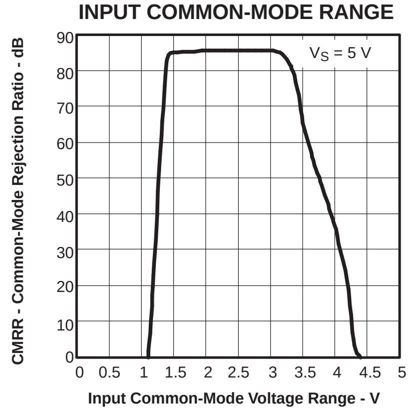


Figure 83.

OUTPUT DRIVE vs CASE TEMPERATURE

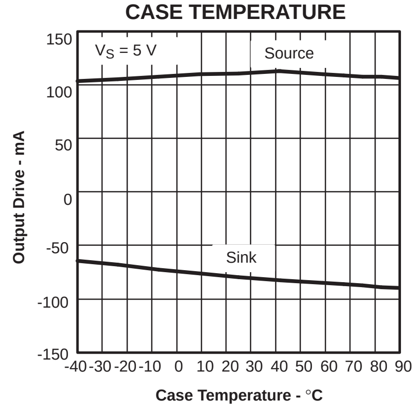


Figure 84.

HARMONIC DISTORTION vs OUTPUT COMMON-MODE VOLTAGE

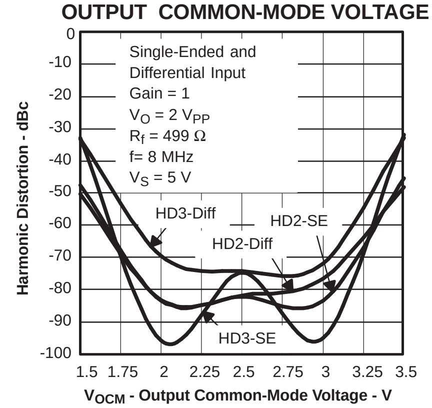


Figure 85.

TYPICAL CHARACTERISTICS (5 V GRAPHS) (continued)

SMALL SIGNAL FREQUENCY RESPONSE at V_{OCM}

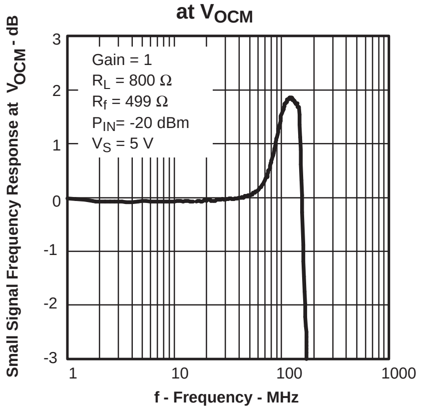


Figure 86.

OUTPUT OFFSET VOLTAGE vs OUTPUT COMMON-MODE VOLTAGE

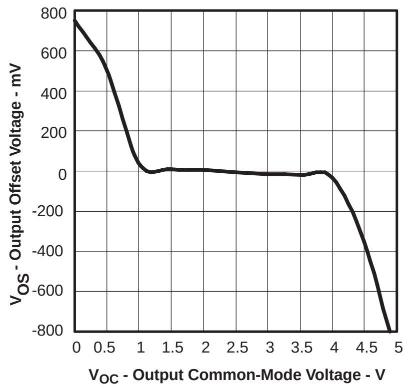


Figure 87.

QUIESCENT CURRENT vs POWER-DOWN VOLTAGE

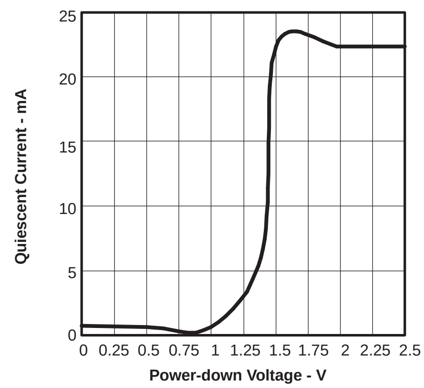


Figure 88.

TURNON AND TURNOFF DELAY TIMES

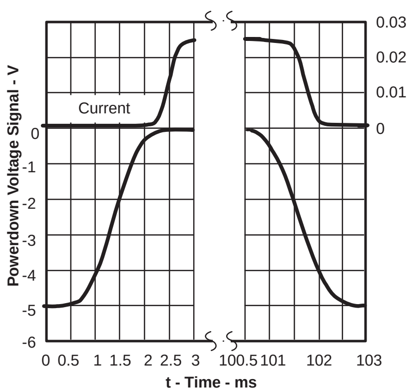


Figure 89.

SINGLE-ENDED OUTPUT IMPEDANCE IN POWER DOWN vs FREQUENCY

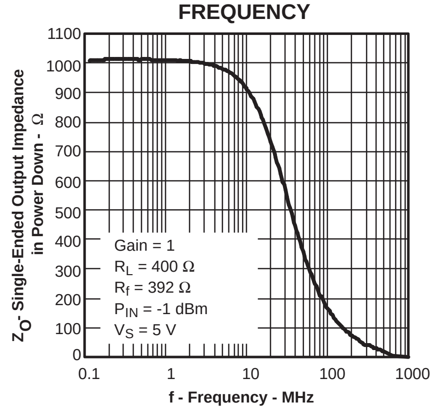


Figure 90.

POWER-DOWN QUIESCENT CURRENT vs CASE TEMPERATURE

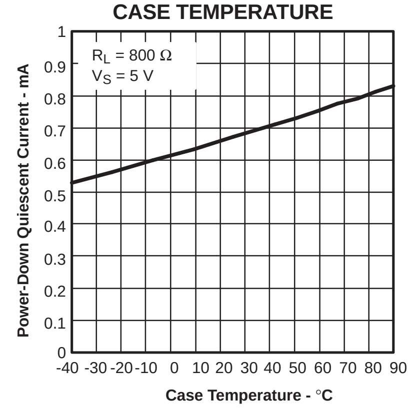


Figure 91.

POWER-DOWN QUIESCENT CURRENT vs SUPPLY VOLTAGE

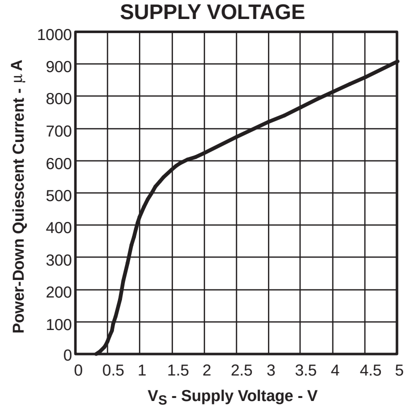


Figure 92.

APPLICATION INFORMATION

MAXIMUM DIE TEMPERATURE TO PREVENT OSCILLATION

The THS4502 and THS4503 may have low level oscillation when the die temperature (also called junction temperature) exceeds +60°C and is not recommended for new designs where the die temperature is expected to exceed +60°C.

The oscillation is due to internal design and external configuration is not expected to mitigate or reduce the problem. This problem is random due to normal process variations and normal testing cannot identify problem units.

The THS4500 and THS4501 are recommended replacement devices.

The die temperature depends on the power dissipation and the thermal resistance of the device and can be approximated with the following formula:

$$\text{Die Temperature} = P_{DISS} \times \theta J_A + T_A$$

Where:

$$P_{DISS} \approx (V_{S\ (TOTAL)} \times I_Q) + (V_{S+} - V_{OUT}) \times I_{OUT}$$

Table 1 shows the estimated maximum ambient temperature (T_A max) in °C for each package option of the THS4502 and THS4503 using the thermal dissipation rating given in the PACKAGE DISSIPATION RATINGS table for a JEDEC standard High-K test PCB. For each case shown, $V_{S\ (TOTAL)}$ = 10V, R_L = 800 Ω differential, and the quiescent current = 32mA (the maximum over 0°C to 70°C temperature range). The last entry for each package option lists the worst case where the output voltage is 5V DC.

Table 1. Estimated Maximum Ambient Temperature Per Package Option

PACKAGE/DEVICE	V_{out}	ΘJ_A	T_A MAX
SOIC	0V	97.5°C/W	28.8°C
	2 Vpp		28.0°C
THS4502D THS4503D	4 Vpp		27.3°C
	6 Vpp		26.8°C
	8 Vpp		26.3°C
Worst Case =>	5 DC		25.8°C
PWR Pad MSOP	0V	58.4°C/W	41.3°C
	2 Vpp		40.8°C
THS4502DGN THS4503DGN	4 Vpp		40.4°C
	6 Vpp		40.1°C
	8 Vpp		39.8°C
Worst Case =>	5 DC		39.5°C
MSOP	0V	260°C/W	-23.2°C
	2 Vpp		-25.3°C
THS4502DGK THS4503DGK	4 Vpp		-27.1°C
	6 Vpp		-28.6°C
	8 Vpp		-29.8°C
Worst Case =>	5 DC		-31.3°C

FULLY DIFFERENTIAL AMPLIFIERS

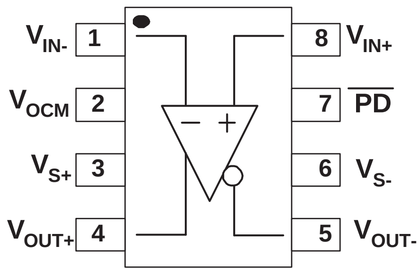
Differential signaling offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order nonlinearities, and increased dynamic range. Fully differential amplifiers not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals for easier, higher performance processing. The THS4500 family of amplifiers contains products in Texas Instruments' expanding line of high-performance fully differential amplifiers. Information on fully differential amplifier fundamentals, as well as implementation specific information, is presented in the applications section of this data sheet to provide a better understanding of the operation of the THS4500 family of devices, and to simplify the design process for designs using these amplifiers.

Applications Section

- Fully Differential Amplifier Terminal Functions
- Input Common-Mode Voltage Range and the THS4500 Family
- Choosing the Proper Value for the Feedback and Gain Resistors
- Application Circuits Using Fully Differential Amplifiers
- Key Design Considerations for Interfacing to an Analog-to-Digital Converter
- Setting the Output Common-Mode Voltage With the V_{OCM} Input
- Saving Power With Power-Down Functionality
- Linearity: Definitions, Terminology, Circuit Techniques, and Design Tradeoffs
- An Abbreviated Analysis of Noise in Fully Differential Amplifiers
- Printed-Circuit Board Layout Techniques for Optimal Performance
- Power Dissipation and Thermal Considerations
- Power Supply Decoupling Techniques and Recommendations
- Evaluation Fixtures, Spice Models, and Applications Support
- Additional Reference Material

FULLY DIFFERENTIAL AMPLIFIER TERMINAL FUNCTIONS

Fully differential amplifiers are typically packaged in eight-pin packages as shown in the diagram. The device pins include two inputs (V_{IN+},V_{IN-}), two outputs (V_{OUT-},V_{OUT+}), two power supplies (V_{S+}, V_{S-}), an output common-mode control pin (V_{OCM}), and an optional power-down pin (PD).

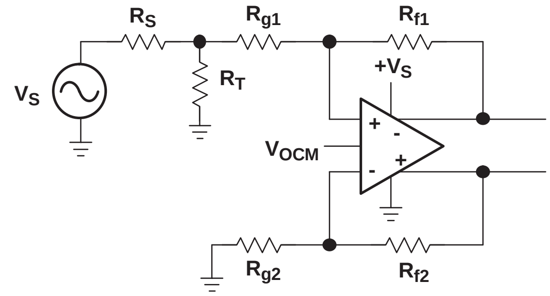


Fully Differential Amplifier Pin Diagram

A standard configuration for the device is shown in the figure. The functionality of a fully differential amplifier can be imagined as two inverting amplifiers that share a common noninverting terminal (though the voltage is not necessarily fixed). For more information on the basic theory of operation for fully differential amplifiers, refer to the Texas Instruments application note titled *Fully Differential Amplifiers*, literature number SLOA054.

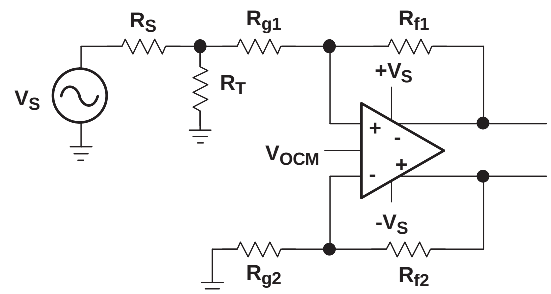
INPUT COMMON-MODE VOLTAGE RANGE AND THE THS4500 FAMILY

The key difference between the THS4500/1 and the THS4502/3 is the input common-mode range for the two devices. The THS4502 and THS4503 have an input common-mode range that is centered around midrail, and the THS4500 and THS4501 have an input common-mode range that is shifted to include the negative power supply rail. Selection of one or the other is determined by the nature of the application. Specifically, the THS4500 and THS4501 are designed for use in single-supply applications where the input signal is ground-referenced, as depicted in Figure 93. The THS4502 and THS4503 are designed for use in single-supply or split-supply applications where the input signal is centered between the power supply voltages, as depicted in Figure 94.



Application Circuit for the THS4500 and THS4501, Featuring Single-Supply Operation With a Ground-Referenced Input Signal

Figure 93.



Application Circuit for the THS4500 and THS4501, Featuring Split-Supply Operation With an Input Signal Referenced at the Midrail

Figure 94.

Equations 1-5 allow for calculation of the required input common-mode range for a given set of input conditions.

The equations allow calculation of the input common-mode range requirements given information about the input signal, the output voltage swing, the gain, and the output common-mode voltage. Calculating the maximum and minimum voltage required for V_N and V_P (the amplifier's input nodes) determines whether or not the input common-mode range is violated or not. Four equations are required. Two calculate the output voltages and two calculate the node voltages at V_N and V_P (note that only one of these needs calculation, as the amplifier forces a virtual short between the two nodes).

$$V_{OUT+} = \frac{V_{IN+}(1-\beta) - V_{IN-}(1-\beta) + 2V_{OCM}\beta}{2\beta} \quad (1)$$

$$V_{OUT-} = \frac{-V_{IN+}(1-\beta) + V_{IN-}(1-\beta) + 2V_{OCM}\beta}{2\beta} \quad (2)$$

$$V_N = V_{IN-}(1-\beta) + V_{OUT+}\beta \quad (3)$$

Where: $$\beta = \frac{R_G}{R_F + R_G} \quad (4)$$

$$V_P = V_{IN+}(1-\beta) + V_{OUT-}\beta \quad (5)$$

NOTE

The equations denote the device inputs as V_N and V_P, and the *circuit* inputs as V_{IN+} and V_{IN-}.

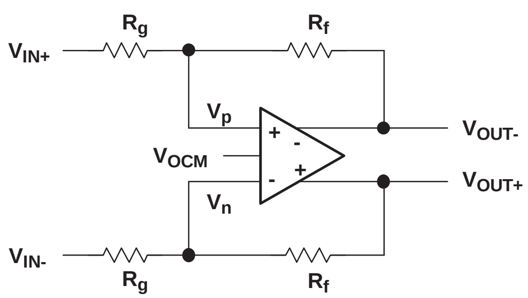


Diagram For Input Common-Mode Range Equations

Figure 95.

The two tables below depict the input common-mode range requirements for two different input scenarios, an input referenced around the negative rail and an input referenced around midrail. The tables highlight the differing requirements on input common-mode range, and illustrate reasoning for choosing either the THS4500/1 or the THS4502/3. For signals referenced around the negative power supply, the THS4500/1 should be chosen since its input common-mode range includes the negative supply rail. For all other situations, the THS4502/3 offers slightly improved distortion and noise performance for applications with input signals centered between the power supply rails.

Table 2. Negative-Rail Referenced

Gain (V/V)	V_{IN+} (V)	V_{IN-} (V)	V_{IN} (V_{PP})	V_{OCM} (V)	V_{OD} (V_{PP})	V_{NMIN} (V)	V_{NMAX} (V)
1	-2.0 to 2.0	0	4	2.5	4	0.75	1.75
2	-1.0 to 1.0	0	2	2.5	4	0.5	1.167
4	-0.5 to 0.5	0	1	2.5	4	0.3	0.7
8	-0.25 to 0.25	0	0.5	2.5	4	0.167	0.389

Table 2. Negative-Rail Referenced (continued)

Gain (V/V)	V_{IN+} (V)	V_{IN-} (V)	V_{IN} (V_{PP})	V_{OCM} (V)	V_{OD} (V_{PP})	V_{NMIN} (V)	V_{NMAX} (V)
NOTE: This table assumes a negative-rail referenced, single-ended input signal on a single 5-V supply as shown in Figure 93. $V_{NMIN} = V_{PMIN}$ and $V_{NMAX} = V_{PMAX}$							

Table 3. Midrail Referenced

Gain (V/V)	V_{IN+} (V)	V_{IN-} (V)	V_{IN} (V_{PP})	V_{OCM} (V)	V_{OD} (V_{PP})	V_{NMIN} (V)	V_{NMAX} (V)
1	0.5 to 4.5	2.5	4	2.5	4	2	3
2	1.5 to 3.5	2.5	2	2.5	4	2.16	2.83
4	2.0 to 3.0	2.5	1	2.5	4	2.3	2.7
8	2.25 to 2.75	2.5	0.5	2.5	4	2.389	2.61
NOTE: This table assumes a midrail referenced, single-ended input signal on a single 5-V supply. $V_{NMIN} = V_{PMIN}$ and $V_{NMAX} = V_{PMAX}$							

CHOOSING THE PROPER VALUE FOR THE FEEDBACK AND GAIN RESISTORS

The selection of feedback and gain resistors impacts circuit performance in a number of ways. The values in this section provide the optimum high frequency performance (lowest distortion, flat frequency response). Since the THS4500 family of amplifiers is developed with a voltage feedback architecture, the choice of resistor values does not have a dominant effect on bandwidth, unlike a current feedback amplifier. However, resistor choices do have second-order effects. For optimal performance, the following feedback resistor values are recommended. In higher gain configurations (gain greater than two), the feedback resistor values have much less effect on the high frequency performance. Example feedback and gain resistor values are given in the section on basic design considerations (Table 4).

Amplifier loading, noise, and the flatness of the frequency response are three design parameters that should be considered when selecting feedback resistors. Larger resistor values contribute more noise and can induce peaking in the ac response in low gain configurations, and smaller resistor values can load the amplifier more heavily, resulting in a reduction in distortion performance. In addition, feedback resistor values, coupled with gain requirements, determine the value of the gain resistors, directly impacting the input impedance of the entire circuit. While there are no strict rules about resistor selection, these trends can provide qualitative design guidance.

APPLICATION CIRCUITS USING FULLY DIFFERENTIAL AMPLIFIERS

Fully differential amplifiers provide designers with a great deal of flexibility in a wide variety of applications. This section provides an overview of some common circuit configurations and gives some design guidelines. Designing the interface to an ADC, driving lines differentially, and filtering with fully differential amplifiers are a few of the circuits that are covered.

BASIC DESIGN CONSIDERATIONS

The circuits in Figures 96 through 100 are used to highlight basic design considerations for fully differential amplifier circuit designs.

Table 4. Resistor Values for Balanced Operation in Various Gain Configurations

Gain $\left(\frac{V_{OD}}{V_{IN}}\right)$	**R2 & R4 (Ω)**	**R1 (Ω)**	**R3 (Ω)**	**R_T (Ω)**
1	392	412	383	54.9
1	499	523	487	53.6
2	392	215	187	60.4
2	1.3k	665	634	52.3
5	1.3k	274	249	56.2
5	3.32k	681	649	52.3
10	1.3k	147	118	64.9
10	6.81k	698	681	52.3
NOTE: Values in this table assume a 50 Ω source impedance.				

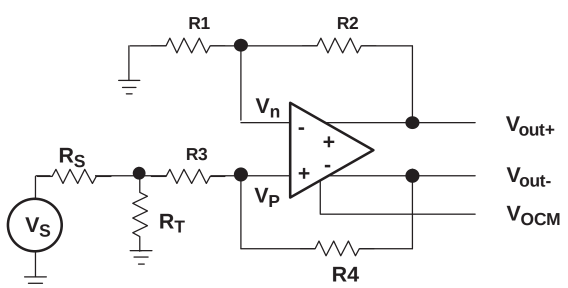


Figure 96.

Equations for calculating fully differential amplifier resistor values in order to obtain balanced operation in the presence of a 50-Ω source impedance are given in equations 6 through 9.

$$R_T = \frac{1}{\frac{1}{R_S} - \frac{1 - \frac{K}{2(1+K)}}{R3}} \qquad K = \frac{R2}{R1} \qquad R2 = R4 \qquad R3 = R1 - \left(R_s \parallel R_T\right) \tag{6}$$

$$\beta_1 = \frac{R1}{R1 + R2} \qquad \beta_2 = \frac{R3 + R_T \parallel R_S}{R3 + R_T \parallel R_S + R4} \tag{7}$$

$$\frac{V_{OD}}{V_S} = 2\left(\frac{1-\beta_2}{\beta_1 + \beta_2}\right)\left(\frac{R_T}{R_T + R_S}\right) \tag{8}$$

$$\frac{V_{OD}}{V_{IN}} = 2\left(\frac{1-\beta_2}{\beta_1 + \beta_2}\right) \tag{9}$$

For more detailed information about balance in fully differential amplifiers, see *Fully Differential Amplifiers*, referenced at the end of this data sheet.

INTERFACING TO AN ANALOG-TO-DIGITAL CONVERTER

The THS4500 family of amplifiers are designed specifically to interface to today's highest-performance analog-to-digital converters. This section highlights the key concerns when interfacing to an ADC and provides example ADC/fully differential amplifier interface circuits.

Key design concerns when interfacing to an analog-to-digital converter:

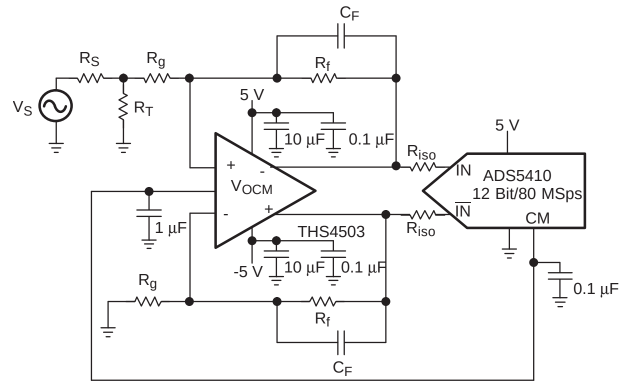
- Terminate the input source properly. In high-frequency receiver chains, the source feeding the fully differential amplifier requires a specific load impedance (e.g., 50Ω).
- Design a symmetric printed-circuit board layout. Even-order distortion products are heavily influenced by layout, and careful attention to a symmetric layout will minimize these distortion products.
- Minimize inductance in power supply decoupling traces and components. Poor power supply decoupling can have a dramatic effect on circuit performance. Since the outputs are differential, differential currents exist in the power supply pins. Thus, decoupling capacitors should be placed in a manner that minimizes the impedance of the current loop.
- Use separate analog and digital power supplies and grounds. Noise (bounce) in the power supplies (created by digital switching currents) can couple directly into the signal path, and power supply noise can create higher distortion products as well.
- Use care when filtering. While an RC low-pass filter may be desirable on the output of the amplifier to filter broadband noise, the excess loading can negatively impact the amplifier linearity. Filtering in the feedback path does not have this effect.
- AC-coupling allows easier circuit design. If dc-coupling is required, be aware of the excess power dissipation that can occur due to level-shifting the output through the output

common-mode voltage control.

- Do not terminate the output unless required. Many open-loop, class-A amplifiers require 50-Ω termination for proper operation, but closed-loop fully differential amplifiers drive a specific output voltage regardless of the load impedance present. Terminating the output of a fully differential amplifier with a heavy load adversely effects the amplifier's linearity.
- Comprehend the V_{OCM} input drive requirements. Determine if the ADC's voltage reference can provide the required amount of current to move V_{OCM} to the desired value. A buffer may be needed.
- Decouple the V_{OCM} pin to eliminate the antenna effect. V_{OCM} is a high-impedance node that can act as an antenna. A large decoupling capacitor on this node eliminates this problem.
- Be cognizant of the input common-mode range. If the input signal is referenced around the negative power supply rail (e.g., around ground on a single 5 V supply), then the THS4500/1 accommodates the input signal. If the input signal is referenced around midrail, choose the THS4502/3 for the best operation.
- Packaging makes a difference at higher frequencies. If possible, choose the smaller, thermally enhanced MSOP package for the best performance. As a rule, lower junction temperatures provide better performance. If possible, use a thermally enhanced package, even if the power dissipation is relatively small compared to the maximum power dissipation rating to achieve the best results.
- Comprehend the effect of the load impedance seen by the fully differential amplifier when performing system-level intercept point calculations. Lighter loads (such as those presented by an ADC) allow smaller intercept points to support the same level of intermodulation distortion performance.

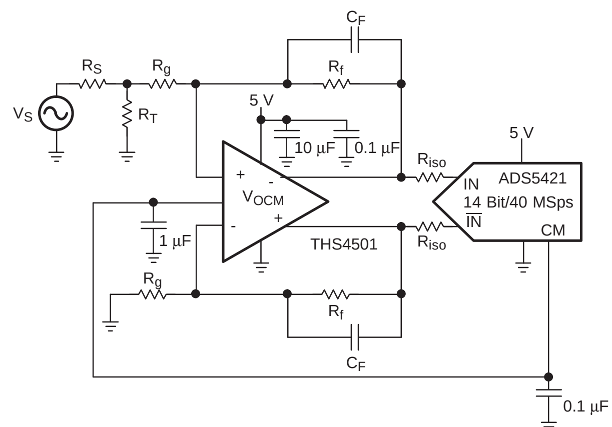
EXAMPLE ANALOG-TO-DIGITAL CONVERTER DRIVER CIRCUITS

The THS4500 family of devices is designed to drive high-performance ADCs with extremely high linearity, allowing for the maximum effective number of bits at the output of the data converter. Two representative circuits shown below highlight single-supply operation and split supply operation. Specific feedback resistor, gain resistor, and feedback capacitor values are not specified, as their values depend on the frequency of interest. Information on calculating these values can be found in the applications material above.



Using the THS4503 With the ADS5410

Figure 97.

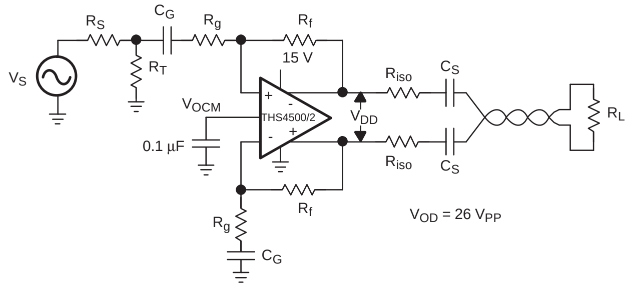


Using the THS4501 With the ADS5421

Figure 98.

FULLY DIFFERENTIAL LINE DRIVERS

The THS4500 family of amplifiers can be used as high-frequency, high-swing differential line drivers. Their high power supply voltage rating (16.5 V absolute maximum) allows operation on a single 12-V or a single 15-V supply. The high supply voltage, coupled with the ability to provide differential outputs enables the ability to drive 26 V_{PP} into reasonably heavy loads (250 Ω or greater). The circuit in Figure 99 illustrates the THS4500 family of devices used as high speed line drivers. For line driver applications, close attention must be paid to thermal design constraints due to the typically high level of power dissipation.

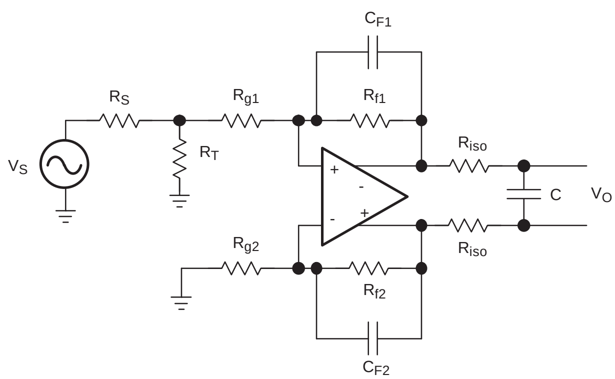


Fully Differential Line Driver With High Output Swing

Figure 99.

Filtering With Fully Differential Amplifiers

Similar to their single-ended counterparts, fully differential amplifiers have the ability to couple filtering functionality with voltage gain. Numerous filter topologies can be based on fully differential amplifiers. Several of these are outlined in *A Differential Circuit Collection*, (literature number SLOA064) referenced at the end of this data sheet. The circuit below depicts a simple two-pole low-pass filter applicable to many different types of systems. The first pole is set by the resistors and capacitors in the feedback paths, and the second pole is set by the isolation resistors and the capacitor across the outputs of the isolation resistors.



A Two-Pole, Low-Pass Filter Design Using a Fully Differential Amplifier With Poles Located at: $P1 = (2\pi R_f C_F)^{-1}$ in Hz and $P2 = (4\pi R_{iso} C)^{-1}$ in Hz

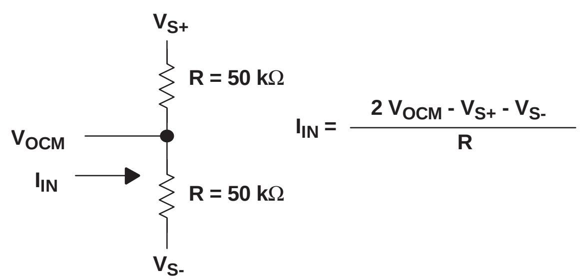
Figure 100.

Often times, filters like these are used to eliminate broadband noise and out-of-band distortion products in signal acquisition systems. It should be noted that the increased load placed on the output of the amplifier by the second low-pass filter has a detrimental effect on the distortion performance. The preferred method of filtering is using the feedback network, as the typically smaller capacitances required at these points in the circuit do not load the amplifier nearly as heavily in the pass-band.

SETTING THE OUTPUT COMMON-MODE VOLTAGE WITH THE V_{OCM} INPUT

The output common-mode voltage pin provides a critical function to the fully differential amplifier; it accepts an input voltage and reproduces that input voltage as the output common-mode voltage. In other words, the V_{OCM} input provides the ability to level-shift the outputs to any voltage inside the output voltage swing of the amplifier.

A description of the input circuitry of the V_{OCM} pin is shown below to facilitate an easier understanding of the V_{OCM} interface requirements. The V_{OCM} pin has two 50-kΩ resistors between the power supply rails to set the default output common-mode voltage to midrail. A voltage applied to the V_{OCM} pin alters the output common-mode voltage as long as the source has the ability to provide enough current to overdrive the two 50-kΩ resistors. This phenomenon is depicted in the V_{OCM} equivalent circuit diagram. The table contains some representative examples to aid in determining the current drive requirement for the V_{OCM} voltage source. This parameter is especially important when using the reference voltage of an analog-to-digital converter to drive V_{OCM}. Output current drive capabilities differ from part to part, so a voltage buffer may be necessary in some applications.



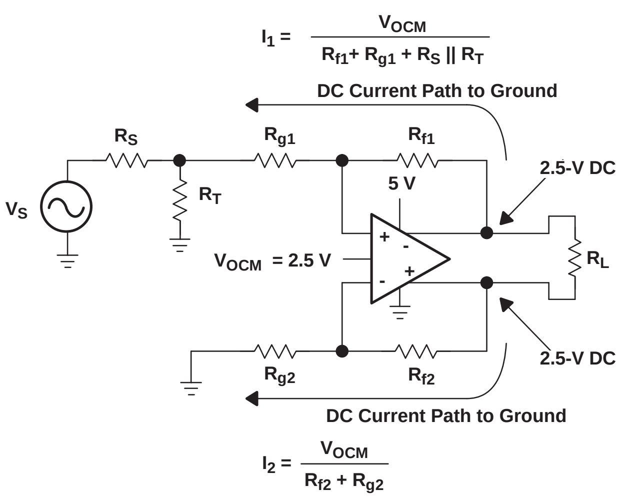
$$I_{IN} = \frac{2\,V_{OCM} - V_{S+} - V_{S-}}{R}$$

Equivalent Input Circuit for V_{OCM}

Figure 101.

By design, the input signal applied to the V_{OCM} pin propagates to the outputs as a common-mode signal. As shown in the equivalent circuit diagram, the V_{OCM} input has a high impedance associated with it, dictated by the two 50-kΩ resistors. While the high impedance allows for relaxed drive requirements, it also allows the pin and any associated printed-circuit board traces to act as an antenna. For this reason, a decoupling capacitor is recommended on this node for the sole purpose of filtering any high frequency noise that could couple into the signal path through the V_{OCM} circuitry. A 0.1-µF or 1-µF capacitance is a reasonable value for eliminating a great deal of broadband interference, but additional, tuned decoupling capacitors should be considered if a specific source of electromagnetic or radio frequency interference is present elsewhere in the system. Information on the ac performance (bandwidth, slew rate) of the V_{OCM} circuitry is included in the specification table and graph section.

Since the V_{OCM} pin provides the ability to set an output common-mode voltage, the ability for increased power dissipation exists. While this does not pose a performance problem for the amplifier, it can cause additional power dissipation of which the system designer should be aware. The circuit shown in Figure 102 demonstrates an example of this phenomenon. For a device operating on a single 5-V supply with an input signal referenced around ground and an output common-mode voltage of 2.5 V, a dc potential exists between the outputs and the inputs of the device. The amplifier sources current into the feedback network in order to provide the circuit with the proper operating point. While there are no serious effects on the circuit performance, the extra power dissipation may need to be included in the system's power budget.



Depiction of DC Power Dissipation Caused By Output Level-Shifting in a DC-Coupled Circuit

Figure 102.

SAVING POWER WITH POWER-DOWN FUNCTIONALITY

The THS4500 family of fully differential amplifiers contains devices that come with and without the power-down option. Even-numbered devices have power-down capability, which is described in detail here.

The power-down pin of the amplifiers defaults to the positive supply voltage in the absence of an applied voltage (i.e. an internal pullup resistor is present), putting the amplifier in the *power-on* mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the negative rail. The threshold voltages for power-on and power-down are relative to the supply rails and given in the specification tables. Above the *enable threshold voltage*, the device is on. Below the *disable threshold voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain setting resistors.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 50% of the nominal quiescent current. The time delays are on the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

LINEARITY; DEFINITIIONS, TERMINOLOGY, CIRCUIT TECHNIQUES, AND DESIGN TRADEOFFS

The THS4500 family of devices features unprecedented distortion performance for monolithic fully differential amplifiers. This section focuses on the fundamentals of distortion, circuit techniques for reducing nonlinearity, and methods for equating distortion of fully differential amplifiers to desired linearity specifications in RF receiver chains.

Amplifiers are generally thought of as*linear* devices. In other words, the output of an amplifier is a linearly scaled version of the input signal applied to it. In reality, however, amplifier transfer functions are nonlinear. Minimizing amplifier nonlinearity is a primary design goal in many applications.

Intercept points are specifications that have long been used as key design criteria in the RF communications world as a metric for the intermodulation distortion performance of a device in the signal chain (e.g., amplifiers, mixers, etc.). Use of the intercept point, rather than strictly the intermodulation distortion, allows for simpler system-level calculations. Intercept points, like noise figures, can be easily cascaded back and forth through a signal chain to determine the overall receiver chain's intermodulation distortion performance. The relationship between intermodulation distortion and intercept point is depicted in Figure 103 and Figure 104.

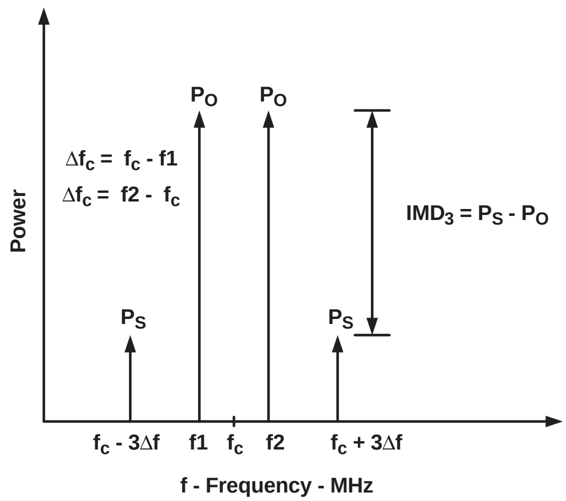


Figure 103.

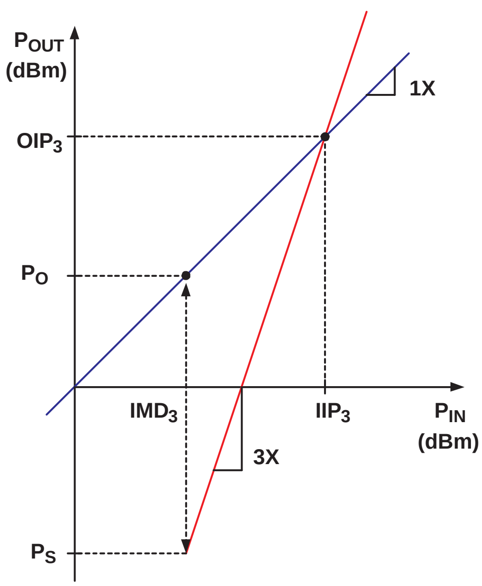


Figure 104.

Due to the intercept point's ease of use in system level calculations for receiver chains, it has become the specification of choice for guiding distortion-related design decisions. Traditionally, these systems use primarily class-A, single-ended RF amplifiers as gain blocks. These RF amplifiers are typically designed to operate in a 50-Ω environment, just like the rest of the receiver chain. Since intercept points are given in dBm, this implies an associated impedance (50 Ω).

However, with a fully differential amplifier, the output does not require termination as an RF amplifier would. Because closed-loop amplifiers deliver signals to their outputs regardless of the impedance present, it is important to comprehend this when evaluating the intercept point of a fully differential amplifier. The THS4500 series of devices yields optimum distortion performance when loaded with 200 Ω to 1 kΩ, very similar to the input impedance of an analog-to-digital converter over its input frequency band. As a result, terminating the input of the ADC to 50 Ω can actually be detrimental to system performance.

This discontinuity between open-loop, class-A amplifiers and closed-loop, class-AB amplifiers becomes apparent when comparing the intercept points of the two types of devices. Equation 10 gives the definition of an intercept point, relative to the intermodulation distortion.

$$OIP_3 = P_O + \left(\frac{|IMD_3|}{2}\right) \text{ where} \tag{10}$$

$$P_O = 10 \log\left(\frac{V_{Pdiff}^2}{2R_L \times 0.001}\right) \tag{11}$$

NOTE

P_o is the output power of a single tone, R_L is the differential load resistance, and $V_{P(diff)}$ is the differential peak voltage for a single tone.

As can be seen in the equation, when a higher impedance is used, the same level of intermodulation distortion performance results in a lower intercept point. Therefore, it is important to comprehend the impedance seen by the output of the fully differential amplifier when selecting a minimum intercept point. The graphic below shows the relationship between the strict definition of an intercept point with a normalized, or equivalent, intercept point for the THS4502.

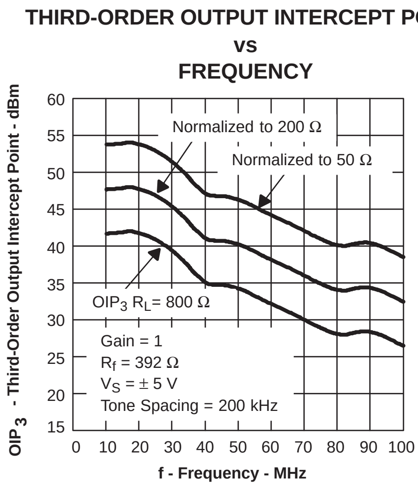


Figure 105.

Comparing specifications between different device types becomes easier when a common impedance level is assumed. For this reason, the intercept points on the THS4500 family of devices are reported normalized to a 50-Ω load impedance.

AN ANALYSIS OF NOICE IN FULLY DIFFERENTIAL AMPLIFIERS

Noise analysis in fully differential amplifiers is analogous to noise analysis in single-ended amplifiers. The same concepts apply. Below, a generic circuit diagram consisting of a voltage source, a termination resistor, two gain setting resistors, two feedback resistors, and a fully differential amplifier is shown, including all the relevant noise sources. From this circuit, the noise factor (F) and noise figure (NF) are calculated. The figures indicate the appropriate scaling factor for each of the noise sources in two different cases. The first case includes the termination resistor, and the second, simplified case assumes that the voltage source is properly terminated by the gain-setting resistors. With these scaling factors, the amplifier's input noise power (N_A) can be calculated by summing each individual noise source with its scaling factor. The noise delivered to the amplifier by the source (N_I) and input noise power are used to calculate the noise factor and noise figure as shown in equations 23 through 27.

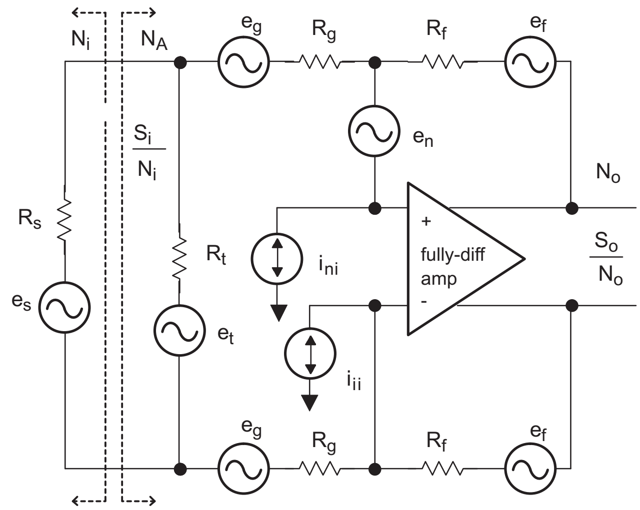


Figure 106. Noise Sources in a Fully Differential Amplifier Circuit

N_A: Fully Differential Amplifier

Noise Source	Scale Factor	
$(e_{ni})^2$	$\left[\dfrac{R_g}{R_f} + \dfrac{R_g}{R_g + \dfrac{R_sR_t}{2(R_s+R_t)}}\right]^2$	(12)
$(i_{ni})^2$	$R_g{}^2$	(13)
$(i_{ii})^2$	$R_g{}^2$	(14)
$4kTR_t$	$\left[\dfrac{\dfrac{2R_sR_G}{R_s+2R_g}}{R_t + \dfrac{2R_sR_g}{R_s+2R_g}}\right]^2$	(15)
$4kTR_f$	$2 \times \left(\dfrac{R_g}{R_f}\right)^2$	(16)
$4kTR_g$	$2 \times \left[\dfrac{R_g}{R_g + \dfrac{R_sR_t}{2(R_s+R_t)}}\right]^2$	(17)

Figure 107. Scaling Factors for Individual Noise Sources Assuming a Finite Value Termination Resistor

N_A: Fully Differential Amplifier; termination = $2R_g$

Noise Source	Scale Factor	
$(e_{ni})^2$	$\left(\frac{R_g}{R_f} + \frac{R_g}{R_g + \frac{R_s}{2}}\right)^2$	(18)
$(i_{ni})^2$	$R_g{}^2$	(19)
$(i_{ii})^2$	$R_g{}^2$	(20)
$4kTR_f$	$2 \times \left(\frac{R_g}{R_f}\right)^2$	(21)
$4kTR_g$	$2 \times \left(\frac{R_g}{R_g + \frac{R_s}{2}}\right)^2$	(22)

Figure 108. Scaling Factors for Individual Noise Sources Assuming No termination Resistance is Used (e.g., R_T is open)

$$N_i = 4kTR_s \left(\frac{\frac{2R_tR_g}{R_t + 2R_g}}{R_s + \frac{2R_tR_g}{R_t + 2R_g}}\right)^2 \quad (23)$$

Figure 109. Input Noise With a Termination Resistor

$$N_i = 4kTR_s \left(\frac{2R_g}{R_s + 2R_g}\right)^2 \quad (24)$$

Figure 110. Input Noise Assuming No Termination Resistor

$$N_A = \Sigma(\text{Noise Source} \times \text{Scale Factor}) \quad (25)$$

$$F = 1 + \frac{N_A}{N_I} \quad (26)$$

$$NF = 10 \log (F) \quad (27)$$

Figure 111. Noise Factor and Noise Figure Calculations

PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES FOR OPTIMAL PERFORMANCE

Achieving optimum performance with high frequency amplifier-like devices in the THS4500 family requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance (< 0.25”) from the power supply pins to high frequency 0.1-μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (6.8 μF or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board. The primary goal is to minimize the impedance seen in the differential-current return paths.
- Careful selection and placement of external components preserve the high frequency performance of the THS4500 family. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound type resistors in a high frequency application. Since the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero below 400 MHz that can

effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations.

- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4 pF) may not need an R_S since the THS4500 family is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques).
- A 50-Ω environment is normally not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS4500 family is used as well as a terminating shunt resistor at the input of the destination device.
- Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.
- Socketing a high speed part like the THS4500 family is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS4500 family parts directly onto the board.

PowerPAD DESIGN CONSIDERATIONS

The THS4500 family is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 112(a) and Figure 112(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 112(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

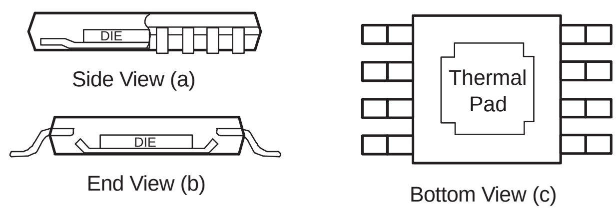


Figure 112. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

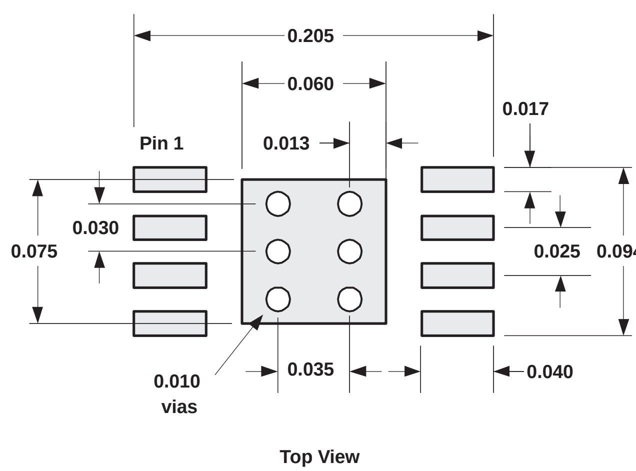


Figure 113. PowerPAD PCB Etch and Via Pattern

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 113. There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS4500 family IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS4500 family PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

Power Dissipation and Thermal Considerations

The THS4500 family of devices does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150°C is exceeded. For best performance, design for a maximum junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}} \qquad (28)$$

Where:
P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS4500 family of devices is offered in an 8-pin MSOP with PowerPAD. The thermal coefficient for the MSOP PowerPAD package is substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the two packages. The data for the DGN package assumes a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application notes in the *Additional Reference Material* section at the end of the data sheet.

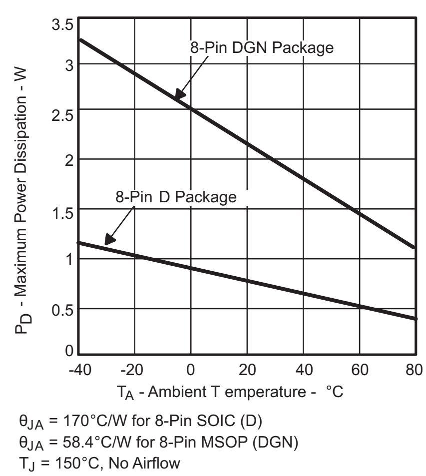
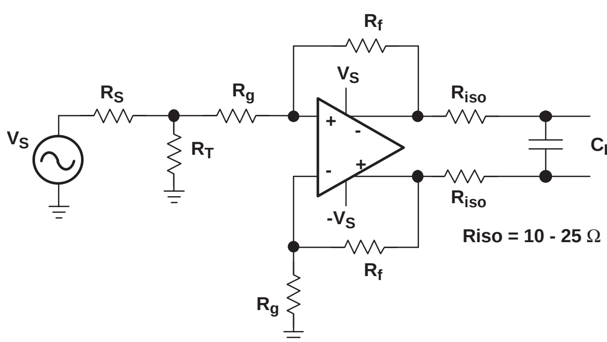


Figure 114. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DRIVING CAPACITIVE LOADS

High-speed amplifiers are typically not well-suited for driving large capacitive loads. If necessary, however, the load capacitance should be isolated by two isolation resistors in series with the output. The requisite isolation resistor size depends on the value of the capacitance, but 10 to 25Ω is a good place to begin the optimization process. Larger isolation resistors decrease the amount of peaking in the frequency response induced by the capacitive load, but this comes at the expense of larger voltage drop across the resistors, increasing the output swing requirements of the system.



Use of Isolation Resistors With a Capacitive Load.

Figure 115.

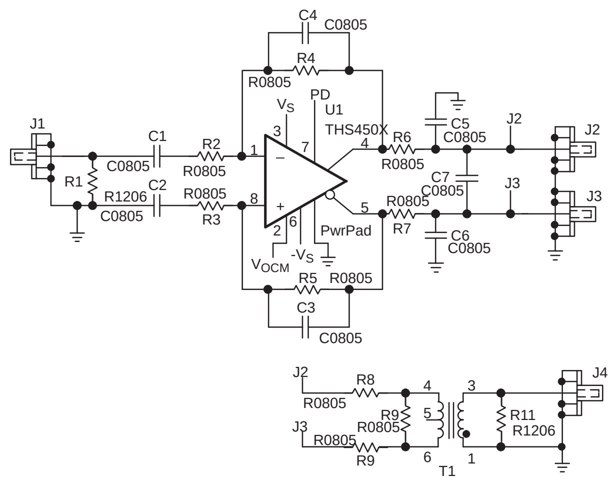
POWER SUPPLY DECOUPLING TECHNIQUES AND RECOMMENDATIONS

Power supply decoupling is a critical aspect of any high-performance amplifier design process. Careful decoupling provides higher quality ac performance (most notably improved distortion performance). The following guidelines ensure the highest level of performance.

1. Place decoupling capacitors as close to the power supply inputs as possible, with the goal of minimizing the inductance of the path from ground to the power supply.
2. Placement priority should be as follows: smaller capacitors should be closer to the device.
3. Use of solid power and ground planes is recommended to reduce the inductance along power supply return current paths.
4. Recommended values for power supply decoupling include 10-μF and 0.1-μF capacitors for each supply. A 1000-pF capacitor can be used across the supplies as well for extremely high frequency return currents, but often is not required.

EVALUATION FIXTURES, SPICE MODELS, AND APPLICTIONS SUPPORT

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal, an evaluation board has been developed for the THS4500 family of fully differential amplifiers. The evaluation board can be obtained by ordering through the Texas Instruments web site, www.ti.com, or through your local Texas Instruments sales representative. Schematic for the evaluation board is shown below with their default component values. Unpopulated footprints are shown to provide insight into design flexibility.



Simplified Schematic of the Evaluation Board. Power Supply Decoupling, V_{OCM}, and Power Down Circuitry Not Shown

Figure 116.

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS4500 family of devices is available through the Texas Instruments web site (www.ti.com). The PIC is also available for design assistance and detailed product information. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

ADDITIONAL REFERENCE MATERIAL

- *PowerPAD Made Easy*, application brief, Texas Instruments Literature Number SLMA004.
- *PowerPAD Thermally Enhanced Packag*e, technical brief, Texas Instruments Literature Number SLMA002.
- Karki, James. *Fully Differential Amplifiers.*application report, Texas Instruments Literature Number SLOA054D.
- Karki, James. *Fully Differential Amplifiers Applications: Line Termination, Driving High-Speed ADCs, and Differential Transmission Lines*. Texas Instruments Analog Applications Journal, February 2001.
- Carter, Bruce. *A Differential Op-Amp Circuit Collection.* application report, Texas Instruments Literature Number SLOA064.
- Carter, Bruce. *Differential Op-Amp Single-Supply Design Technique*, application report, Texas Instruments Literature Number SLOA072.
- Karki, James. *Designing for Low Distortion with High-Speed Op Amps*. Texas Instruments Analog Applications Journal, July 2001.

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4502CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4502C	Samples
THS4502CDG4	ACTIVE	SOIC	D	8	75	TBD	Call TI	Call TI	0 to 70		Samples
THS4502CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCG	Samples
THS4502CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCG	Samples
THS4502ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4502I	Samples
THS4502IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASX	Samples
THS4502IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCI	Samples
THS4502IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCI	Samples
THS4502IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4502I	Samples
THS4503CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4503C	Samples
THS4503CDG4	ACTIVE	SOIC	D	8	75	TBD	Call TI	Call TI	0 to 70		Samples
THS4503CDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ATY	Samples
THS4503CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCK	Samples
THS4503CDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	BCK	Samples
THS4503ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4503I	Samples
THS4503IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASY	Samples
THS4503IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCL	Samples
THS4503IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BCL	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF THS4503 :

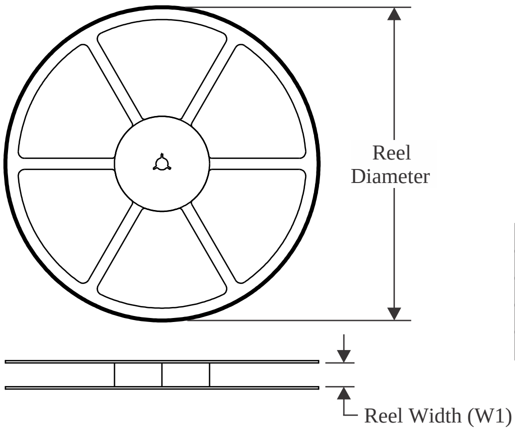
- Enhanced Product : THS4503-EP

NOTE: Qualified Version Definitions:

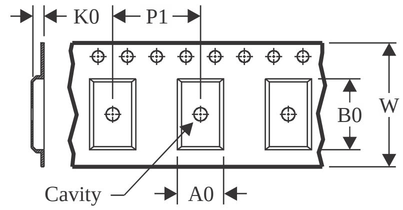
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

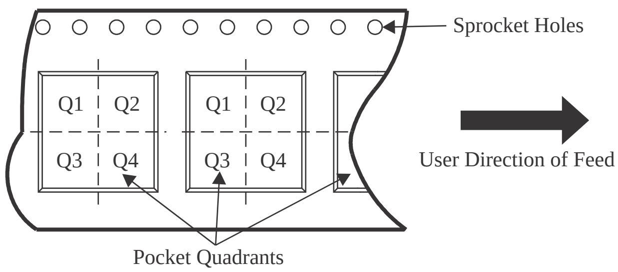


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

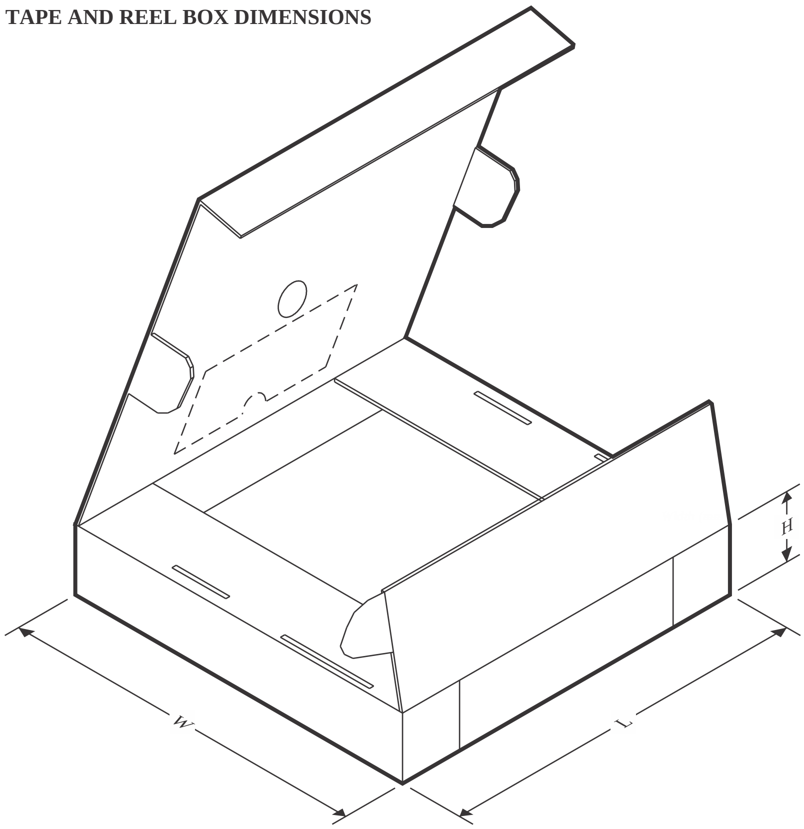
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4502CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4502IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4502IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4503CDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4503IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

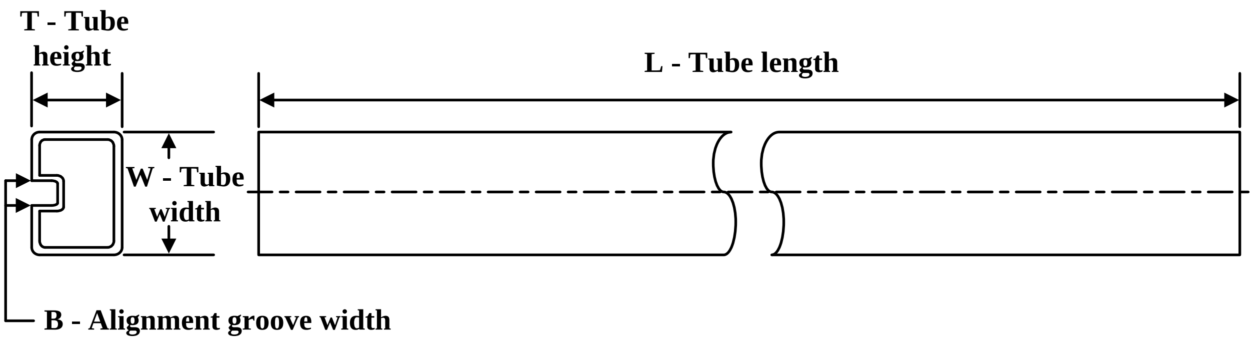
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4502CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4502IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4502IDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4503CDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4503IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4502CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4502ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4503CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4503ID	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

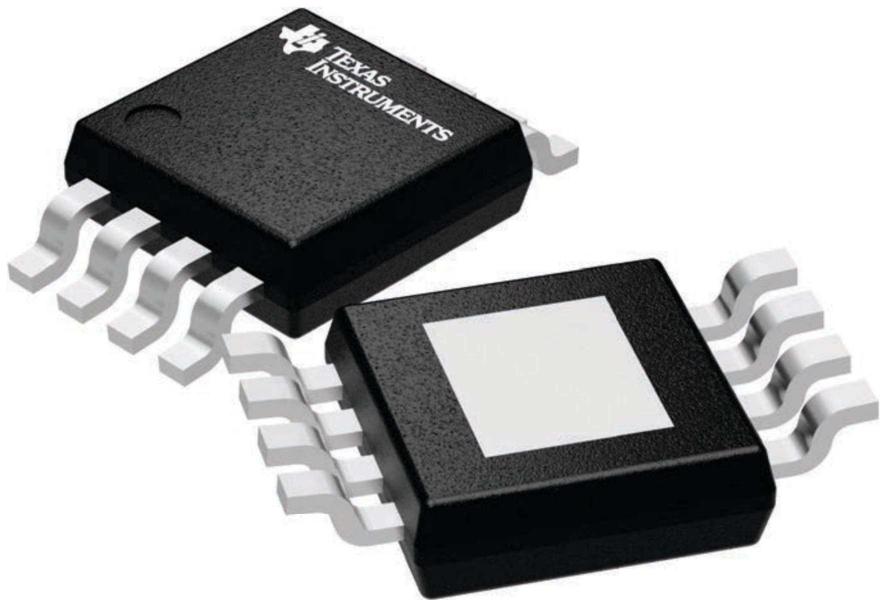
DGN 8

PowerPAD VSSOP - 1.1 mm max height

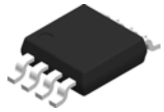
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



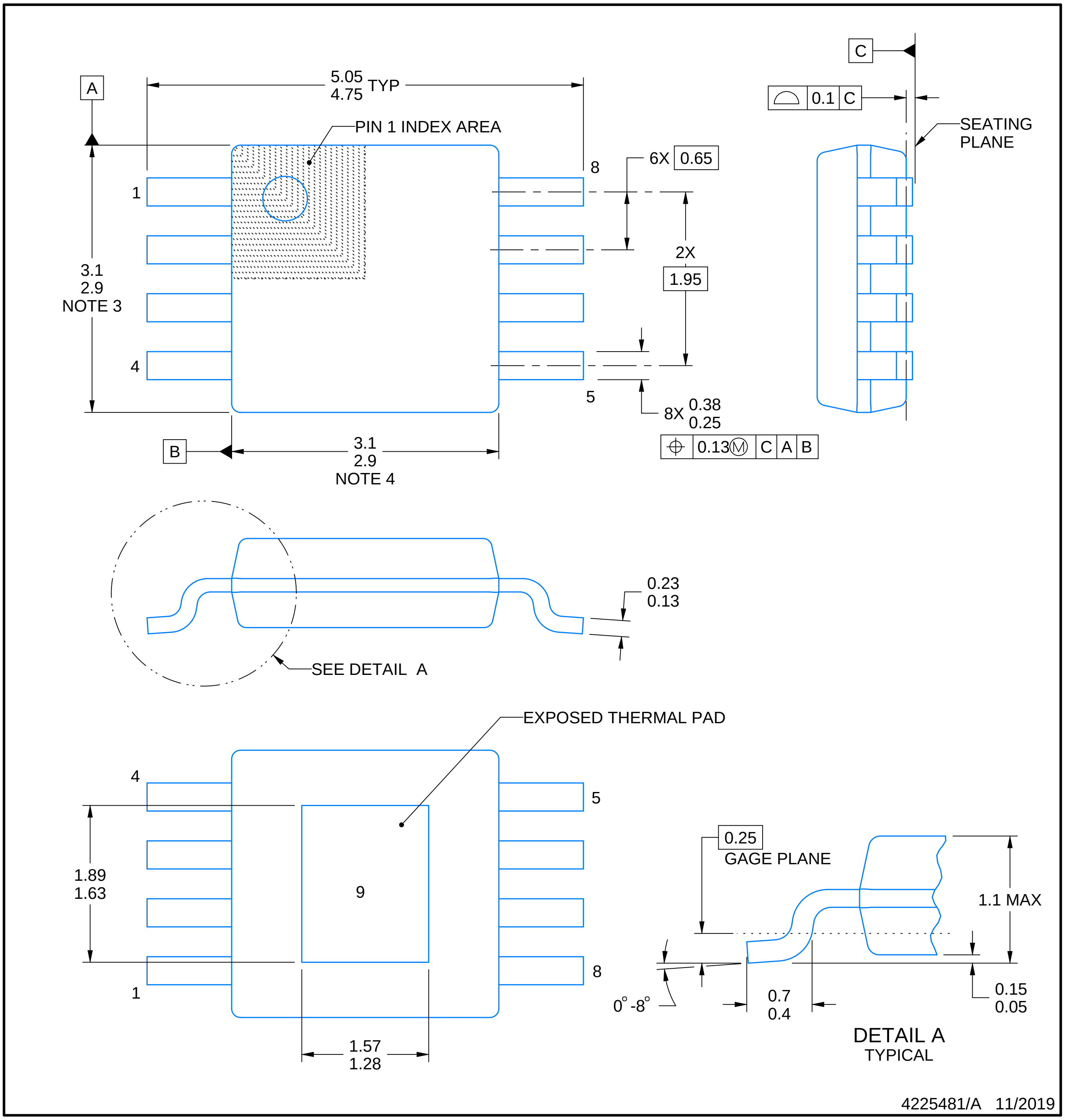
4225482/A



PACKAGE OUTLINE

PowerPAD™ VSSOP - 1.1 mm max height

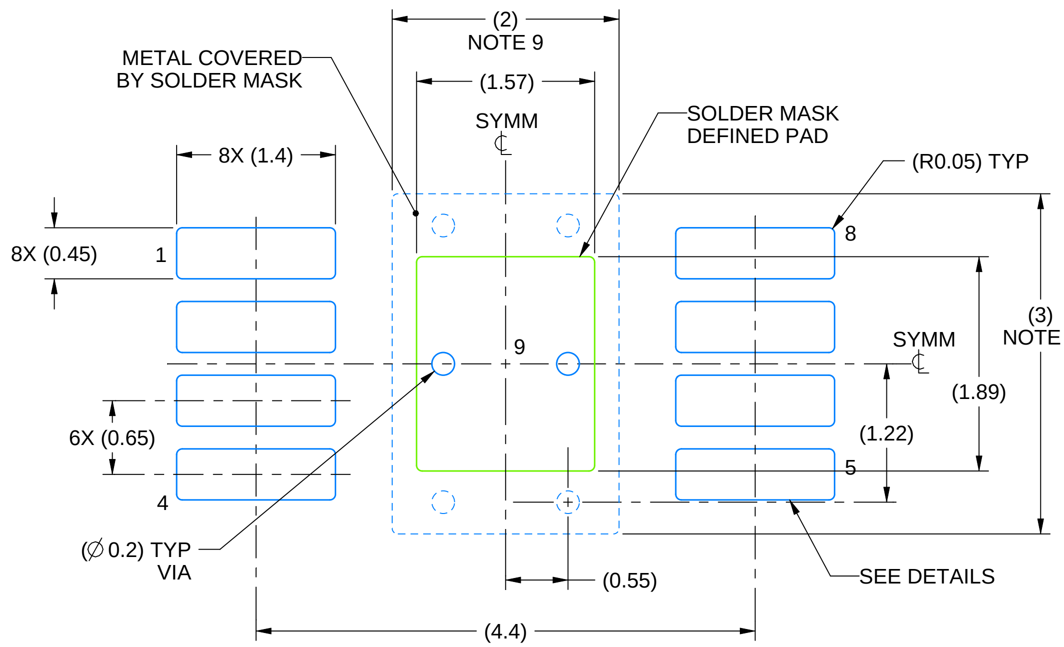
SMALL OUTLINE PACKAGE



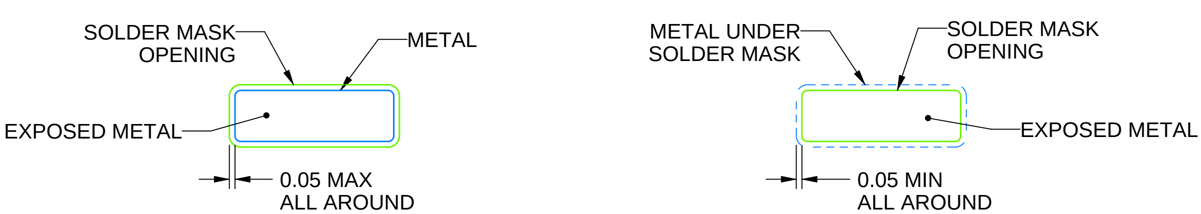
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

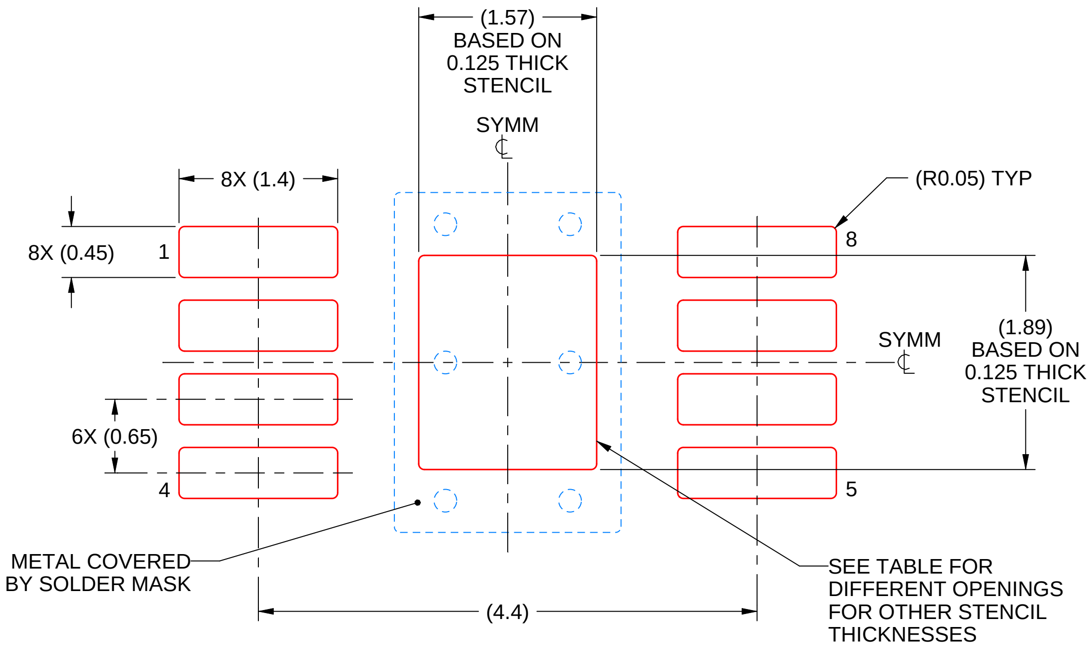


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



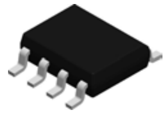
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

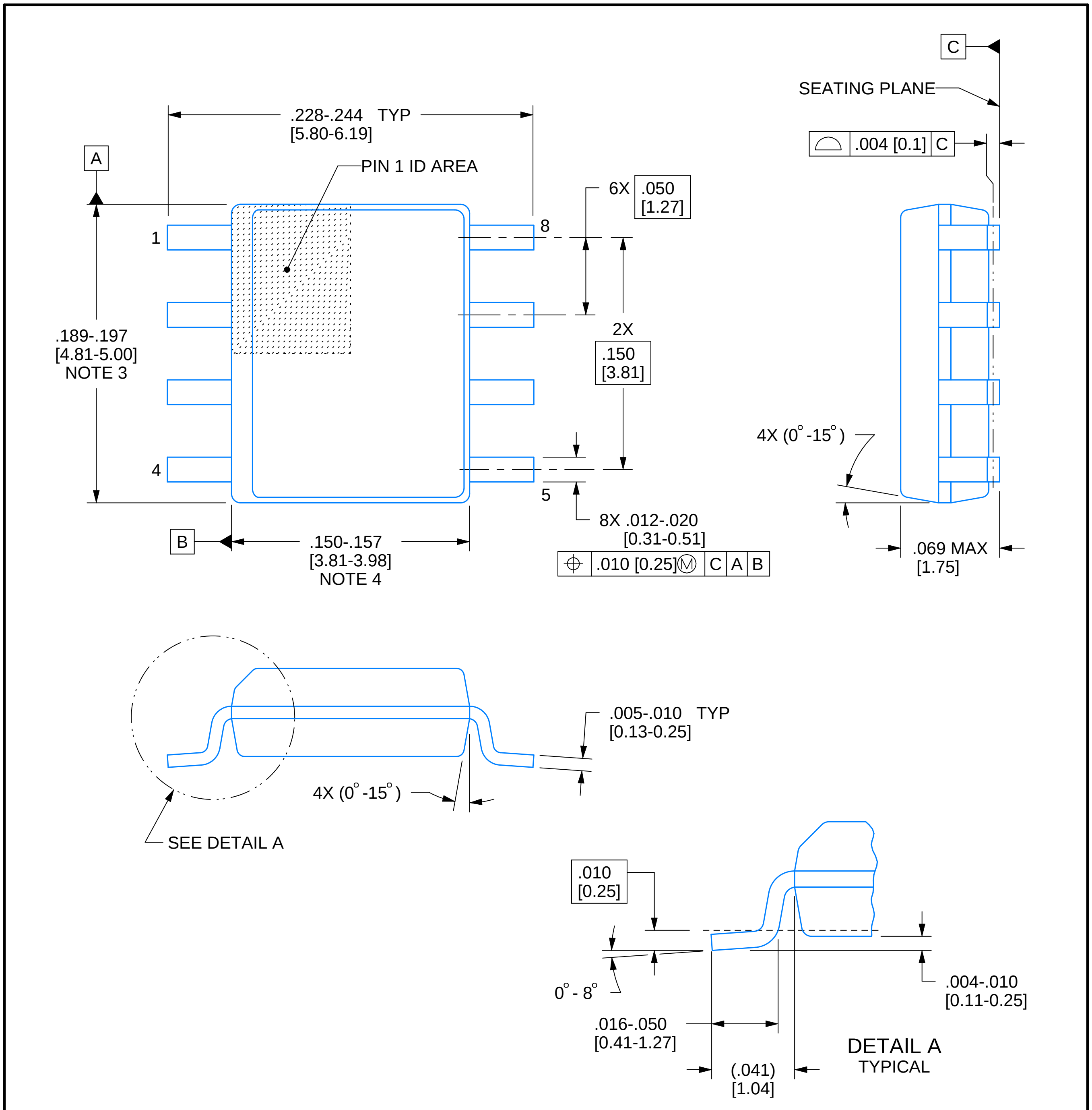


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

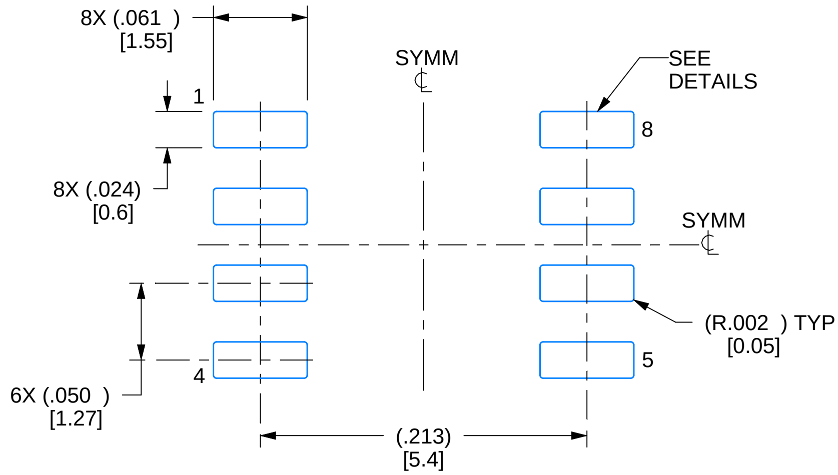
SMALL OUTLINE INTEGRATED CIRCUIT



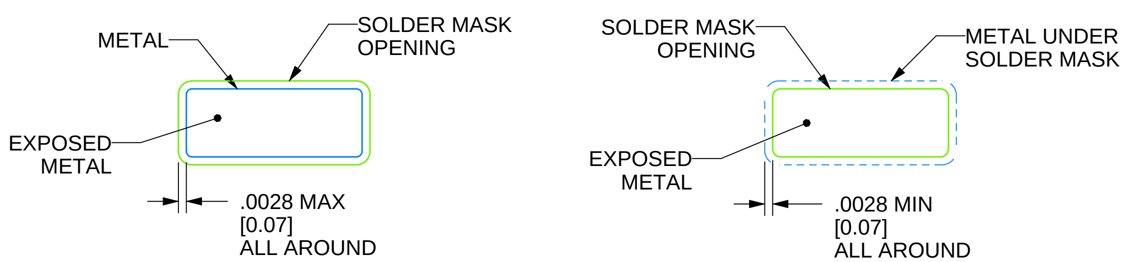
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

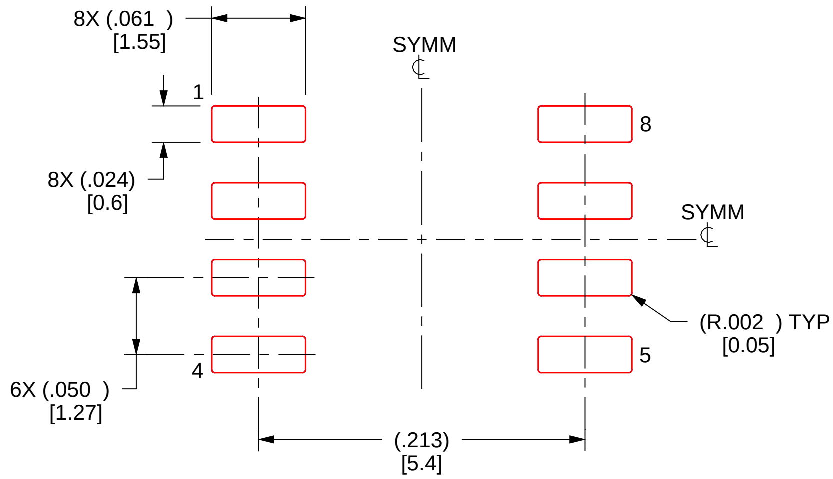
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



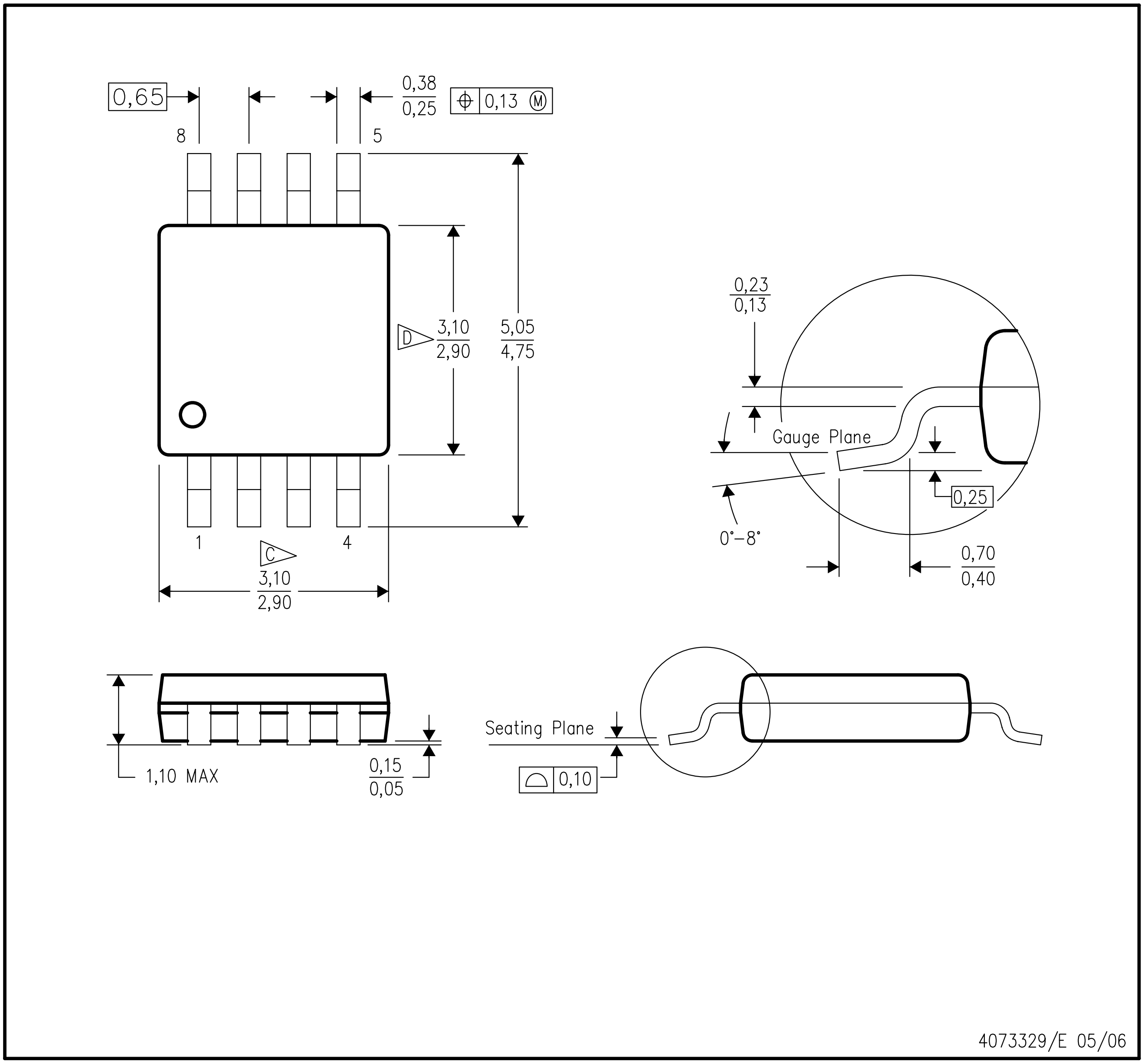
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

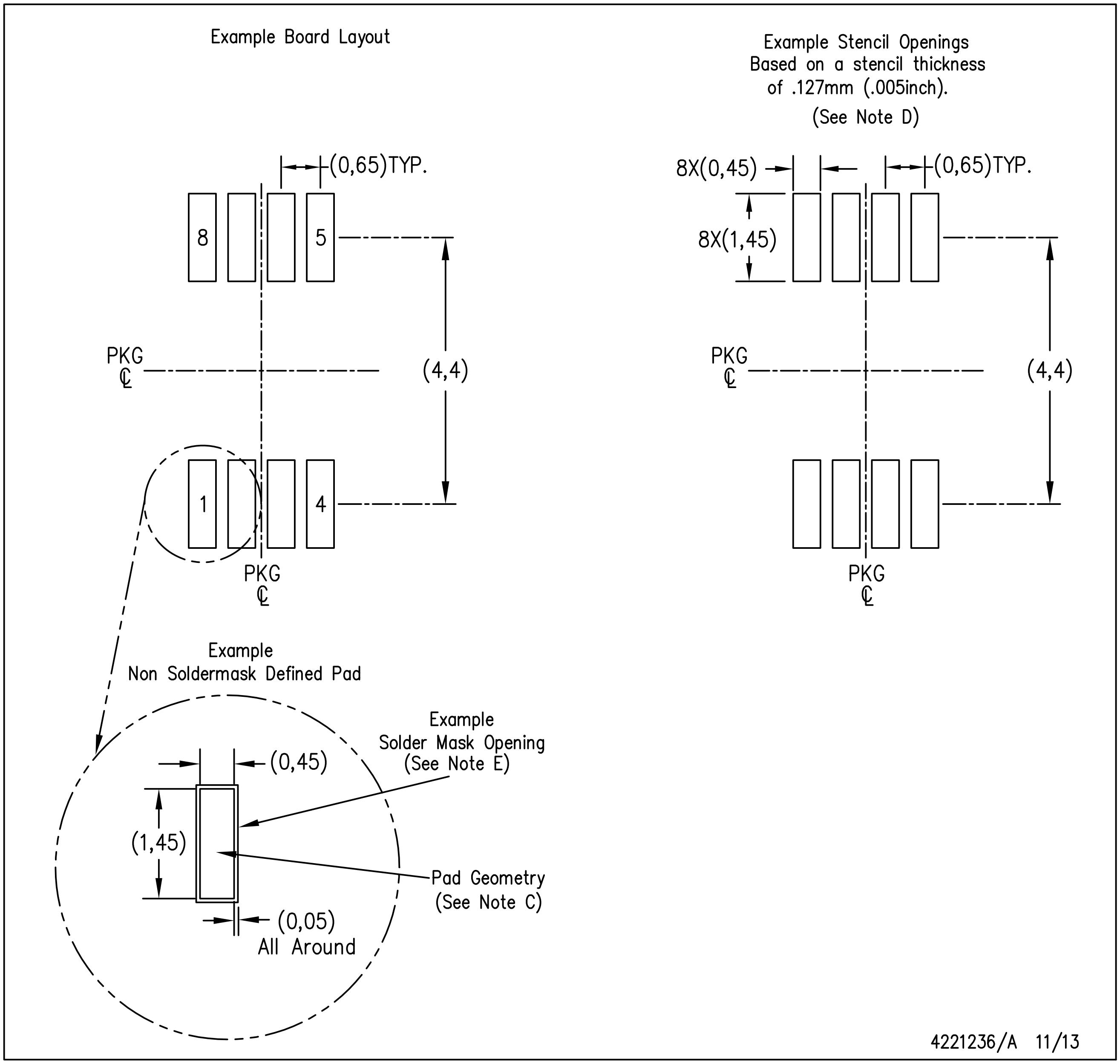
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.