

SNx4HCT373 Octal Transparent D-Type Latches With 3-State Outputs

1 Features

- Operating voltage range of 4.5 V to 5.5 V
- High-current 3-state true outputs can drive up to 15 LSTTL loads
- Low power consumption, 80- μ A max I_{CC}
- Typical t_{pd} = 21 ns
- ± 6 -mA output drive at 5 V
- Low input current of 1 μ A max
- Inputs are TTL-voltage compatible
- Eight high-current latches in a single package
- Full parallel access for loading

2 Description

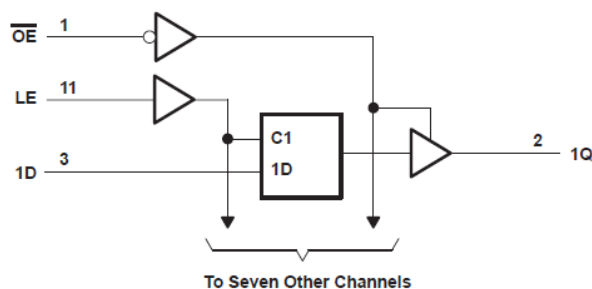
These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HCT373 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|---------------|------------------------|---------------------------|
| SN74HCT373DW | SOIC (20) | 12.80 mm \times 7.50 mm |
| SN74HCT373N | PDIP (20) | 25.40 mm \times 6.35 mm |
| SN74HCT373NSR | SO (20) | 15.00 mm \times 5.30 mm |
| SN74HCT373PW | TSSOP (20) | 6.50 mm \times 4.40 mm |
| SN54HCT373J | CDIP (20) | 26.92 mm \times 6.92 mm |
| SNJ54HCT373FK | LCCC (20) | 8.89 mm \times 8.45 mm |
| SNJ54HCT373W | CFP (20) | 13.72 mm \times 6.92 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram



Table of Contents

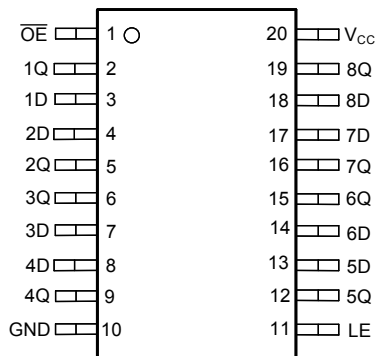
| | | | |
|---|---|--|----|
| 1 Features | 1 | 7.1 Overview..... | 8 |
| 2 Description | 1 | 7.2 Functional Block Diagram..... | 8 |
| 3 Revision History | 2 | 7.3 Device Functional Modes..... | 8 |
| 4 Pin Configuration and Functions | 3 | 8 Power Supply Recommendations | 9 |
| 5 Specifications | 4 | 9 Layout | 9 |
| 5.1 Absolute Maximum Ratings | 4 | 9.1 Layout Guidelines..... | 9 |
| 5.2 Recommended Operating Conditions ⁽¹⁾ | 4 | 10 Device and Documentation Support | 10 |
| 5.3 Thermal Information..... | 4 | 10.1 Receiving Notification of Documentation Updates.. | 10 |
| 5.4 Electrical Characteristics..... | 5 | 10.2 Support Resources..... | 10 |
| 5.5 Timing Requirements..... | 5 | 10.3 Trademarks..... | 10 |
| 5.6 Switching Characteristics | 5 | 10.4 Electrostatic Discharge Caution..... | 10 |
| 5.7 Switching Characteristics..... | 6 | 10.5 Glossary..... | 10 |
| 5.8 Operating Characteristics..... | 6 | 11 Mechanical, Packaging, and Orderable Information | 10 |
| 6 Parameter Measurement Information | 7 | | |
| 7 Detailed Description | 8 | | |

3 Revision History

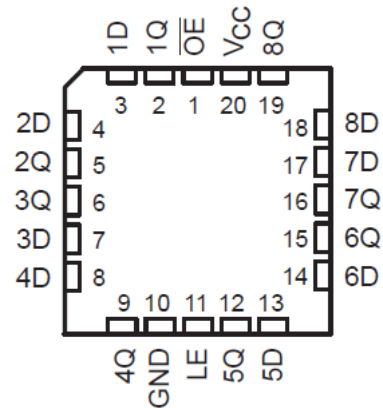
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (December 2021) to Revision G (July 2022) | Page |
|--|-------------|
| • Removed DB package..... | 4 |
| Changes from Revision E (December 2021) to Revision F (December 2021) | Page |
| • Junction-to-ambient thermal resistance values increased. DW was 58 is now 109.1, N was 69 is now 84.6, NS was 60 is now 113.4, DB was 70 is now 122.7, PW was 83 is now 131.8..... | 4 |
| Changes from Revision D (August 2003) to Revision E (December 2021) | Page |
| • Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards..... | 1 |

4 Pin Configuration and Functions



J, W, DB, DW, N, NS, or PW package
20-Pin CDIP, CFP, SOIC, PDIP, SO, TSSOP
Top View



FK package
20-Pin LCCC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|--|------|------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| I _{IK} | Input clamp current ⁽²⁾ | V _I < 0 or V _I > V _{CC} | ± 20 | mA |
| I _{OK} | Output clamp current ⁽²⁾ | V _O < 0 or V _O > V _{CC} | ± 20 | mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | ± 35 | mA |
| | Continuous current through V _{CC} or GND | | ± 70 | mA |
| T _J | Junction temperature | | 150 | °C |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 Recommended Operating Conditions⁽¹⁾

| | | SN54HCT373 | | | SN74HCT373 | | | UNIT |
|-----------------|---------------------------------|----------------------------------|-----------------|-----|------------|-----------------|-----|------|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 4.5 V to 5.5 V | | 2 | 2 | | V | |
| V _{IL} | Low-level input voltage | V _{CC} = 4.5 V to 5.5 V | | 0.8 | 0.8 | | V | |
| V _I | Input voltage | 0 | V _{CC} | | 0 | V _{CC} | | V |
| V _O | Output voltage | 0 | V _{CC} | | 0 | V _{CC} | | V |
| t _i | Input transition rise/fall time | 500 | | 500 | | ns | | |
| T _A | Operating free-air temperature | -55 | 125 | | -40 | 85 | | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.3 Thermal Information

| THERMAL METRIC | | SN74HCT373 | | | | UNIT |
|------------------------|---|------------|----------|---------|------------|------|
| | | DW (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | |
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽¹⁾ | 109.1 | 84.6 | 113.4 | 131.8 | °C/W |
| R _{θJC (top)} | Junction-to-case (top) thermal resistance | 76 | 72.5 | 78.6 | 72.2 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 77.6 | 65.3 | 78.4 | 82.8 | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 51.5 | 55.3 | 47.1 | 21.5 | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 77.1 | 65.2 | 78.1 | 82.4 | °C/W |
| R _{θJC (bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | T _A = 25°C | | | SN54HCT373 | | SN74HCT373 | | UNIT |
|---------------------------------|---|--------------------------|-----------------|-----------------------|-------|------|------------|-------|------------|-------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | V _I = V _{IH} or V _{IL} | I _{OH} = -20 mA | 4.5 V | 4.4 | 4.499 | | 4.4 | | 4.4 | | V |
| | | I _{OH} = -6 mA | | 3.98 | 4.3 | | 3.7 | | 3.84 | | |
| V _{OL} | V _I = V _{IH} or V _{IL} | I _{OL} = 20 mA | 4.5 V | | 0.001 | 0.1 | | 0.1 | | 0.1 | V |
| | | I _{OL} = 6 mA | | | 0.17 | 0.26 | | 0.4 | | 0.33 | |
| I _I | V _I = V _{CC} or 0 | | 5.5 V | | ±0.1 | ±100 | | ±1000 | | ±1000 | nA |
| I _{OZ} | V _O = V _{CC} or 0 | | 5.5 V | | ±0.01 | ±0.5 | | ±10 | | ±5 | μA |
| I _{CC} | V _I = V _{CC} or 0, I _O = 0 | | 5.5 V | | | 8 | | 160 | | 80 | μA |
| ΔI _{CC} ⁽¹⁾ | One input at 0.5 V or 2.4 V, Other inputs at 0 or V _{CC} | | 5.5 V | | 1.4 | 2.4 | | 3 | | 2.9 | mA |
| C _i | | | 4.5 V to 5.5 V | | 3 | 10 | | 10 | | 10 | pF |

(1) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

5.5 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

| | | V _{CC} | T _A = 25°C | | SN54HCT373 | | SN74HCT373 | | UNIT |
|-----------------|-----------------------------|-----------------|-----------------------|-----|------------|-----|------------|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, LE high | 4.5V | 20 | | 30 | | 25 | | ns |
| | | 5.5V | 17 | | 27 | | 23 | | |
| t _{su} | Setup time, data before LE↓ | 4.5V | 10 | | 15 | | 13 | | ns |
| | | 5.5V | 9 | | 14 | | 12 | | |
| t _h | Hold time, data after LE↓ | 4.5V | 10 | | 10 | | 10 | | ns |
| | | 5.5V | 10 | | 10 | | 10 | | |

5.6 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see [Parameter Measurement Information](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} | T _A = 25°C | | | SN54HCT373 | | SN74HCT373 | | UNIT |
|------------------|--------------|-------------|-----------------|-----------------------|-----|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | D | Q | 4.5 V | | 25 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 21 | 32 | | 48 | | 40 | |
| | LE | Any Q | 4.5 V | | 28 | 35 | | 53 | | 44 | |
| | | | 5.5 V | | 25 | 32 | | 48 | | 40 | |
| t _{en} | OE | Any Q | 4.5 V | | 26 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 23 | 32 | | 48 | | 40 | |
| t _{dis} | OE | Any Q | 4.5 V | | 23 | 35 | | 53 | | 44 | ns |
| | | | 5.5 V | | 22 | 32 | | 48 | | 40 | |
| t _t | | Any Q | 4.5 V | | 10 | 12 | | 18 | | 15 | ns |
| | | | 5.5 V | | 9 | 11 | | 16 | | 14 | |

5.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 150$ pF (unless otherwise noted) (see [Parameter Measurement Information](#))

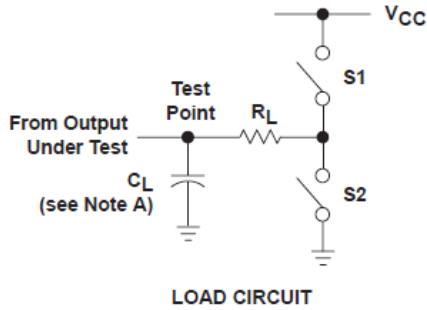
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V_{CC} | $T_A = 25^\circ\text{C}$ | | | SN54HCT373 | | SN74HCT373 | | UNIT |
|-----------|-----------------|-------------|----------|--------------------------|-----|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | D | Q | 4.5 V | 32 | 52 | 79 | 65 | ns | | | |
| | | | 5.5 V | 27 | 47 | 71 | 59 | | | | |
| | LE | Any Q | 4.5 V | 38 | 52 | 79 | 65 | | | | |
| | | | 5.5 V | 36 | 47 | 71 | 59 | | | | |
| t_{en} | \overline{OE} | Any Q | 4.5 V | 33 | 52 | 79 | 65 | ns | | | |
| | | | 5.5 V | 28 | 47 | 71 | 59 | | | | |
| t_r | | Any Q | 4.5 V | 18 | 42 | 63 | 53 | ns | | | |
| | | | 5.5 V | 16 | 38 | 57 | 48 | | | | |

5.8 Operating Characteristics

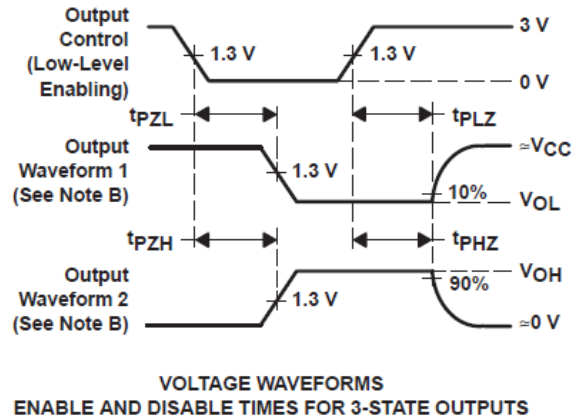
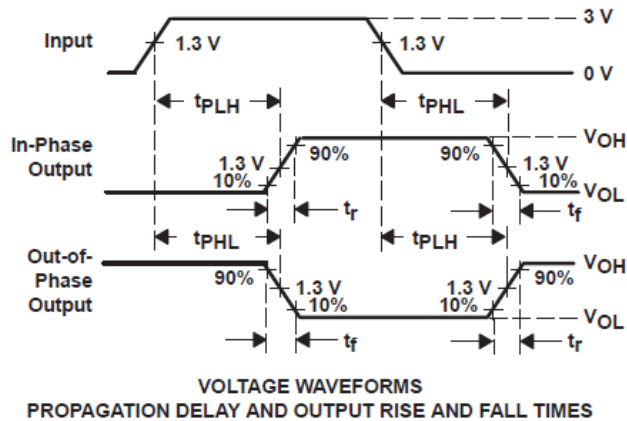
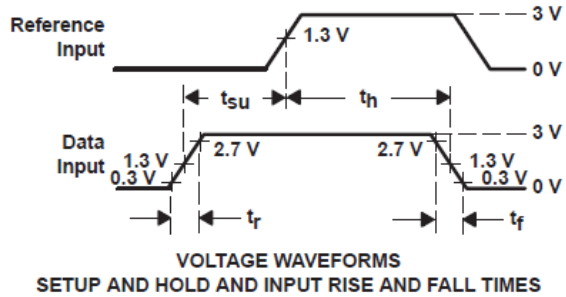
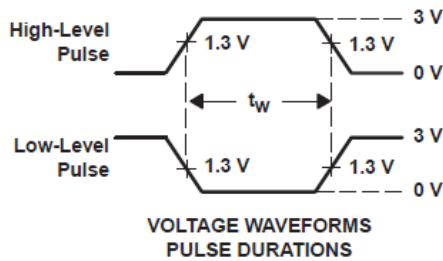
$T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|---|-----------------|-----|------|
| C_{pd} | Power dissipation capacitance per latch | No load | 50 | pF |

6 Parameter Measurement Information



| PARAMETER | R_L | C_L | S1 | S2 |
|-------------------|--------------|-----------------|--------|--------|
| t_{en} | 1 k Ω | 50 pF or 150 pF | Open | Closed |
| | | | Closed | Open |
| t_{dis} | 1 k Ω | 50 pF | Open | Closed |
| | | | Closed | Open |
| t_{pd} or t_t | — | 50 pF or 150 pF | Open | Open |



- C_L includes probe and test-fixture capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
- The outputs are measured one at a time with one input transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- t_{PZL} and t_{PZH} are the same as t_{en} .
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

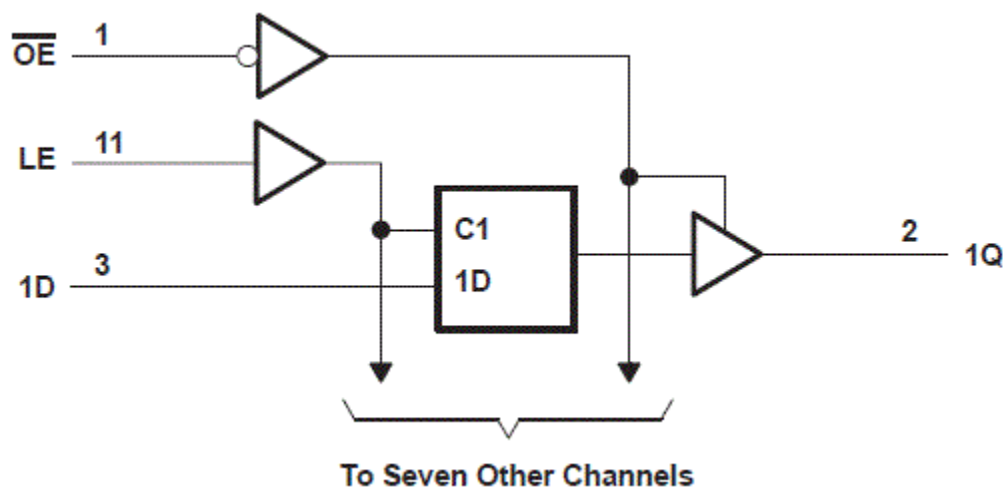
These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'HCT373 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels that were set up at the D inputs.

An output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

7.2 Functional Block Diagram



7.3 Device Functional Modes

**Table 7-1. Function Table
(Each Latch)**

| INPUTS | | | OUTPUT Q |
|-----------------|----|---|-------------|
| \overline{OE} | LE | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|---|-------------------------|
| 5962-86867012A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962- 86867012A SNJ54HCT 373FK | Samples |
| 5962-8686701RA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8686701RA SNJ54HCT373J | Samples |
| 5962-8686701VSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8686701VS A SNV54HCT373W | Samples |
| JM38510/65453BRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65453BRA | Samples |
| JM38510/65453BSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65453BSA | Samples |
| M38510/65453BRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65453BRA | Samples |
| M38510/65453BSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | JM38510/ 65453BSA | Samples |
| SN54HCT373J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SN54HCT373J | Samples |
| SN74HCT373DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT373 | Samples |
| SN74HCT373N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HCT373N | Samples |
| SN74HCT373NE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74HCT373N | Samples |
| SN74HCT373NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HCT373 | Samples |
| SN74HCT373PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HT373 | Samples |
| SNJ54HCT373FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962- 86867012A SNJ54HCT 373FK | Samples |
| SNJ54HCT373J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8686701RA SNJ54HCT373J | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| SNJ54HCT373W | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | SNJ54HCT373W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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OTHER QUALIFIED VERSIONS OF SN54HCT373, SN54HCT373-SP, SN74HCT373 :

- Catalog : [SN74HCT373](#), [SN54HCT373](#)
- Military : [SN54HCT373](#)
- Space : [SN54HCT373-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74HCT373DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74HCT373DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74HCT373NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74HCT373PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74HCT373PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74HCT373DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 41.0 |
| SN74HCT373DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HCT373NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74HCT373PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74HCT373PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-86867012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8686701VSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| JM38510/65453BSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| M38510/65453BSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74HCT373N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74HCT373NE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54HCT373FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54HCT373W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

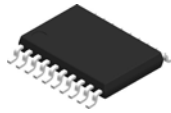
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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