LF412QML Low Offset, Low Drift Dual JFET Input Operational Amplifier

Check for Samples: LF412QML

FEATURES

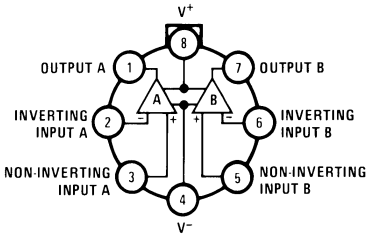
- **Input Offset Voltage Drift: 20 µV/°C (Max)**
- **Low Input Bias Current: 50 pA (Typ)**
- **Low Input Noise Current: 0.01 pA/$\sqrt{Hz}$ (Typ)**
- **Wide Gain Bandwidth: 2.7 MHz (Min)**
- **High Slew Rate: 8V/µs (Min)**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Total Harmonic Distortion <0.02%**
- **Low 1/f Noise Corner: 50 Hz**
- **Fast Settling Time to 0.01%: 2 µs**

DESCRIPTION

This device is a low cost, high speed, JFET input operational amplifier with very low input offset voltage and ensured input offset voltage drift. It requires low supply current yet maintains a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

This amplifier may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

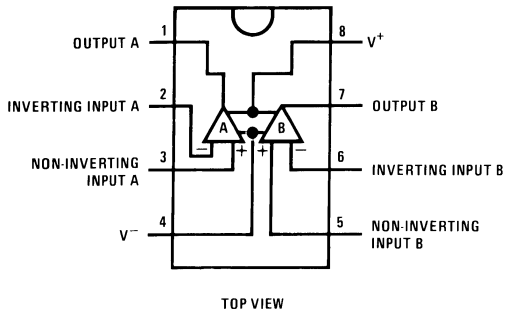
Connection Diagram



Note. Pin 4 connected to case.

TOP VIEW

Figure 1. TO-99 Package



TOP VIEW

Figure 2. CDIP Package

Simplified Schematic

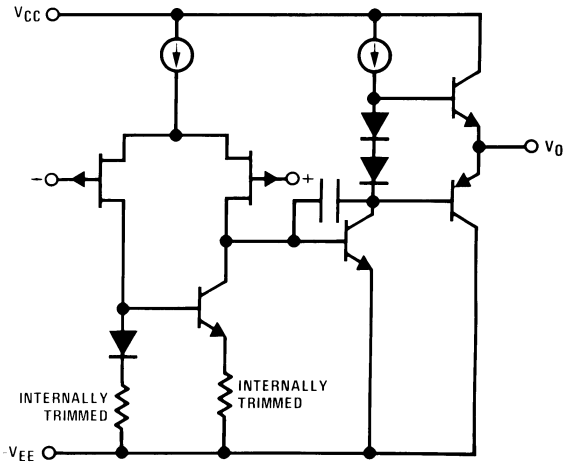
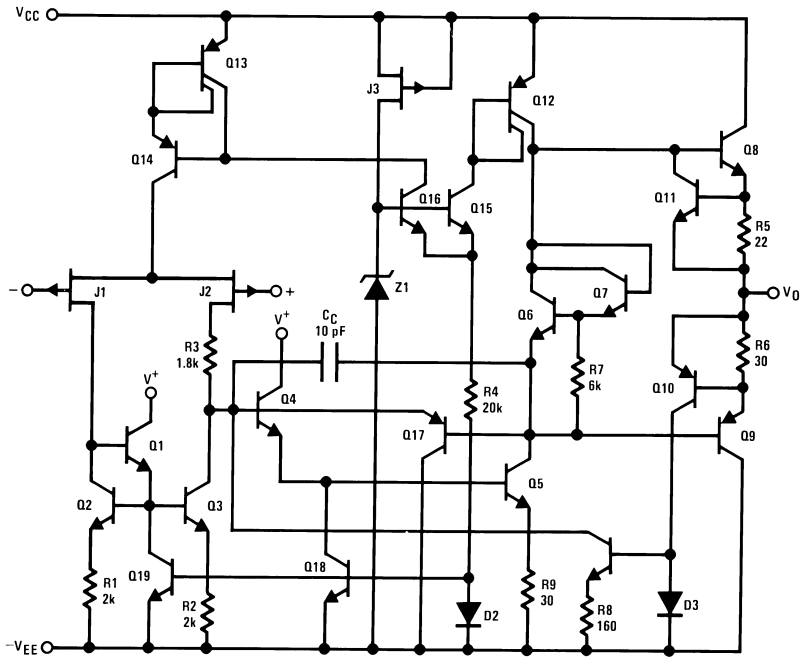


Figure 3. 1/2 Dual

Detailed Schematic



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1]

Supply Voltage			±18V
Differential Input Voltage			±30V
Input voltage Range[2]			±15V
Output Short Circuit Duration[3]			Continuous
Power Dissipation[4]		TO-99 Package	800mW
		CDIP Package	800mW
T_{Jmax}			150°C
Thermal Resistance	θ_{JA}	TO-99 Package (Still Air)	160°C/W
		TO-99 Package (500 LF/Min Air Flow)	83°C/W
		CDIP Package (Still Air)	122°C/W
		CDIP Package (500 LF/Min Air Flow)	66°C/W
	θ_{JC}	TO-99 Package	38°C/W
		CDIP Package	15°C/W
Supply voltage Range			±5V to ±15V
Operating Temperature Range			$-55°C \le T_A \le 125°C$
Storage Temperature Range			$-65°C \le T_A \le 150°C$
Lead Temperature Soldering (10 Sec)			260°C
ESD Tolerance[5]			1,700V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(3) Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
(5) Human body model, 1.5 kΩ in series with 100 pF.

Quality Conformance Inspection

Table 1. Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55
12	Settling time at	+25
13	Settling time at	+125
14	Settling time at	-55

Electrical Characteristics DC parameters

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
V_{IO}	Input offset Voltage	R_S = 10KΩ		-3.0	3.0	mV	1
				-5.0	5.0	mV	2, 3
ΔV_{IO} / ΔT	Temperature Coefficient of Input Offset Voltage	R_S = 10KΩ, 25°C ≤ T_A ≤ 125°C	See (1)	-20	20	µV/°C	2
		R_S = 10KΩ, -55°C ≤ T_A ≤ 25°C	See (1)	-20	20	µV/°C	3
I_{IO}	Input Offset Current		See (2)	-0.1	0.1	nA	1
				-25	25	nA	2
±I_{IB}	Input Bias Current		See (2)		0.2	nA	1
					50	nA	2
CMRR	Common Mode Rejection Ratio	R_S ≤ 10KΩ, V_{CM} = ±11V		70		dB	1, 2, 3
+PSRR	Supply Voltage Rejection Ratio	6V ≤ +V_{CC} ≤ 15V, -V_{CC} = -15V		70		dB	1, 2, 3
-PSRR	Supply Voltage Rejection Ratio	+V_{CC} = 15V, -15V ≤ -V_{CC} ≤ -6V		70		dB	1, 2, 3
I_S	Supply Current				6.5	mA	1, 2, 3
-I_{OS}	Output Short Circuit Current			13	45	mA	1
				6.0	45	mA	2, 3
+I_{OS}	Output Short Circuit Current			-45	-13	mA	1
				-45	-6.0	mA	2, 3
+A_{VS}	Large Signal Voltage Gain	V_O = 0 to 10V, R_L = 2KΩ	See (3)	25		V/mV	4
				15		V/mV	5, 6
-A_{VS}	Large Signal Voltage Gain	V_O = 0 to -10V, R_L = 2KΩ	See (3)	25		V/mV	4
				15		V/mV	5, 6
+V_O	Output Voltage Swing	R_L = 10KΩ, +V_I = 11V, -V_I = -11V		12		V	4, 5, 6
-V_O	Output Voltage Swing	R_L = 10KΩ, +V_I = -11V, -V_I = 11V			-12	V	4, 5, 6
V_{CM}	Input Common Mode Voltage Range		See (4)	−11	11	V	1, 2, 3

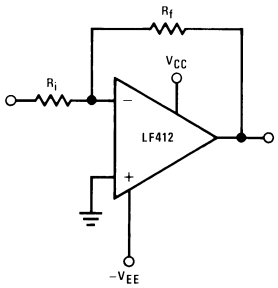
(1) Specified parameter, not tested.
(2) R_S = 10KΩ @ +125°C
(3) Datalog reading in K = V/mV.
(4) Specified by CMRR.

Electrical Characteristics AC Parameters

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0V, R_S = 0Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-group
SR+	Slew Rate	V_O = -5V to 5V		8.0		V/µs	7
SR-	Slew Rate	V_O = 5V to -5V		8.0		V/µs	7
GBW	Gain Bandwidth Product			2.7		MHz	7

Typical Connection



Typical Performance Characteristics

Input Bias Current

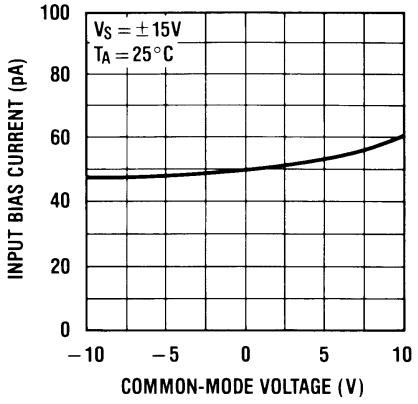


Figure 4.

Input Bias Current

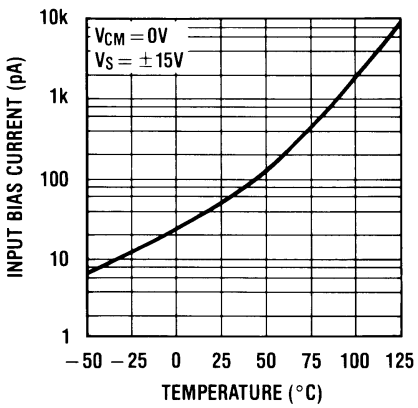


Figure 5.

Supply Current

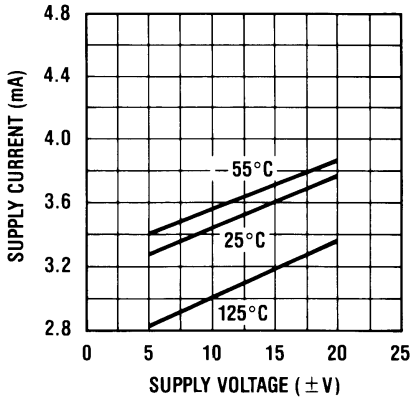


Figure 6.

Positive Common-Mode Input Voltage Limit

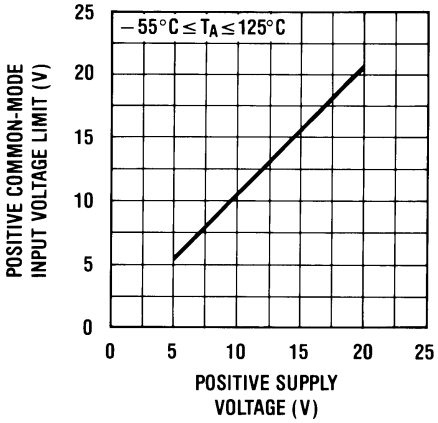


Figure 7.

Negative Common-Mode Input Voltage Limit

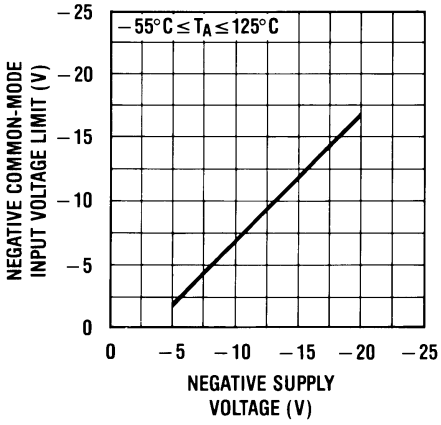


Figure 8.

Positive Current Limit

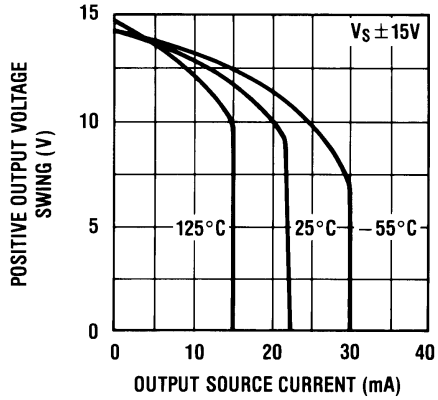


Figure 9.

Typical Performance Characteristics (continued)

Negative Current Limit

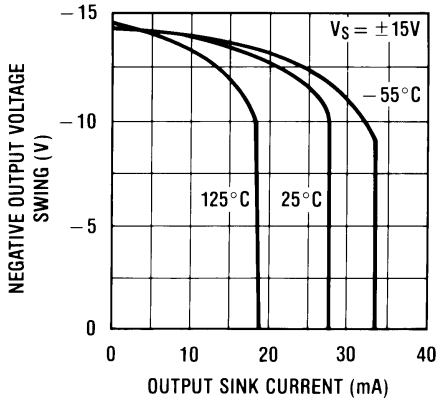


Figure 10.

Output Voltage Swing

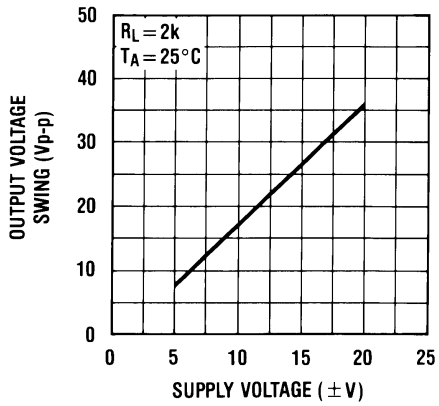


Figure 11.

Output Voltage Swing

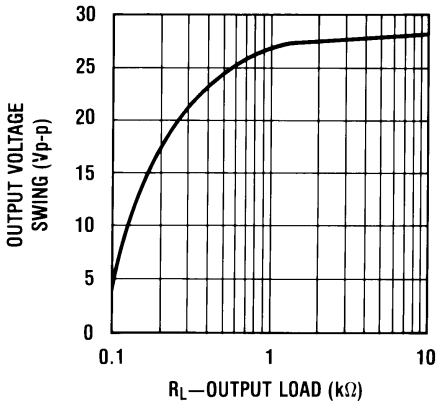


Figure 12.

Gain Bandwidth

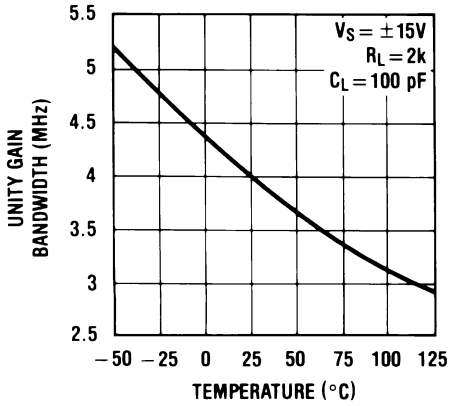


Figure 13.

Bode Plot

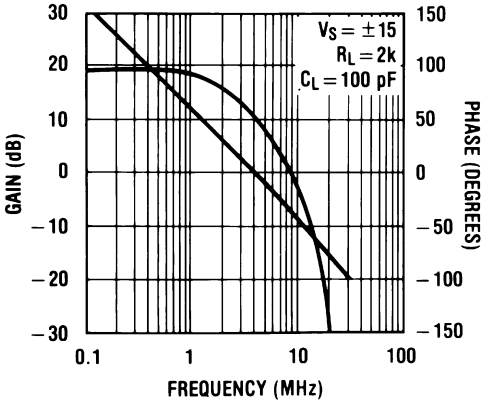


Figure 14.

Slew Rate

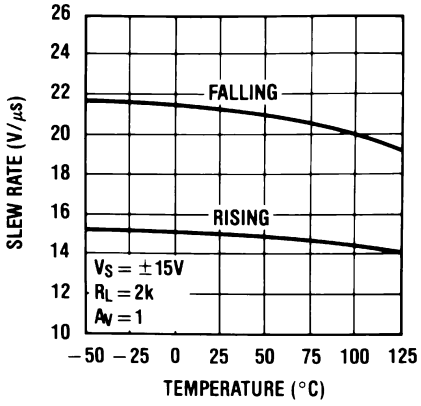


Figure .

Typical Performance Characteristics (continued)

Distortion vs Frequency

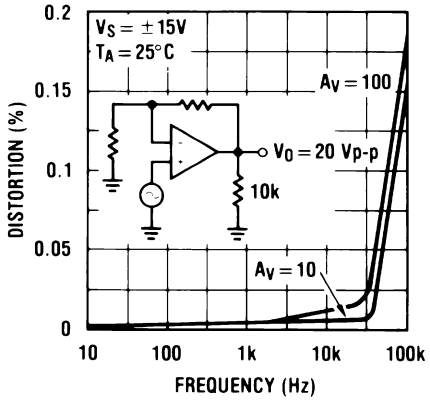


Figure 15.

Undistorted Output Voltage Swing

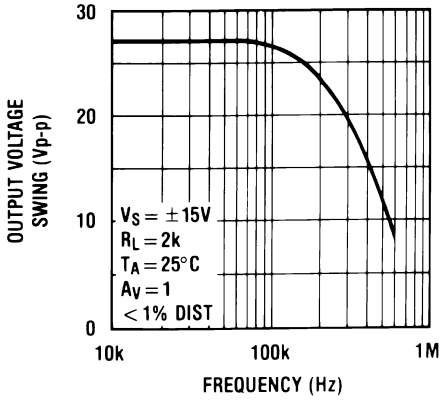


Figure 16.

Open Loop Frequency Response

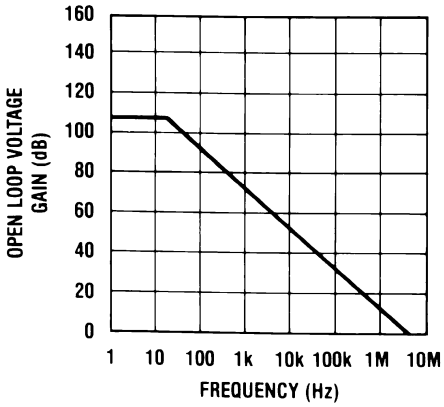


Figure 17.

Common-Mode Rejection Ratio

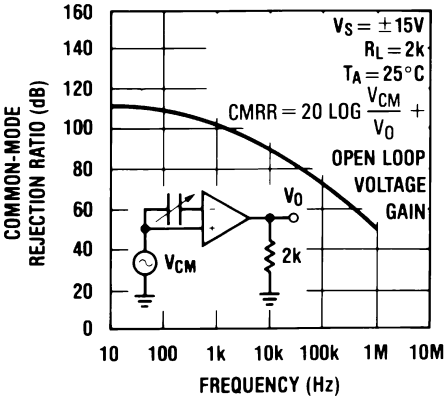


Figure 18.

Power Supply Rejection Ratio

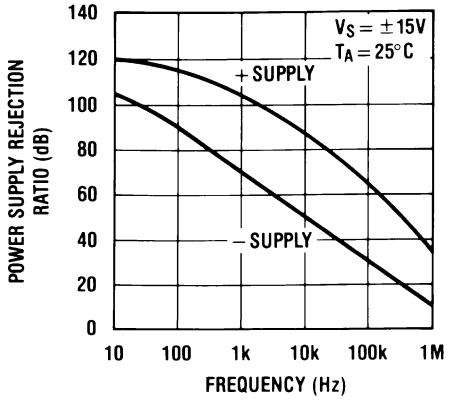


Figure 19.

Equivalent Input Noise Voltage

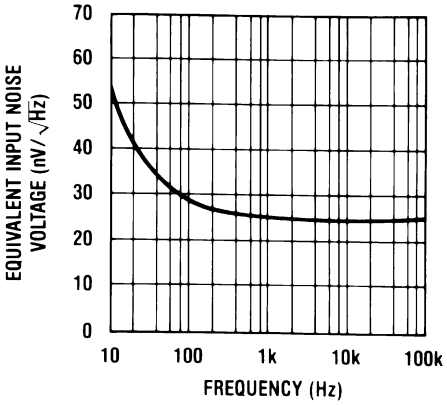


Figure 20.

Typical Performance Characteristics (continued)

Open Loop Voltage Gain

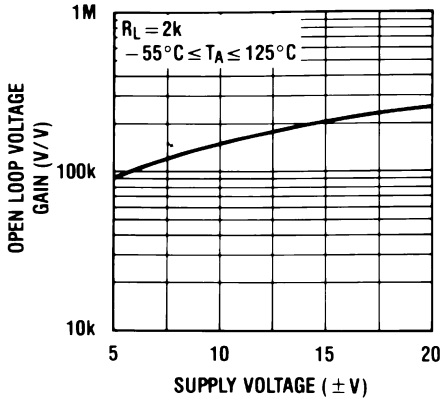


Figure 21.

Output Impedance

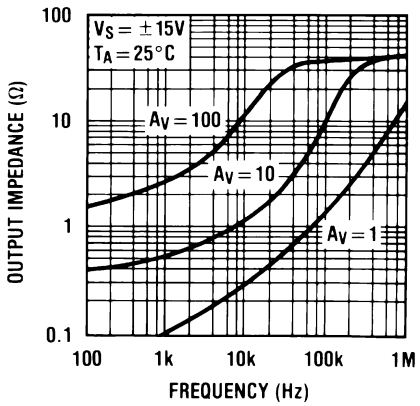


Figure 22.

Inverter Settling Time

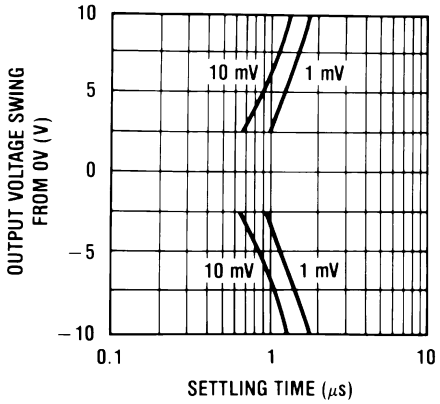


Figure 23.

Pulse Response

R_L=2 kΩ, C_L=10 pF

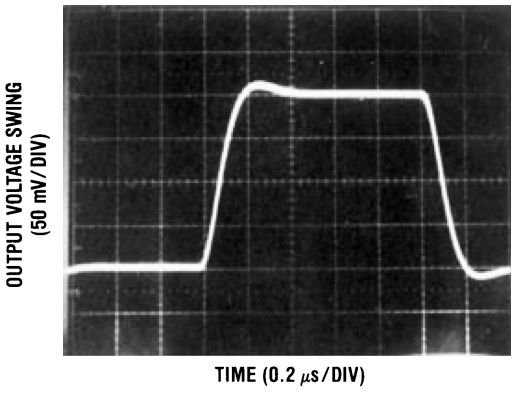


Figure 24. Small Signal Inverting

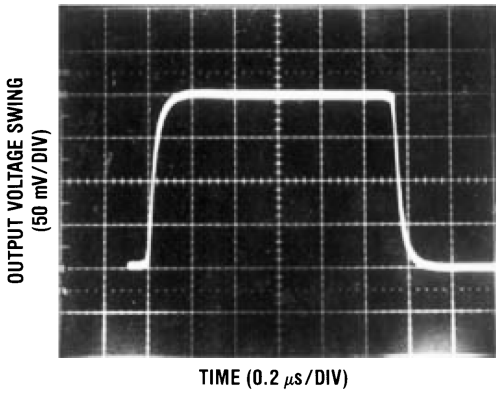


Figure 25. Small Signal Non-Inverting

Pulse Response (continued)

R_L=2 kΩ, C_L=10 pF

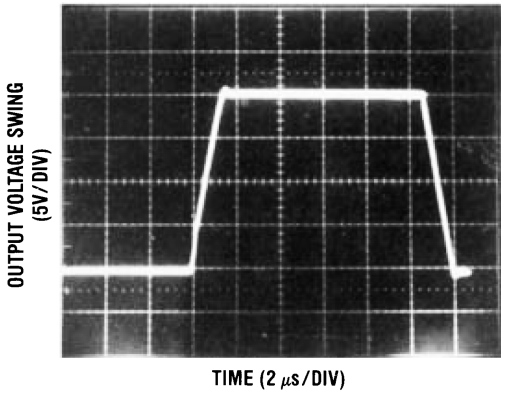


Figure 26. Large Signal Inverting

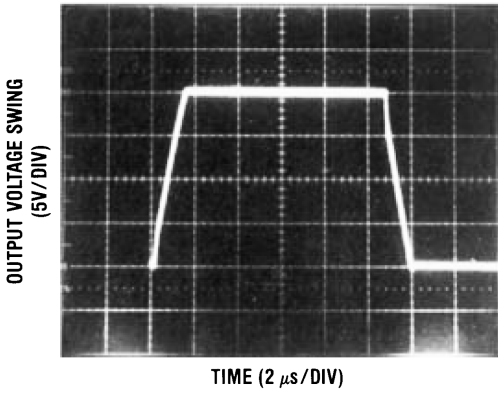


Figure 27. Large Signal Non-Inverting

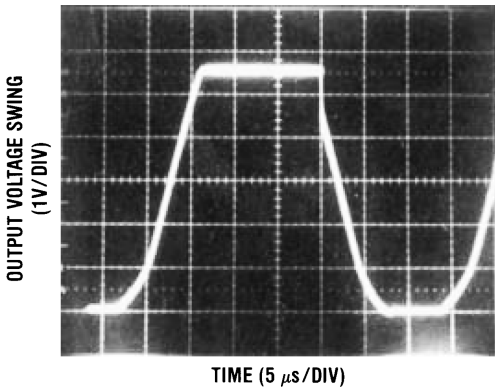


Figure 28. Current Limit (R_L=100Ω)

APPLICATION HINTS

The LF412 JFET input dual op amp is internally trimmed (BI-FET II™) providing very low input offset voltages and ensured input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on ±6.0V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Application

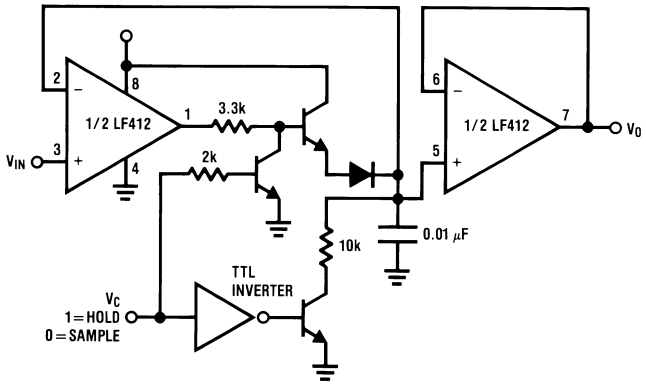


Figure 29. Single Supply Sample and Hold

Table 2. Revision History

Date Released	Revision	Section	Changes
12/08/2010	A	New Release to Corporate format	1 MDS datasheet converted into Corporate datasheet format. MNLF412-X Rev 0C1 will be archived.
03/26/2013	A	All Sections	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LF412 MD8	ACTIVE	DIESALE	Y	0	154	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125		Samples
LF412MH/883	ACTIVE	TO-99	LMC	8	20	RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LF412MH/883 Q ACO LF412MH/883 Q >T	Samples
LF412MJ/883	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LF412MJ /883 Q ACO /883 Q >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

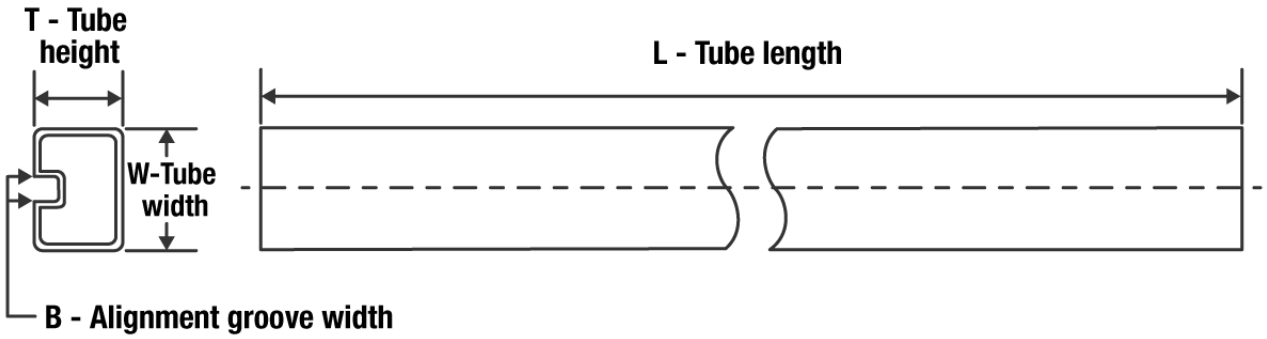
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

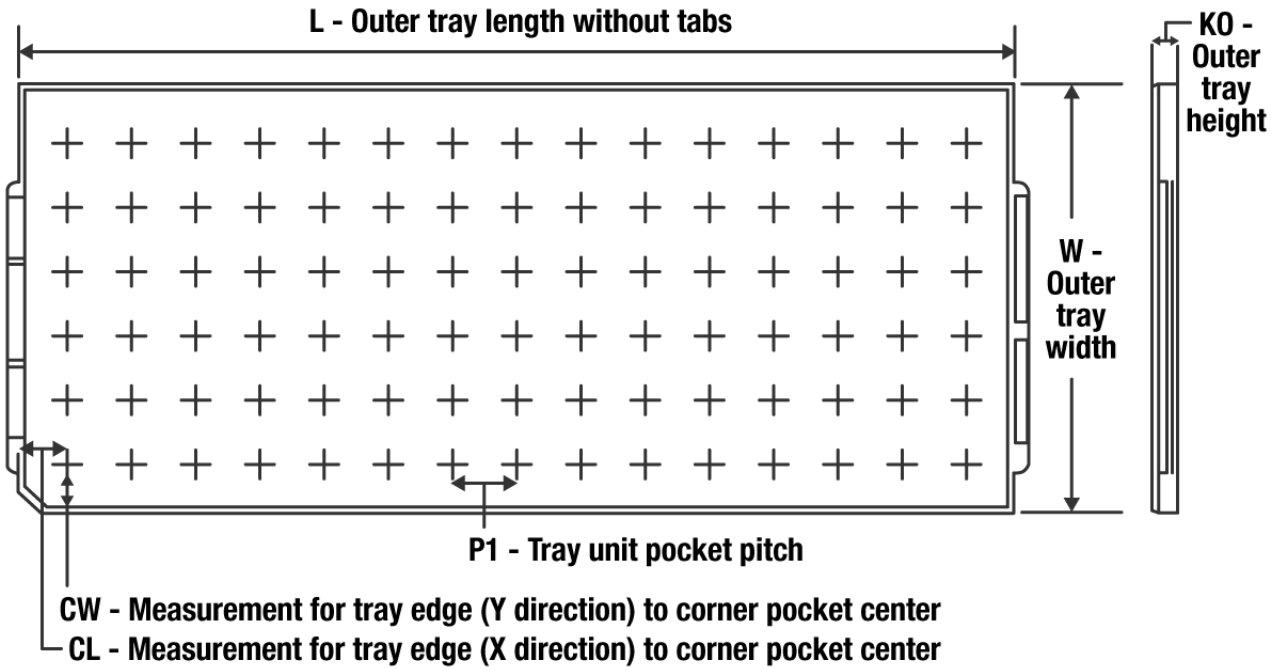
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LF412MJ/883	NAB	CDIP	8	40	506.98	15.24	13440	NA

TRAY

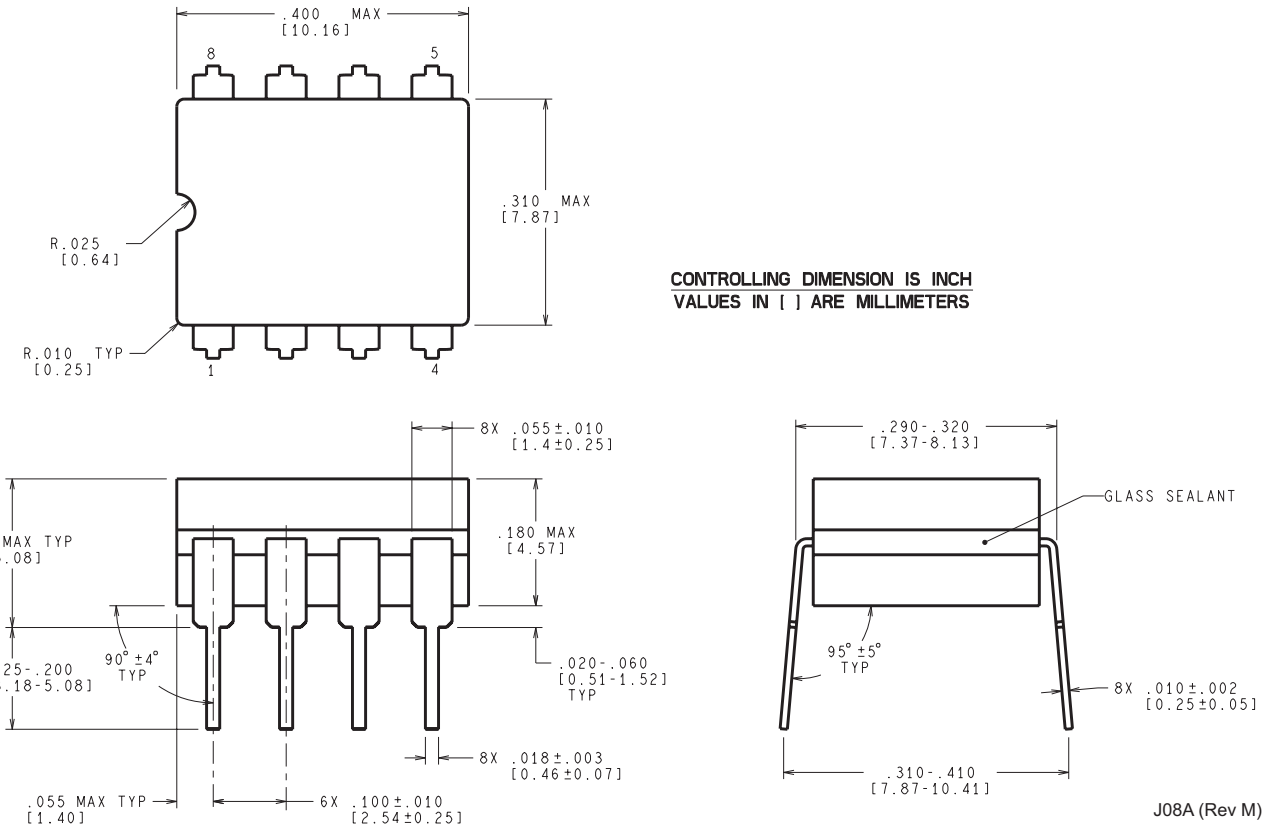


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

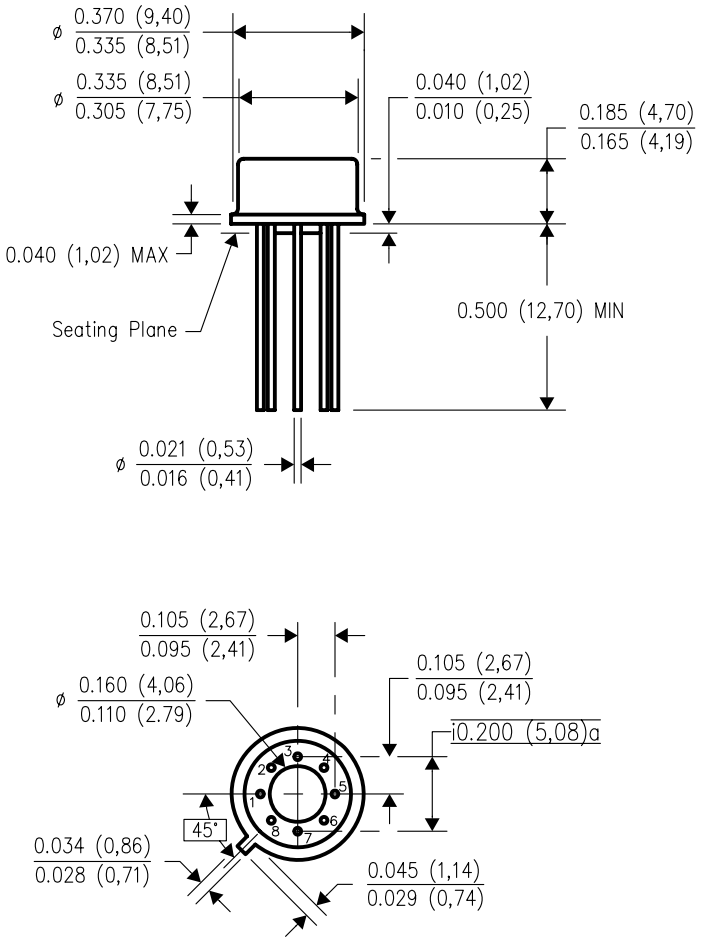
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
LF412MH/883	LMC	TO-CAN	8	20	2 X 10	150	126.49	61.98	8890	11.18	12.95	18.54

NAB0008A


.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

LMC (O–MBCY–W8) METAL CYLINDRICAL PACKAGE



4202483/B 09/07

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Leads in true position within 0.010 (0,25) R @ MMC at seating plane.
D. Pin numbers shown for reference only. Numbers may not be marked on package.
E. Falls within JEDEC MO–002/TO–99.

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