

Power Supply Supervisory Circuit

FEATURES

- Includes Over-Voltage, Under-Voltage, and Current Sensing Circuits
- Internal 1% Accurate Reference
- Programmable Time Delays
- SCR “Crowbar” Drive of 300 mA
- Remote Activation Capability
- Optional Over-Voltage Latch
- Uncommitted Comparator Inputs for Low Voltage Sensing (UC1544 Series Only)

DESCRIPTION

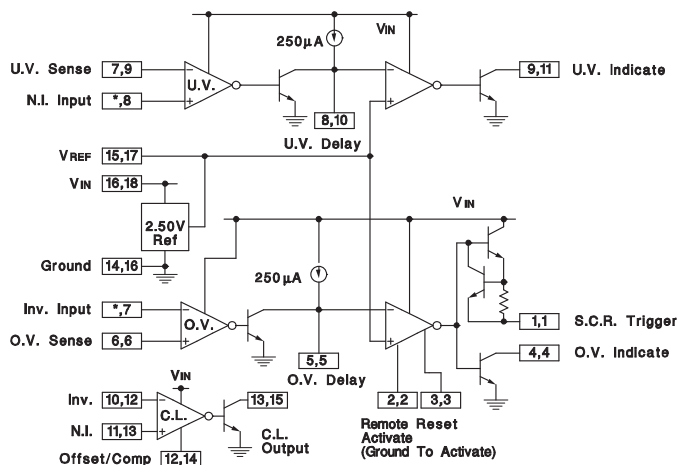
The monolithic integrated circuits contain all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR “crowbar” shutdown; an undervoltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this device, together with an independent, accurate reference generator.

Both over- and under-voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or’ed together, and although the SCR trigger is directly connected only to the over-voltage sensing circuit, it may be optionally activated by any of the other outputs, or from an external signal. The O.V. circuit also includes an optional latch and external reset capability.

The UC1544/2544/3544 devices have the added versatility of completely uncommitted inputs to the voltage sensing comparators so that levels less than 2.5 V may be monitored by dividing down the internal reference voltage. The current sense circuit may be used with external compensation as a linear amplifier or as a highgain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

BLOCK DIAGRAM



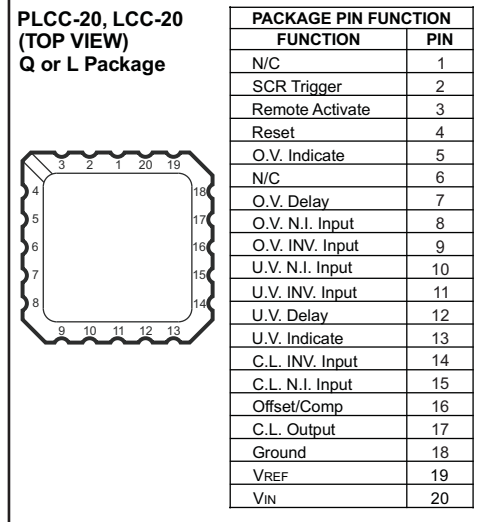
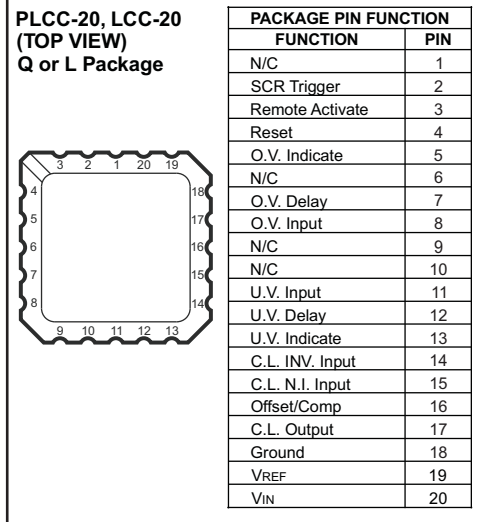
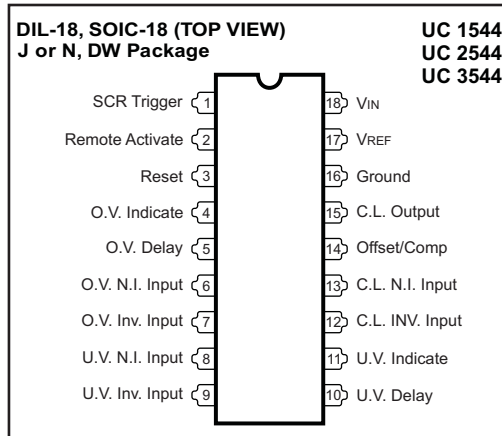
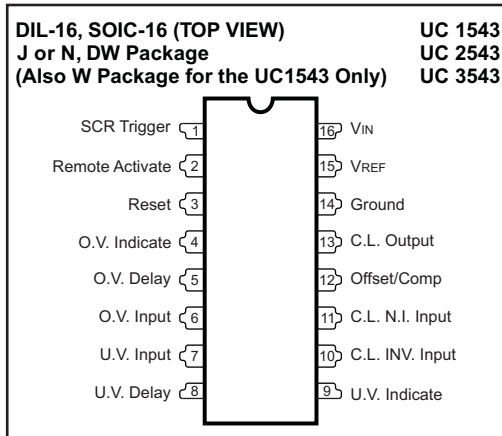
NOTE:

For each terminal, first number refers to 1543 series, second to 1544 series.
*On 1543 series, this function is internally connected to VREF.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Connection Diagrams



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | UNIT |
|-----------|--|----------------|------|
| V_{IN} | Input supply voltage | 40 | V |
| | Sense inputs, voltage range | 0 to V_{IN} | |
| | SCR trigger current ⁽²⁾ | -600 | mA |
| | Indicator output voltage | 40 | V |
| | Indicator output sink current | 50 | mA |
| | Power dissipation (package limitation) | 1000 | mW |
| T_J | Operating temperature range | UC1543, UC1544 | °C |
| | | UC2543, UC2544 | |
| | | UC3543, UC3544 | |
| T_{stg} | Storage temperature range | -65 to 150 | |

(1) Currents are positive-into, negative-out of the specified terminal.

(2) At higher input voltages, a dissipation limiting resistor, R_G , is required.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to 125°C for the UC1543 and UC1544; -25°C to 85°C for the UC2543 and UC2544; and 0°C to 70°C for the UC3543 and UC3544. Electrical tests are performed with $V_{IN} = 10\text{ V}$ and 2-k Ω pull-up resistors on all indicator outputs. All electrical specifications for the UC1544, UC2544, and UC3544 devices are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5 V reference. $T_A = T_J$.

| PARAMETER | | TEST CONDITIONS | UC1543/UC1544/UC2543/ UC2544 | | | UC3543/UC3544 | | | UNIT |
|----------------------------|--|---|---------------------------------|------|------|---------------|------|------|-----------------------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V_{IN} | Input voltage range | $T_J = 25^\circ\text{C}$ to T_{MAX} | 4.5 | | 40 | 4.5 | | 40 | V |
| | | T_{MIN} to T_{MAX} | 4.7 | | 40 | 4.7 | | 40 | |
| I_{CC} | Supply current | $V_{IN} = 40\text{ V}$, output open, $T_J = 25^\circ\text{C}$ | | 7 | 10 | | 7 | 10 | mA |
| | | $T_{MIN} \leq T_J \leq T_{MAX}$ | | | 15 | | | 15 | |
| Reference Section | | | | | | | | | |
| V_{OUT} | Output voltage | $T_J = 25^\circ\text{C}$ | 2.48 | 2.5 | 2.52 | 2.45 | 2.50 | 2.55 | V |
| | | Over temperature range | 2.45 | | 2.55 | 2.40 | | 2.60 | |
| | Line regulation | $V_{IN} = 5$ to 30 V | | 1 | 5 | | 1 | 5 | mV |
| | Load regulation | $I_{REF} = 0$ to 10 mA | | 1 | 10 | | 1 | 10 | |
| | Short circuit current | $V_{REF} = 0$ | -10 | -20 | -40 | -12 | -20 | -40 | mA |
| | Temperature stability | | | 50 | | | 50 | | ppm/ $^\circ\text{C}$ |
| SCR Trigger Section | | | | | | | | | |
| | Peak output current | $V_{IN} = 5\text{ V}$, $R_G = 0$, $V_O = 0$ | -100 | -300 | -600 | -100 | -300 | -600 | mA |
| | Peak output voltage | $V_{IN} = 15\text{ V}$, $I_O = -100\text{ mA}$ | 12 | 13 | | 12 | 13 | | V |
| | Output OFF voltage | $V_{IN} = 40\text{ V}$ | | 0 | 0.1 | | 0 | 0.1 | |
| | Remote activate current | R/A Pin = GND | | -0.4 | -0.8 | | -0.4 | -0.8 | mA |
| | Remote activate voltage | R/A Pin Open | | 2 | 6 | | 2 | 6 | V |
| | Reset current | Reset = GND, R/A = GND | | -0.4 | -0.8 | | -0.4 | -0.8 | mA |
| | Reset voltage | Reset open, R/A = GND | | 2 | 6 | | 2 | 6 | V |
| | Output current rise time | $R_L = 50$, $T_J = 25^\circ\text{C}$, $C_D = 0$ | | 400 | | | 400 | | mA/ μs |
| | Prop. delay from R/A | $R_L = 50$, $T_J = 25^\circ\text{C}$, $C_D = 0$ | | 300 | | | 300 | | ns |
| | Prop. delay from O/V input | $R_L = 50$, $T_J = 25^\circ\text{C}$, $C_D = 0$ | | 500 | | | 500 | | |
| Comparator Section | | | | | | | | | |
| | Input threshold (Input voltage rising on O.V. and falling on U.V.) | $T_J = 25^\circ\text{C}$ | 2.45 | 2.50 | 2.55 | 2.40 | 2.50 | 2.60 | V |
| | | Over temperature range | 2.40 | | 2.60 | 2.35 | | 2.65 | |
| | Input hysteresis | | | 25 | | | 25 | | mV |
| | Input bias current | Sense input = 0 V | | -0.3 | -1.0 | | -0.3 | -1.0 | μA |
| | Delay saturation | | | 0.2 | 0.5 | | 0.2 | 0.5 | V |
| | Delay high level | | | 6 | 7 | | 6 | 7 | |
| | Delay charging current | $V_O = 0$ | -200 | -250 | -300 | -200 | -250 | -300 | μA |
| | Indicate saturation | $I_L = 10\text{ mA}$ | | 0.2 | 0.5 | | 0.2 | 0.5 | V |
| | Indicate leakage | $V_{IND} = 40\text{ V}$ | | 0.01 | 1.0 | | 0.01 | 1.0 | μA |
| | Propagation delay | Input over drive = 200 mV, $T_J = 25^\circ\text{C}$, $C_D = 0$ | | 400 | | | 400 | | ns |
| | | Input over drive = 200 mV, $T_J = 25^\circ\text{C}$, $C_D = 1\ \mu\text{F}$ | | 10 | | | 10 | | ms |

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for $T_A = -55^{\circ}\text{C}$ to 125°C for the UC1543 and UC1544; -25°C to 85°C for the UC2543 and UC2544; and 0°C to 70°C for the UC3543 and UC3544. Electrical tests are performed with $V_{IN} = 10\text{ V}$ and 2-k Ω pull-up resistors on all indicator outputs. All electrical specifications for the UC1544, UC2544, and UC3544 devices are tested with the inverting over-voltage input and the non-inverting under-voltage input externally connected to the 2.5 V reference. $T_A = T_J$.

| Current Limit Section | | | | | | | | |
|------------------------|---|----|------|---------|----|------|---------|---------------|
| Input voltage range | | 0 | | VIN -3V | 0 | | VIN -3V | V |
| Input Bias Current | Offset pin open, $V_{CM} = 0$ | | -0.3 | -1.0 | | -0.3 | -1.0 | μA |
| Input offset voltage | Offset pin open, $V_{CM} = 0$ | | 0 | 10 | | 0 | 10 | mV |
| | 10k from offset pin to GND | 80 | 100 | 120 | 80 | 100 | 120 | |
| CMRR | $0 \leq V_{CM} \leq 12\text{ V}$, $V_{IN} = 15\text{ V}$ | 60 | 70 | | 60 | 70 | | dB |
| AVOL | Offset pin open, $V_{CM} = 0$ V_i , $R_L = 10\text{ k}\Omega$ to $15\text{ k}\Omega$, $V_{OUT} = 1$ to 6 V | 72 | 80 | | 72 | 80 | | |
| Output saturation | $I_L = 10\text{ mA}$ | | 0.2 | 0.5 | | 0.2 | 0.5 | V |
| Output leakage | $V_{IND} = 40\text{ V}$ | | 0.01 | 1.0 | | 0.01 | 1.0 | μA |
| Small signal bandwidth | $A_V = 0\text{ dB}$, $T_J = 25^{\circ}\text{C}$ | | 5 | | | 5 | | MHz |
| Propagation delay | $V_{OVERDRIVE} = 100\text{ mV}$, $T_J = 25^{\circ}\text{C}$ | | 200 | | | 200 | | ns |

TYPICAL CHARACTERISTICS

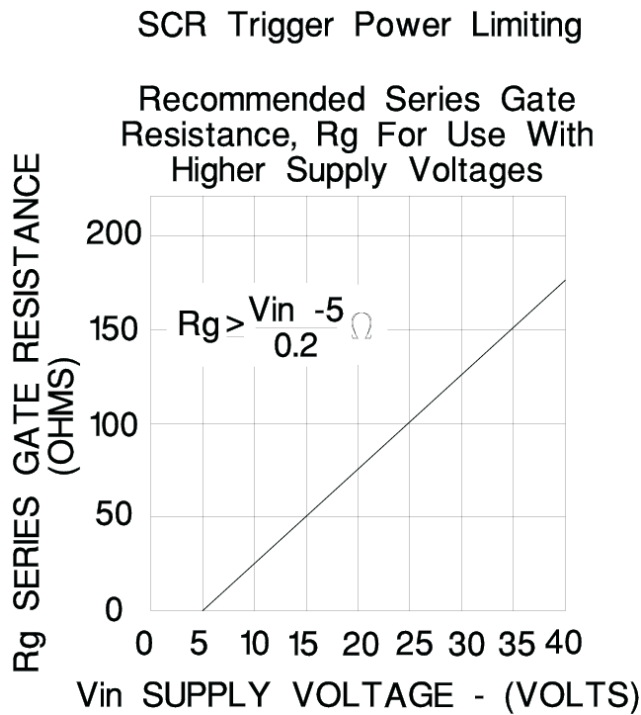


Figure 1.

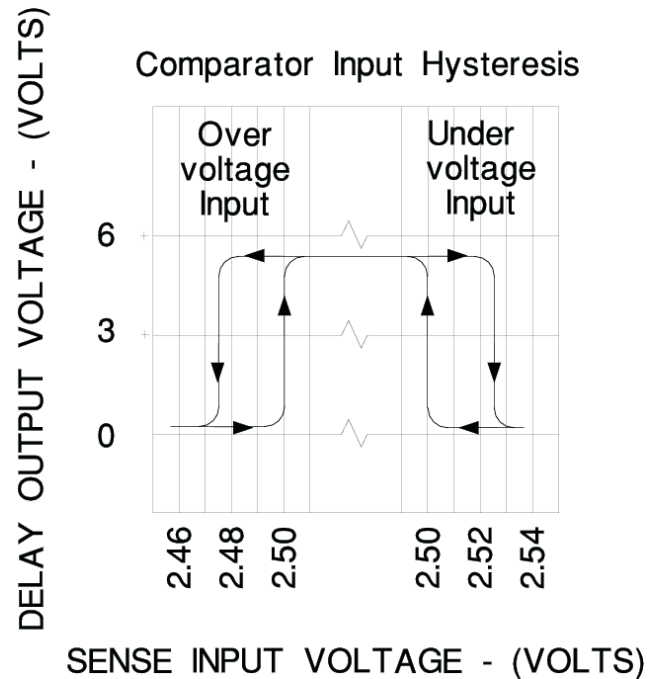


Figure 2.

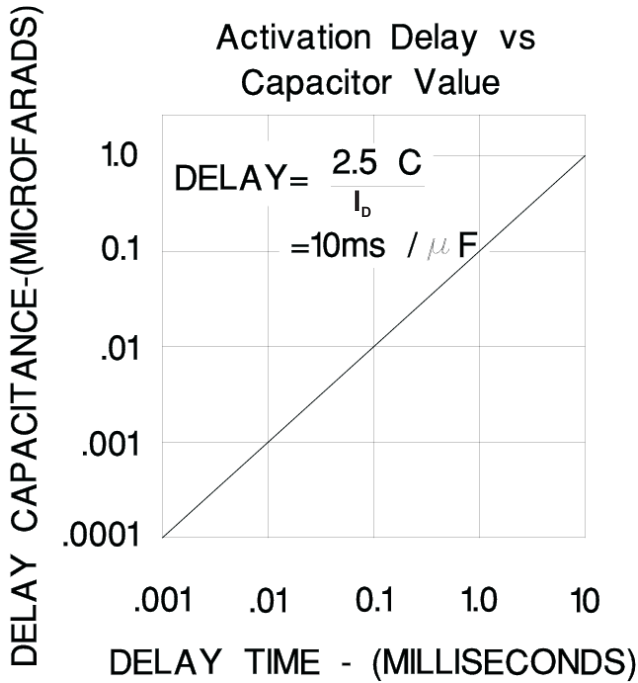


Figure 3.

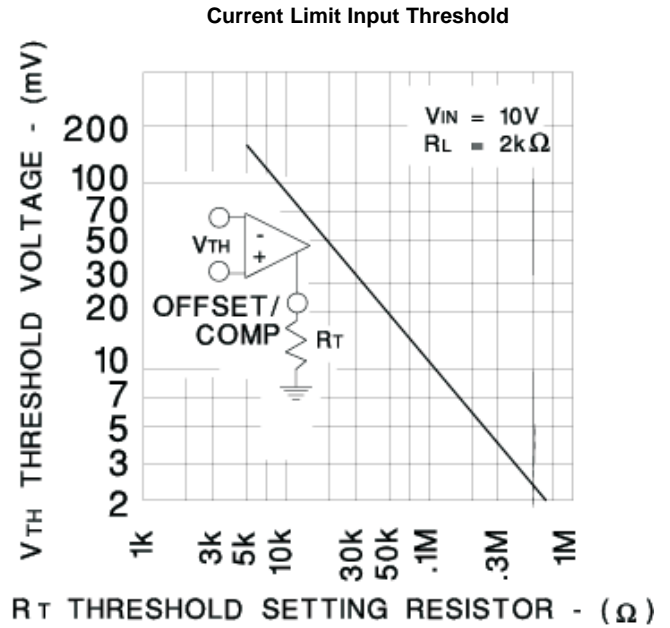


Figure 4.

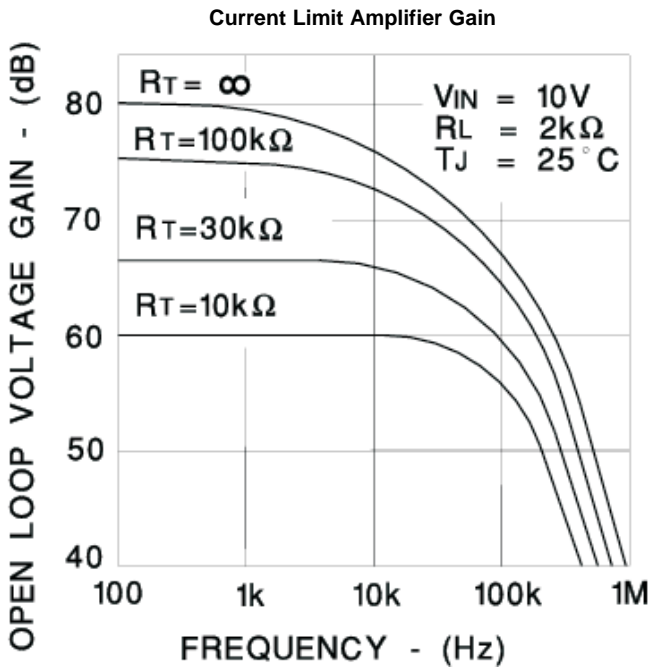


Figure 5.

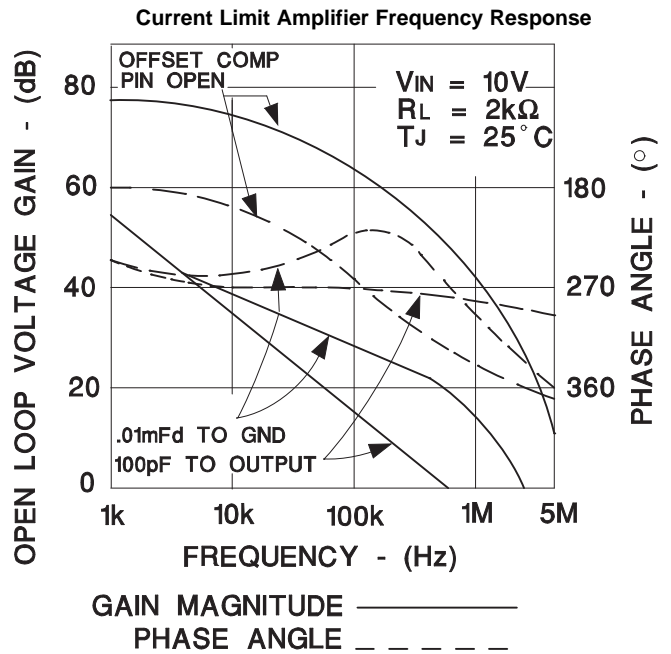


Figure 6.

APPLICATION INFORMATION

The values for the external components are determined as follows:

$$V_{TH} = \frac{1000}{R1}$$

Current limit input threshold,

C_S is determined by the current loop dynamics

$$I_P \cong \frac{V_{TH}}{R_{SC}} + \frac{V_O}{R_{SC}} \left(\frac{R2}{R2 + R3} \right)$$

Peak current to load,

$$I_{SC} = \frac{V_{TH}}{R_{SC}}$$

Short circuit current,

$$V_{O(low)} = \frac{2.5(R4 + R5 + R6)}{R5 + R6}$$

Low output voltage limit,

$$V_{O(high)} = \frac{2.5(R4 + R5 + R6)}{R6}$$

High output voltage limit,

Voltage sensing delay, $t_D = 10,000C_d$

$$R_G > \frac{V_{IN} - 5}{0.2}$$

SCR trigger power limiting resistor,

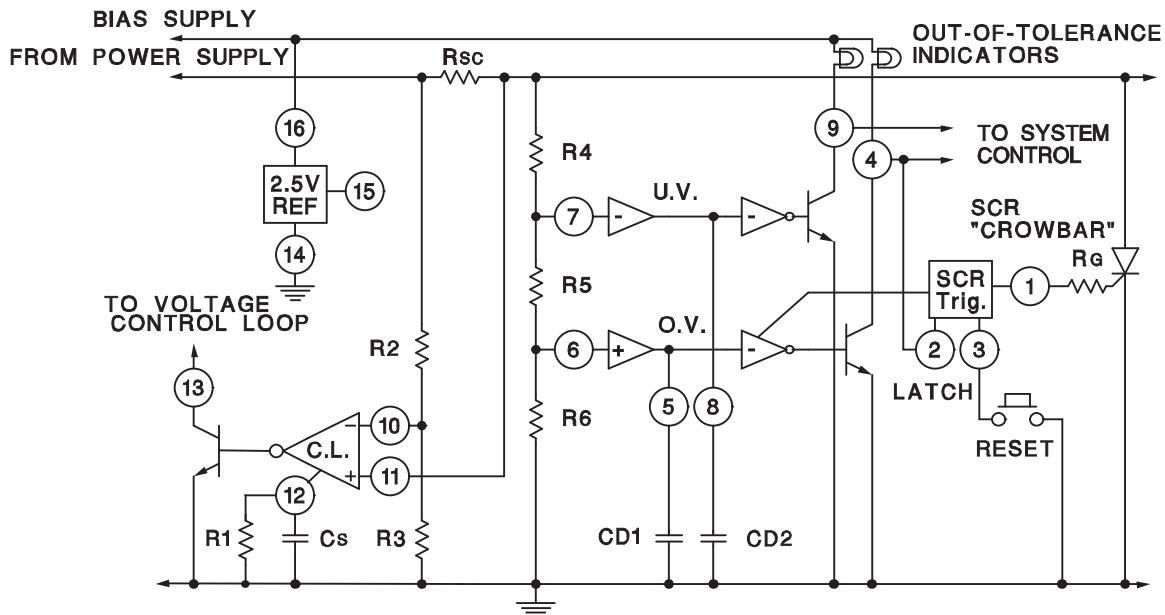


Figure 7. Typical Application

APPLICATION INFORMATION (continued)

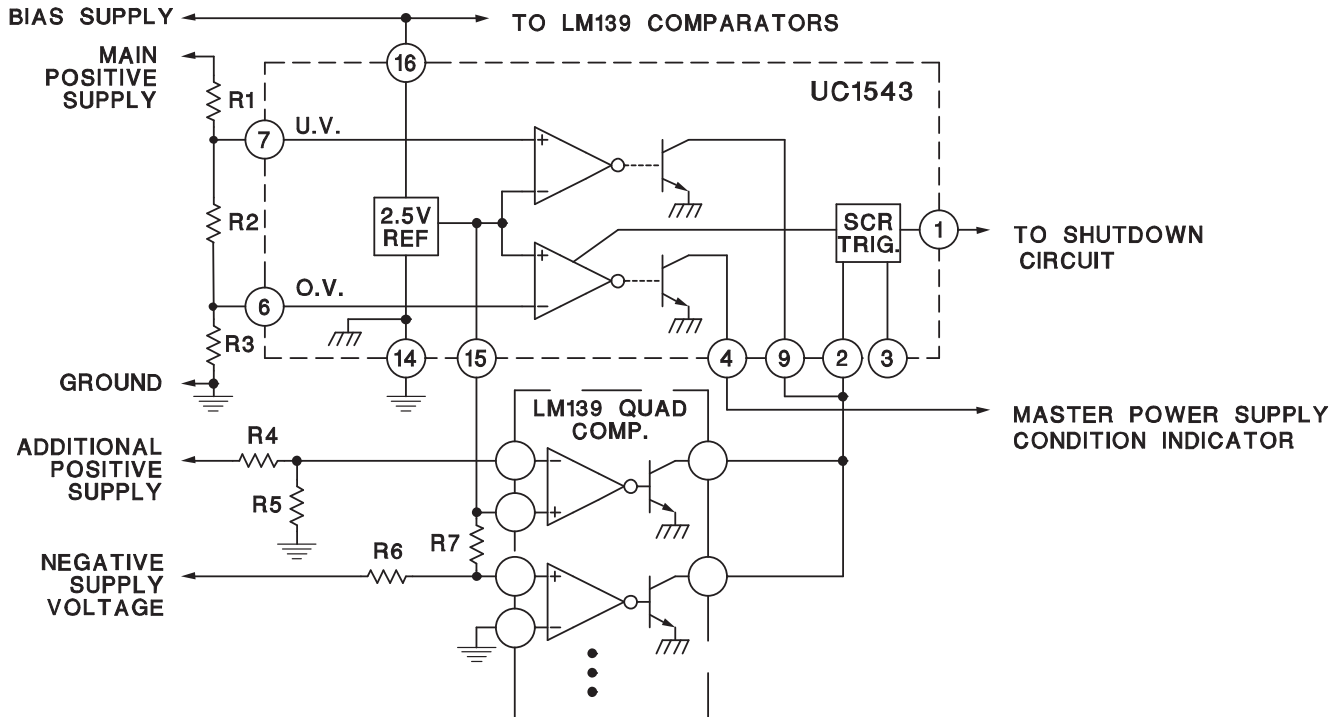


Figure 8. Sensing Multiple Supply Voltages

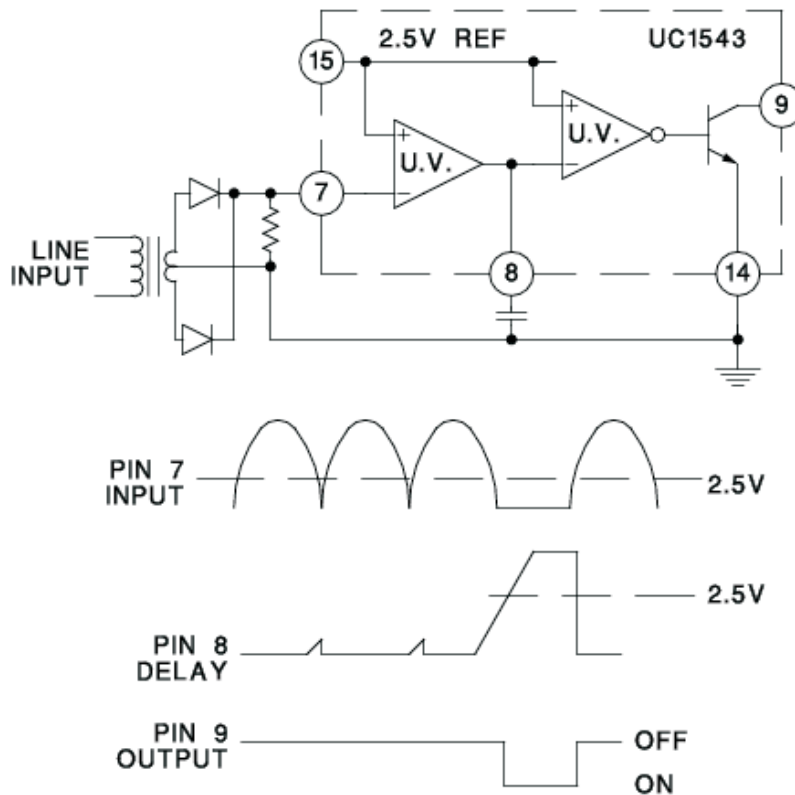


Figure 9. Input Line Monitor

APPLICATION INFORMATION (continued)

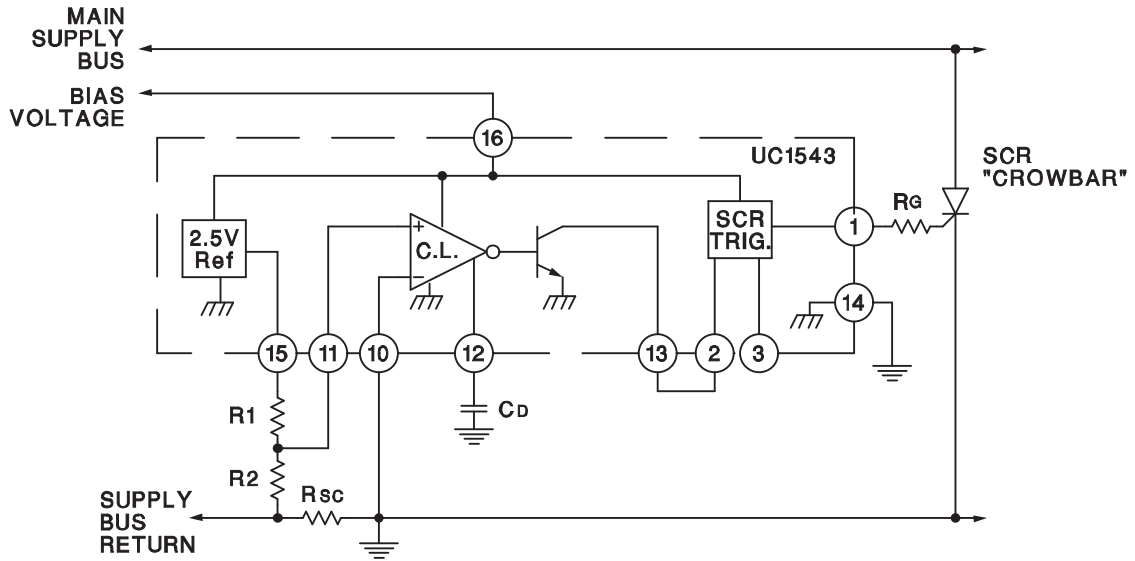


Figure 10. Overcurrent Shutdown

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--------------------------------|-------------------------|
| 5962-8774001EA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8774001EA UC1543J/883B | Samples |
| 5962-8774001FA | LIFEBUY | CFP | W | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | | 5962-8774001FA UC1543W/883B | |
| UC1543J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | UC1543J | Samples |
| UC1543J883B | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8774001EA UC1543J/883B | Samples |
| UC1543L | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | UC1543L | Samples |
| UC1543L883B | LIFEBUY | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | UC1543L/ 883B | |
| UC1543W883B | LIFEBUY | CFP | W | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | | 5962-8774001FA UC1543W/883B | |
| UC2543DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2543DW | Samples |
| UC2543J | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -25 to 85 | UC2543J | Samples |
| UC3543J | LIFEBUY | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | 0 to 70 | UC3543J | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UC2543, UC2543M, UC3543M :

- Catalog : [UC2543](#)
- Military : [UC2543M](#), [UC1543](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-8774001FA | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| UC1543L | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1543L883B | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1543W883B | W | CFP | 16 | 25 | 506.98 | 26.16 | 6220 | NA |
| UC2543DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

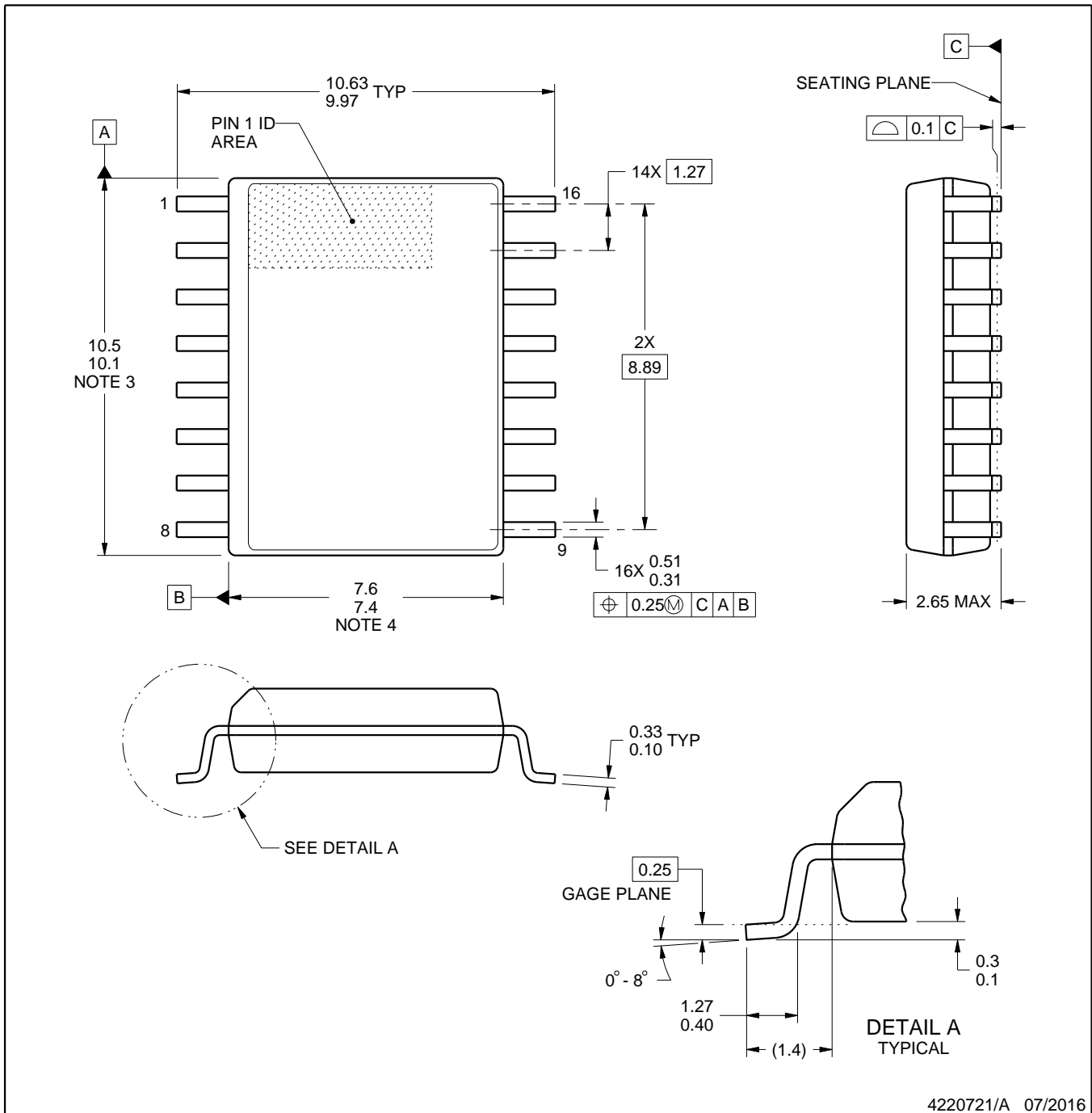


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

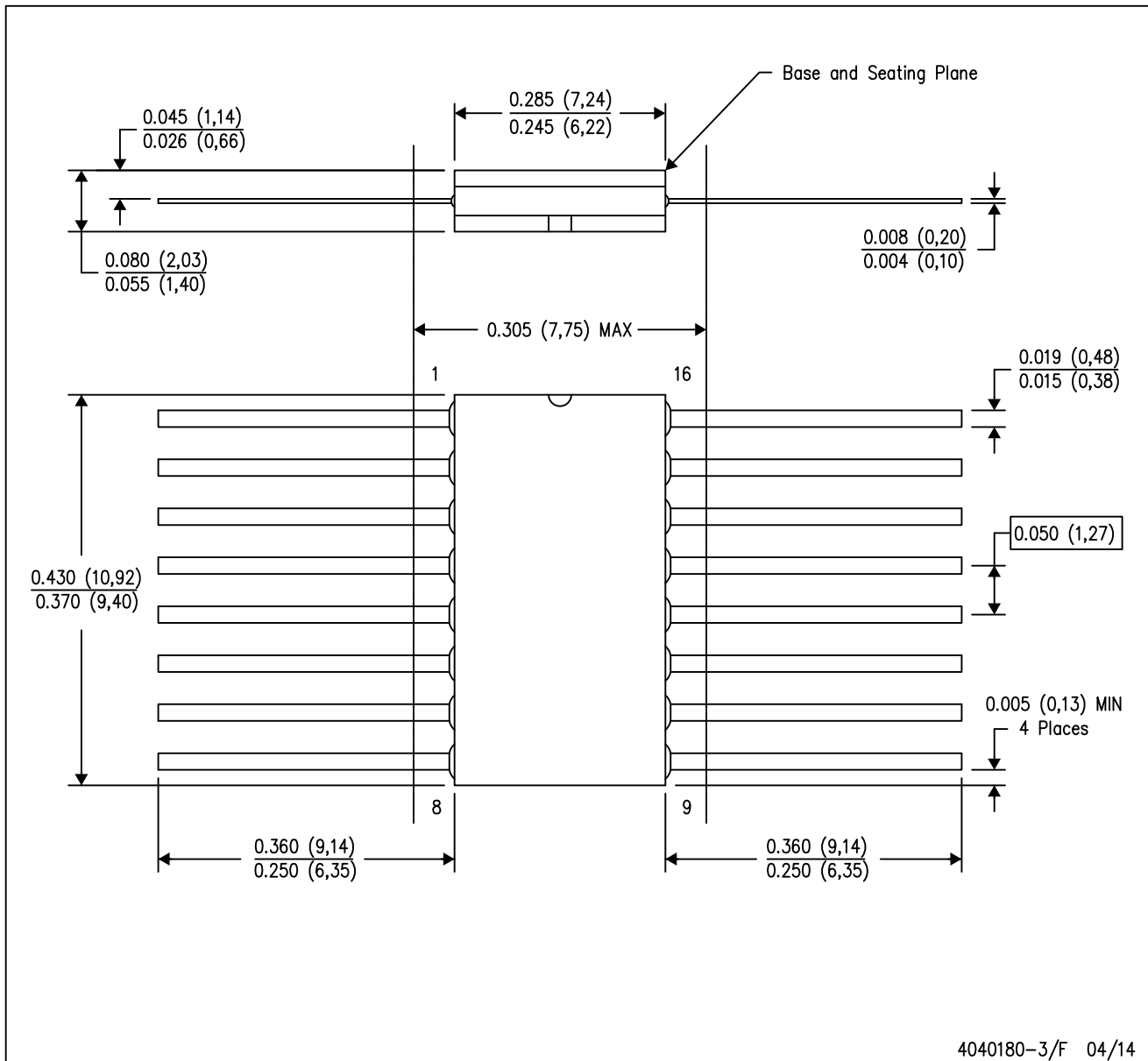
4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP2-F16

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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