TMP411 ±1°C Remote and Local Temperature Sensor With N-Factor and Series Resistance Correction

1 Features

- ±1°C Remote Diode Sensor
- ±1°C Local Temperature Sensor
- Programmable Non-Ideality Factor
- Series Resistance Cancellation
- Alert Function
- Offset Registers for System Calibration
- Pin and Registers Compatible With ADT7461 and ADM1032
- Programmable Resolution: 9 to 12 Bits
- Programmable Threshold Limits
- Two-Wire and SMBus Serial Interface
- Minimum and Maximum Temperature Monitors
- Multiple Interface Addresses
- $\overline{\text{ALERT}}$ and $\overline{\text{THERM2}}$ Pin Configuration
- Diode Fault Detection

2 Applications

- LCD and DLP and LCOS Projectors
- Servers
- Industrial Controllers
- Central Office Telecom Equipment
- Desktop and Notebook Computers
- Storage Area Networks (SAN)
- Industrial and Medical Equipment
- Processor and FPGA Temperature Monitoring

3 Description

The TMP411 device is a remote temperature sensor monitor with a built-in local temperature sensor. The remote temperature-sensor, diode-connected transistors are typically low-cost, NPN- or PNP-type transistors or diodes that are an integral part of microcontrollers, microprocessors, or FPGAs.

Remote accuracy is ±1°C for multiple device manufacturers, with no calibration needed. The two-wire serial interface accepts SMBus write byte, read byte, send byte and receive byte commands to program the alarm thresholds and to read temperature data.

Features that are included in the TMP411 device are: series resistance cancellation, programmable non-ideality factor, programmable resolution, programmable threshold limits, user-defined offset register for maximum accuracy, minimum and maximum temperature monitors, wide remote temperature measurement range (up to 150°C), diode fault detection, and temperature alert function.

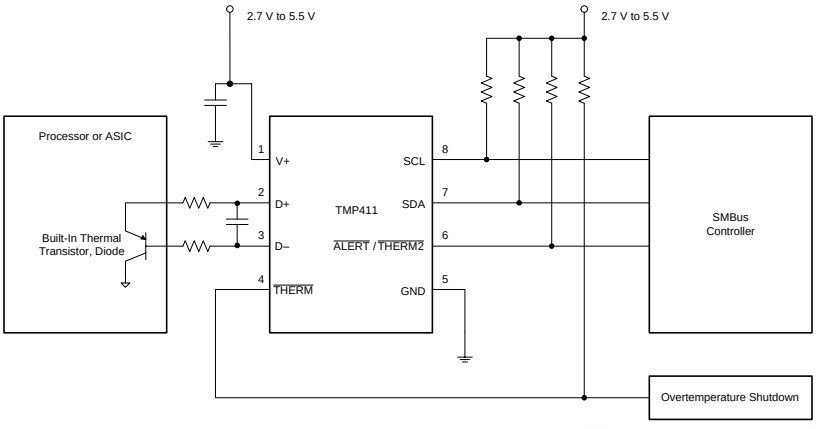
The TMP411 device is available in VSSOP-8 and SOIC-8 packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP411	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram



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4 Revision History

Changes from Revision C (May 2008) to Revision D **Page**

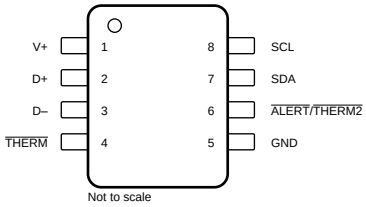
- Added "Offset Registers for System Calibration" and "Pin and Registers Compatible With ADT7461 and ADM1032" to *Features* section ... 1
- Kept VSSOP as a package option in *Device Information* table to match POA and eMSG information ... 1
- Changed "MSOP-8" to "VSSOP-8" throughout document ... 1
- Added package designators to pinout images in *Pin Configurations and Functions* section ... 3
- Added *ESD Ratings* information ... 4
- Added *Recommended Operating Conditions* information ... 4
- Added *Thermal Information* ... 4
- Added package designator information to *Thermal Information* table header ... 4
- Reformatted *Thermal Information* table note ... 4
- Changed typical local temperature sensor value from ±0.0625°C to ±0.25°C in *Electrical Characteristics* table ... 5
- Deleted "vs supply" from T_{ERROR}_PS test conditions in *Electrical Characteristics* table ... 5
- Deleted Vs = 3.3 V test condition in Temperature error power supply sensitivity vs supply (local and remote) parameter in *Electrical Characteristics* table ... 5
- Deleted *Temperature Range* subsection in *Electrical Characteristics* table ... 6
- Changed typical power-on-reset threshold value from 16 V to 1.6 V in *Electrical Characteristics* table ... 6
- Added *Functional Block Diagram* ... 11
- Added *Timing Diagrams* section ... 16
- Added *Power Supply Recommendations* information ... 34
- Added *Receiving Notification of Documentation Updates* section ... 37

5 Device Comparison Table

PART NUMBER	I^2C BINARY ADDRESS	I^2C HEX ADDRESS	OFFSET REGISTERS
TMP411A	100 1100b	4Ch	No
TMP411B	100 1101b	4Dh	No
TMP411C	100 1110b	4Eh	No
TMP411E	100 1100b	4Ch	Yes

6 Pin Configuration and Functions

DGK and D Packages
8-Pin VSSOP, SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ALERT/ THERM2	6	Digital output	Alert (reconfigurable as second thermal flag), active low, open-drain; requires pullup resistor to V+
D+	2	Analog input	Positive connection to remote temperature sensor
D–	3	Analog input	Negative connection to remote temperature sensor
GND	5	Ground	Ground
SCL	8	Digital input	Serial clock line for SMBus, open-drain; requires pull-up resistor to V+
SDA	7	Bidirectional digital input-output	Serial data line for SMBus, open-drain; requires pull-up resistor to V+
THERM	4	Digital output	Thermal flag, active low, open-drain; requires pull-up resistor to V+
V+	1	Power supply	Positive supply (2.7 V to 5.5 V)

7 Specifications

7.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Input voltage	Pins 2, 3, 4 only	–0.5	V_S + 0.5	V
Input voltage	Pins 6, 7, 8 only	–0.5	7	V
Input current			10	mA
Power supply, V_S			7	V
Operating temperature range		–55	127	°C
Junction temperature, $T_{J(max)}$			150	°C
Storage temperature, T_{stg}		–60	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Supply voltage	2.7	3.3	5.5	V
T_A	Operating free-air temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC (1)		TMP411		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.3	166.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	59.4	58.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53.0	86.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.6	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.4	85.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

at T_A = –40°C to +125°C and V_S = 2.7 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE ERROR							
$T_{ERROR(LOCAL)}$	Local temperature sensor		T_A = –40°C to 125°C	–2.5	±1.25	2.5	°C
			T_A= 15°C to 85°C V_S = 3.3 V	–1	±0.25	1	°C
$T_{ERROR(REMOTE)}$	Remote temperature sensor(1)		T_A = 15°C to 75°C T_{DIODE} = –40°C to 150°C V_S = 3.3 V	–1	±0.0625	1	°C
			T_A = –40°C to 100°C T_{DIODE} = –40°C to 150°C V_S = 3.3 V	–3	±1	3	°C
			T_A = –40°C to 125°C T_{DIODE} = –40°C to 150°C V_S = 3.3 V	–5	±3	5	°C
T_{ERROR_PS}	Temperature error power supply sensitivity (local and remote)		V_S = 2.7 V to 5.5 V T_{DIODE} = –40°C to 150°C	–0.5	±0.2	0.5	°C/V
TEMPERATURE MEASUREMENT							
	Conversion time (per channel)		One-shot mode	105	115	125	ms
	Resolution	Local temperature sensor (programmable)		9		12	Bits
		Remote temperature sensor			12		Bits
	Remote sensor source currents	High	Series resistance: 3 kΩ maximum		120		µA
		Medium high			60		µA
		Medium low			12		µA
		Low			6		µA
η	Remote transistor ideality factor		Optimized ideality factor		1.008		
SMBUS INTERFACE							
V_{IH}	Logic input high voltage (SCL, SDA)			2.1			V
V_{IL}	Logic input low voltage (SCL, SDA)					0.8	V
	Hysteresis				500		mV
	SMBus output low sink current			6			mA
	Logic input current			–1		1	µA
	SMBus input capacitance (SCL, SDA)				3		pF
	SMBus clock frequency					3.4	MHz
	SMBus timeout			25	30	35	ms
	SCL falling edge to SDA valid time					1	µs
DIGITAL OUTPUTS							
V_{OL}	Output low voltage		I_{OUT} = 6 mA		0.15	0.4	V
I_{OH}	High-level output leakage current		V_{OUT} = V_S		0.1	1	µA
	$\overline{ALERT}$ or $\overline{THERM2}$ output low sink current		$\overline{ALERT}$/$\overline{THERM2}$ forced to 0.4 V	6			mA
	$\overline{THERM}$ output low sink current		$\overline{THERM}$ forced to 0.4 V	6			mA
POWER SUPPLY							
V_S	Specified voltage range			2.7		5.5	V
I_Q	Quiescent current		0.0625 conversions per second V_S = 3.3 V		28	30	µA
			Eight conversions per second V_S = 3.3 V		400	475	µA
			Serial bus inactive, shutdown mode		3	10	µA
			Serial bus active, f_S = 40 kHz, shutdown mode		90		µA
			Serial bus active, f_S = 3.4 MHz, shutdown mode		350		µA
	Undervoltage lockout			2.3	2.4	2.6	V

(1) Tested with less than 5-Ω effective series resistance and 100-pF differential input capacitance. T_A is the ambient temperature of the TMP411. T_{DIODE} is the temperature at the remote diode sensor.

Electrical Characteristics (continued)

at T_A = –40°C to +125°C and V_S = 2.7 V to 5.5 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POR	Power-on-reset threshold			1.6	2.3	V

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
$f_{(SCL)}$	SCL operating frequency	Fast mode	0.001		0.4	MHz
		High-speed mode	0.001		3.4	
$t_{(BUF)}$	Bus free time between STOP and START condition	Fast mode	600			ns
		High-speed mode	160			
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated	Fast mode	100			ns
		High-speed mode	100			
$t_{(SUSTA)}$	Repeated START condition setup time	Fast mode	100			ns
		High-speed mode	100			
$t_{(SUSTO)}$	STOP condition setup time	Fast mode	100			ns
		High-speed mode	100			
$t_{(HDDAT)}$	Data hold time	Fast mode	0 (1)			ns
		High-speed mode	0 (2)			
$t_{(SUDAT)}$	Data setup time	Fast mode	100			ns
		High-speed mode	10			
$t_{(LOW)}$	SCL clock LOW period	Fast mode	1300			ns
		High-speed mode	160			
$t_{(HIGH)}$	SCL clock HIGH period	Fast mode	600			ns
		High-speed mode	60			
t_F	Clock and data fall time	Fast mode			300	ns
		High-speed mode			160	
t_R	Clock and data rise time	Fast mode			300	ns
		High-speed mode			160	
	SCLK ≤ 100 kHz	Fast mode			1000	
		High-speed mode				

(1) For cases with an SCL fall time of less than 20 ns, or an SDA rise or fall time of less than 20 ns, the hold time must be greater than 20 ns.
(2) For cases with an SCL fall time of less than 10 ns, or an SDA rise or fall time of less than 10 ns, the hold time must be greater than 10 ns.

8 Typical Characteristics

at T_A = 25°C and V_S = 5 V (unless otherwise noted)

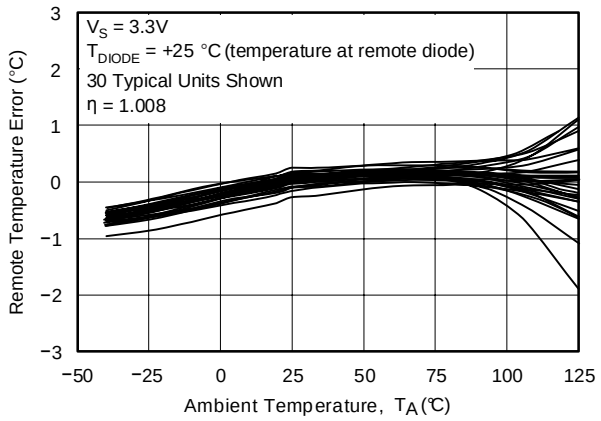


Figure 1. Remote Temperature Error vs TMP411 Ambient Temperature

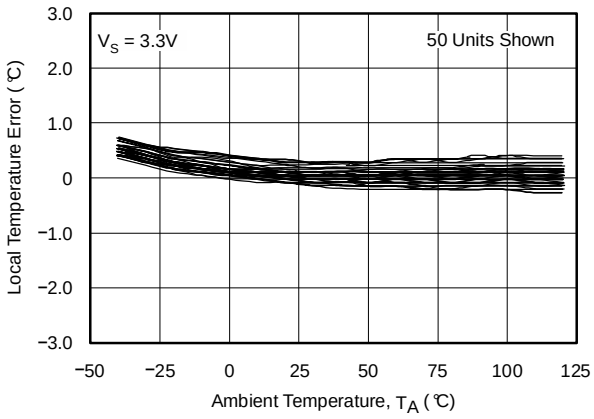


Figure 2. Local Temperature Error vs TMP411 Ambient Temperature

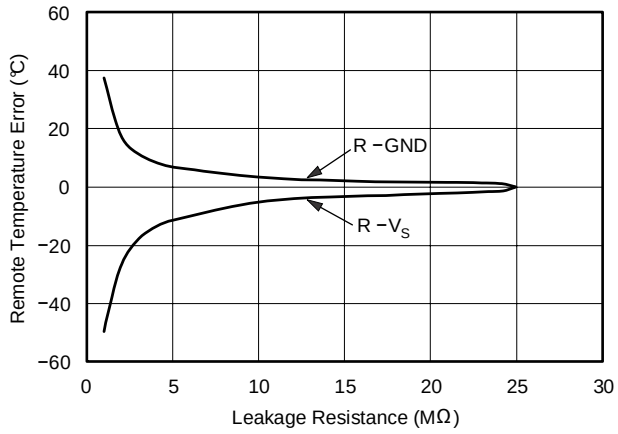


Figure 3. Remote Temperature Error vs Leakage Resistance

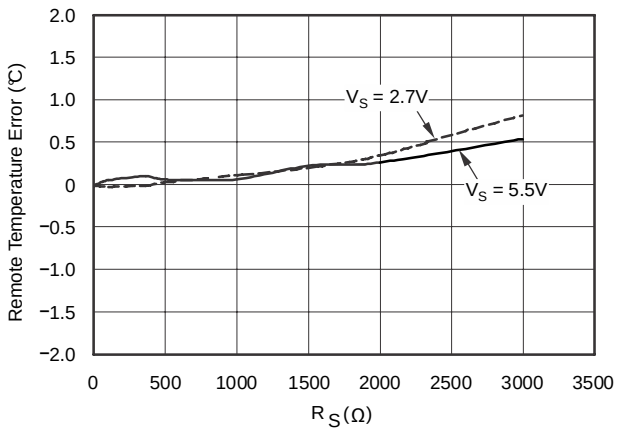


Figure 4. Remote Temperature Error vs Series Resistance (Diode-Connected Transistor, 2N3906 PNP)

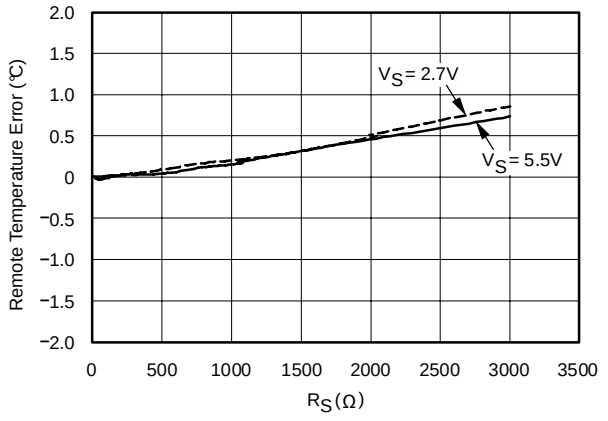


Figure 5. Remote Temperature Error vs Series Resistance (GND Collector-Connected Transistor, 2N3906 PNP)

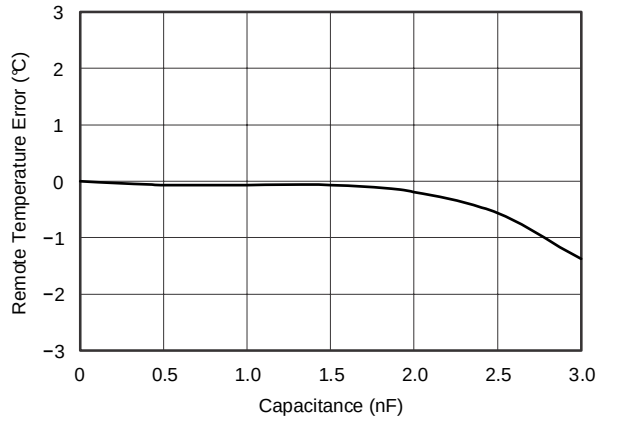


Figure 6. Remote Temperature Error vs Differential Capacitance

Typical Characteristics (continued)

at T_A = 25°C and V_S = 5 V (unless otherwise noted)

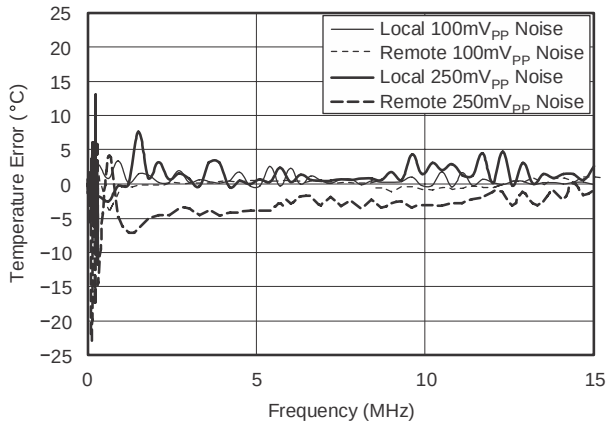


Figure 7. Temperature Error vs Power-Supply Noise Frequency

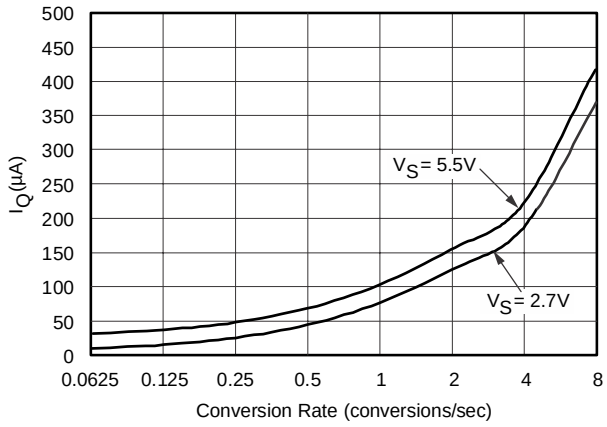


Figure 8. Quiescent Current vs Conversion Rate

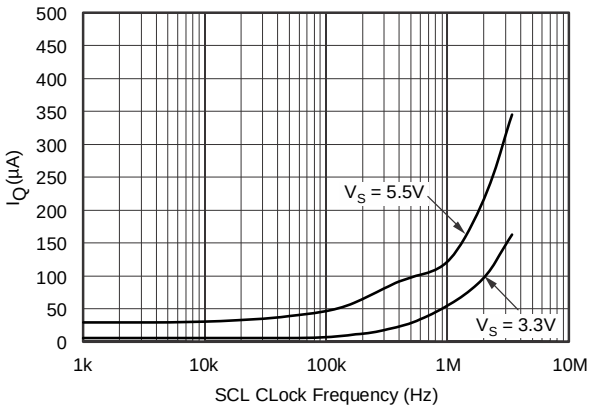


Figure 9. Shutdown Quiescent Current vs SCL Clock Frequency

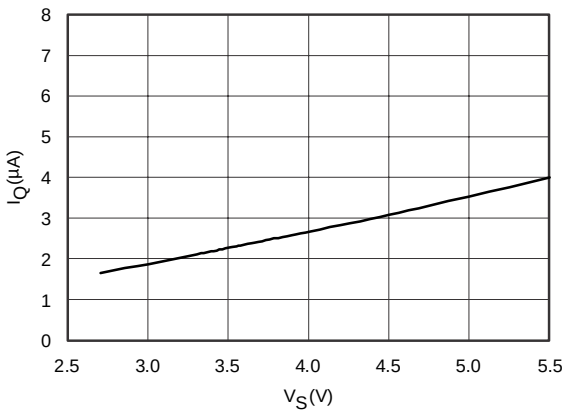


Figure 10. Shutdown Quiescent Current vs Supply Voltage

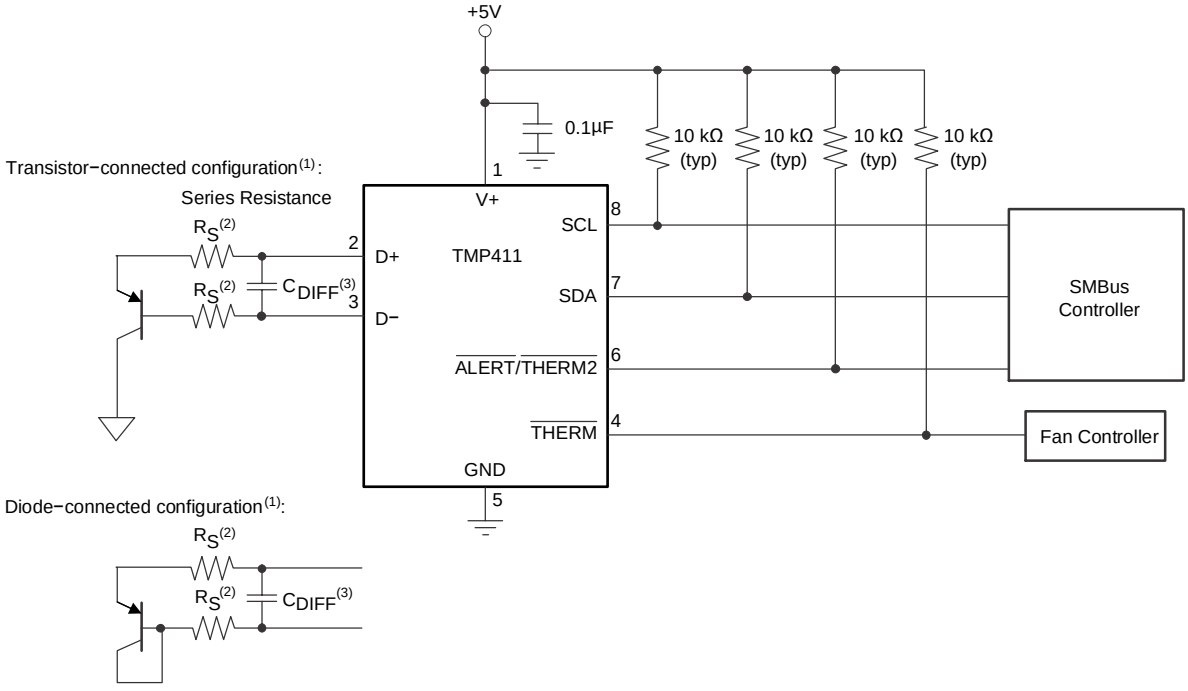
9 Detailed Description

9.1 Overview

The TMP411 is a dual-channel digital temperature sensor that combines a local die-temperature measurement channel in a single VSSOP-8 or SOIC-8 package. The TMP411 is two-wire and SMBus interface-compatible and is specified over a temperature range of –40°C to +125°C. The TMP411 device contains multiple registers for holding configuration information, temperature measurement results, temperature comparator maximum and minimum limits, and status information.

User-programmed high and low temperature limits stored in the TMP411 triggers an overtemperature or undertemperature alarm ($\overline{\text{ALERT}}$) on local and remote temperatures. Additional thermal limits can be programmed into the TMP411 and can trigger another flag ($\overline{\text{THERM}}$) that initiates a system response to rising temperatures.

The TMP411 requires only a transistor connected between D+ and D– for proper remote temperature sensing operation. The SCL and SDA interface pins require pullup resistors as part of the communication bus, while $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins are open-drain outputs that require pullup resistors. $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins can be shared with other devices for a wired-OR implementation, if desired. TI recommends using a 0.1-µF power-supply bypass capacitor for good local bypassing. Figure 11 shows a typical configuration for the TMP411 .



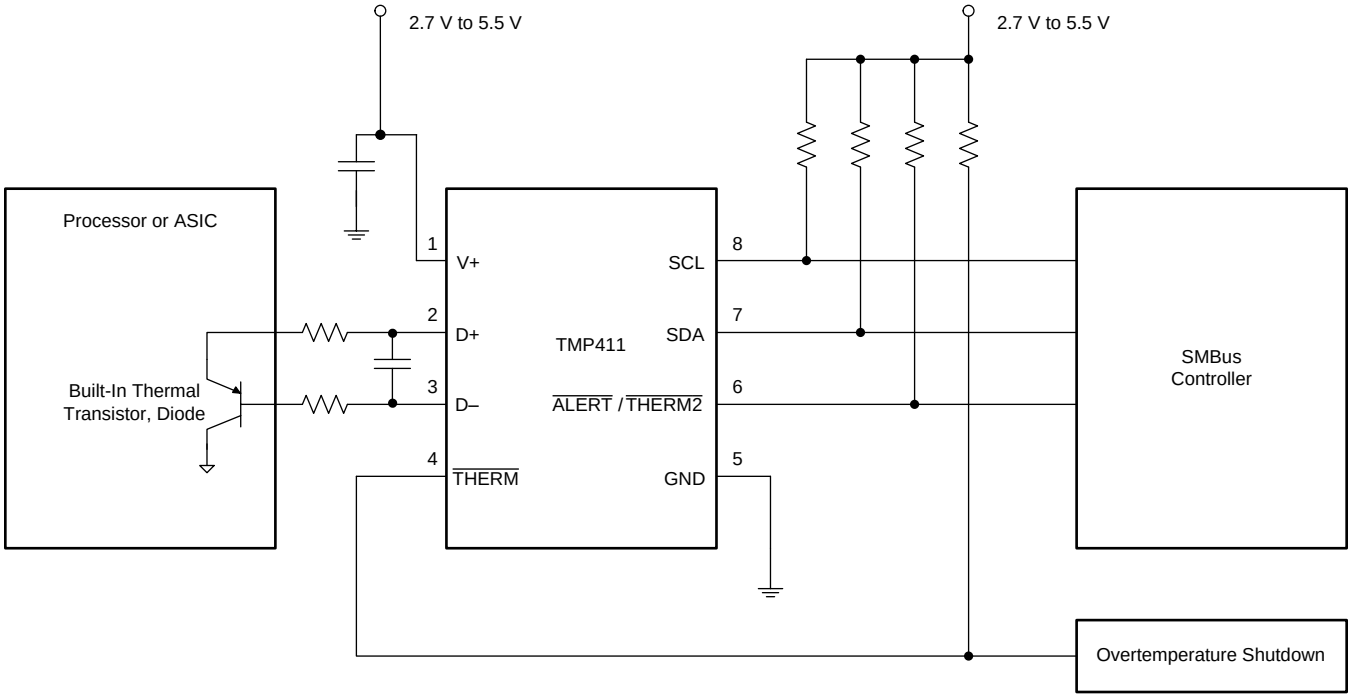
(1) Diode-connected configuration provides better settling time. Transistor-connected configuration provides better series resistance cancellation. NPN transistors must be diode-connected. PNP transistors can either be transistor or diode-connected. TI recommends this layout for the MMBT3906LP and MMBT3904LP devices.

(2) R_S (optional) must be < 1.5 kΩ in most applications. Selections of R_S depends on specific applications; see the *Filtering* section.

(3) C_{DIFF} (optional) must be < 1000 pF in most applications. Selection of C_{DIFF} depends on specific application; see the *Filtering* section and Figure 5.

Figure 11. Basic Connections

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Series Resistance Cancellation

Figure 11 shows series resistance in an application circuit that results from printed circuit board (PCB) trace resistance and remote line length. The TMP411 automatically cancels the resistance, which prevents a temperature offset.

The TMP411 device cancels up to 3 kΩ of series line resistance that eliminates the need for additional characterization and temperature offset correction.

See Figure 4 and Figure 5 for details on the effect of series resistance and power-supply voltage on sensed remote temperature error.

9.3.2 Differential Input Capacitance

The TMP411 tolerates differential input capacitance of up to 1000 pF with minimal change in temperature error. The effect of capacitance on sensed remote temperature error is shown in Figure 6.

9.3.3 Temperature Measurement Data

Temperature measurement data is taken over a default range of 0°C to 127°C for local and remote locations. Measurements from –55°C to +150°C can be made locally and remotely by reconfiguring the TMP411 device for the extended temperature range. To change the TMP411 configuration from the standard to the extended temperature range, switch bit 2 (RANGE) of the Configuration Register from low to high.

Temperature data resulting from conversions within the default measurement range are represented in binary form, as listed in the standard binary column of Table 1. Note that any temperature below 0°C results in a data value of zero (00h). Likewise, temperatures above 127°C results in a value of 127 (7Fh). The device can be set to measure over an extended temperature range by changing bit 2 of the Configuration Register from low to high. The change in measurement range and data format from standard binary to extended binary occurs at the next temperature conversion. For data captured in the extended temperature range configuration, an offset of 64 (40h) is added to the standard binary value, as listed in the extended binary column in Table 1. This configuration allows measurement of temperatures below 0°C. It is possible to have binary values in the range of –64°C to +191°C, but most temperature-sensing diodes measure in the range of –55°C to +150°C. The TMP411 device is rated only for ambient local temperatures ranging from –40°C to +125°C. Parameters in the *Absolute Maximum Ratings* table must be observed.

Feature Description (continued)

Table 1. Temperature Data Format (Local and Temperature High Bytes)

TEMP (°C)	LOCAL AND REMOTE TEMPERATURE REGISTER HIGH BYTE VALUE (1°C RESOLUTION)			
	STANDARD BINARY		EXTENDED BINARY	
	BINARY	HEX	BINARY	HEX
–64	0000 0000	00	0000 0000	00
–50	0000 0000	E	0000 1110	0E
–25	0000 0000	00	0010 0111	27
0	0000 0000	00	0100 0000	40
1	0000 0001	01	0100 0001	41
5	0000 0101	05	0100 0101	45
10	0000 1010	0A	0100 1010	4A
25	0001 1001	19	0101 1001	59
50	0011 0010	32	0111 0010	72
75	0100 1011	4B	1000 1011	8b
100	0110 0100	64	1010 0100	A4
125	0111 1101	7D	1011 1101	BD
127	0111 1101	7F	1011 1111	BF
150	0111 1111	7F	1101 0110	D6
175	0111 1111	7F	1110 1111	EF
191	0111 1111	7F	1111 1111	FF

9.3.4 $\overline{\text{THERM}}$ (Pin 4) and $\overline{\text{ALERT}}$or $\overline{\text{THERM2}}$ (Pin 6)

The $\overline{\text{THERM}}$ and $\overline{\text{ALERT}}$ or $\overline{\text{THERM2}}$ pins on the TMP411 device are dedicated to alarm functions. The pins are open-drain outputs that each require a pullup resistor to V+. These pins can be wire-ORed together with other alarm pins for system monitoring of multiple sensors. The $\overline{\text{THERM}}$ pin provides a thermal interrupt that cannot be software disabled. The $\overline{\text{ALERT}}$ pin is an earlier warning interrupt, and can be software disabled or masked. The $\overline{\text{ALERT}}$ or $\overline{\text{THERM2}}$ pin can be configured as a$\overline{\text{THERM2}}$ pin, which is a second $\overline{\text{THERM}}$ pin (Configuration Register: AL or TH bit = 1). The default setting configures pin 6 to function as an $\overline{\text{ALERT}}$ pin (AL or TH = 0).

The $\overline{\text{THERM}}$ pin asserts low when the measured local or remote temperature is outside of the temperature range programmed in the corresponding Local and Remote THERM Limit Register. The THERM temperature limit range can be programmed with a wider range than that of the limit registers, which allows the $\overline{\text{ALERT}}$pin to provide an earlier warning than the $\overline{\text{THERM}}$ pin. The $\overline{\text{THERM}}$ alarm resets automatically when the measured temperature falls within the $\overline{\text{THERM}}$ temperature limit range minus the hysteresis value stored in the $\overline{\text{THERM}}$ Hysteresis Register. The permitted hysteresis values are listed in Table 10. The default hysteresis is 10°C. When the $\overline{\text{ALERT}}$ or $\overline{\text{THERM2}}$ pin is configured as a second thermal alarm (Configuration Register: bit 7 = 0, bit 5 = 1), the pin functions the same as the $\overline{\text{THERM}}$ pin, but uses the temperatures stored in the Local and Remote Temperature High and Low Limit Registers to set the comparison range.

When $\overline{\text{ALERT}}$ or $\overline{\text{THERM2}}$ (pin 6) is configured as an $\overline{\text{ALERT}}$ pin, (Configuration Register: bit 7 = 0, bit 5 = 0), the pin asserts low when the measured local or remote temperature violates the range limit set by the corresponding Local and Remote Temperature High and Low Limit Registers. The alert function configures to assert only if the range is violated a specified number of consecutive times (either one, two, three or four times). The consecutive violation limit is set in the Consecutive Alert Register. Required consecutive faults prevent false alerts that are caused by environmental noise. The $\overline{\text{ALERT}}$ pin asserts low if the remote temperature sensor is open-circuit. When the MASK function is enabled (Configuration Register: bit 7 = 1), the $\overline{\text{ALERT}}$ pin is disabled (that is, masked). The$\overline{\text{ALERT}}$ pin resets when the master reads the device address, as long as the condition that caused the alert no longer persists, and the Status Register is reset.

9.3.5 Sensor Fault

The TMP411 senses a fault at the D+ input resulting from an incorrect diode connection or an open circuit. The detection circuitry consists of a voltage comparator that trips when the voltage at D+ exceeds (V+) − 0.6 V (typical). The comparator output is checked during a conversion. If a fault is detected, the last valid measured temperature is the temperature measurement result, the OPEN bit (Status Register, bit 2) is set high, and the ALERT pin asserts low if the alert function is enabled.

The D+ and D− inputs must be connected together to prevent meaningless fault warnings when the TMP411 remote sensor is not in use.

9.3.6 Undervoltage Lockout

The TMP411 senses when the power-supply voltage reaches a minimum voltage level for the ADC converter to function. The detection circuitry consists of a voltage comparator that enables the ADC converter after the power supply (V+) exceeds 2.45 V (typical). The comparator output is checked during a conversion. The TMP411 does not perform a temperature conversion if the power supply is not valid. The last valid measured temperature is the temperature measurement result.

9.3.7 Filtering

Remote junction temperature sensors are typically implemented in a noisy environment. Noise is often created by fast digital signals that corrupt measurements. The TMP411 has a built-in 65-kHz filter on the D+ and D− inputs to minimize the effects of noise. TI recommends placing a bypass capacitor differentially across the sensor inputs to protect the application against unwanted coupled signals. The value of the capacitor must be between 100 pF and 1 nF. Some applications have better overall accuracy with additional series resistance, however, this increased accuracy is specific to the setup. When series resistance is added, the value must not be greater than 3 kΩ.

If filtering is needed, TI recommends component values of 100-pF and 50-Ω on each input. Exact values are specific to the application.

NOTE

Whenever changing between standard and extended temperature ranges, be aware that the temperatures stored in the temperature limit registers are NOT automatically reformatted to correspond to the new temperature range format. These temperature limit values must be reprogrammed in the appropriate binary or extended binary format.

Local and remote temperature data uses two bytes for data storage. The high byte stores the temperature with a resolution of 1°C. The second or low byte stores the decimal fraction value of the temperature and allows a higher measurement resolution, as listed in Table 2. The measurement resolution for the remote channel is 0.0625°C, and is not adjustable. The measurement resolution for the local channel is adjustable, and can be set for either 0.5°C, 0.25°C, 0.125°C, or 0.0625°C by setting the RES1 and RES0 bits listed in Table 6.

Table 2. Decimal Fraction Temperature Data Format (Local and Remote Temperature Low Bytes)

TEMP (°C)	REMOTE TEMPERATURE REGISTER LOW BYTE VALUE		LOCAL TEMPERATURE REGISTER LOW BYTE VALUE							
	0.0625°C RESOLUTION		0.5°C RESOLUTION		0.25°C RESOLUTION		0.125°C RESOLUTION		0.0625°C RESOLUTION	
	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX	STANDARD AND EXTENDED BINARY	HEX
0.0000	0000 0000	00	0000 0000	00	0000 0000	00	0000 0000	00	0000 0000	00
0.0625	0001 0000	10	0000 0000	00	0000 0000	00	0000 0000	00	0001 0000	10
0.1250	0010 0000	20	0000 0000	00	0000 0000	00	0010 0000	20	0010 0000	20
0.1875	0011 0000	30	0000 0000	00	0000 0000	00	0010 0000	20	0011 0000	30
0.2500	0100 0000	40	0000 0000	00	0100 0000	40	0100 0000	40	0100 0000	40
0.3125	0101 0000	50	0000 0000	00	0100 0000	40	0100 0000	40	0101 0000	50
0.3750	0110 0000	60	0000 0000	00	0100 0000	40	0110 0000	60	0110 0000	60
0.4375	0111 0000	70	0000 0000	00	0100 0000	40	0110 0000	60	0111 0000	70
0.5000	1000 0000	80	1000 0000	80	1000 0000	80	1000 0000	80	1000 0000	80
0.5625	1001 0000	90	1000 0000	80	1000 0000	80	1000 0000	80	1001 0000	90
0.6250	1010 0000	A0	1000 0000	80	1000 0000	80	1010 0000	A0	1010 0000	A0
0.6875	1011 0000	B0	1000 0000	80	1000 0000	80	1010 0000	A0	1011 0000	B0
0.7500	1100 0000	C0	1000 0000	80	1100 0000	C0	1100 0000	C0	1100 0000	C0
0.8125	1101 0000	D0	1000 0000	80	1100 0000	C0	1100 0000	C0	1101 0000	D0
0.8750	1110 0000	E0	1000 0000	80	1100 0000	C0	1110 0000	E0	1110 0000	E0
0.9375	1111 0000	F0	1000 0000	80	1100 0000	C0	1110 0000	E0	1111 0000	F0

9.4 Device Functional Modes

9.4.1 Shutdown Mode (SD)

The TMP411 shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, which reduces current consumption to typically less than 3 μA; see Figure 10. Shutdown mode is enabled when the shutdown bit (SD) of the Configuration Register is high; the device shuts down once the current conversion is completed. When shutdown is low, the device maintains a continuous conversion state.

9.4.2 One-Shot Conversion

When the TMP411 is in shutdown mode (SD = 1 in the Configuration Register), a single conversion on both channels starts by writing any value to the One-Shot Start Register (pointer address 0Fh). This write operation starts one conversion, and the TMP411 device returns to shutdown mode when the conversion is complete. The value of the data sent in the write command is irrelevant, and is not stored by the TMP411. When the TMP411 is in shutdown mode, an initial 200 μs is required before a one-shot command is given.

NOTE

When a shutdown command is issued, the TMP411 device completes the current conversion before shutting down. The wait time only applies to the 200 μs immediately following shutdown. One-shot commands can be issued without delay thereafter.

9.5 Programming

9.5.1 Serial Interface

The TMP411 operates only as a slave device on either the two-wire bus or the SMBus. Connections to either bus are made through the SDA and SCL open-drain I/O lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers that minimize the effects of input spikes and bus noise. The TMP411 supports the transmission protocol for fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted with the MSB first.

Programming (continued)

9.5.2 Bus Overview

The TMP411 is SMBus interface-compatible. In SMBus protocol, the device that initiates the transfer is a master, and the master controls devices known as slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. START is indicated by pulling the data line (SDA) from a high to low logic level while the SCL line is high. All slaves on the bus shift are in the slave address byte, with the last bit indicating if a read or write operation is needed. During the ninth clock pulse, the slave that is addressed responds to the master by generating an acknowledge bit and pulling the SDA line low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, the SDA line must remain stable while the SCL is high. A change in the SDA while the SCL is high is interpreted as a control signal.

Once all data transfers, the master generates a STOP condition. STOP is indicated by pulling the SDA line from low to high, while the SCL line is high.

9.5.3 Timing Diagrams

The TMP411 is two-wire and SMBus-compatible. Figure 12 to Figure 16 describe the various operations on the TMP411. Parameters for Figure 12 are defined in the *Timing Requirements* section. Bus definitions are given below:

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line, from high to low (while the SCL line is high) defines a START condition. A START condition initiates each data transfer.

Stop Data Transfer: A change in the state of the SDA line from low to high (while the SCL line is high) defines a STOP condition. A STOP or repeated START condition terminates each data transfer.

Data Transfer: The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the master device. The receiver acknowledges the data transfer.

Acknowledge: Each receiving device (when addressed) is required to generate an acknowledge bit. A device that acknowledges must pull the SDA line down during the acknowledge clock pulse so the SDA line is stable and low during the high period of the acknowledge clock pulse. Setup and hold times must be taken into account. On a master receive, the master signals data transfer termination by generating a not-acknowledge bit transmitted by the slave.

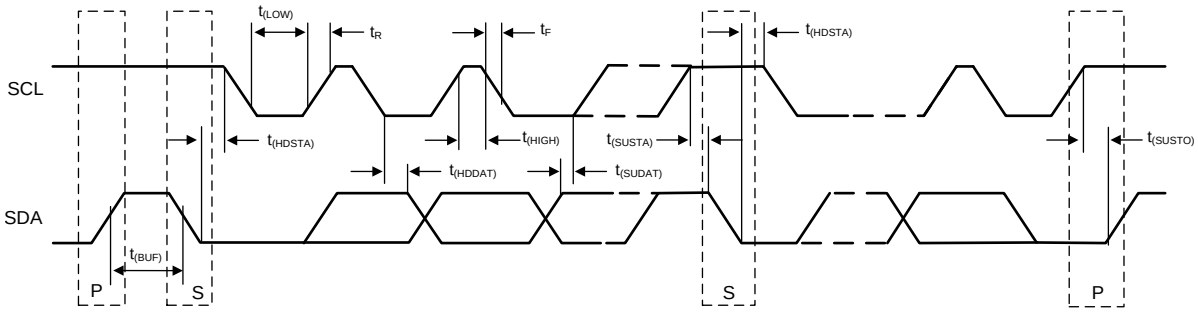
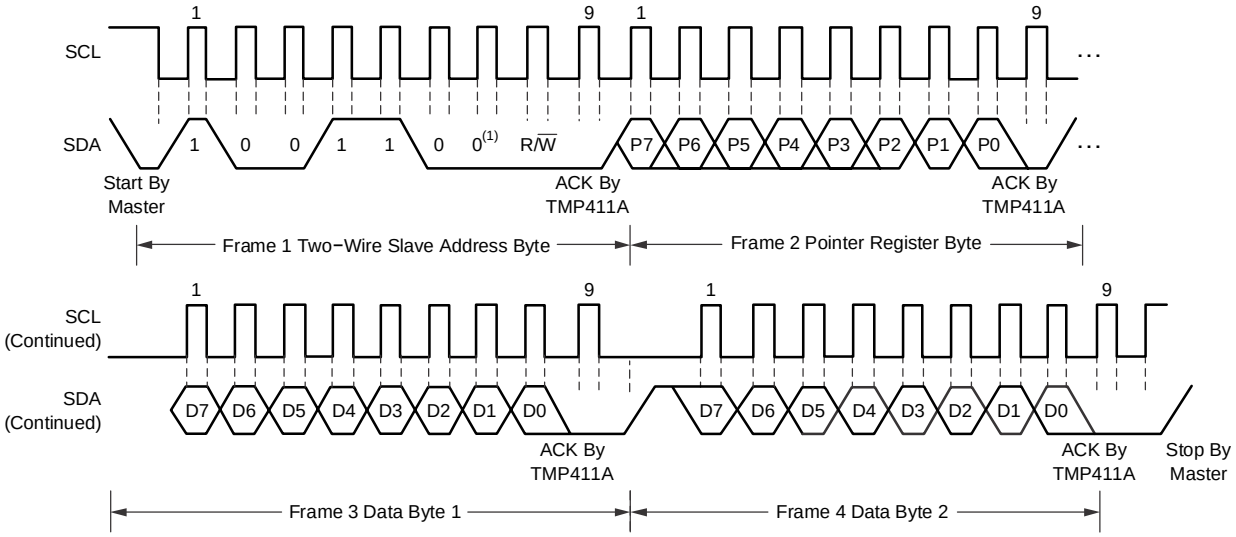


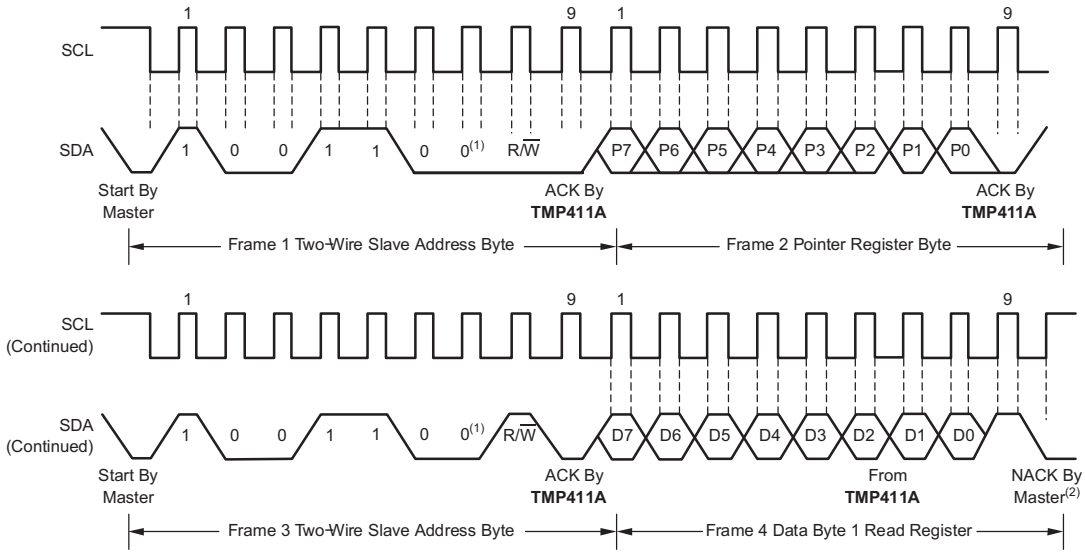
Figure 12. Two-Wire Timing Diagram

Programming (continued)



(1) Slave address 1001100 (TMP411A) shown. Slave address changes for TMP411B and TMP411C. See *Ordering Information* table for more details.

Figure 13. Two-Wire Timing Diagram for Write Word Format

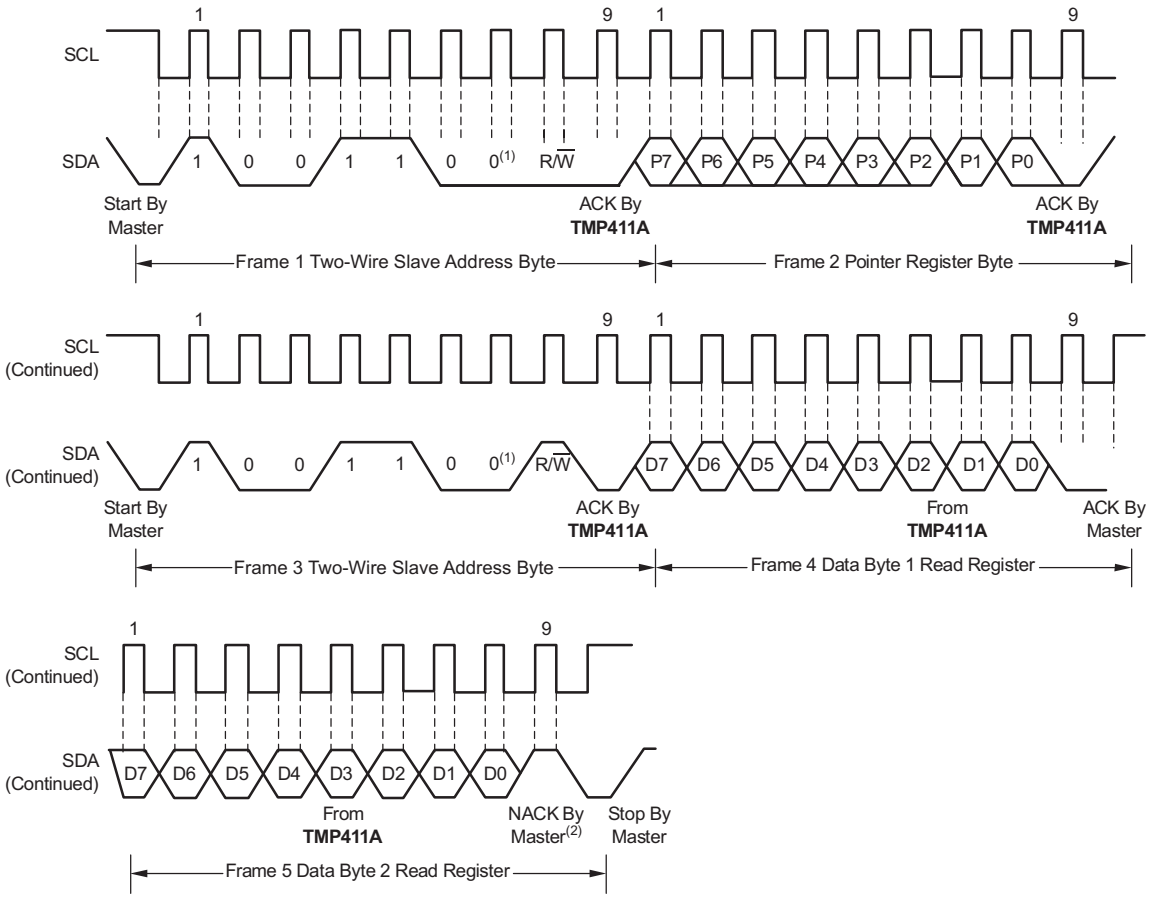


(1) Slave address 1001100 (TMP411A) shown. Slave address changes for TMP411B and TMP411C. See *Ordering Information* table for more details.

(2) Master must leave the SDA high to terminate a single−byte read operation.

Figure 14. Two-Wire Timing Diagram for Single-Byte Read Format

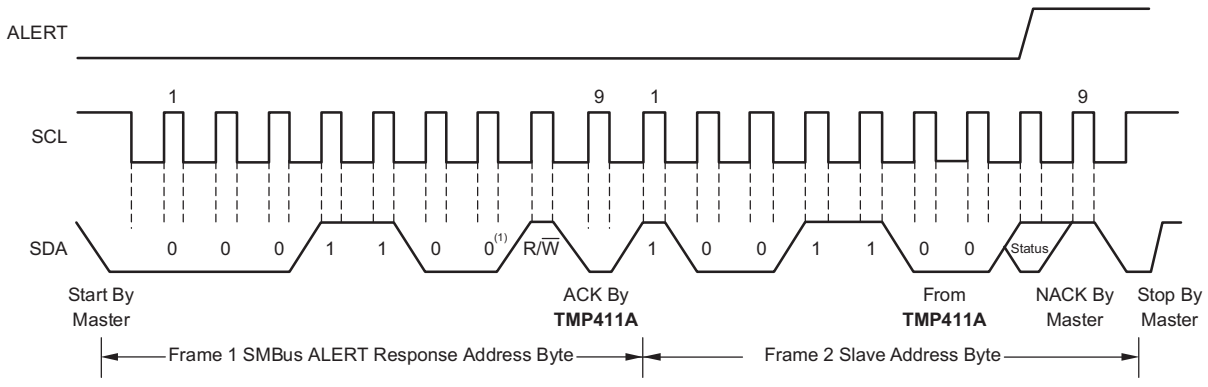
Programming (continued)



(1) Slave address 1001100 (TMP411A) is shown. Slave address changes for TMP411B and TMP411C. See Ordering Information table for more details.

(2) Master must leave SDA high to terminate a two−byte read operation.

Figure 15. Two-Wire Timing Diagram for Two-Byte Read Format



NOTE (1): Slave address 1001100 (TMP411A) shown. Slave address changesfor TMP411B and TMP411C. See *Ordering Information* table for more details.

(1) Slave address 1001100 (TMP411A) is shown. Slave address changes for TMP411B and TMP411C. See *Ordering Information* table for more details.

Figure 16. Timing Diagram for SMBus Alert

Programming (continued)

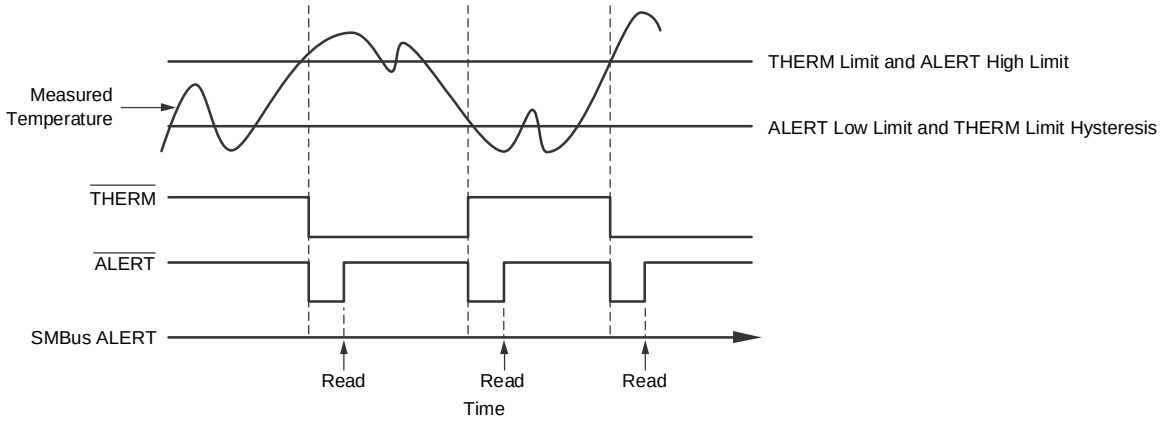


Figure 17. SMBus Alert Timing Diagram

Programming (continued)

9.5.4 Serial Bus Address

To communicate with the TMP411, the master must first address slave devices through a slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates whether the operation is read or write. The address of the TMP411A is 4Ch (1001100b). The address of the TMP411B is 4Dh (1001101b). The address of the TMP411E is 4Ch (1001100b).

9.5.5 Read and Write Operations

To access a particular register on the TMP411, the appropriate value must be written to the Pointer Register. With the read and write bit low, the value for the Pointer Register is the first byte transferred after the slave address byte. Every write operation to the TMP411 requires a value for the Pointer Register, as shown in Figure 13.

When reading from the TMP411, the last value stored in the Pointer Register by a write operation determines which register is read by a read operation. A new value must be written to the Pointer Register to change the register pointer for a read operation. This transaction is accomplished by issuing a slave address byte with the read and write bit low, followed by the Pointer Register byte. No additional data is required. The master then generates a START condition and sends the slave address byte with the read and write bit high to initiate the read command. See Figure 14 for details of this sequence. If repeated reads from the same register are desired, it is not necessary to continually send the Pointer Register bytes, because the TMP411 device retains the Pointer Register value until the next write operation changes the value. Note that the MSB sends the register bytes first, followed by the LSB.

9.5.6 Timeout Function

When bit 7 of the Consecutive Alert Register is set high, the TMP411 timeout function is enabled. The TMP411 device resets the serial interface if the SCL or SDA lines are held low for 30 ms (typical) between a START and STOP condition. If the TMP411 device is holding the bus low, the device releases the bus and waits for a START condition. To avoid activating the timeout function, it is necessary to maintain a communication speed of at least 1 kHz for the SCL operating frequency. The default state of the timeout function is enabled (bit 7 = high).

9.5.7 High-Speed Mode

For the two-wire bus to operate at frequencies above 400 kHz, the master device must issue a high-speed mode (Hs-mode) master code (00001XXX) as the first byte after a START condition to switch the bus to high-speed operation. The TMP411 device does not acknowledge this byte, but switches the input filters on the SDA and SCL lines, switches the output filter on SDA to operate in Hs-mode, which allows transfers at up to 3.4 MHz. After the Hs-mode master code is issued, the master transmits a two-wire slave address to initiate a data transfer operation. The bus operates in high-speed mode until a STOP condition occurs on the bus. The TMP411 switches the input and output filter after receiving the STOP condition.

9.5.8 General Call Reset

The TMP411 device supports reset through the two-wire general call address 00h (0000 0000b). The TMP411 device reads the general call address and responds to the second byte. If the second byte is 06h (0000 0110b), the TMP411 executes a software reset. The software reset restores the power-on-reset state to all TMP411 registers, aborts any conversion in progress, and clears the $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins. The TMP411 does not respond to other values in the second byte.

9.5.9 Software Reset

The TMP411 resets by writing any value to Pointer Register FCh. This restores the power-on-reset state to all of the TMP411 registers, aborts any conversion in process, and clears the $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins.

Programming (continued)

9.5.10 SMBus Alert Function

The TMP411 device supports the SMBus alert function. When pin 6 is configured as an alert output, the $\overline{\text{ALERT}}$ pin of the TMP411 can connect as an SMBus alert signal. When a master detects an alert condition on the ALERT line, the master sends an SMBus alert command (00011001) on the bus. If the $\overline{\text{ALERT}}$ pin of the TMP411 is active, the device acknowledges the SMBus alert command and returns the slave address on the SDA line. The eighth bit of the slave address byte indicates if the high limit or low limit temperature settings caused the alert condition. The bit is high if the temperature is greater than or equal to one of the temperature high limit settings; the bit is low if the temperature is less than one of the temperature low limit settings. See Figure 16 for details of this sequence.

If multiple devices on the bus respond to the SMBus alert command, arbitration during the slave address portion of the SMBus alert command determines which device clears the alert status. If the TMP411 wins the arbitration, the $\overline{\text{ALERT}}$ pin inactivates when the SMBus alert command is complete. If the TMP411 device loses the arbitration, the $\overline{\text{ALERT}}$ pin remains active.

9.6 Register Map

Table 3. Register Map Summary

POINTER ADDRESS (HEX)		POWER-ON-RESET (HEX)	BIT DESCRIPTION								REGISTER DESCRIPTIONS
READ	WRITE		D7	D6	D5	D4	D3	D2	D1	D0	
00	NA (1)	00	LT11	LT10	LT9	LT8	LT7	LT6	LT5	LT4	Local Temperature (High Byte)
01	NA	00	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	Remote Temperature (High Byte)
02	NA	XX	BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	RTHRM	LTHRM	Status Register
03	09	00	MASK1	SD	AL/TH	0	0	RANGE	0	0	Configuration Register
04	0A	08	0	0	0	0	R3	R2	R1	R0	Conversion Rate Register
05	0B	55	LTH11	LTH10	LTH9	LTH8	LTH7	LTH6	LTH5	LTH4	Local Temperature High Limit (High Byte)
06	0C	00	LTL11	LTL10	LTL9	LTL8	LTL7	LTL6	LTL5	LTL4	Local Temperature Low Limit (High Byte)
07	0D	55	RTH11	RTH10	RTH9	RTH8	RTH7	RTH6	RTH5	RTH4	Remote Temperature High Limit (High Byte)
08	0E	00	RTL11	RTL10	RTL9	RTL8	RTL7	RTL6	RTL5	RTL4	Remote Temperature :Low Limit (High Byte)
NA	0F	XX	X (2)	X	X	X	X	X	X	X	One-Shot Start
10	NA	00	RT3	RT2	RT1	RT0	0	0	0	0	Remote Temperature (Low Byte)
11	11	00	RTOS11	RTOS10	RTOS9	RTOS8	RTOS7	RTOS6	RTOS5	RTOS4	Remote Temperature Offset Register (High Byte) (3)
12	12	00	RTOS3	RTOS2	RTOS1	RTOS0	0	0	0	0	Remote Temperature Offset Register (Low Byte)(3)
13	13	00	RTH3	RTH2	RTH1	RTH0	0	0	0	0	Remote Temperature High Limit (Low Byte)
14	14	00	RTL3	RTL2	RTL1	RTL0	0	0	0	0	Remote Temperature Low Limit (Low Byte)
15	NA	00	LT3	LT2	LT1	LT0	0	0	0	0	Local Temperature (Low Byte)
16	16	00	LTH3	LTH2	LTH1	LTH0	0	0	0	0	Local Temperature HIgh Limit (Low Byte)
17	17	00	LTL3	LTL2	LTL1	LTL0	0	0	0	0	Local Temperature Low Limit (Low Byte)
18	18	00	NC7	NC6	NC5	NC4	NC3	NC2	NC1	NC0	N-factor correction
19	19	55	RTHL11	RTHL10	RTHL9	RTHL8	RTHL7	RTHL6	RTHL5	RTHL4	Remote $\overline{\text{THERM}}$ Limit
1A	1A	1C	0	0	0	1	1	1	RES1	RES0	Resolution Register
20	20	55	LTHL11	LTHL10	LTHL9	LTHL8	LTHL7	LTHL6	LTHL5	LTHL4	Local $\overline{\text{THERM}}$ Limit
21	21	0A	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4	$\overline{\text{THERM}}$ Hysteresis
22	22	81	TO_EN	0	0	0	C2	C1	C0	0	Consecutive Alert Register
30	30	FF	LMT11	LMT10	LMT9	LMT8	LMT7	LMT6	LMT5	LMT4	Local Temperature Minimum (High Byte)

(1) NA = not applicable; register is write- or read-only.
(2) X = indeterminable state.
(3) Offset registers 11 and 12 are only available for the TMP411E device.

Register Map (continued)

Table 3. Register Map Summary (continued)

POINTER ADDRESS (HEX)		POWER-ON-RESET (HEX)	BIT DESCRIPTION								REGISTER DESCRIPTIONS
READ	WRITE		D7	D6	D5	D4	D3	D2	D1	D0	
31	31	F0	LMT3	LMT2	LMT1	LMT0	0	0	0	0	Local Temperature Minimum (Low Byte)
32	32	00	LXT11	LXT10	LXT9	LXT8	LXT7	LXT6	LXT5	LXT4	Local Temperature Maximum (High Byte)
33	33	00	LXT3	LXT2	LXT1	LXT0	0	0	0	0	Local Temperature Maximum (Low Byte)
34	34	FF	RMT11	RMT10	RMT9	RMT8	RMT7	RMT6	RMT5	RMT4	Remote Temperature Minimum (High Byte)
35	35	F0	RTM3	RTM2	RTM1	RTM0	0	0	0	0	Remote Temperature Minimum (Low Byte)
36	36	00	RXT11	RXT10	RXT9	RXT8	RXT7	RXT6	RXT5	RXT4	Remote Temperature Maximum (High Byte)
37	37	00	RXT3	RXT2	RXT1	RXT0	0	0	0	0	Remote Temperature Maximum (Low Byte)
NA	FC	XX	X [(2)]	X	X	X	X	X	X	X	Software Reset
FE	NA	55	0	1	0	1	0	1	0	1	Manufacturer ID
FF	NA	12	0	0	0	1	0	0	1	0	Device ID for TMP411A
FF	NA	13	0	0	0	1	0	0	1	1	Device ID for TMP411B
FF	NA	10	0	0	0	1	0	0	0	0	Device ID for TMP411C
FF	NA	12	0	0	0	1	0	0	1	0	Device ID for TMP411E

9.6.1 Register Information

The TMP411 contains multiple registers for holding configuration information, temperature measurement results, maximum and minimum temperature comparator limits, and status information. These registers are described in Figure 18 and Table 3.

9.6.2 Pointer Register

Figure 18 shows the internal register structure of the TMP411 . The 8-bit pointer register addresses a given data register. The Pointer Register identifies which of the data registers must respond to a read or write command on the two-wire bus. This register is set with every write command. A write command must be issued to set the proper value in the pointer register before executing a read command. Table 3 lists the pointer address of the registers available in the TMP411 . Offset registers 11 and 12 are only available for the TMP411E device . The power-on-reset (POR) value of the Pointer Register is 00h (0000 0000b).

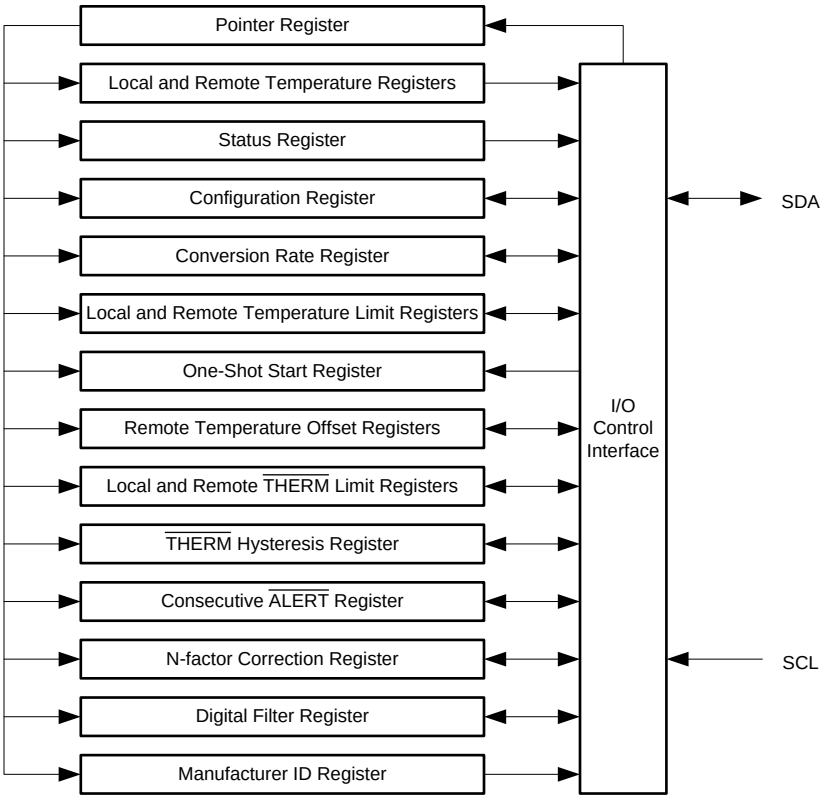


Figure 18. Internal Register Structure

9.6.3 Temperature Registers

The TMP411 has four 8-bit registers that hold temperature measurement results. The local and remote channels have a high byte register that contains the most significant bits (MSBs) of the temperature analog-to-digital converter (ADC) result and a low byte register that contains the least significant bits (LSBs) of the temperature ADC result. The local channel high byte address is 00h; the local channel low byte address is 15h. The remote channel high byte is at address 01h; the remote channel low byte address is 10h. These registers are read-only and are updated by the ADC each time a temperature measurement is completed.

The TMP411 contains circuitry to assure that a low byte register read command returns data from the same ADC conversion as the immediately preceding high byte read command. This assurance remains valid only until another register is read. For proper operation, the high byte of a temperature register must be read first. The low byte register must be read in the next read command. The low byte register may be left unread if the LSBs are not needed. The temperature registers may be read as a 16-bit register using a single two-byte read command from address 00h for the local channel result, or from address 01h for the remote channel result. The high byte is read output first, followed by the low byte. Both bytes of this read operation are from the same ADC conversion. The power-on-reset value of both temperature registers is 00h.

9.6.4 Limit Registers

The TMP411 has 11 registers for setting comparator limits for the local and remote measurement channels. These registers have read and write capability. The High and Low Limit Registers for both channels span two registers, as do the temperature registers. The local temperature high limit is set by writing the high byte to pointer address 0Bh, writing the low byte to pointer address 16h, or by using a single two-byte write command (high byte first) to pointer address 0Bh. The local temperature high limit is read by the high byte from pointer address 05h, the low byte from pointer address 16h, or by using a two-byte read command from pointer address 05h. The power-on-reset value of the local temperature high limit is 55h or 00h. The power-on-reset value of the local temperature high limit is 55h or 00h (85°C in standard temperature mode and 21°C in extended temperature mode).

Similarly, the local temperature low limit is set by writing the high byte to pointer address 0Ch, writing the low byte to pointer address 17h, or by using a single two-byte write command to pointer address 0Ch. The local temperature low limit is read by the high byte from pointer address 06h, the low byte from pointer address 17h, or by using a two-byte read from pointer address 06h. The power-on-reset value of the local temperature low limit register is 00h (0°C in standard temperature mode, and −64°C in extended mode).

The remote temperature high limit is set by writing the high byte to pointer address 0Dh, writing the low byte to pointer address 13h, or by using a two-byte write command to pointer address 0Dh. The remote temperature high limit is read by the high byte from pointer address 07h, the low byte from pointer address 13h, or by using a two-byte read command from pointer address 07h. The power-on-reset value of the Remote Temperature High Limit Register is 55h or 00h (85°C in standard temperature mode, and 21°C in extended temperature mode).

The remote temperature low limit is set by writing the high byte to pointer address 0Eh,writing the low byte to pointer address 14h, or by using a two-byte write to pointer address 0Eh. The remote temperature low limit is read by the high byte from pointer address 08h, the low byte from pointer address 14h, or by using a two-byte read from pointer address 08h. The power-on-reset value of the Remote Temperature Low Limit Register is 00h (0°C in standard temperature mode, and −64°C in extended mode).

The TMP411 has a $\overline{\text{THERM}}$ limit register for the local and remote channels. These registers are eight bits and allow for $\overline{\text{THERM}}$ limits to be set to 1°C resolution. The local channel $\overline{\text{THERM}}$ limit is set by writing to pointer address 20h. The remote channel $\overline{\text{THERM}}$ limit is set by writing to pointer address 19h. The local channel $\overline{\text{THERM}}$ limit is read from pointer address 20h, and the remote channel $\overline{\text{THERM}}$ limit is read from pointer address 19h. The power-on-reset value of the $\overline{\text{THERM}}$ limit registers is 55h (85°C in standard temperature mode or 21°C in extended temperature mode). The $\overline{\text{THERM}}$ limit comparators have hysteresis. The hysteresis of the comparators is set by writing to pointer address 21h. The hysteresis value is obtained by reading from pointer address 21h. The Hysteresis Register value is an unsigned number that is always positive. The power-on-reset value of this register is 0Ah (10°C).

When changing between standard and extended temperature ranges, note that the temperatures stored in the temperature limit registers do not automatically reformat to correspond to the new temperature range format. These values must be reprogrammed in the appropriate binary or extended binary format.

9.6.5 Status Register

The TMP411 has a Status Register that reports the state of the temperature comparators. Table 4 lists the Status Register bits. The Status Register is read-only from pointer address 02h.

The BUSY bit reads as 1 if the ADC is making a conversion, and 0 if the ADC is not converting.

The OPEN bit reads as 1 if the remote transistor is detected as OPEN since the last read of the Status Register. The OPEN status is only detected when the ADC is attempting to convert a remote temperature.

The RTHRM bit reads as 1 if the remote temperature exceeds the remote $\overline{\text{THERM}}$ limit, remains greater than the remote $\overline{\text{THERM}}$ limit, and less than the value in the shared Hysteresis Register, as shown in Figure 17.

The LTHRM bit reads as 1 if the local temperature exceeds the local $\overline{\text{THERM}}$ limit, remains greater than the local $\overline{\text{THERM}}$ limit, and less than the value in the shared Hysteresis Register, as shown in Figure 17.

The LHIGH and RHIGH bit values depend on the state of the AL or TH bit in the Configuration Register. If the AL or TH bit is 0, the LHIGH bit reads as 1 if the local high limit was exceeded since the last clearing of the Status Register. The RHIGH bit reads as 1 if the remote high limit was exceeded since the last clearing of the Status Register. If the AL or TH bit is 1, the remote high limit and the local high limit implement a THERM2 function. LHIGH reads as 1 if the local temperature has exceeded the local high limit and remains greater than the local high limit, and less than the value in the Hysteresis Register.

The RHIGH bit reads as 1 if the remote temperature exceeds the remote high limit and remains greater than the remote high limit, and less than the value in the Hysteresis Register.

The LLOW and RLOW bits are not effected by the AL or TH bit. The LLOW bit reads as 1 if the local low limit was exceeded since the last clearing of the Status Register. The RLOW bit reads as 1 if the remote low limit was exceeded since the last clearing of the Status Register.

The values of the LLOW, RLOW, and OPEN (as well as LHIGH and RHIGH when AL or TH is 0) are latched and are read as 1 until the Status Register is read or a device reset occurs. These bits are cleared by reading the Status Register, provided that the condition causing the flag to be set no longer exists. The values of BUSY, LTHRM, and RTHRM (as well as LHIGH and RHIGH when ALERT or THERM2 is 1) are not latched and are not cleared by reading the Status Register. The values indicate the current state, and are updated appropriately at the end of the corresponding ADC conversion. Clearing the Status Register bits does not clear the state of the ALERT pin. An SMBus alert response address command must clear the ALERT pin.

The TMP411 NORs LHIGH, LLOW, RHIGH, RLOW, and OPEN, so a status change for any of these flags from 0 to 1 automatically causes the ALERT pin to go low. (This only applies when the ALERT or THERM2 pin is configured for ALERT mode).

Table 4. Status Register Format

STATUS REGISTER (READ = 02h, WRITE = NA)								
Bit Number	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	BUSY	LHIGH	LLOW	RHIGH	RLOW	OPEN	RTHRM	LTHRM
POR Value	0 (1)	0	0	0	0	0	0	0

(1) The BUSY bit changes to 1 almost immediately (<< 100 µs) following power-up, as the TMP411 device begins the first temperature conversion. The BUSY bit is high whenever the TMP411 device is converting a temperature reading.

9.6.6 Configuration Register

The Configuration Register sets the temperature range, controls shutdown mode, and determines how the ALERT and THERM2 pins function. The Configuration Register is set by writing to pointer address 09h and by reading from pointer address 03h.

The MASK bit (bit 7) enables or disables the ALERT pin output if AL or TH = 0. If AL or TH = 1, then the MASK bit has no effect. If MASK is set to 0, the ALERT pin goes low when one of the temperature measurement channels exceeds the high or low limits for the selected number of consecutive conversions. If the MASK bit is set to 1, the TMP411 retains the ALERT pin status, but the ALERT pin does not go low.

The shutdown (SD) bit (bit 6) enables or disables the temperature measurement circuitry. If SD = 0, the TMP411 converts continuously at the rate set in the conversion rate register. When SD is set to 1, the TMP411 immediately stops converting and enters shutdown mode. When SD is set to 0 again, the TMP411 resumes continuous conversions. A single conversion starts by writing to the One-Shot Register when SD = 1.

The AL or TH bit (bit 5) controls if the ALERT pin functions in ALERT mode or THERM2 mode. If AL or TH = 0, the ALERT pin operates as an interrupt pin. In this mode, the ALERT pin goes low after the set number of consecutive out-of-limit temperature measurements occur.

If AL or TH = 1, the ALERT /THERM2 pin implements a THERM function (THERM2). In this mode, THERM2 functions similarly to the THERM pin, except that the local high limit and remote high limit registers are used for the thresholds. THERM2 goes low when RHIGH or LHIGH is set.

The temperature range is set by configuring bit 2 of the Configuration Register. Setting this bit low configures the TMP411 device for the standard measurement range (0°C to 127°C). Temperature conversions are stored in the standard binary format. Setting bit 2 high configures the TMP411 for the extended measurement range (−55°C to +150°C). Temperature conversions are stored in the extended binary format, as listed in Table 1.

The remaining bits of the Configuration Register are reserved and must be set to 0. The power-on-reset value for this register is 00h. Table 5 lists the Configuration Register bits.

Table 5. Configuration Register Bit Descriptions

CONFIGURATION REGISTER (READ = 03h, WRITE = 09h, POR = 00h)			
BIT	**NAME**	**FUNCTION**	**POWER-ON-RESET VALUE**
7	MASK	0 = $\overline{\text{ALERT}}$ enabled 1 = $\overline{\text{ALERT}}$ masked	0
6	SD	0 = Run 1 = Shutdown	0
5	AL or TH	0 = $\overline{\text{ALERT}}$ mode 1 = $\overline{\text{THERM}}$ mode	0
4, 3	Reserved	—	0
2	Temperature range	0 = 0°C to 127°C 1 = –55°C to 150°C	0
1, 0	Reserved	—	0

9.6.7 Resolution Register

The RES1 and RES0 bits (resolution bits 1 and 0) of the Resolution Register set the resolution of the local temperature measurement channel. Remote temperature measurement channel resolution is not effected. Changing the local channel resolution affects the conversion time and rate of the TMP411. The Resolution Register is set by writing to pointer address 1Ah, and is read from pointer address 1Ah. Table 6 lists the resolution bits for the Resolution Register.

Table 6. Resolution Register: Local Channel Programmable Resolution

RESOLUTION REGISTER (READ = 1Ah, WRITE = 1Ah, POR = 1Ch)			
RES1	**RES0**	**RESOLUTION**	**CONVERSION TIME (TYPICAL)**
0	0	9 Bits (0.5°C)	12.5 ms
0	1	10 Bits (0.25°C)	25 ms
1	0	11 Bits (0.125°C)	50 ms
1	1	12 Bits (0.0625°C)	100 ms

Bits 2 through 4 of the resolution register must be set to 1. Bits 5 through 7 of the resolution register must be set to 0. The power-on-reset value of this register is 1Ch.

9.6.8 Conversion Rate Register

The Conversion Rate Register controls the rate at which temperature conversions are performed. The register adjusts the idle time between conversions but not the conversion timing itself, which allows the TMP411 power dissipation to balance with the temperature register update rate. Table 7 lists the conversion rate options and corresponding current consumption.

Table 7. Conversion Rate Register

CONVERSION RATE REGISTER (READ = 04h, WRITE = 0Ah, POR = 08h										
R7	R6	R5	R4	R3	R2	R1	R0	CONVERSIONS PER SECOND	AVERAGE IQ (TYPICAL) (μA)	
									V_S = 2.7 V	V_S = 5.5 V
0	0	0	0	0	0	0	0	0.0625	11	32
0	0	0	0	0	0	0	1	0.125	17	38
0	0	0	0	0	0	1	0	0.25	28	49
0	0	0	0	0	0	1	1	0.5	47	69
0	0	0	0	0	1	0	0	1	80	103
0	0	0	0	0	1	0	1	2	128	155
0	0	0	0	0	1	1	0	4	190	220
07h to 0Fh								8	373	413

9.6.9 *N*-Factor Correction Register

The TMP411 allows for a different *n*-factor value to convert remote channel measurements to temperature. The remote channel uses sequential current excitation to extract a differential V_{BE} voltage measurement to determine the temperature of the remote transistor. Equation 1 relates the voltage and temperature.

$$V_{BE2} - V_{BE1} = \frac{nkT}{q} \ln\left(\frac{I_2}{I_1}\right) \quad (1)$$

The value *n* in is a characteristic of the particular transistor used for the remote channel. The default value for the TMP411 is *n* = 1.008. The value in the Table 8 adjusts the effective *n*-factor according to Equation 2 and Equation 3:

$$n_{eff} = \frac{1.008 \times 300}{(300 - N_{ADJUST})} \quad (2)$$

$$N_{ADJUST} = 300 - \left(\frac{300 \times 1.008}{n_{eff}}\right) \quad (3)$$

The *n*-correction value must be stored in two's-complement format, yielding an effective data range from −128 to 127, as listed in Table 8. The *n*-correction value is written to and read from pointer address 18h. The register power-on-reset value is 00h, which is not effected unless the value is written to.

Table 8. *N*-Factor Range

N_{ADJUST}			N
BINARY	HEX	DECIMAL	
01111111	7F	127	1.747977
00001010	0A	10	1.042759
00001000	08	8	1.035616
00000110	06	6	1.028571
00000100	04	4	1.021622
00000010	02	2	1.014765
00000001	01	1	1.011371
00000000	00	0	1.008
11111111	FF	–1	1.004651
11111110	FE	–2	1.001325
11111100	FC	–4	0.994737
11111010	FA	–6	0.988235
11111000	F8	–8	0.981818
11110110	F6	–10	0.975484
10000000	80	–128	0.706542

9.6.10 Minimum and Maximum Registers

The TMP411 stores the measured minimum and maximum temperatures since power-on, chip-reset, or minimum and maximum register reset for the local and remote channels. The Local Temperature Minimum Register is read with the high byte from pointer address 30h, and the low byte is read from pointer address 31h. The Local Temperature Minimum Register is read with a two-byte read command from pointer address 30h. The Local Temperature Minimum Register resets at power-on by executing the chip-reset command, or by writing any value to any of the pointer addresses 30h through 37h. The reset value for these registers is FFh and F0h.

The Local Temperature Maximum Register is read with the high byte from pointer address 32h, and the low byte is read from pointer address 33h. The Local Temperature Maximum Register is read with a two-byte read command from pointer address 32h. The Local Temperature Maximum Register resets at power-on by executing the chip reset command, or by writing any value to any of the pointer addresses 30h through 37h. The reset value for these registers is 00h and 00h.

The Remote Temperature Minimum Register is read with the high byte from pointer address 34h, and the low byte is read from pointer address 35h. The Remote Temperature Minimum Register is read with a two-byte read command from pointer address 34h. The Remote Temperature Minimum Register resets at power-on by executing the chip reset command, or by writing any value to any of the pointer addresses 30h through 37h. The reset value for these registers is FFh and F0h.

The Remote Temperature Maximum Register is read with the high byte from pointer address 36h and the low byte is read from pointer address 37h. The Remote Temperature Maximum Register is read with a two-byte read command from pointer address 36h. The Remote Temperature Maximum Register resets at power-on by executing the chip reset command, or by writing any value to any of the pointer addresses 30h through 37h. The reset value for these registers is 00h and 00h.

9.6.11 Consecutive Alert Register

The value in the Consecutive Alert Register (address 22h) determines how many consecutive out-of-limit measurements must occur on a measurement channel before the ALERT signal is activated. The value in this register does not effect bits in the Status Register. Values of one, two, three, or four consecutive conversions can be selected; one conversion is the default. The function allows additional filtering for the ALERT pin. The consecutive alert bits are listed in Table 9:

Table 9. Consecutive Alert Register

CONSECUTIVE ALERT REGISTER (READ = 22h, WRITE = 22h, POR = 01h)			
C2	C1	C0	NUMBER OF CONSECUTIVE OUT OF LIMIT MEASUREMENTS
0	0	0	1
0	0	1	2
0	1	1	3
1	1	1	4

NOTE

Bit 7 of the Consecutive Alert Register controls the enable/disable of the timeout function. See the *Timeout Function* section for a description of this feature.

9.6.12 THERM Hysteresis Register

The THERM Hysteresis Register, shown in Table 11, stores the hysteresis value for the THERM pin alarm function. This register must be programmed with a value that is less than the Local Temperature High Limit Register value, Remote Temperature High Limit Register value, Local THERM Limit Register value, or Remote THERM Limit Register value, otherwise the respective temperature comparator does not trip on the falling edges of the measured temperature. Permitted hysteresis values are listed in Table 10. The default hysteresis value is 10°C, whether the device is operating in the standard or extended mode setting.

Table 10. Allowable THERM Hysteresis Values

TEMPERATURE (°C)	THERM HYSTERESIS VALUES	
	TH [11:1] (STANDARD BINARY)	(HEX)
0	0000 0000	00
1	0000 0001	01
5	0000 0101	05
10	0000 1010	0A
25	0001 1001	19
50	0011 0010	32
75	0100 1011	4B
100	0110 0100	64
125	0111 1101	7D
127	0111 1111	7F
150	1001 0110	96
175	1010 1111	AF
200	1100 1000	C8
225	1110 0001	E1
255	1111 1111	FF

Table 11. $\overline{\text{THERM}}$ Hysteresis Register Format

$\overline{\text{THERM}}$ HYSTERESIS REGISTER (READ = 21h, WRITE = 21h, POR = 0Ah)								
BIT NUMBER	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4
POR VALUE	0	0	0	0	1	0	1	0

9.6.13 Remote Temperature Offset Register

The offset register allows the TMP411E to store any system offset compensation value that may result from precision calibration. The value in the register is stored in the same format as the temperature result, and is added to the remote temperature result after each conversion. Combined with the η-factor correction, the function allows for an accurate system calibration over the entire temperature range.

9.6.14 Identification Registers

The TMP411 allows for the two-wire bus controller to query the device for manufacturer and device identification. This feature allows for software identification of the device at the particular two-wire bus address. The manufacturer identification is obtained by reading from pointer address FEh. The TMP411 manufacturer code is 55h. The device identification depends on the specific model, as listed in Table 3. These registers are read-only.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TMP411 only requires a transistor connected between the D+ and D– pins for remote temperature measurement. Tie the D+ pin to D– if the remote channel is not used and only the local temperature is measured. The SDA, $\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins (and SCL, if driven by an open-drain output) require pullup resistors as part of the communication bus. TI recommends using a 0.1-µF power-supply decoupling capacitor for local bypassing. Figure 11 illustrates the typical configurations for the TMP411.

10.2 Typical Application

10.2.1 Design Requirements

The TMP411 is designed to be used with discrete transistors or substrate transistors built into processor chips and ASICs. NPN or PNP transistors can be used, as long as the base-emitter junction is the remote temperature sensor. A transistor or diode connection can be used, as shown in Figure 11.

Errors in remote temperature sensor readings are the result of the ideality factor and current excitation from the TMP411 versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a high-level and low-level current for the temperature-sensing substrate transistors. The TMP411 has an I_{LOW} value of 6 µA, and an I_{HIGH} value of 120 µA. The TMP411 allows for different *n*-factor values, as shown in Table 8.

The ideality factor (*n*) is a measured characteristic of a remote temperature sensor diode compared to an ideal diode. The ideality factor reduces to a value of 1.008. For transistors with an ideality factor that does not match the TMP411, Equation 4 calculates the temperature error. Note that the actual temperature (°C) must be converted to Kelvin (°K) for the equation to yield the correct results.

$$T_{ERR} = \left(\frac{n - 1.008}{1.008}\right) \times \left(273.15 + T(^{\circ}C)\right) \quad (4)$$

where:

- *n* = the ideality factor of the remote temperature sensor
- T(°C) = actual temperature
- T_{ERR} = device reading error due to $n \neq 1.008$
- Degree delta is the same for °C and °K

For n = 1.004 and T(°C) = 100°C, use Equation 5:

$$T_{ERR} = \left(\frac{1.004 - 1.008}{1.008}\right) \times \left(273.15 + 100^{\circ}C\right)$$

$$T_{ERR} = -1.48^{\circ}C \quad (5)$$

If a discrete transistor is used as the remote temperature sensor, selecting the transistor according to the following criteria results in the best accuracy.

1. Base-emitter voltage > 0.25 V at 6 µA, at the highest sensed temperature.
2. Base-emitter voltage < 0.95 V at 120 µA, at the lowest sensed temperature.
3. Base resistance < 100 Ω
4. Tight control of V_{BE} characteristics indicated by small variations in h_{FE} (that is, 50 to 150).

Typical Application (continued)

Based on these criteria, TI recommends using two small-signal transistors, such as the 2N3904 (NPN) or 2N3906 (PNP).

10.2.2 Detailed Design Procedure

The temperature measurement accuracy of the TMP411 depends on the remote or local temperature sensor being at the same temperature as the monitored system point. If the temperature sensor is not in good thermal contact with the part of the system being monitored, then there is a delay in the response of the sensor to a temperature change in the system. For remote temperature sensing applications using a substrate transistor (or a small, SOT-23 transistor) placed close to the device , this delay is usually not a concern.

The local temperature sensor inside the TMP411 monitors the ambient air around the device. The thermal time constant for the TMP411 is approximately two seconds. This constant implies that if the ambient air changes quickly by 100°C, the TMP411 takes approximately 10 seconds (that is, five thermal time constants) to settle within 1°C of the final value. In most applications, the TMP411 package is in electrical (and thermal contact) with the printed circuit board (PCB), and subjected to forced airflow. The accuracy of the temperature measurement directly depends on how accurately the PCB and forced airflow temperatures represent the temperature measured by the device. Additionally, the internal power dissipation of the TMP411 can cause the temperature to rise above the ambient or PCB temperature. The internal power dissipated is a result of exciting the remote temperature sensor is negligible because of the small currents used.

For a 3.3-V supply and maximum conversion rate of eight conversions per second, the TMP411 dissipates 1.32 mW (PD IQ = 3.3 V × 400 µA). If the $\overline{\text{ALERT}}$/THERM2 and THERM pins are each sinking 1 mA, an additional power of 0.8 mW is dissipated (PD OUT = 1 mA × 0.4 V + 1 mA × 0.4 V = 0.8 mW). Total power dissipation equals 2.12 mW (PD IQ + PD OUT) and (with a θ_{JA} value of 150°C/W) causes the junction temperature to rise approximately 0.318°C above the ambient.

10.2.3 Application Curves

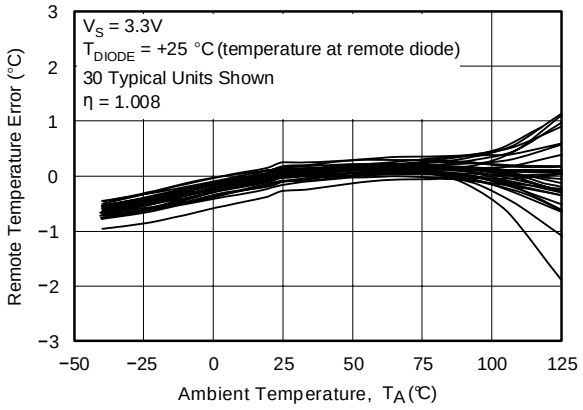


Figure 19. Remote Temperature Error vs TMP411 Ambient Temperature

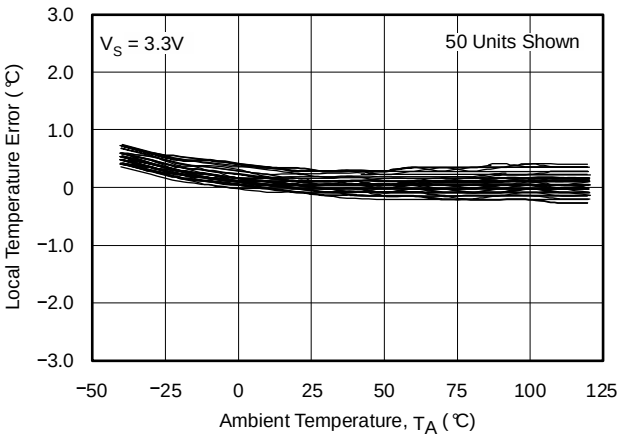


Figure 20. Local Temperature Error vs TMP411 Ambient Temperature

11 Power Supply Recommendations

The TMP411 operates with a power supply range of 2.7 V to 5.5 V. The device is optimized for operation at a 3.3-V supply, but measures temperature accurately in the full supply range. TI recommends using a power supply bypass capacitor. Place the capacitor as close as possible to the supply and ground pins of the device. 0.1 µF is a typical value for the supply bypass capacitor. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

12 Layout

12.1 Layout Guidelines

Remote temperature sensing on the TMP411 measures small voltages using low currents, and therefore noise at the device inputs must be minimized. Most applications using the TMP411 have high digital content with several clocks and logic-level transitions that create a noisy environment. The layout must adhere to the following guidelines:

- Place the TMP411 as close to the remote junction sensor as possible.
- Route the D+ and D– traces next to each other and shield the traces from adjacent signals using ground guard traces, as shown in Figure 21. If a multilayer PCB is used, bury these traces between ground or VDD planes to shield them from extrinsic noise sources. TI recommends using 5-mm (0.127 mm) PCB traces.
- Minimize additional thermocouple junctions caused by copper-to-solder connections. If these junctions are used, make the same number and approximate location of copper-to-solder connections in the D+ and D– connections to cancel any thermocouple effects.
- Use a 0.1–µF local bypass capacitor directly between the V+ and GND pins of the TMP411, as shown in Figure 22. Minimize filter capacitance between D+ and D– to 1000 pF or less for optimum measurement performance. This capacitance includes any cable capacitance between the remote temperature sensor and the TMP411 .
- If the connection between the remote temperature sensor and the TMP411 is less than eight inches (20 cm), use a twisted-wire pair connection. If the connection measures more than eight inches (20 cm), use a twisted, shielded pair with the shield grounded as close to the TMP411 as possible. Leave the remote sensor connection end of the shield wire open to avoid grounded loops and 60-Hz pickup.

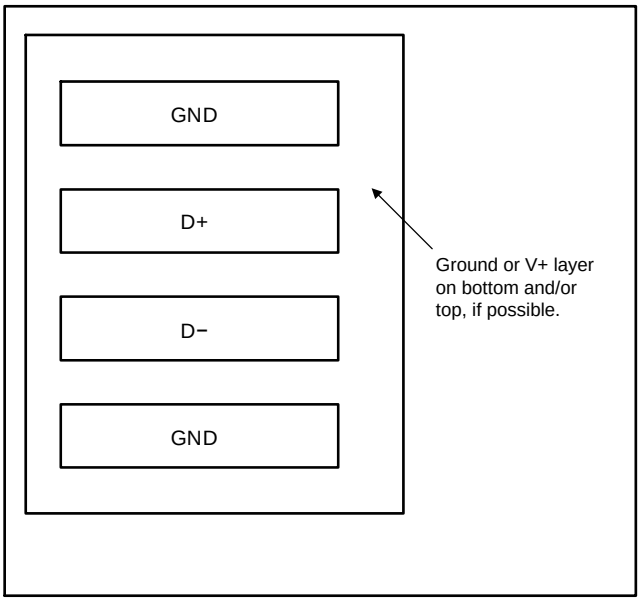


Figure 21. Example Signal Traces

Layout Guidelines (continued)

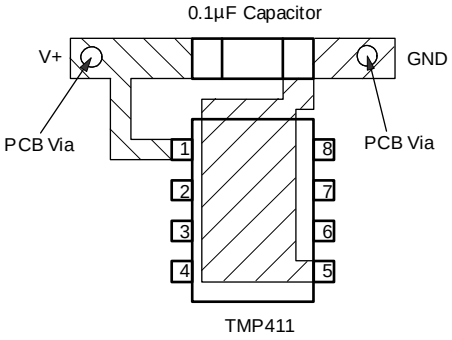


Figure 22. Suggested Bypass Capacitor Placement

12.2 Layout Example

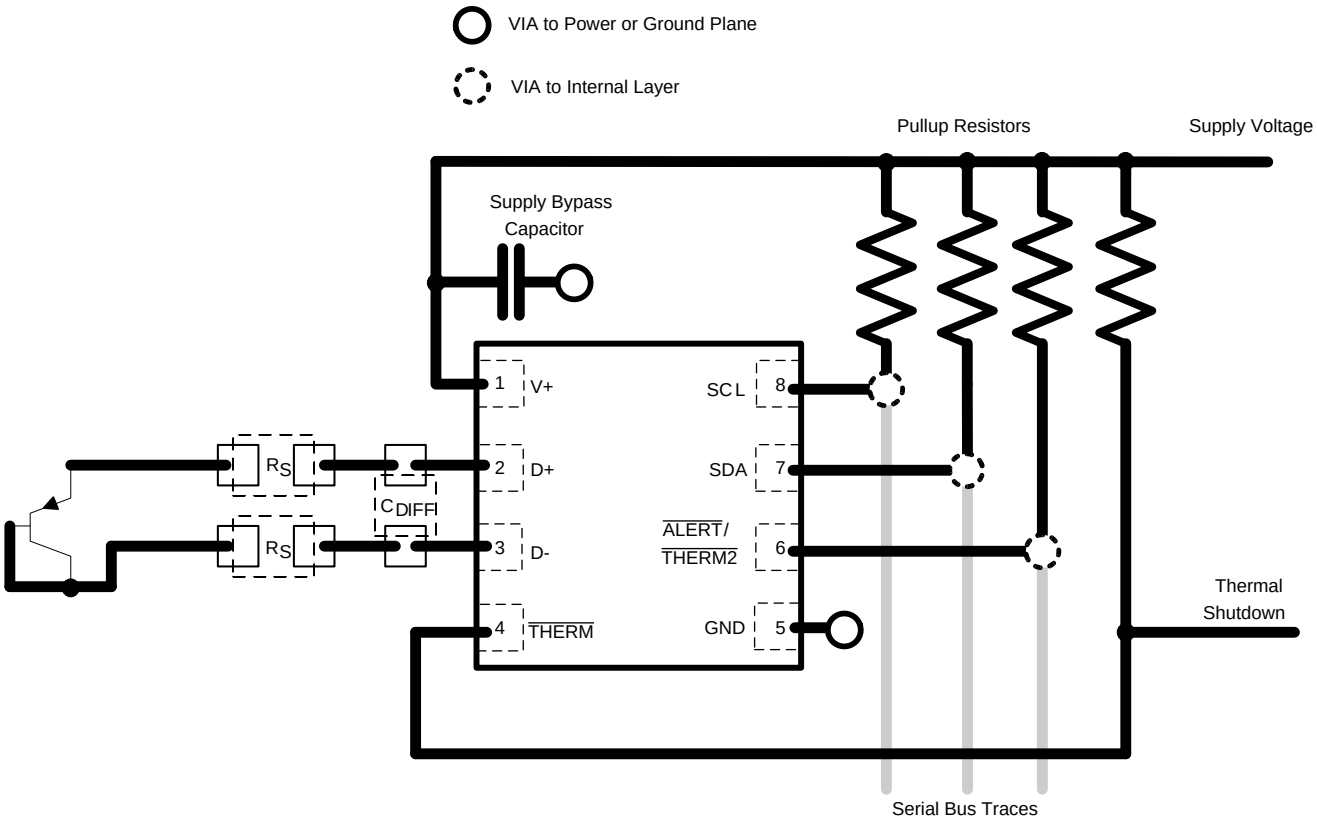


Figure 23. TMP411 Device Layout

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
DLP is a trademark of others.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMP411AD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T411A	
TMP411ADG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T411A	
TMP411ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411A	Samples
TMP411ADGKRG4	LIFEBUY	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	411A	
TMP411ADGKT	LIFEBUY	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411A	
TMP411ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T411A	Samples
TMP411BD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T411B	
TMP411BDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411B	Samples
TMP411BDGKT	LIFEBUY	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411B	
TMP411BDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T411B	Samples
TMP411CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T411C	
TMP411CDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411C	Samples
TMP411CDGKT	LIFEBUY	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411C	
TMP411CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T411C	Samples
TMP411EDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411E	Samples
TMP411EDGKT	LIFEBUY	VSSOP	DGK	8	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	411E	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TMP411 :

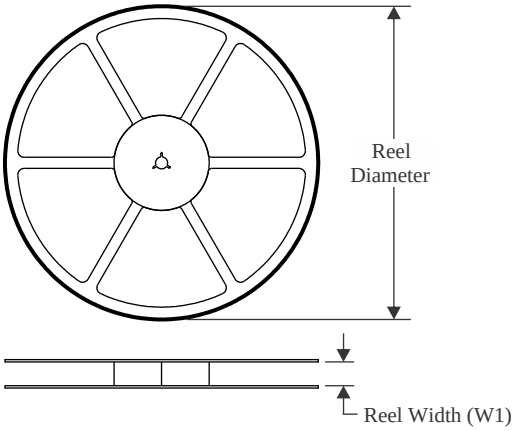
- Automotive : TMP411-Q1

NOTE: Qualified Version Definitions:

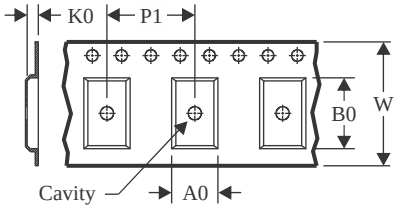
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

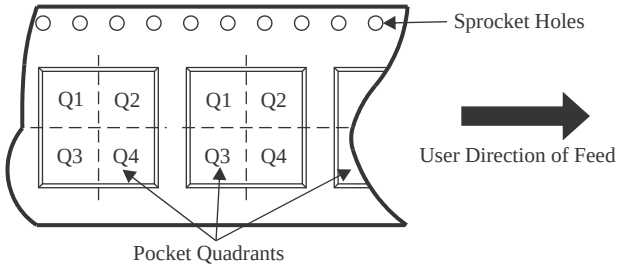


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

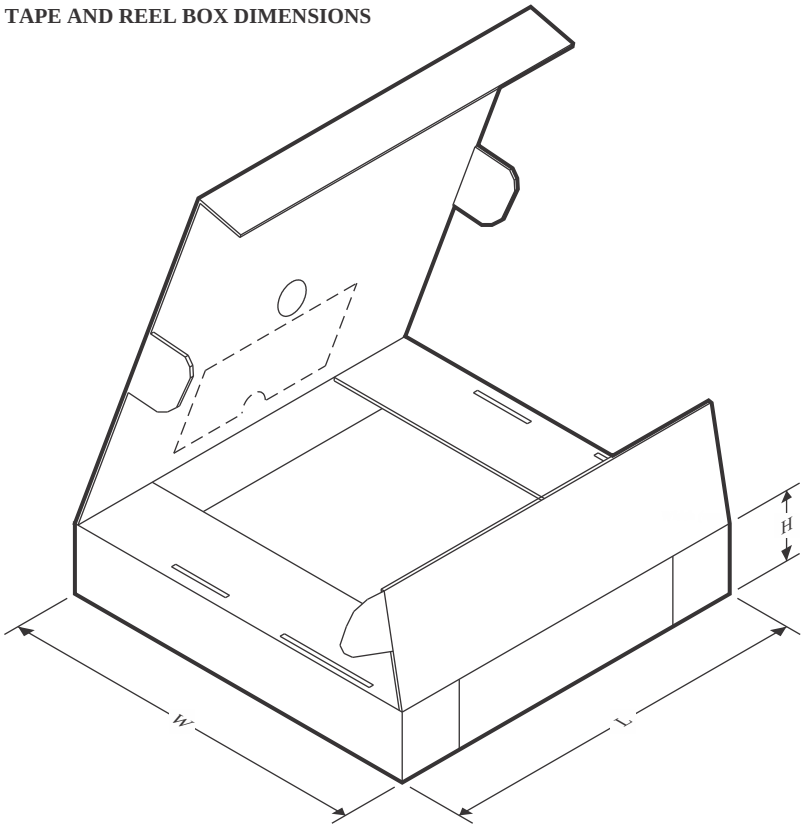
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP411ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP411ADGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP411BDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP411BDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411BDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP411CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411CDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411CDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TMP411CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TMP411EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TMP411EDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

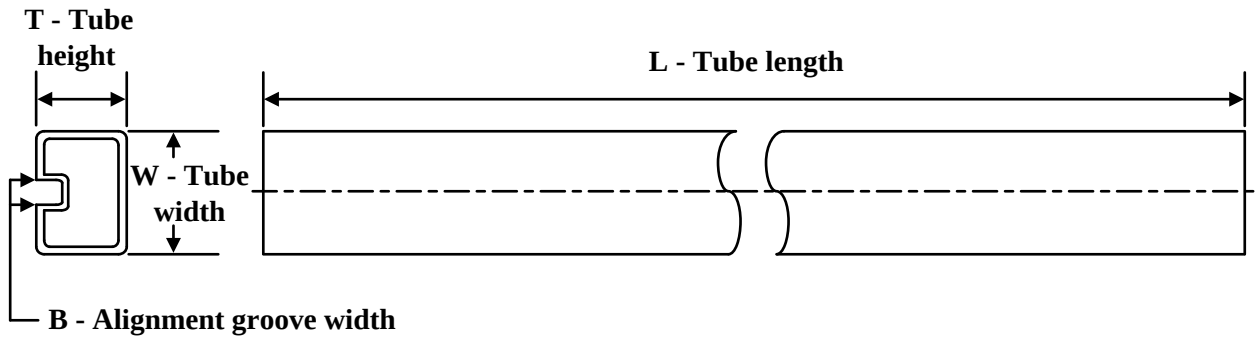
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

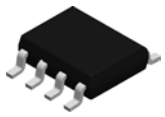
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP411ADGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP411ADGKR	VSSOP	DGK	8	2500	367.0	367.0	38.0
TMP411ADGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP411ADR	SOIC	D	8	2500	356.0	356.0	35.0
TMP411BDGKR	VSSOP	DGK	8	2500	367.0	367.0	38.0
TMP411BDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP411BDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP411BDR	SOIC	D	8	2500	356.0	356.0	35.0
TMP411CDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP411CDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
TMP411CDGKT	VSSOP	DGK	8	250	213.0	191.0	35.0
TMP411CDR	SOIC	D	8	2500	356.0	356.0	35.0
TMP411EDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TMP411EDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TMP411AD	D	SOIC	8	75	506.6	8	3940	4.32
TMP411ADG4	D	SOIC	8	75	506.6	8	3940	4.32
TMP411BD	D	SOIC	8	75	506.6	8	3940	4.32
TMP411CD	D	SOIC	8	75	506.6	8	3940	4.32

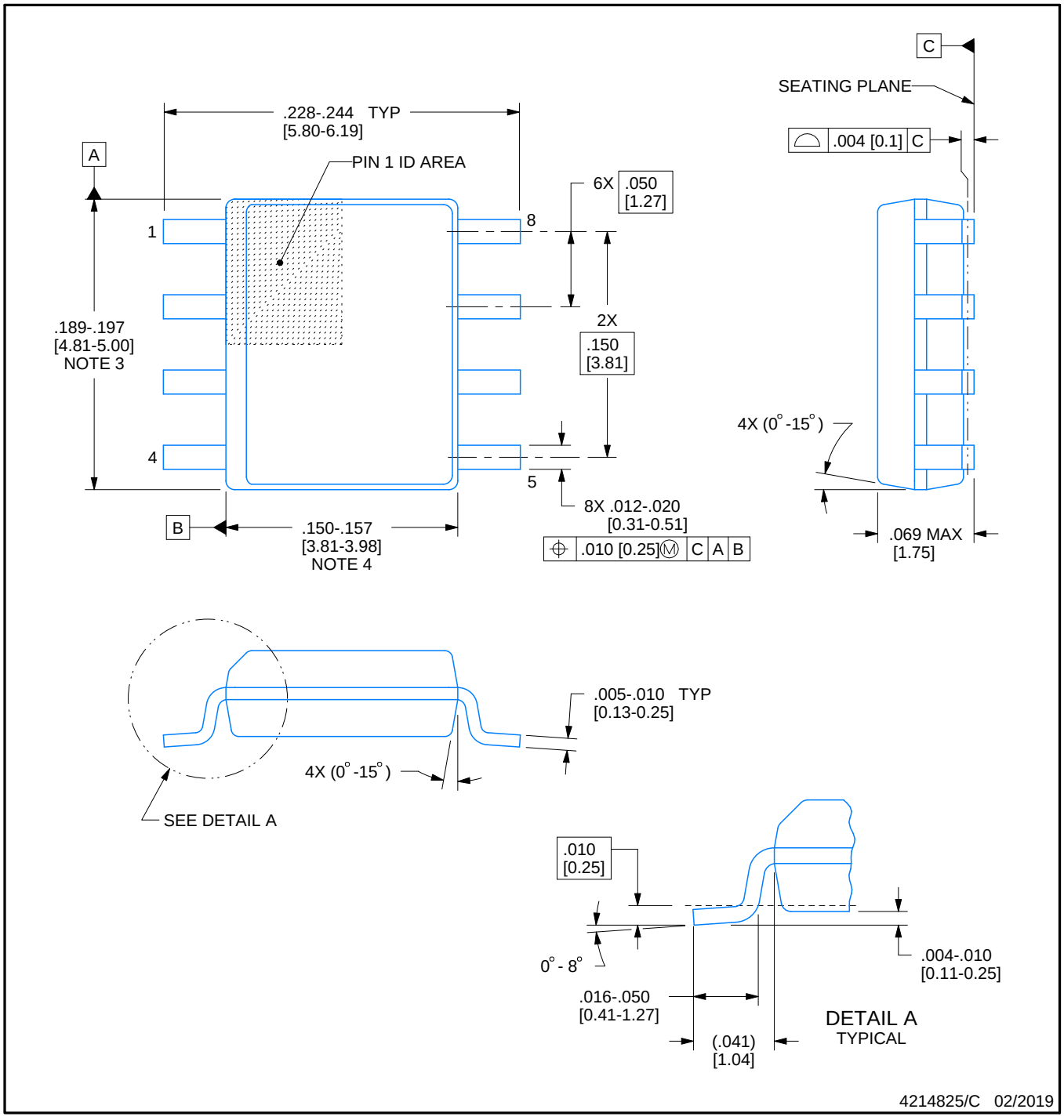


PACKAGE OUTLINE

D0008A

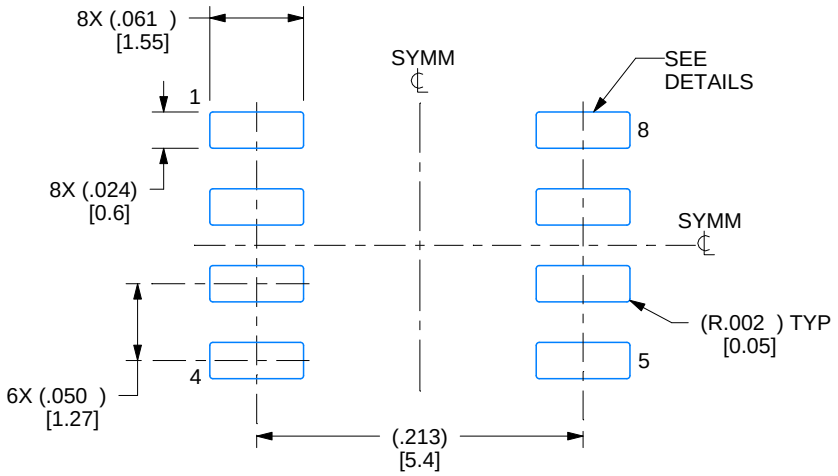
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

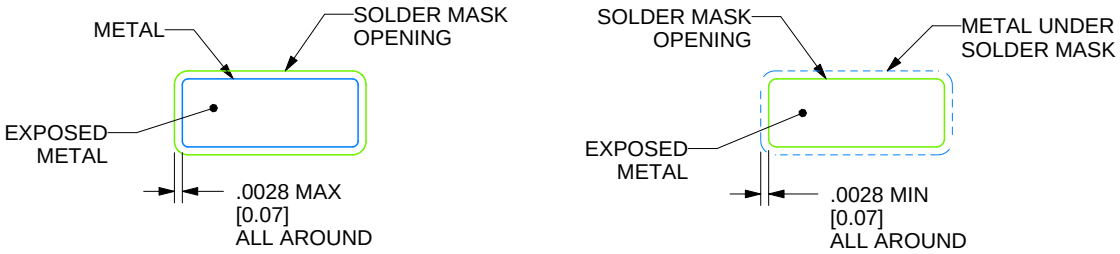


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

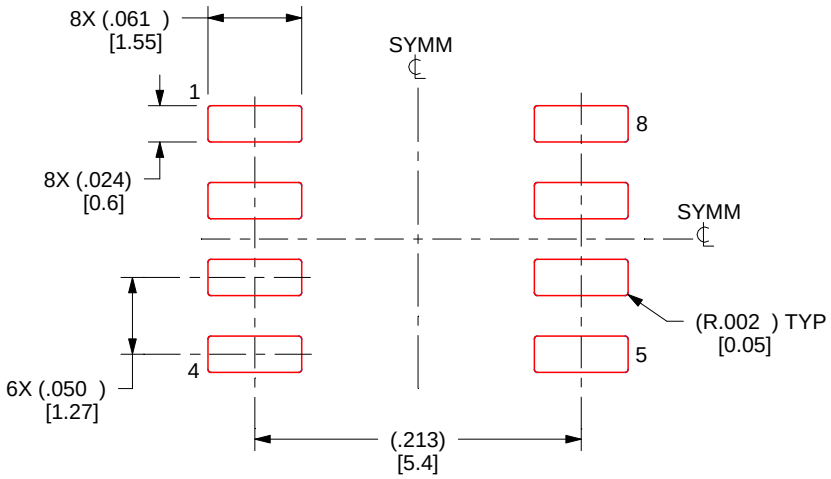
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



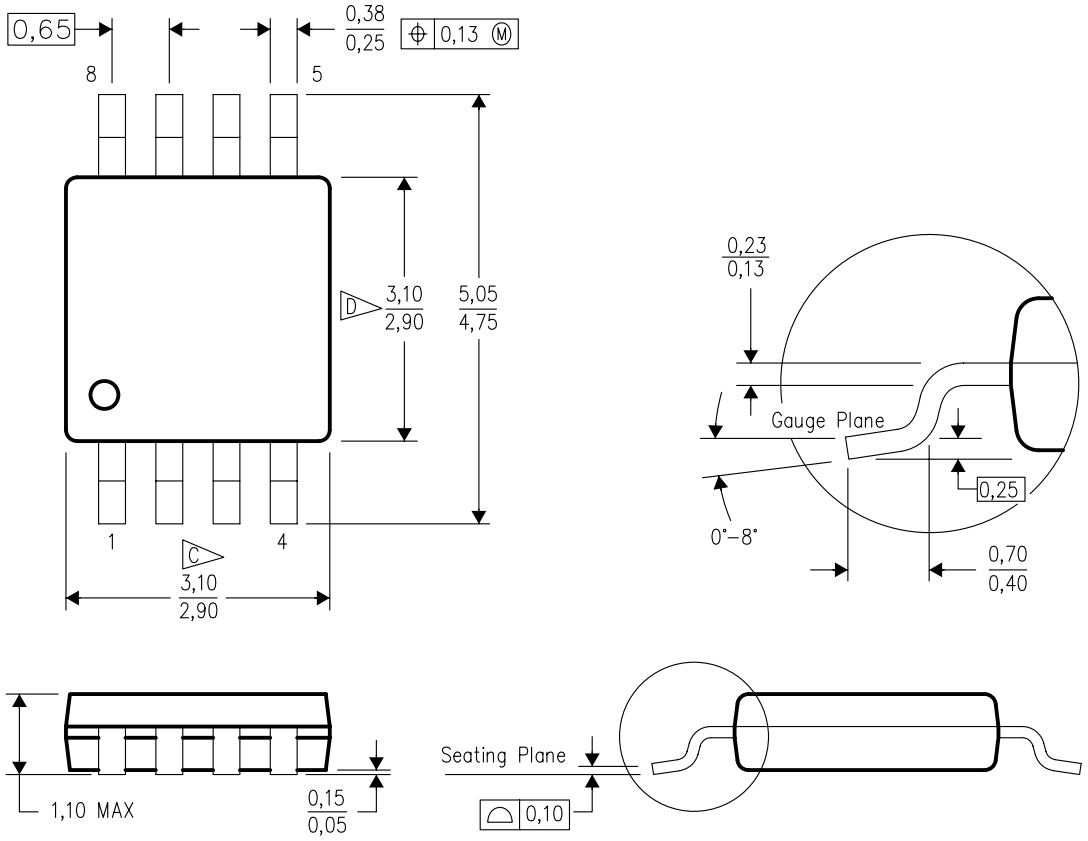
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

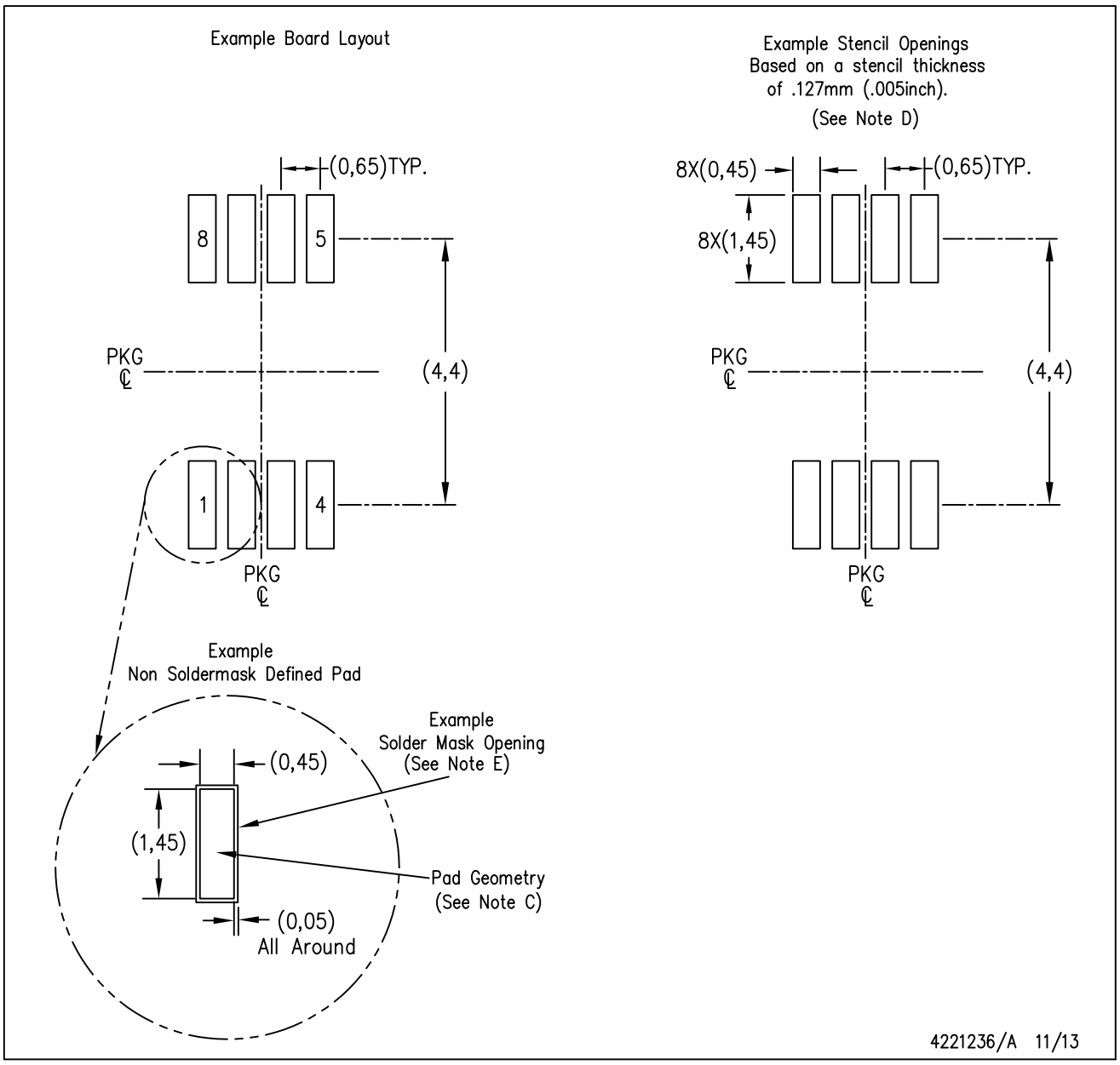
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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