SN74AUC1G125 Single Bus Buffer Gate With 3-State Output

1 Features

- Optimized for 1.8-V operation
- ±8-mA output drive at 1.8 V
- Maximum t_{pd} of 2.5 ns at 1.8 V, 30 pF load
- Wide operating voltage range of 0.8 V to 2.7 V
- Over-voltage tolerant I/Os support up to 3.6 V, independent of V_{CC}
- Available in the Texas Instruments NanoFree™ package
- I_{off} feature supports partial power down mode and back drive protection
- Low power consumption, 10-µA maximum I_{CC}
- Latch-up performance exceeds 100 mA per JESD 78, Class II

2 Applications

- Redrive digital signals
- Enable or disable a digital signal
- Drive transmission lines with logic

3 Description

The SN74AUC1G125 device is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high.

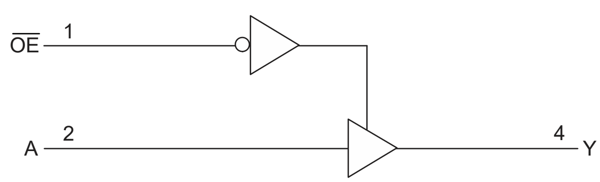
The AUC logic family is specifically designed for speed and is optimized for operation between 1.65-V and 1.95-V V_{CC}. With an optimal supply and 15-pF load the device can operate at over 250 MHz, or 500 Mbps. The unique output structure of the AUC family provides great signal integrity without the need for external termination when driving 50- to 65-Ω transmission lines of moderate length (less than 15 cm). See *Application of the Texas Instruments AUC Sub-1-V Little Logic Devices* for more details on this technology.

This device is available in the popular SOT-23 and SC70 packages, as well as the advanced NanoFree™ DSBGA package. NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Package Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUC1G125	DBV (SOT-23, 5)	2.90 mm × 1.60 mm
	DCK (SC70, 5)	2.00 mm × 1.25 mm
	YZP (DSBGA, 5)	1.39 mm × 0.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Diagram (Positive Logic)

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (June 2017) to Revision M (August 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document ...1
- Updated the *Features* section, *Applications* section, and *Device Information* table...1
- Changed the YZP (DSBGA, 5) body size from: *1.75 mm × 1.25 mm* to: *1.39 mm × 0.89 mm* ...1
- Added the *Application and Implementation*, *Application Information*, *Typical Application*, *Power Supply Recommendations*, *Layout*, *Layout Guidelines*, and *Layout Examples* sections...1
- Updated the *Pin Configuration and Functions* section...3
- Updated the *ESD Ratings* section...4
- Updated the *Thermal Information* section...5

Changes from Revision K (April 2007) to Revision L (June 2017) **Page**

- Deleted DRY package throughout data sheet...1
- Added *Applications*, *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section...1
- Deleted *Ordering Information* table, see *Mechanical, Packaging, and Orderable Information* at the end of the data sheet ...1

5 Pin Configuration and Functions

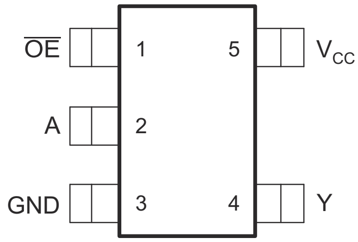


Figure 5-1. DBV Package, 5-Pin SOT-23 (Top View)

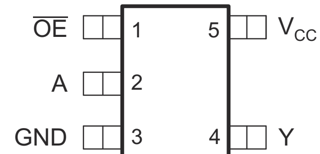


Figure 5-2. DCK Package, 5-Pin SC70 (Top View)

Table 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	DBV, DCK		
A	2	I	Logic input
GND	3	G	Ground
$\overline{OE}$	1	I	Active-low output enable
V_{CC}	5	P	Positive supply
Y	4	O	Output

(1) I = input, O = output, P = power, G = ground

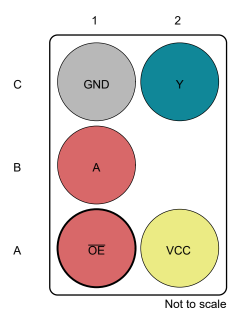


Figure 5-3. YZP Package, 5-Pin DSBGA (Bottom View)

Legend	
Input	Power
Ground	Output

Table 5-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
A1	$\overline{OE}$	I	Output enable, active low
A2	V_{CC}	P	Positive supply
B1	A	I	Logic input
C1	GND	G	Ground
C2	Y	O	Output

(1) I = input, O = output, P = power, G = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	3.6	V
V_I	Input voltage[2]		–0.5	3.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		–0.5	3.6	V
V_O	Output voltage range[2]		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	
		Machine Model (A115-A)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	2.7	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.7		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		–0.7	mA
		V_{CC} = 1.1 V		–3	
		V_{CC} = 1.4 V		–5	
		V_{CC} = 1.65 V		–8	
		V_{CC} = 2.3 V		–9	

6.3 Recommended Operating Conditions (continued)

See [(1)]

			MIN	MAX	UNIT
I_{OL}	Low-level output current	V_{CC} = 0.8 V		0.7	mA
		V_{CC} = 1.1 V		3	
		V_{CC} = 1.4 V		5	
		V_{CC} = 1.65 V		8	
		V_{CC} = 2.3 V		9	
Δt/Δv	Input transition rise or fall rate	V_{CC} = 0.8 V to 1.6 V		20	ns/V
		V_{CC} = 1.65 V to 1.95 V		10	
		V_{CC} = 2.3 V to 2.7 V		3	
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See *Implications of Slow or Floating CMOS Inputs*

6.4 Thermal Information

THERMAL METRIC[(1)]		DBV (SOT-23)	DCK (SC70)	YZP (DSBGA)	UNIT
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220.7	262.5	144.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.9	181.4	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	123.20	153.4	47.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	58.3	67.60	0.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	122.5	152.80	47.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP[(1)]	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		0.8 V to 2.7 V	V_{CC} – 0.1			V
		I_{OH} = –0.7 mA		0.8 V		0.55		
		I_{OH} = –3 mA		1.1 V	0.8			
		I_{OH} = –5 mA		1.4 V	1			
		I_{OH} = –8 mA		1.65 V	1.2			
		I_{OH} = –9 mA		2.3 V	1.8			
V_{OL}		I_{OL} = 100 μA		0.8 V to 2.7 V			0.2	V
		I_{OL} = 0.7 mA		0.8 V		0.25		
		I_{OL} = 3 mA		1.1 V			0.3	
		I_{OL} = 5 mA		1.4 V			0.4	
		I_{OL} = 8 mA		1.65 V			0.45	
		I_{OL} = 9 mA		2.3 V			0.6	
I_I	A or $\overline{OE}$ input	$V_I = V_{CC}$ or GND		0 to 2.7 V			±5	μA
I_{off}		V_I or V_O = 2.7 V		0			±10	μA
I_{OZ}		$V_O = V_{CC}$ or GND		2.7 V			±10	μA
I_{CC}		$V_I = V_{CC}$ or GND	I_O = 0	0.8 V to 2.7 V			10	μA
C_I		$V_I = V_{CC}$ or GND		2.5 V		2.5		pF

6.5 Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
C_o	$V_O = V_{CC}$ or GND	2.5 V		5.5		pF

(1) All typical values are at T_A = 25°C.

6.6 Switching Characteristics: C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V		V_{CC} = 1.5 V ± 0.1 V		V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	4.7	0.8	3.6	0.4	2.3	0.6	1	1.5	0.5	1.3	ns
t_{en}	$\overline{OE}$	Y	5.4	0.7	4.1	0.5	2.6	0.6	1.1	1.8	0.5	1.4	ns
t_{dis}	$\overline{OE}$	Y	4.8	1.4	4.3	1.4	4	1.5	2.2	2.9	0.9	2.2	ns

6.7 Switching Characteristics: C_L = 30 pF

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V			V_{CC} = 2.5 V ± 0.2 V		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	0.7	1.5	2.5	0.9	1.7	ns
t_{en}	$\overline{OE}$	Y	1	1.6	2.6	1.1	1.9	ns
t_{dis}	$\overline{OE}$	Y	1.8	2.2	3.1	0.8	1.7	ns

6.8 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 0.8 V	V_{CC} = 1.2 V	V_{CC} = 1.5 V	V_{CC} = 1.8 V	V_{CC} = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	14	14	14	15	16	pF
		Outputs disabled		1.5	1.5	1.5	2	2.5	

6.9 Typical Characteristics

T_A = 25°C

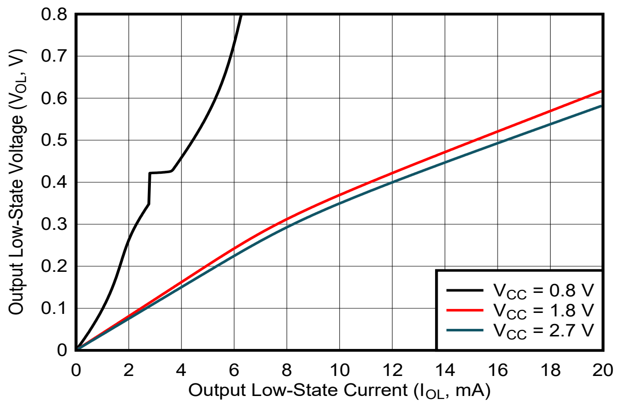


Figure 6-1. Output Low-State Voltage Across Output Current, 0.8-, 1.8-, and 2.7-V Supply

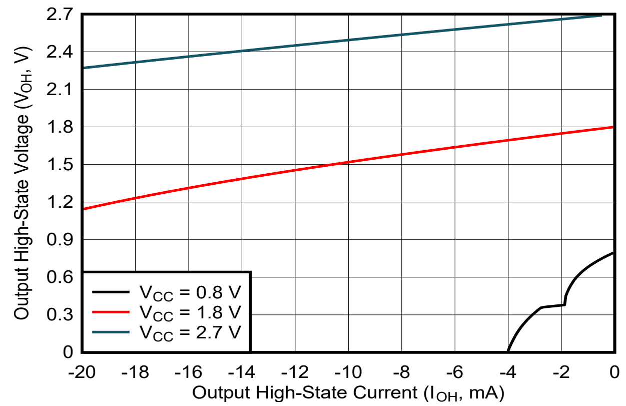


Figure 6-2. Output High-State Voltage Across Output Current, 0.8-, 1.8-, and 2.7-V Supply

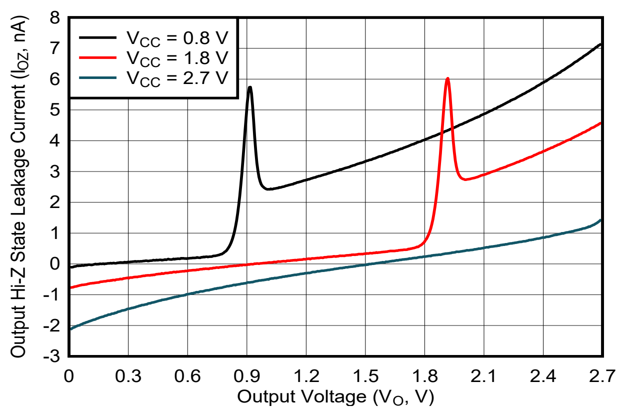
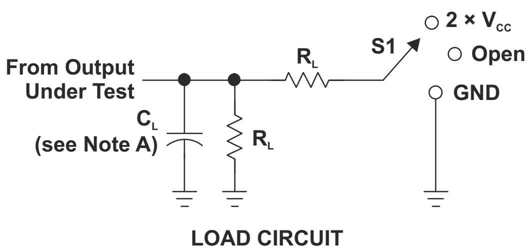


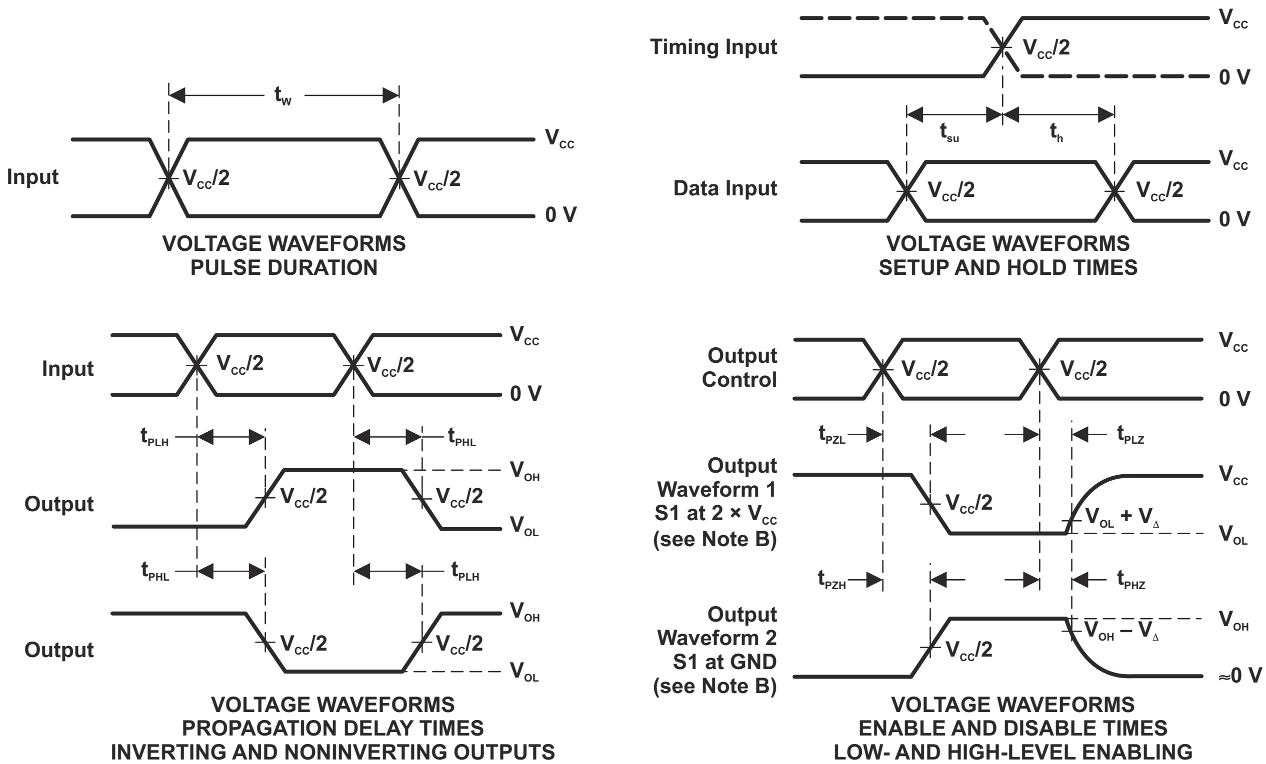
Figure 6-3. Output High-Impedance State Leakage Current Across Output Voltage, 0.8-, 1.8-, and 2.7-V Supply

7 Parameter Measurement Information



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_Δ
0.8 V	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V



NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AUC1G125 bus buffer gate is operational from 0.8-V to 2.7-V V_{CC}, but is optimized for 1.65-V to 1.95-V V_{CC} operation.

This device is a single line driver with a 3-state output. The output is disabled when the output-enable ($\overline{OE}$) input is high.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

8.2 Functional Block Diagram

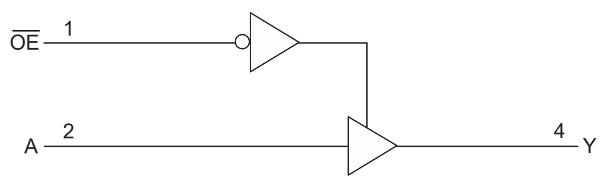


Figure 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 ULTTL CMOS Outputs

This device includes ultra-low-voltage transistor-transistor logic (ULTTL) output drivers. ULTTL outputs are *balanced*, indicating that the device can sink and source similar currents. They are also specially designed for applications requiring high-speed, low power consumption, and optimal signal integrity while minimizing switching noise.

The ULTTL output driver changes impedance during transition to maximize transition rate while limiting ringing and transmission line reflections. The output is optimized for operation with a direct connection to a 50- to 65-Ω controlled impedance transmission line of up to 15 cm, although it can operate with acceptable signal integrity for controlled impedances of between 30 and 70 Ω.

The outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in *Implications of Slow or Floating CMOS Inputs*.

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10-kΩ resistor, however, is recommended and will typically meet all requirements.

8.3.3 Partial Power Down (I_{off})

This device includes circuitry to disable all outputs when the supply pin is held at 0 V. When disabled, the outputs will neither source nor sink current, regardless of the input voltages applied. The amount of leakage current at each output is defined by the I_{off} specification in the *Electrical Characteristics* table.

8.3.4 Clamp Diode Structure

Figure 8-2 shows the inputs and outputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

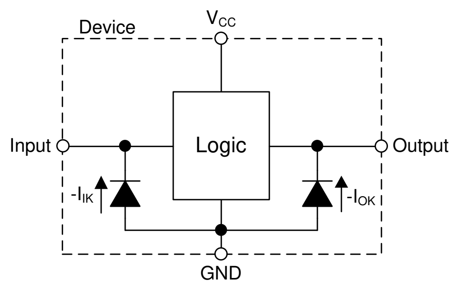


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Table 8-1 lists the functional modes of the SN74AUC1G125.

Table 8-1. Function Table

INPUTS[1]		OUTPUT[2]
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

(1) L = Low Voltage Level, H = High Voltage Level, X = Do Not Care
(2) L = Driving Low, H = Driving High, Z = High Impedance

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

In this application, the SN74AUC1G125 is used to control a high-speed digital signal. The output enable ($\overline{OE}$) input is connected to the system controller and allows the output to be disabled. Not shown is a 10-kΩ pull-down resistor which will ensure that the output will return to the low state when placed in the high-impedance mode of operation.

9.2 Typical Application

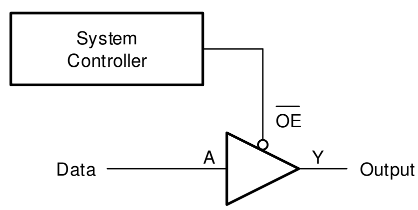


Figure 9-1. Application Block Diagram

9.2.1 Design Requirements

- All signals in the system operate at 1.8 V ± 0.15 V
- Input signals transition faster than 10 ns/V
- Y output is enabled when $\overline{OE}$ is LOW
- Output transmission line impedance should be between 50 and 65 Ω

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the output tranmission line is less than 15 cm in total length for optimal signal integrity results. For the best signal integrity, avoid sharp turns, stubs, and branches.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, CMOS Power Consumption and Cpd Calculation.

9.2.3 Application Curves

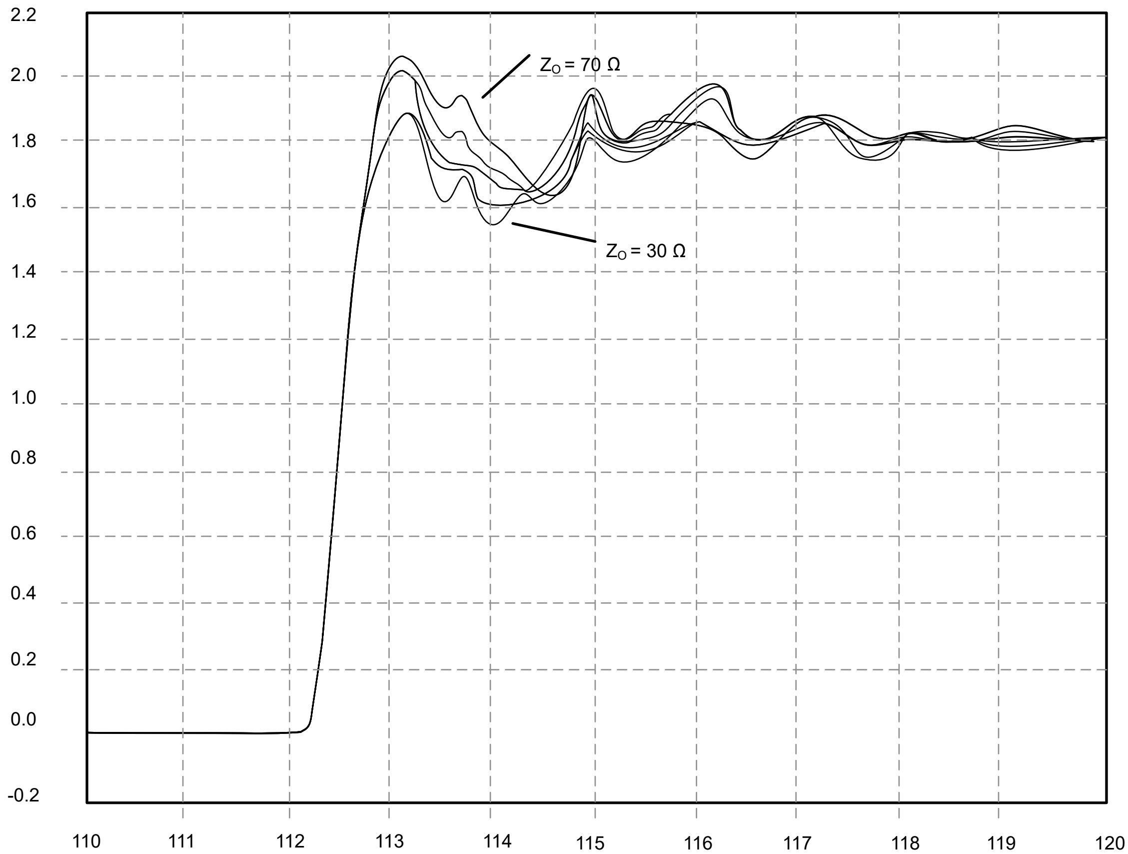


Figure 9-2. Simulated Output Voltage Waveforms for AUC Family Directly Driving Short (< 15 cm) Transmission Lines With Characteristic Impedances from 30 to 70 Ω (Volts vs Nanoseconds)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

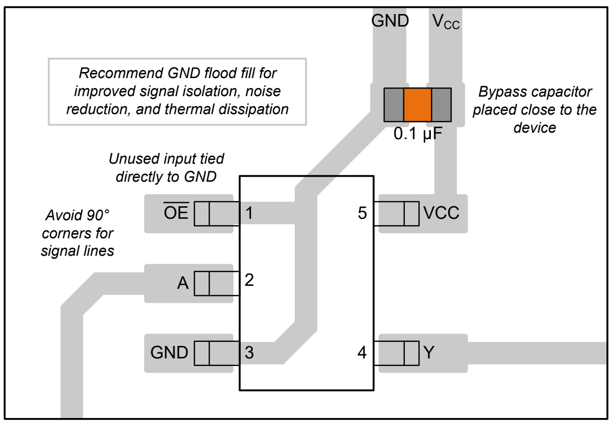


Figure 11-1. Example Layout for DCK Package

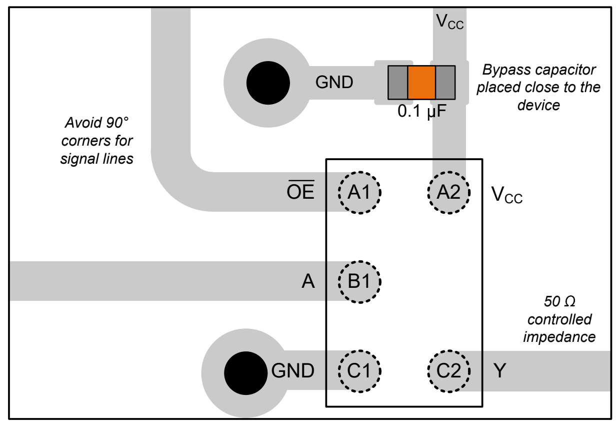


Figure 11-2. Example Layout for YZP Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

NanoFree™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AUC1G125DBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	U25R	Samples
74AUC1G125DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	U25R	Samples
SN74AUC1G125DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	U25R	Samples
SN74AUC1G125DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(UM5, UMF, UMR)	Samples
SN74AUC1G125YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	UMN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

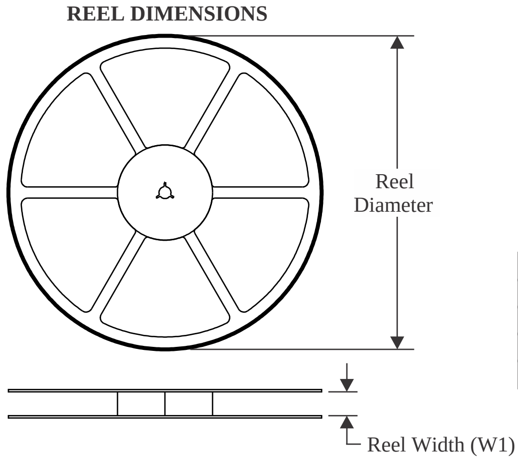
OTHER QUALIFIED VERSIONS OF SN74AUC1G125 :

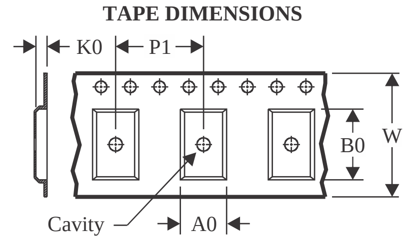
- Enhanced Product : SN74AUC1G125-EP

NOTE: Qualified Version Definitions:

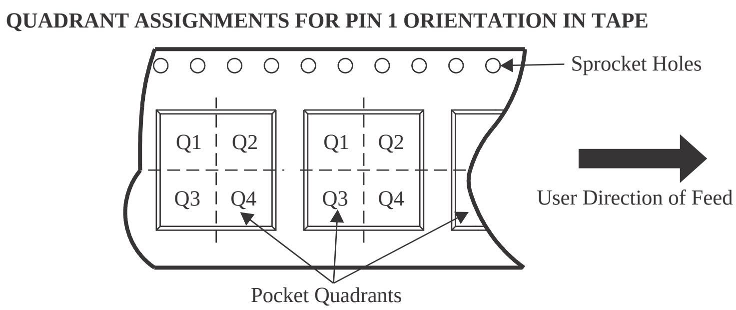
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION





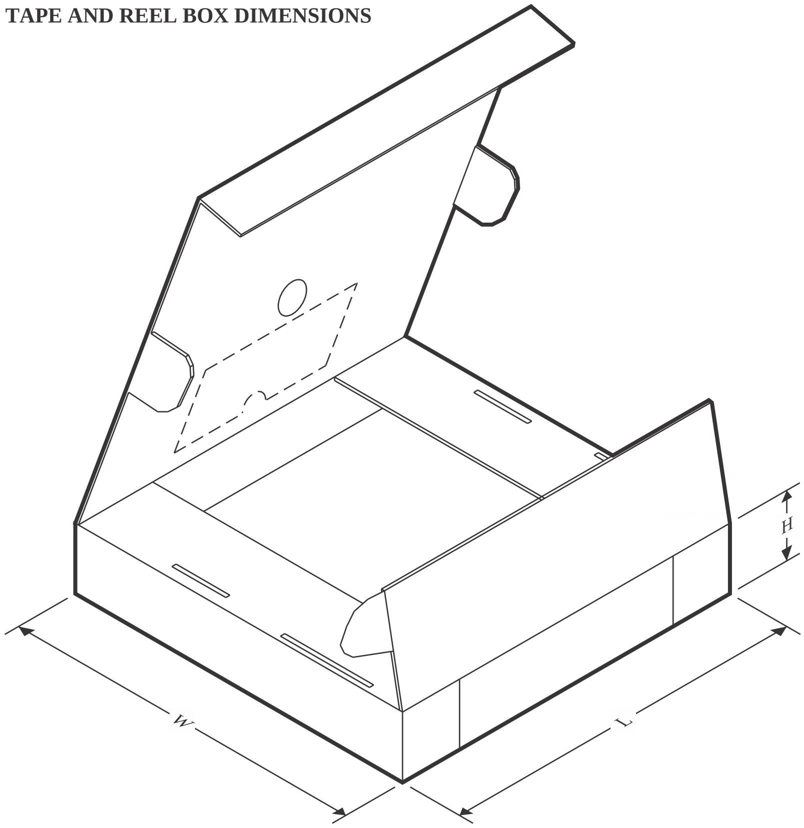
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

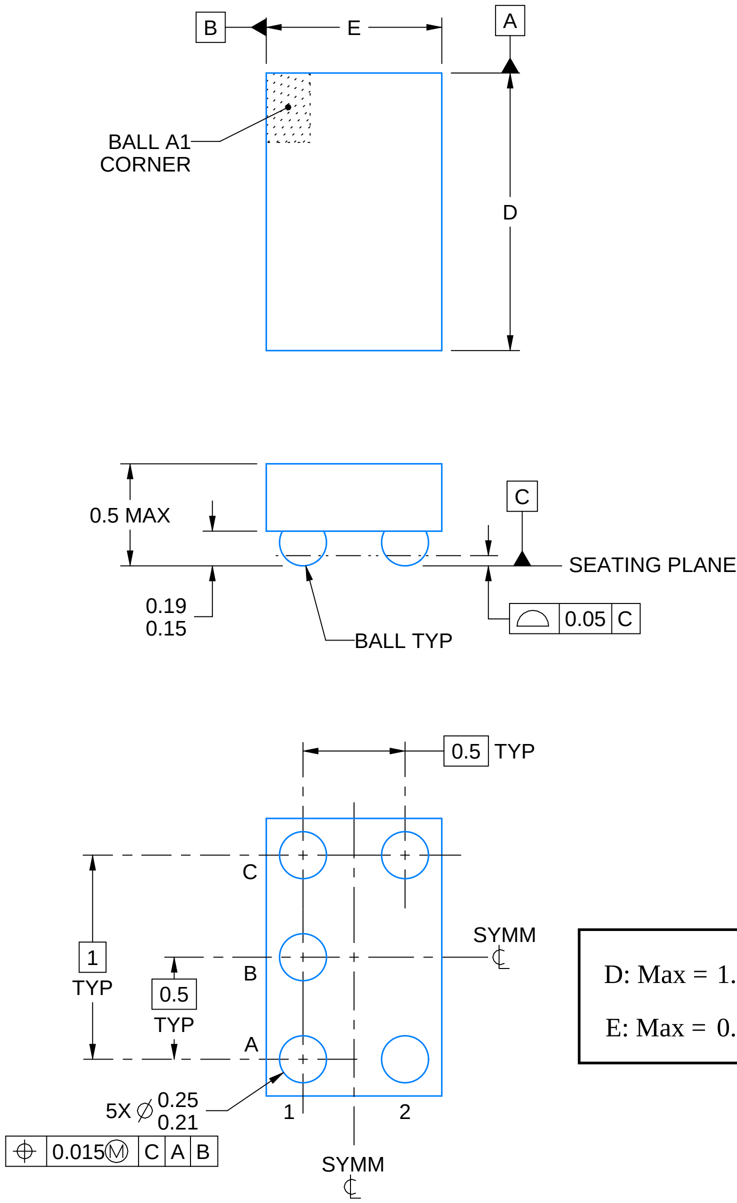
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUC1G125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AUC1G125DCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
SN74AUC1G125YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUC1G125DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AUC1G125DCKR	SC70	DCK	5	3000	210.0	185.0	35.0
SN74AUC1G125YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0



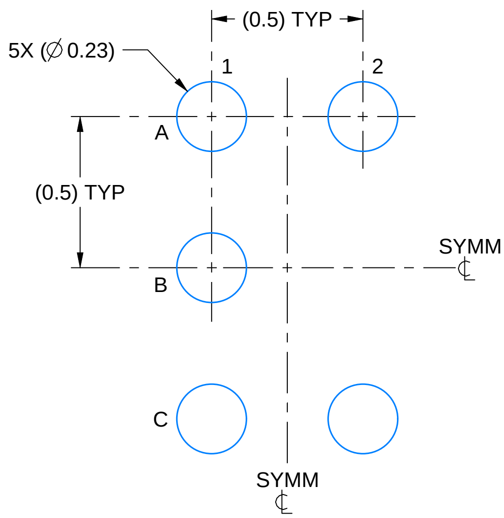
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

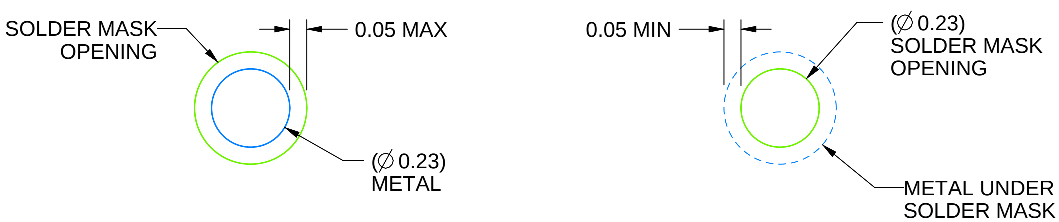
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



NON-SOLDER MASK DEFINED (PREFERRED)

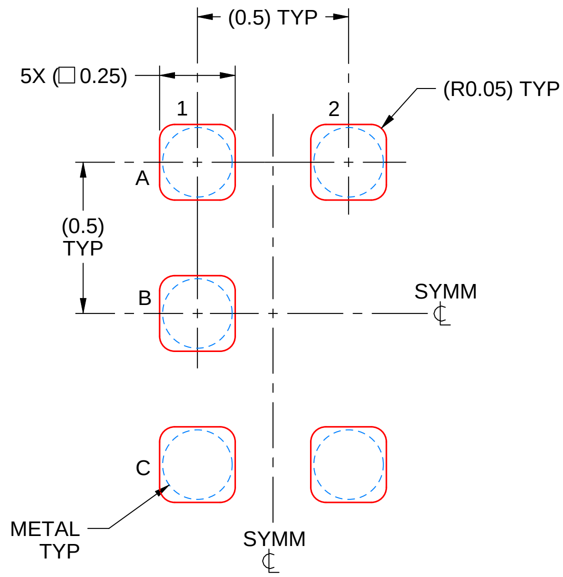
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

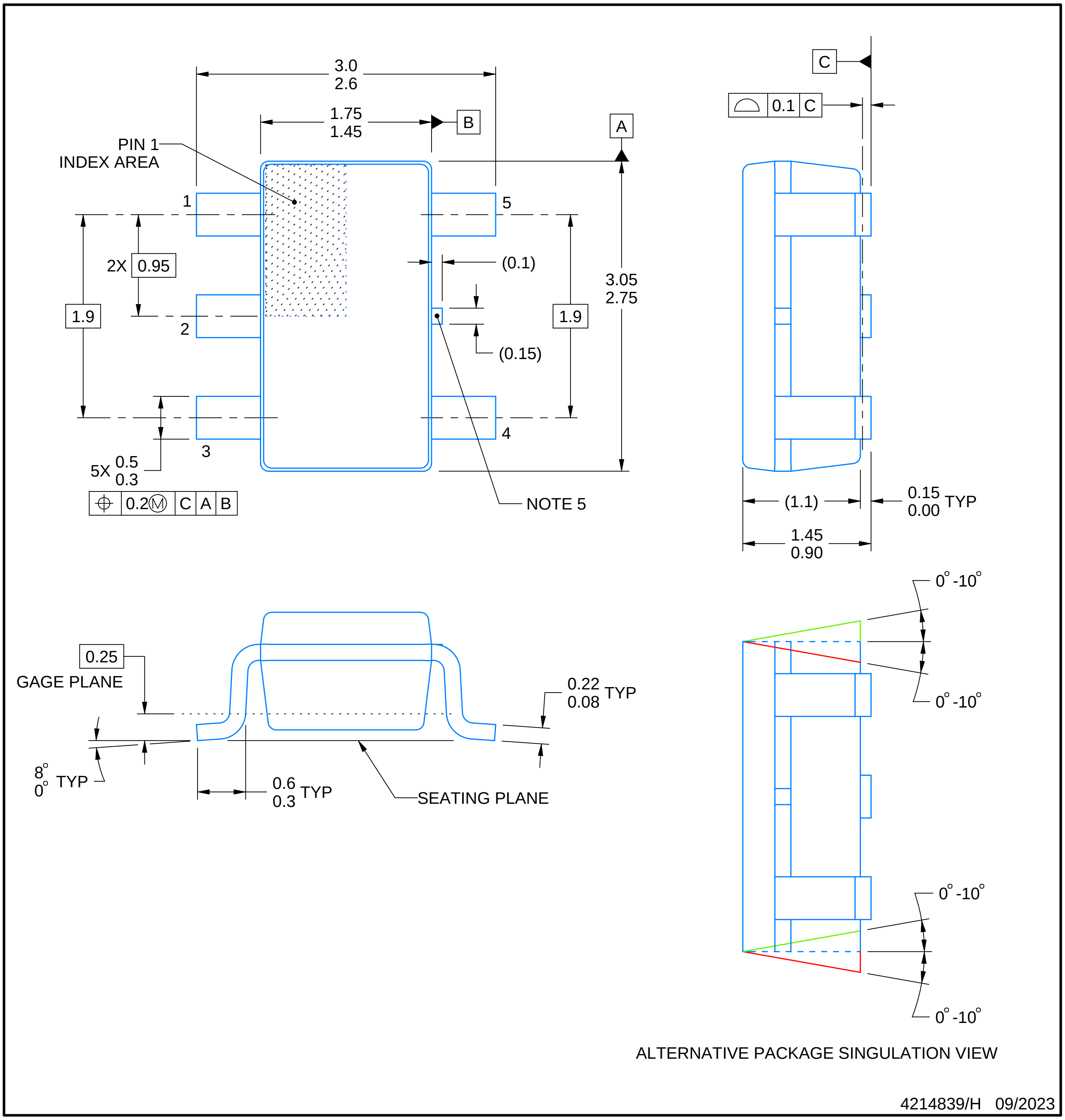


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

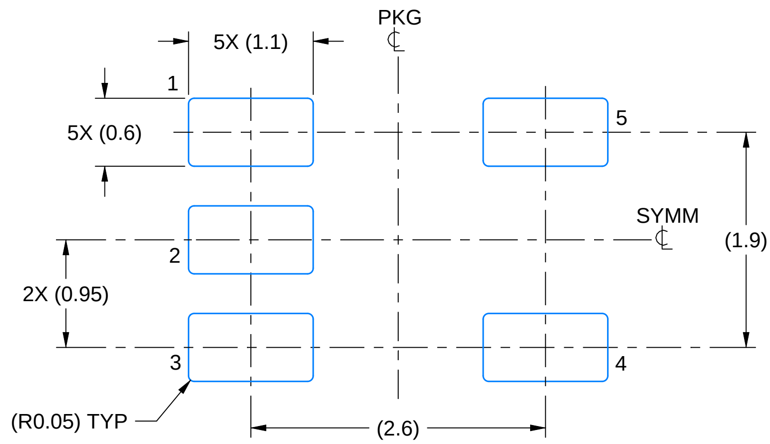
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

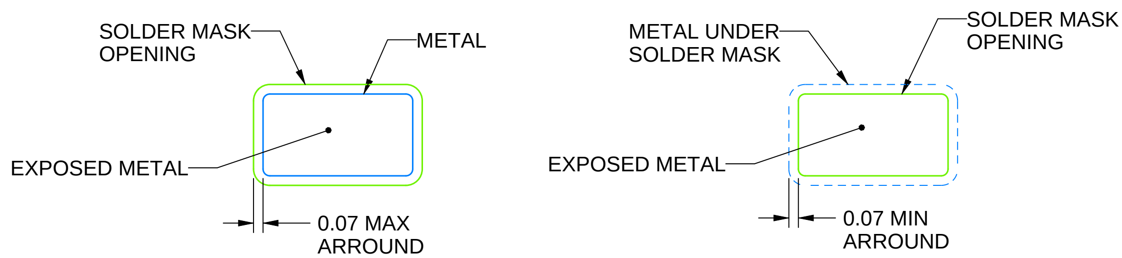


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

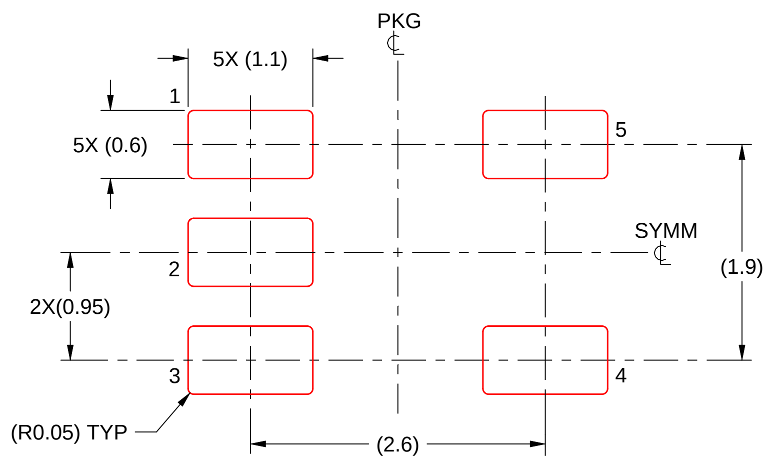


SOLDER MASK DETAILS

4214839/H 09/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

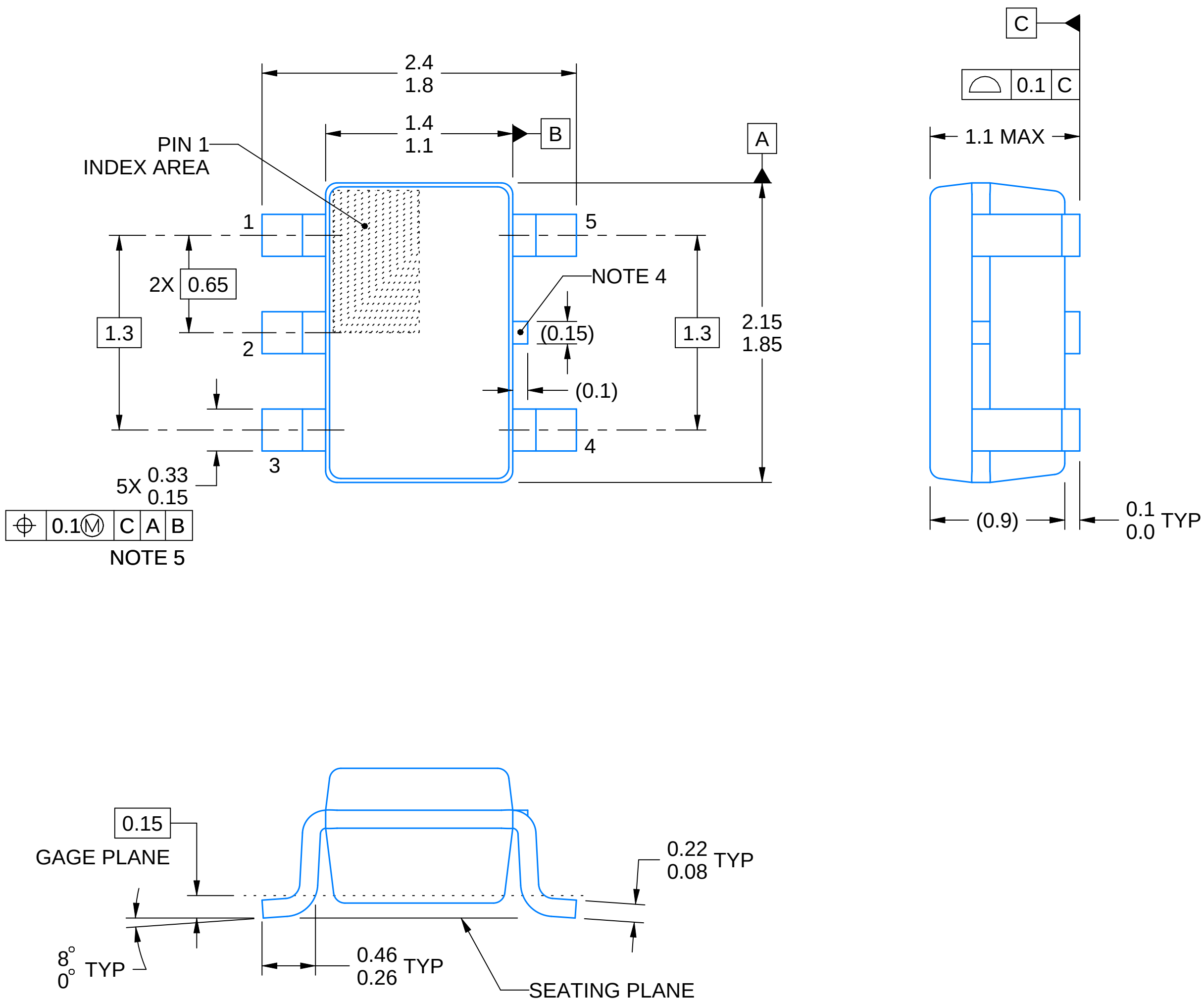


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/H 09/2023

NOTES: (continued)

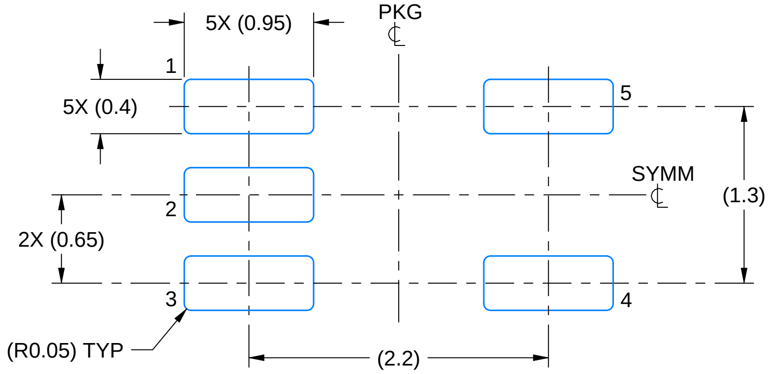
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



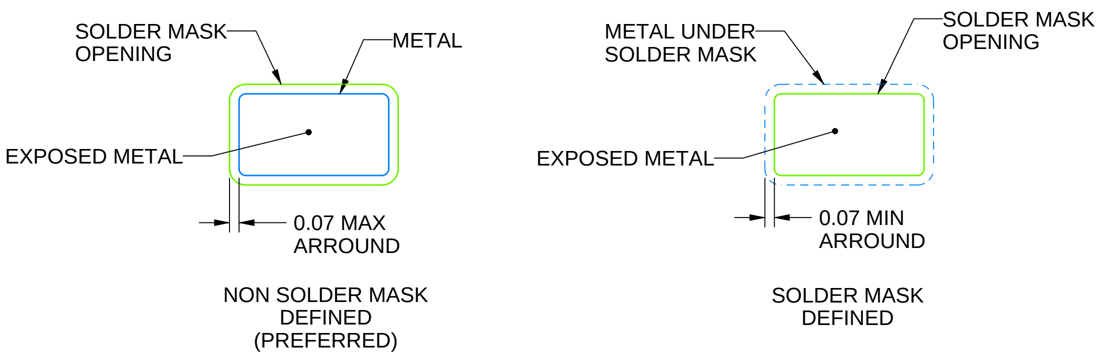
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

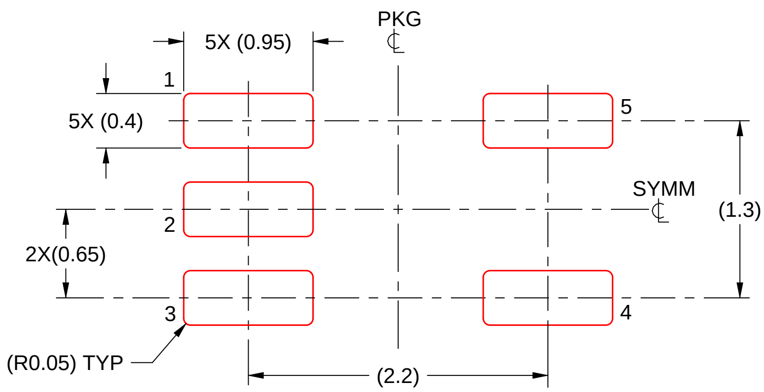


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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