

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

- Direct Upgrades for the TL06x Low-Power BiFETs
- Low Power Consumption . . . 6.5 mW/Channel Typ
- On-Chip Offset-Voltage Trimming for Improved DC Performance (1.5 mV, TL031A)
- Higher Slew Rate and Bandwidth Without Increased Power Consumption
- Available in TSSOP for Small Form-Factor Designs

description

The TL03x series of JFET-input operational amplifiers offer improved dc and ac characteristics over the TL06x family of low-power BiFET operational amplifiers. On-chip zener trimming of offset voltage yields precision grades as low as 1.5 mV (TL031A) for greater accuracy in dc-coupled applications. The Texas Instruments improved BiFET process and optimized designs also yield improved bandwidths and slew rates without increased power consumption. The TL03x devices are pin-compatible with the TL06x and can be used to upgrade existing circuits or for optimal performance in new designs.

BiFET operational amplifiers offer the inherently higher input impedance of the JFET-input transistors without sacrificing the output drive associated with bipolar amplifiers. This higher input impedance makes the TL3x amplifiers better suited for interfacing with high-impedance sensors or very low-level ac signals. These devices also feature inherently better ac response than bipolar or CMOS devices having comparable power consumption.

The TL03x family has been optimized for micropower operation, while improving on the performance of the TL06x series. Designers requiring significantly faster ac response should consider the Excalibur™ TLE206x family of low-power BiFET operational amplifiers.

Because BiFET operational amplifiers are designed for use with dual power supplies, care must be taken to observe common-mode input-voltage limits and output swing when operating from a single supply. DC biasing of the input signal is required, and loads should be terminated to a virtual-ground node at midsupply. The TI TLE2426 integrated virtual-ground generator is useful when operating BiFET amplifiers from single supplies.

The TL03x devices are fully specified at ± 15 V and ± 5 V. For operation in low-voltage and/or single-supply systems, the TI LinCMOS families of operational amplifiers (TLC prefix) are recommended. When moving from BiFET to CMOS amplifiers, particular attention should be paid to slew rate, bandwidth requirements, and output loading.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from -40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of -55°C to 125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Excalibur is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



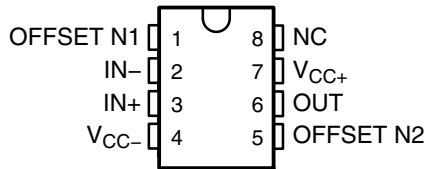
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2001, Texas Instruments Incorporated

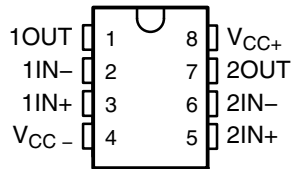
TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

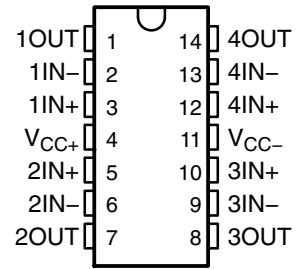
TL031x, TL031Ax
D, JG, OR P PACKAGE
(TOP VIEW)



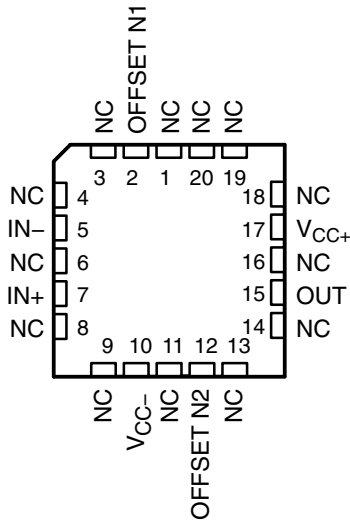
TL032x, TL032Ax
D, JG, OR P PACKAGE
(TOP VIEW)



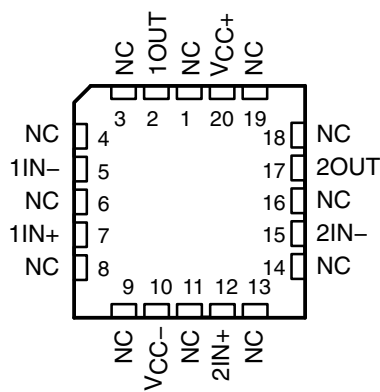
TL034x, TL034Ax
D, J, N, OR PW PACKAGE
(TOP VIEW)



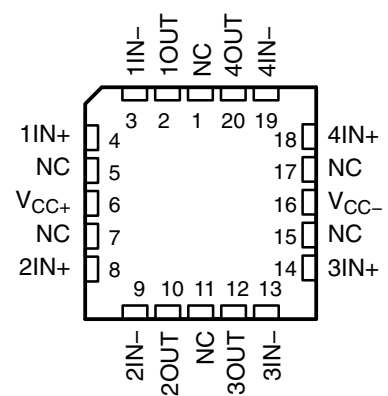
TL031M, TL031AM
FK PACKAGE
(TOP VIEW)



TL032M, TL032AM
FK PACKAGE
(TOP VIEW)



TL034M, TL034AM
FK PACKAGE
(TOP VIEW)



NC – No internal connection

TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

AVAILABLE OPTIONS

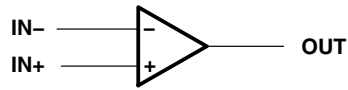
| T_A | $V_{IO\text{MAX}}$ AT 25°C | PACKAGED DEVICES | | | | | | |
|----------------|-------------------------------|--------------------------------|-----------------------------------|-----------------------|------------------------|-----------------------|-----------------------|---------------|
| | | SMALL OUTLINE (D) | CHIP CARRIER (FK) | CERAMIC DIP (J) | CERAMIC DIP (JG) | PLASTIC DIP (N) | PLASTIC DIP (P) | TSSOP (PW) |
| 0°C to 70°C | 0.8 mV | TL031ACD TL032ACD | — | — | — | — | TL031ACP TL032ACP | — |
| | 1.5 mV | TL031CD TL032CD TL034ACD | — | — | — | TL034ACN | TL031CP TL032CP | — |
| | 4 mV | TL034CD | — | — | — | TL034CN | — | TL034CPW |
| –40°C to 85°C | 0.8 mV | TL031AID TL032AID | — | — | — | — | TL031AIP TL032AIP | — |
| | 1.5 mV | TL031ID TL032ID TL034AID | — | — | — | TL034AIN | TL031IP TL032IP | — |
| | 4 mV | TL034ID | — | — | — | TL034IN | — | — |
| –55°C to 125°C | 0.8 mV | TL031AMD TL032AMD | TL031AMFK TL032AMFK | — | TL031AMJG TL032AMJG | — | TL031AMP TL032AMP | — |
| | 1.5 mV | TL031MD TL032MD TL034AMD | TL031MFK TL032MFK TL034AMFK | TL034AMJ | TL031MJG TL032MJG | TL034AMN | TL031MP TL032MP | — |
| | 4 mV | TL034MD | TL034MFK | TL034MJ | — | TL034MN | — | — |

The D and PW packages are available taped and reeled and are indicated by adding an R suffix to device type (e.g., TL034CDR or TL034CPWR).

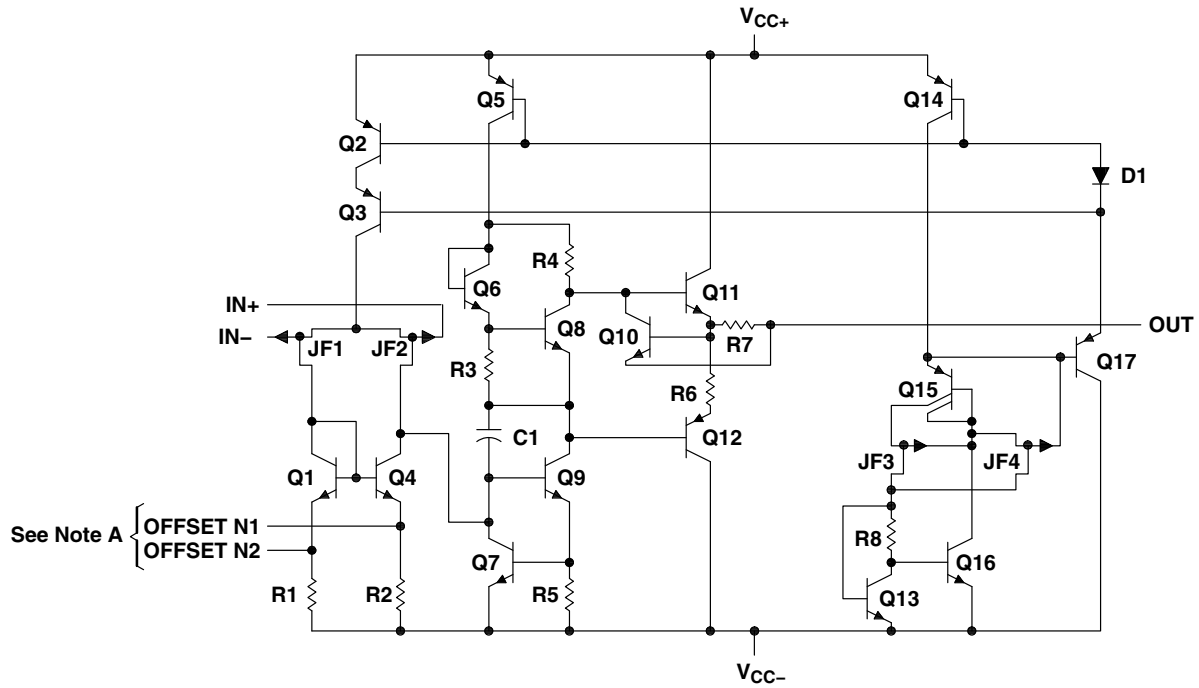
TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

symbol (each amplifier)



equivalent schematic (each amplifier)



NOTE A: OFFSET N1 and OFFSET N2 are available only on the TL031, TL031A.

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|------------------------------|
| Supply voltage (see Note 1): V_{CC+} | 18 V |
| V_{CC-} | -18 V |
| Differential input voltage, V_{ID} (see Note 2) | ± 30 V |
| Input voltage, V_I (any input) (see Notes 1 and 3) | ± 15 V |
| Input current, I_I (each input) | ± 1 mA |
| Output current, I_O (each output) | ± 40 mA |
| Total current into V_{CC+} | 160 mA |
| Total current out of V_{CC-} | 160 mA |
| Duration of short-circuit current at (or below) 25°C (see Note 4) | Unlimited |
| Continuous total power dissipation | See Dissipation Rating Table |
| Package thermal impedance, θ_{JA} (see Note 5): D package (8 pin) | 97°C/W |
| D package (14 pin) | 86°C/W |
| N package | 80°C/W |
| P package | 85°C/W |
| PW package | 113°C/W |
| Lead temperature 1,6 mm (1 /16 inch) from case for 10 seconds: D, N, P, or PW package | 260°C |
| Lead temperature 1,6 mm (1 /16 inch) from case for 60 seconds: J or JG package | 300°C |
| Case temperature for 60 seconds: FK package | 260°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 4. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ | DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ | $T_A = 125^\circ\text{C}$ |
|---------|-----------------------------|---|--------------------------|--------------------------|---------------------------|
| | POWER RATING | | POWER RATING | POWER RATING | POWER RATING |
| FK | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 275 mW |
| J | 1375 mW | 11.0 mW/°C | 880 mW | 715 mW | 275 mW |
| JG | 1050 mW | 8.4 mW/°C | 672 mW | 546 mW | 210 mW |

recommended operating conditions

| | | C SUFFIX | | I SUFFIX | | M SUFFIX | | UNIT |
|-------------|--------------------------------|------------------------|----------|----------|----------|----------|----------|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC\pm}$ | Supply voltage | ± 5 | ± 15 | ± 5 | ± 15 | ± 5 | ± 15 | V |
| V_{IC} | Common-mode input voltage | $V_{CC\pm} = \pm 5$ V | | -1.5 | 4 | -1.5 | 4 | V |
| | | $V_{CC\pm} = \pm 15$ V | | -11.5 | 14 | -11.5 | 14 | |
| T_A | Operating free-air temperature | 0 | 70 | -40 | 85 | -55 | 125 | °C |



TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL031C and TL031AC electrical characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | | T _A | TL031C, TL031AC | | | | | | UNIT |
|--|--|---------|----------------|-------------------------|-------------|------------------|--------------------------|-------|-----|------|
| | | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{IO} Input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL031C | 25°C | 0.54 3.5 | | 0.5 1.5 | | mV | | |
| | | | Full range† | 4.5 | | 2.5 | | | | |
| | | TL031AC | 25°C | 0.41 | 2.8 | 0.34 | 0.8 | | | |
| | | | Full range† | 3.8 | | 1.8 | | | | |
| α _{V_{IO}} Temperature coefficient of input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL031C | 25°C to 70°C | 7.1 | | 5.9 | | μV/°C | | |
| | | TL031AC | 25°C to 70°C | 7.1 | | 5.9 25 | | | | |
| Input offset voltage long-term drift‡ | V _O = 0, V _{IC} = 0, R _S = 50 Ω | | 25°C | 0.04 | | 0.04 | | μV/mo | | |
| I _{IO} Input offset current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 1 | 100 | 1 | 100 | pA | | |
| | | | 70°C | 9 | 200 | 12 | 200 | | | |
| I _{IB} Input bias current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 2 | 200 | 2 | 200 | pA | | |
| | | | 70°C | 50 | 400 | 80 | 400 | | | |
| V _{ICR} Common-mode input voltage range | | | 25°C | -1.5 to 4 | -3.4 to 5.4 | -11.5 to 14 | -13.4 to 15.4 | V | | |
| | | | Full range† | -1.5 to 4 | | -11.5 to 14 | | | | |
| V _{OM+} Maximum positive peak output voltage swing | R _L = 10 kΩ | | 25°C | 3 | 4.3 | 13 | 14 | V | | |
| | | | 0°C | 3 | 4.2 | 13 | 14 | | | |
| | | | 70°C | 3 | 4.3 | 13 | 14 | | | |
| V _{OM-} Maximum negative peak output voltage swing | R _L = 10 kΩ | | 25°C | -3 | -4.2 | -12.5 | -13.9 | V | | |
| | | | 0°C | -3 | -4.1 | -12.5 | -13.9 | | | |
| | | | 70°C | -3 | -4.2 | -12.5 | -14 | | | |
| A _{VD} Large-signal differential voltage amplification§ | R _L = 10 kΩ | | 25°C | 4 | 12 | 5 | 14.3 | V/mV | | |
| | | | 0°C | 3 | 11.1 | 4 | 13.5 | | | |
| | | | 70°C | 4 | 13.3 | 5 | 15.2 | | | |
| r _i Input resistance | | | 25°C | 10 ¹² | | 10 ¹² | | Ω | | |
| c _i Input capacitance | | | 25°C | 5 | | 4 | | pF | | |
| CMRR Common-mode rejection ratio | V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω | | 25°C | 70 | 87 | 75 | 94 | dB | | |
| | | | 0°C | 70 | 87 | 75 | 94 | | | |
| | | | 70°C | 70 | 87 | 75 | 94 | | | |
| k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO}) | V _O = 0, R _S = 50 Ω | | 25°C | 75 | 96 | 75 | 96 | dB | | |
| | | | 0°C | 75 | 96 | 75 | 96 | | | |
| | | | 70°C | 75 | 96 | 75 | 96 | | | |

† Full range is 0°C to 70°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V_{CC±} = ±5 V, V_O = ±2.3 V; at V_{CC±} = ±15 V, V_O = ±10 V



TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL031C and TL031AC electrical characteristics at specified free-air temperature (continued)

| PARAMETER | TEST CONDITIONS | T _A | TL031C, TL031AC | | | | | | UNIT |
|--|-----------------------------|----------------|-------------------------|-----|-----|--------------------------|-----|-----|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| P _D Total power dissipation | V _O = 0, No load | 25°C | | 1.9 | 2.5 | | 6.5 | 8.4 | mW |
| | | 0°C | | 1.8 | 2.5 | | 6.3 | 8.4 | |
| | | 70°C | | 1.9 | 2.5 | | 6.3 | 8.4 | |
| I _{CC} Supply current | V _O = 0, No load | 25°C | | 192 | 250 | | 217 | 280 | μA |
| | | 0°C | | 184 | 250 | | 211 | 280 | |
| | | 70°C | | 189 | 250 | | 210 | 280 | |

TL031C and TL031AC operating characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | T _A | TL031C, TL031AC | | | | | | UNIT |
|---|--|----------------|-------------------------|-------|-----|--------------------------|--------|--------|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR ⁺ Positive slew rate at unity gain [†] | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 2 | | 1.5 | 2.9 | V/μs | |
| | | 0°C | | 1.8 | | 1 | 2.6 | | |
| | | 70°C | | 2.2 | | 1.5 | 3.2 | | |
| SR ⁻ Negative slew rate at unity gain [†] | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 3.9 | | 1.5 | 5.1 | V/μs | |
| | | 0°C | | 3.7 | | 1.5 | 5 | | |
| | | 70°C | | 4 | | 1.5 | 5 | | |
| t _r Rise time | V _{I(PP)} = ±10 mV, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 138 | | 132 | | ns | |
| | | 0°C | | 134 | | 127 | | | |
| | | 70°C | | 150 | | 142 | | | |
| t _f Fall time | V _{I(PP)} = ±10 mV, R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 138 | | 132 | | ns | |
| | | 0°C | | 134 | | 127 | | | |
| | | 70°C | | 150 | | 142 | | | |
| Overshoot factor | V _{I(PP)} = ±10 mV, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 11% | | 5% | | | |
| | | 0°C | | 10% | | 4% | | | |
| | | 70°C | | 12% | | 6% | | | |
| V _n Equivalent input noise voltage | TL031C R _S = 20 Ω See Figure 3 | 25°C | f = 10 Hz | | 61 | | 61 | nV/√Hz | |
| | | | f = 1 kHz | | 41 | | 41 | | |
| | | 25°C | f = 10 Hz | | 61 | | 61 | | |
| | | | f = 1 kHz | | 41 | | 41 | | 60 |
| I _n Equivalent input noise current | f = 1 kHz | 25°C | | 0.003 | | 0.003 | pA/√Hz | | |
| B ₁ Unity-gain bandwidth | V _I = 10 mV R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 1 | | 1.1 | MHz | | |
| | | 0°C | | 1 | | 1.1 | | | |
| | | 70°C | | 1 | | 1 | | | |
| φ _m Phase margin at unity gain | V _I = 10 mV R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 61° | | 65° | | | |
| | | 0°C | | 61° | | 65° | | | |
| | | 70°C | | 60° | | 64° | | | |

[†] For V_{CC±} = ±5 V, V_{I(PP)} = ±1 V; for V_{CC±} = ±15 V, V_{I(PP)} = ±5 V



TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL031I and TL031AI electrical characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | | T _A | TL031I, TL031AI | | | | | | UNIT |
|--|--|---------|----------------|-------------------------|-------------|------------------|--------------------------|-------|-----|------|
| | | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{IO} Input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL031I | 25°C | 0.54 | 3.5 | | 0.5 | 1.5 | mV | |
| | | | Full range† | | 5.3 | | 3.3 | | | |
| | | TL031AI | 25°C | 0.41 | 2.8 | | 0.34 | 0.8 | | |
| | | | Full range† | | 4.6 | | 2.6 | | | |
| α _{V_{IO}} Temperature coefficient of input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL031I | 25°C to 85°C | 6.5 | | 6.2 | | μV/°C | | |
| | | TL031AI | 25°C to 85°C | 6.5 | | 6.2 | 25 | | | |
| Input offset voltage long-term drift‡ | V _O = 0, V _{IC} = 0, R _S = 50 Ω | | 25°C | 0.04 | | 0.04 | | μV/mo | | |
| I _{IO} Input offset current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 1 | 100 | 1 | 100 | pA | | |
| | | | 85°C | 0.02 | 0.45 | 0.02 | 0.45 | nA | | |
| I _{IB} Input bias current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 2 | 200 | 2 | 200 | pA | | |
| | | | 85°C | 0.2 | 0.9 | 0.2 | 0.9 | nA | | |
| V _{ICR} Common-mode input voltage range | | | 25°C | -1.5 to 4 | -3.4 to 5.4 | -11.5 to 14 | -13.4 to 15.4 | V | | |
| | | | Full range† | -1.5 to 4 | | -11.5 to 14 | | | | |
| V _{OM+} Maximum positive peak output voltage swing | R _L = 10 kΩ | | 25°C | 3 | 4.3 | 13 | 14 | V | | |
| | | | -40°C | 3 | 4.1 | 13 | 14 | | | |
| | | | 85°C | 3 | 4.4 | 13 | 14 | | | |
| V _{OM-} Maximum negative peak output voltage swing | R _L = 10 kΩ | | 25°C | -3 | -4.2 | -12.5 | -13.9 | V | | |
| | | | -40°C | -3 | -4.1 | -12.5 | -13.8 | | | |
| | | | 85°C | -3 | -4.2 | -12.5 | -14 | | | |
| A _{VD} Large-signal differential voltage amplification§ | R _L = 10 kΩ | | 25°C | 4 | 12 | 5 | 14.3 | V/mV | | |
| | | | -40°C | 3 | 8.4 | 4 | 11.6 | | | |
| | | | 85°C | 4 | 13.5 | 5 | 15.3 | | | |
| r _i Input resistance | | | 25°C | 10 ¹² | | 10 ¹² | | Ω | | |
| c _i Input capacitance | | | 25°C | 5 | | 4 | | pF | | |
| CMRR Common-mode rejection ratio | V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω | | 25°C | 70 | 87 | 75 | 94 | dB | | |
| | | | -40°C | 70 | 87 | 75 | 94 | | | |
| | | | 85°C | 70 | 87 | 75 | 94 | | | |
| k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO}) | V _O = 0, R _S = 50 Ω | | 25°C | 75 | 96 | 75 | 96 | dB | | |
| | | | -40°C | 75 | 96 | 75 | 96 | | | |
| | | | 85°C | 75 | 96 | 75 | 96 | | | |

† Full range is -40°C to 85°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V_{CC±} = ±5 V, V_O = ±2.3 V; at V_{CC±} = ±15 V, V_O = ±10 V



TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL031I and TL031AI electrical characteristics at specified free-air temperature (continued)

| PARAMETER | TEST CONDITIONS | T _A | TL031I, TL031AI | | | | | | UNIT |
|-----------------|-------------------------|-----------------------------|-------------------------|-----|-----|--------------------------|-----|-----|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| P _D | Total power dissipation | V _O = 0, No load | 25°C | 1.9 | 2.5 | 6.5 | 8.4 | mW | |
| | | | -40°C | 1.4 | 2.5 | 5.4 | 8.4 | | |
| | | | 85°C | 1.9 | 2.5 | 6.2 | 8.4 | | |
| I _{CC} | Supply current | V _O = 0, No load | 25°C | 192 | 250 | 217 | 280 | μA | |
| | | | -40°C | 144 | 250 | 181 | 280 | | |
| | | | 85°C | 189 | 250 | 207 | 280 | | |

TL031I and TL031AI operating characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | T _A | TL031I, TL031AI | | | | | | UNIT | | |
|------------------|-----------------------------------|--|---------------------------------------|-----------|-----|--------------------------|---------|-------|------|--------|--------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | | |
| SR ₊ | Positive slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | 2 | | | 1.5 2.9 | | | V/μs | |
| | | | -40°C | 1.6 | | | 1 2.1 | | | | |
| | | | 85°C | 2.3 | | | 1.5 3.3 | | | | |
| SR ₋ | Negative slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | 3.9 | | | 1.5 5.1 | | | V/μs | |
| | | | -40°C | 3.3 | | | 1.5 4.8 | | | | |
| | | | 85°C | 4.1 | | | 1.5 4.9 | | | | |
| t _r | Rise time | V _{I(PP)} = ±10 mV, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | 138 | | | 132 | | | ns | |
| | | | -40°C | 132 | | | 123 | | | | |
| | | | 85°C | 154 | | | 146 | | | | |
| t _f | Fall time | V _{I(PP)} = ±10 mV, R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | 138 | | | 132 | | | ns | |
| | | | -40°C | 132 | | | 123 | | | | |
| | | | 85°C | 154 | | | 146 | | | | |
| Overshoot factor | Overshoot factor | V _{I(PP)} = ±10 mV, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | 11% | | | 5% | | | | |
| | | | -40°C | 12% | | | 5% | | | | |
| | | | 85°C | 13% | | | 7% | | | | |
| V _n | Equivalent input noise voltage | TL031I | R _S = 20 Ω See Figure 3 | f = 10 Hz | 61 | | | 61 | | | nV/√Hz |
| | | | | f = 1 kHz | 41 | | | 41 | | | |
| | | TL031AI | | f = 10 Hz | 61 | | | 61 | | | |
| | | | | f = 1 kHz | 41 | | | 41 60 | | | |
| I _n | Equivalent input noise current | f = 1 kHz | 25°C | 0.003 | | | 0.003 | | | pA/√Hz | |
| B ₁ | Unity-gain bandwidth | V _I = 10 mV R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | 1 | | | 1.1 | | | MHz | |
| | | | -40°C | 1 | | | 1.1 | | | | |
| | | | 85°C | 0.9 | | | 1 | | | | |
| φ _m | Phase margin at unity gain | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | 61° | | | 65° | | | | |
| | | | -40°C | 60° | | | 65° | | | | |
| | | | 85°C | 60° | | | 64° | | | | |

† For V_{CC±} = ±5 V, V_{I(PP)} = ±1 V; for V_{CC±} = ±15 V, V_{I(PP)} = ±5 V



TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL031M and TL031AM electrical characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | | T _A | TL031M, TL031AM | | | | | | UNIT |
|--|--|---------|----------------|-------------------------|-------------|------------------|--------------------------|-------|-----|------|
| | | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{IO} Input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL031M | 25°C | 0.54 3.5 | | 0.5 1.5 | | mV | | |
| | | | Full range† | 6.5 | | 4.5 | | | | |
| | | TL031AM | 25°C | 0.41 2.8 | | 0.34 0.8 | | | | |
| | | | Full range† | 5.8 | | 3.8 | | | | |
| α _{V_{IO}} Temperature coefficient of input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL031M | 25°C to 125°C | 5.1 | | 4.3 | | μV/°C | | |
| | | TL031AM | 25°C to 125°C | 5.1 | | 4.3 | | | | |
| Input offset voltage long-term drift‡ | V _O = 0, V _{IC} = 0, R _S = 50 Ω | | 25°C | 0.04 | | 0.04 | | μV/mo | | |
| I _{IO} Input offset current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 1 100 | | 1 100 | | pA | | |
| | | | 125°C | 0.2 10 | | 0.2 10 | | nA | | |
| I _{IB} Input bias current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 2 200 | | 2 200 | | pA | | |
| | | | 125°C | 7 20 | | 8 20 | | nA | | |
| V _{ICR} Common-mode input voltage range | | | 25°C | -1.5 to 4 | -3.4 to 5.4 | -11.5 to 14 | -13.4 to 15.4 | V | | |
| | | | Full range† | -1.5 to 4 | | -11.5 to 14 | | | | |
| V _{OM+} Maximum positive peak output voltage swing | R _L = 10 kΩ | | 25°C | 3 4.3 | | 13 14 | | V | | |
| | | | -55°C | 3 4.1 | | 13 14 | | | | |
| | | | 125°C | 3 4.4 | | 13 14 | | | | |
| V _{OM-} Maximum negative peak output voltage swing | R _L = 10 kΩ | | 25°C | -3 -4.2 | | -12.5 -13.9 | | V | | |
| | | | -55°C | -3 -4 | | -12.5 -13.8 | | | | |
| | | | 125°C | -3 -4.3 | | -12.5 -14 | | | | |
| A _{VD} Large-signal differential voltage amplification§ | R _L = 10 kΩ | | 25°C | 4 12 | | 5 14.3 | | V/mV | | |
| | | | -55°C | 3 7.1 | | 4 10.4 | | | | |
| | | | 125°C | 3 12.9 | | 4 15 | | | | |
| r _i Input resistance | | | 25°C | 10 ¹² | | 10 ¹² | | Ω | | |
| c _i Input capacitance | | | 25°C | 5 | | 4 | | pF | | |
| CMRR Common-mode rejection ratio | V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω | | 25°C | 70 87 | | 75 94 | | dB | | |
| | | | -55°C | 70 87 | | 70 94 | | | | |
| | | | 125°C | 70 87 | | 70 94 | | | | |
| k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO}) | V _O = 0, R _S = 50 Ω | | 25°C | 75 96 | | 75 96 | | dB | | |
| | | | -55°C | 75 96 | | 75 95 | | | | |
| | | | 125°C | 75 96 | | 75 96 | | | | |
| P _D Total power dissipation | V _O = 0, No load | | 25°C | 1.9 2.5 | | 6.5 8.4 | | mW | | |
| | | | -55°C | 1.1 2.5 | | 4.7 8.4 | | | | |
| | | | 125°C | 1.8 2.5 | | 5.8 8.4 | | | | |

† Full range is -55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V_{CC±} = ±5 V, V_O = ±2.3 V; at V_{CC±} = ±15 V, V_O = ±10 V



TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL031M and TL031AM electrical characteristics at specified free-air temperature (continued)

| PARAMETER | TEST CONDITIONS | T _A | TL031M, TL031AM | | | | | | UNIT | |
|-----------------|-----------------|-----------------------------|-------------------------|-----|-----|--------------------------|-----|-----|------|----|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| I _{CC} | Supply current | V _O = 0, No load | 25°C | | 192 | 250 | | 217 | 280 | μA |
| | | | -55°C | | 114 | 250 | | 156 | 280 | |
| | | | 125°C | | 178 | 250 | | 197 | 280 | |

TL031M and TL031AM operating characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | T _A | TL031M, TL031AM | | | | | | UNIT |
|------------------|-----------------------------------|--|---------------------------------------|-----------|-------|--------------------------|-------|--------|--------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR ₊ | Positive slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 2 | | 1.5 | 2.9 | V/μs |
| | | | -55°C | | 1.4 | | 1 | 1.9 | |
| | | | 125°C | | 2.4 | | 1 | 3.5 | |
| SR ₋ | Negative slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 3.9 | | 1.5 | 5.1 | V/μs |
| | | | -55°C | | 3.2 | | 1 | 4.6 | |
| | | | 125°C | | 4.1 | | 1 | 4.7 | |
| t _r | Rise time | V _{I(PP)} = ±10 mV, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 138 | | 132 | ns | |
| | | | -55°C | | 142 | | 123 | | |
| | | | 125°C | | 166 | | 158 | | |
| t _f | Fall time | V _{I(PP)} = ±10 mV, R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 138 | | 132 | ns | |
| | | | -55°C | | 142 | | 123 | | |
| | | | 125°C | | 166 | | 158 | | |
| Overshoot factor | | V _{I(PP)} = ±10 mV, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 11% | | 5% | | |
| | | | -55°C | | 16% | | 6% | | |
| | | | 125°C | | 14% | | 8% | | |
| V _n | Equivalent input noise voltage | TL031M | R _S = 20 Ω See Figure 3 | f = 10 Hz | 25°C | | 61 | 61 | nV/√Hz |
| | | | | f = 1 kHz | | 41 | 41 | | |
| | | TL031AM | | f = 10 Hz | 25°C | | 61 | 61 | |
| | | | | f = 1 kHz | | 41 | 41 | | |
| I _n | Equivalent input noise current | f = 1 kHz | 25°C | | 0.003 | | 0.003 | pA/√Hz | |
| B ₁ | Unity-gain bandwidth | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 1 | | 1.1 | MHz | |
| | | | -55°C | | 1 | | 1.1 | | |
| | | | 125°C | | 0.9 | | 0.9 | | |
| φ _m | Phase margin at unity gain | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 61° | | 65° | | |
| | | | -55°C | | 57° | | 64° | | |
| | | | 125°C | | 59° | | 62° | | |

† For V_{CC±} = ±5 V, V_{I(PP)} = ±1 V; for V_{CC±} = ±15 V, V_{I(PP)} = ±5 V



TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL032C and TL032AC electrical characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | | T _A | TL032C, TL032AC | | | | | | UNIT |
|--|--|---------------------|----------------|-------------------------|-------------|------------------|--------------------------|-------|-----|------|
| | | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{IO} Input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL032C | 25°C | 0.69 3.5 | | 0.57 1.5 | | mV | | |
| | | | Full range† | 4.5 | | 2.5 | | | | |
| | | TL032AC | 25°C | 0.53 2.8 | | 0.39 0.8 | | | | |
| | | | Full range† | 3.8 | | 1.8 | | | | |
| α _{V_{IO}} Temperature coefficient of input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL032C | 25°C to 70°C | 11.5 | | 10.8 | | μV/°C | | |
| | | TL032AC | 25°C to 70°C | 11.5 | | 10.8 25 | | | | |
| Input offset voltage long-term drift‡ | V _O = 0, V _{IC} = 0, R _S = 50 Ω | | 25°C | 0.04 | | 0.04 | | μV/mo | | |
| I _{IO} Input offset current | V _O = 0, See Figure 5 | V _{IC} = 0 | 25°C | 1 100 | | 1 100 | | pA | | |
| | | | 70°C | 9 200 | | 12 200 | | | | |
| I _{IB} Input bias current | V _O = 0, See Figure 5 | V _{IC} = 0 | 25°C | 2 200 | | 2 200 | | pA | | |
| | | | 70°C | 50 400 | | 80 400 | | | | |
| V _{ICR} Common-mode input voltage range | | | 25°C | -1.5 to 4 | -3.4 to 5.4 | -11.5 to 14 | -13.4 to 15.4 | V | | |
| | | | Full range† | -1.5 to 4 | | -11.5 to 14 | | | | |
| V _{OM+} Maximum positive peak output voltage swing | R _L = 10 kΩ | | 25°C | 3 4.3 | | 13 14 | | V | | |
| | | | 0°C | 3 4.2 | | 13 14 | | | | |
| | | | 70°C | 3 4.3 | | 13 14 | | | | |
| V _{OM-} Maximum negative peak output voltage swing | R _L = 10 kΩ | | 25°C | -3 -4.2 | | -12.5 -13.9 | | V | | |
| | | | 0°C | -3 -4.1 | | -12.5 -13.9 | | | | |
| | | | 70°C | -3 -4.2 | | -12.5 -14 | | | | |
| A _{VD} Large-signal differential voltage amplification§ | R _L = 10 kΩ | | 25°C | 4 12 | | 5 14.3 | | V/mV | | |
| | | | 0°C | 3 11.1 | | 4 13.5 | | | | |
| | | | 70°C | 4 13.3 | | 5 15.2 | | | | |
| r _i Input resistance | | | 25°C | 10 ¹² | | 10 ¹² | | Ω | | |
| c _i Input capacitance | | | 25°C | 5 | | 14 | | pF | | |
| CMRR Common-mode rejection ratio | V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω | | 25°C | 70 87 | | 75 94 | | dB | | |
| | | | 0°C | 70 87 | | 75 94 | | | | |
| | | | 70°C | 70 87 | | 75 94 | | | | |
| k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO}) | V _{CC±} = ±5 V to ±15 V, V _O = 0, R _S = 50 Ω | | 25°C | 75 96 | | 75 96 | | dB | | |
| | | | 0°C | 75 96 | | 75 96 | | | | |
| | | | 70°C | 75 96 | | 75 96 | | | | |

† Full range is 0°C to 70°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V_{CC±} = ±5 V, V_O = 2.3 V; at V_{CC±} = ±15 V, V_O = ±10 V



TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL032C and TL032AC electrical characteristics at specified free-air temperature (continued)

| PARAMETER | TEST CONDITIONS | T _A | TL032C, TL032AC | | | | | | UNIT |
|---|-----------------------------|----------------|-------------------------|-----|-----|--------------------------|------|-----|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| P _D Total power dissipation (two amplifiers) | V _O = 0, No load | 25°C | | 3.8 | 5 | | 13 | 17 | mW |
| | | 0°C | | 3.7 | 5 | | 12.7 | 17 | |
| | | 70°C | | 3.8 | 5 | | 12.6 | 17 | |
| I _{CC} Supply current (two amplifiers) | V _O = 0, No load | 0°C | | 368 | 500 | | 422 | 560 | μA |
| | | 70°C | | 378 | 500 | | 420 | 560 | |
| V _{O1} /V _{O2} Crosstalk attenuation | A _{VD} = 100 dB | 25°C | | 120 | | | 120 | | dB |

TL032C and TL032AC operating characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | T _A | TL032C, TL032AC | | | | | | UNIT |
|---|---|---------------------------------------|-------------------------|-------|-----|--------------------------|--------|--------|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR ₊ Positive slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 1.2 | | 1.5 | 2.9 | V/μs | |
| | | 0°C | | 1.8 | | 1 | 2.6 | | |
| | | 70°C | | 2.2 | | 1.5 | 3.2 | | |
| SR ₋ Negative slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 3.9 | | 1.5 | 5.1 | V/μs | |
| | | 0°C | | 3.7 | | 1.5 | 5 | | |
| | | 70°C | | 4 | | 1.5 | 5 | | |
| t _r Rise time | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 138 | | 132 | ns | | |
| | | 0°C | | 134 | | 127 | | | |
| | | 70°C | | 150 | | 142 | | | |
| t _f Fall time | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 138 | | 132 | ns | | |
| | | 0°C | | 134 | | 127 | | | |
| | | 70°C | | 150 | | 142 | | | |
| Overshoot factor | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 11% | | 5% | | | |
| | | 0°C | | 10% | | 4% | | | |
| | | 70°C | | 12% | | 6% | | | |
| V _n Equivalent input noise voltage | TL032C | R _S = 20 Ω See Figure 3 | f = 10 Hz | | | 49 | | nV/√Hz | |
| | | | f = 1 kHz | | | 41 | | | |
| | TL032AC | f = 10 Hz | | | 49 | | 49 | | |
| | | f = 1 kHz | | | 41 | | 41 60 | | |
| I _n Equivalent input noise current | f = 1 kHz | 25°C | | 0.003 | | 0.003 | pA/√Hz | | |
| B ₁ Unity-gain bandwidth | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 1 | | 1.1 | MHz | | |
| | | 0°C | | 1 | | 1.1 | | | |
| | | 70°C | | 1 | | 1 | | | |
| φ _m Phase margin at unity gain | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 61° | | 65° | | | |
| | | 0°C | | 61° | | 65° | | | |
| | | 70°C | | 60° | | 64° | | | |

† For V_{CC±} = ±5 V, V_{I(PP)} = ±1 V; for V_{CC±} = ±15 V, V_{I(PP)} = ±5 V

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL032I and TL032AI electrical characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | | T _A | TL032I, TL032AI | | | | | | UNIT |
|--|--|---------------------|----------------|-------------------------|-------------|------------------|--------------------------|---------------|------|------|
| | | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{IO} Input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL032I | 25°C | 0.69 | 3.5 | | 0.57 | 1.5 | mV | |
| | | | Full range† | | | 5.3 | | 3.3 | | |
| | | TL032AI | 25°C | 0.53 | 2.8 | | 0.39 | 0.8 | | |
| | | | Full range† | | | 4.6 | | 2.6 | | |
| α _{V_{IO}} Temperature coefficient of input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL032I | 25°C to 85°C | 11.4 | | 10.8 | | μV/°C | | |
| | | TL032AI | 25°C to 85°C | 11.4 | | 10.8 | 25 | | | |
| Input offset voltage long-term drift‡ | V _O = 0, V _{IC} = 0, R _S = 50 Ω | | 25°C | 0.04 | | 0.04 | | μV/mo | | |
| I _{IO} Input offset current | V _O = 0, See Figure 5 | V _{IC} = 0 | 25°C | 1 | 100 | | 1 | 100 | pA | |
| | | | 85°C | 0.02 | 0.45 | | 0.02 | 0.45 | nA | |
| I _{IB} Input bias current | V _O = 0, See Figure 5 | V _{IC} = 0 | 25°C | 2 | 200 | | 2 | 200 | pA | |
| | | | 85°C | 0.2 | 0.9 | | 0.3 | 0.9 | nA | |
| V _{ICR} Common-mode input voltage range | | | 25°C | -1.5 to 4 | -3.4 to 5.4 | | -11.5 to 14 | -13.4 to 15.4 | V | |
| | | | Full range† | -1.5 to 4 | | | -11.5 to 14 | | | |
| V _{OM+} Maximum positive peak output voltage swing | R _L = 10 kΩ | | 25°C | 3 | 4.3 | | 13 | 14 | V | |
| | | | -40°C | 3 | 4.2 | | 13 | 14 | | |
| | | | 85°C | 3 | 4.4 | | 13 | 14 | | |
| V _{OM-} Maximum negative peak output voltage swing | R _L = 10 kΩ | | 25°C | -3 | -4.2 | | -12.5 | -13.9 | V | |
| | | | -40°C | -3 | -4.1 | | -12.5 | -13.8 | | |
| | | | 85°C | -3 | -4.2 | | -12.5 | -14 | | |
| A _{VD} Large-signal differential voltage amplification§ | R _L = 10 kΩ | | -40°C | 3 | 8.4 | | 4 | 11.6 | V/mV | |
| | | | 85°C | 4 | 13.5 | | 5 | 15.3 | | |
| r _i Input resistance | | | 25°C | 10 ¹² | | 10 ¹² | | Ω | | |
| c _i Input capacitance | | | 25°C | 5 | | 4 | | pF | | |
| CMRR Common-mode rejection ratio | V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω | | 25°C | 70 | 87 | | 75 | 94 | dB | |
| | | | -40°C | 70 | 87 | | 75 | 94 | | |
| | | | 85°C | 70 | 87 | | 75 | 94 | | |
| k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO}) | V _{CC±} = ±5 V to ±15 V, V _O = 0, R _S = 50 Ω | | 25°C | 75 | 96 | | 75 | 96 | dB | |
| | | | -40°C | 75 | 96 | | 75 | 96 | | |
| | | | 85°C | 75 | 96 | | 75 | 96 | | |

† Full range is -40°C to 85°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V_{CC±} = ±5 V, V_O = 2.3 V; at V_{CC±} = ±15 V, V_O = ±10 V



TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL032I and TL032AI electrical characteristics at specified free-air temperature (continued)

| PARAMETER | TEST CONDITIONS | T _A | TL032I, TL032AI | | | | | | UNIT |
|---|-----------------------------|----------------|-------------------------|-----|-----|--------------------------|------|-----|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| P _D Total power dissipation (two amplifiers) | V _O = 0, No load | 25°C | | 3.8 | 5 | | 13 | 17 | mW |
| | | -40°C | | 2.9 | 5 | | 10.9 | 17 | |
| | | 85°C | | 3.7 | 5 | | 12.4 | 17 | |
| I _{CC} Supply current (two amplifiers) | V _O = 0, No load | 25°C | | 384 | 500 | | 434 | 560 | μA |
| | | -40°C | | 288 | 500 | | 362 | 560 | |
| | | 85°C | | 372 | 500 | | 414 | 560 | |
| V _{O1} /V _{O2} Crosstalk attenuation | A _{VD} = 100 dB | 25°C | | 120 | | | 120 | | dB |

TL032I and TL032AI operating characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | T _A | TL032I, TL032AI | | | | | | UNIT |
|---|---|----------------|-------------------------|-------|-----|--------------------------|--------|--------|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR ₊ Positive slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF | 25°C | | 2 | | 1.5 | 2.9 | V/μs | |
| | | -40°C | | 1.6 | | 1 | 2.1 | | |
| | | 85°C | | 2.3 | | 1.5 | 3.3 | | |
| SR ₋ Negative slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF | 25°C | | 3.9 | | 1.5 | 5.1 | V/μs | |
| | | -40°C | | 3.3 | | 1.5 | 4.8 | | |
| | | 85°C | | 4.1 | | 1.5 | 4.9 | | |
| t _r Rise time | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 138 | | 132 | | ns | |
| | | -40°C | | 132 | | 123 | | | |
| | | 85°C | | 154 | | 146 | | | |
| t _f Fall time | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 138 | | 132 | | ns | |
| | | -40°C | | 132 | | 123 | | | |
| | | 85°C | | 154 | | 146 | | | |
| Overshoot factor | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 11% | | 5% | | | |
| | | -40°C | | 12% | | 5% | | | |
| | | 85°C | | 13% | | 7% | | | |
| V _n Equivalent input noise voltage | TL032I R _S = 20 Ω See Figure 3 | 25°C | f = 10 Hz | | 49 | | 49 | nV/√Hz | |
| | | | f = 1 kHz | | 41 | | 41 | | |
| | | 25°C | f = 10 Hz | | 49 | | 49 | | |
| | | | f = 1 kHz | | 41 | | 41 60 | | |
| I _n Equivalent input noise current | f = 1 kHz | 25°C | | 0.003 | | 0.003 | pA/√Hz | | |
| B ₁ Unity-gain bandwidth | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 1 | | 1.1 | MHz | | |
| | | -40°C | | 1 | | 1.1 | | | |
| | | 85°C | | 0.9 | | 1 | | | |
| φ _m Phase margin at unity gain | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 61° | | 65° | | | |
| | | -40°C | | 61° | | 65° | | | |
| | | 85°C | | 60° | | 64° | | | |

† For V_{CC±} = ±5 V, V_{I(PP)} = ±1 V; for V_{CC±} = ±15 V, V_{I(PP)} = ±5 V



TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL032M and TL032AM electrical characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | | T _A | TL032M, TL032AM | | | | | | UNIT |
|--|--|-------------|----------------|-------------------------|-------------|-----|--------------------------|---------------|-------|------|
| | | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{IO} Input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL032M | 25°C | 0.69 | 3.5 | | 0.57 | 1.5 | mV | |
| | | | Full range† | | 6.5 | | 4.5 | | | |
| | | TL032AM | 25°C | 0.53 | 2.8 | | 0.39 | 0.8 | | |
| | | | Full range† | | 5.8 | | 3.8 | | | |
| α _{V_{IO}} Temperature coefficient of input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL032M | 25°C to 125°C | 9.7 | | | 9.7 | | μV/°C | |
| | | TL032AM | 25°C to 125°C | 9.7 | | | 9.7 | | | |
| Input offset voltage long-term drift‡ | V _O = 0, V _{IC} = 0, R _S = 50 Ω | | 25°C | 0.04 | | | 0.04 | | μV/mo | |
| I _{IO} Input offset current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 1 | 100 | | 1 | 100 | pA | |
| | | | 125°C | 0.2 | 10 | | 0.2 | 10 | nA | |
| I _{IB} Input bias current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 2 | 200 | | 2 | 200 | pA | |
| | | | 125°C | 7 | 20 | | 8 | 20 | nA | |
| V _{ICR} Common-mode input voltage range | | | 25°C | -1.5 to 4 | -3.4 to 5.4 | | -11.5 to 14 | -13.4 to 15.4 | V | |
| | | Full range† | | -1.5 to 4 | | | -11.5 to 14 | | | |
| V _{OM+} Maximum positive peak output voltage swing | R _L = 10 kΩ | | 25°C | 3 | 4.3 | | 13 | 14 | V | |
| | | | -55°C | 3 | 4.1 | | 13 | 14 | | |
| | | | 125°C | 3 | 4.4 | | 13 | 14 | | |
| V _{OM-} Maximum negative peak output voltage swing | R _L = 10 kΩ | | 25°C | -3 | -4.2 | | -12.5 | -13.9 | V | |
| | | | -55°C | -3 | -4 | | -12.5 | -13.8 | | |
| | | | 125°C | -3 | -4.3 | | -12.5 | -14 | | |
| A _{VD} Large-signal differential voltage amplification§ | R _L = 10 kΩ | | 25°C | 4 | 12 | | 5 | 14.3 | V/mV | |
| | | | -55°C | 3 | 7.1 | | 4 | 10.4 | | |
| | | | 125°C | 3 | 12.9 | | 4 | 15 | | |
| r _i Input resistance | | | 25°C | 10 ¹² | | | 10 ¹² | | Ω | |
| c _i Input capacitance | | | 25°C | 5 | | | 4 | | pF | |
| CMRR Common-mode rejection ratio | V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω | | 25°C | 70 | 87 | | 75 | 94 | dB | |
| | | | -55°C | 70 | 87 | | 70 | 94 | | |
| | | | 125°C | 70 | 87 | | 70 | 94 | | |
| k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO}) | V _{CC±} = ±5 V to ±15 V, V _O = 0, R _S = 50 Ω | | 25°C | 75 | 96 | | 75 | 96 | dB | |
| | | | -55°C | 75 | 95 | | 75 | 95 | | |
| | | | 125°C | 75 | 96 | | 75 | 96 | | |

† Full range is -55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V_{CC±} = ±5 V, V_O = 2.3 V; at V_{CC±} = ±15 V, V_O = ±10 V



TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL032M and TL032AM electrical characteristics at specified free-air temperature (continued)

| PARAMETER | TEST CONDITIONS | T _A | TL032M, TL032AM | | | | | | UNIT |
|--|-----------------------------|----------------|-------------------------|-----|-----|--------------------------|------|-----|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| P _D Total power dissipation (two amplifiers) V _O = 0, | V _O = 0, No load | 25°C | | 3.8 | 5 | | 13 | 17 | mW |
| | | -55°C | | 2.3 | 5 | | 9.4 | 17 | |
| | | 125°C | | 3.6 | 5 | | 11.8 | 17 | |
| I _{CC} Supply current (two amplifiers) | V _O = 0, No load | 25°C | | 384 | 500 | | 434 | 560 | μA |
| | | -55°C | | 228 | 500 | | 312 | 560 | |
| | | 125°C | | 356 | 500 | | 394 | 560 | |
| V _{O1} /V _{O2} Crosstalk attenuation | A _{VD} = 100 dB | 25°C | | 120 | | | 120 | | dB |

TL032M and TL032AM operating characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | T _A | TL032M, TL032AM | | | | | | UNIT |
|---|---|----------------|-------------------------|-------|-----|--------------------------|--------|--------|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR ₊ Positive slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See and Figure 1 | 25°C | | 2 | | 1.5 | 2.9 | V/μs | |
| | | -55°C | | 1.4 | | 1 | 1.9 | | |
| | | 125°C | | 2.4 | | 1 | 3.5 | | |
| SR ₋ Negative slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See and Figure 1 | 25°C | | 3.9 | | 1.5 | 5.1 | V/μs | |
| | | -55°C | | 3.2 | | 1 | 4.6 | | |
| | | 125°C | | 4.1 | | 1 | 4.7 | | |
| t _r Rise time | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 138 | | 132 | ns | | |
| | | -55°C | | 142 | | 123 | | | |
| | | 125°C | | 166 | | 58 | | | |
| t _f Fall time | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 138 | | 132 | ns | | |
| | | -55°C | | 142 | | 123 | | | |
| | | 125°C | | 166 | | 158 | | | |
| Overshoot factor | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 11% | | 5% | | | |
| | | -55°C | | 16% | | 6% | | | |
| | | 125°C | | 14% | | 8% | | | |
| V _n Equivalent input noise voltage | TL032M R _S = 20 Ω See Figure 3 | 25°C | f = 10 Hz | | 49 | | 49 | nV/√Hz | |
| | | | f = 1 kHz | | 41 | | 41 | | |
| | | 25°C | f = 10 Hz | | 49 | | 49 | | |
| | | | f = 1 kHz | | 41 | | 41 | | |
| I _n Equivalent input noise current | f = 1 kHz | 25°C | | 0.003 | | 0.003 | pA/√Hz | | |
| B1 Unity-gain bandwidth | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 1 | | 1.1 | MHz | | |
| | | -55°C | | 1 | | 1.1 | | | |
| | | 125°C | | 0.9 | | 0.9 | | | |
| φ _m Phase margin at unity gain | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 61° | | 65° | | | |
| | | -55°C | | 57° | | 64° | | | |
| | | 125°C | | 59° | | 62° | | | |

† For V_{CC±} = ±5 V, V_{I(PP)} = ±1 V; for V_{CC±} = ±15 V, V_{I(PP)} = ±5 V



TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL034C and TL034AC electrical characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | T _A | TL034C, TL034AC | | | | | | UNIT |
|--|---|----------------|-------------------------|------------------|-------------|--------------------------|-------------|---------------|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{IO} Input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL034C | 25°C | 0.91 | 6 | | 0.79 | 4 | mV |
| | | | Full range† | | | 8.2 | | 6.2 | |
| | | TL034AC | 25°C | 0.7 | 3.5 | | 0.58 | 1.5 | |
| | | | Full range† | | | 5.7 | | 3.7 | |
| α _{V_{IO}} Temperature coefficient of input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL034C | 25°C to 70°C | 11.6 | | 12 | | μV/°C | |
| | | TL034AC | 25°C to 70°C | 11.6 | | 12 | 25 | | |
| Input offset voltage long-term drift‡ | V _O = 0, V _{IC} = 0, R _S = 50 Ω | | 25°C | 0.04 | | 0.04 | | μV/mo | |
| I _{IO} Input offset current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 1 | 100 | | 1 | 100 | pA |
| | | | 70°C | 9 | 200 | | 12 | 200 | |
| I _{IB} Input bias current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 2 | 200 | | 2 | 200 | pA |
| | | | 70°C | 50 | 400 | | 80 | 400 | |
| V _{ICR} Common-mode input voltage range | | | 25°C | -1.5 to 4 | -3.4 to 5.4 | | -11.5 to 14 | -13.4 to 15.4 | V |
| | | | Full range† | -1.5 to 4 | | | -11.5 to 14 | | |
| V _{OM+} Maximum positive peak output voltage swing | R _L = 10 kΩ | | 25°C | 3 | 4.3 | | 13 | 14 | V |
| | | | 0°C | 3 | 4.2 | | 13 | 14 | |
| | | | 70°C | 3 | 4.3 | | 13 | 14 | |
| V _{OM-} Maximum negative peak output voltage swing | R _L = 10 kΩ | | 25°C | -3 | -4.2 | | -12.5 | -13.9 | V |
| | | | 0°C | -3 | -4.1 | | -12.5 | -13.9 | |
| | | | 70°C | -3 | -4.2 | | -12.5 | -14 | |
| A _{VD} Large-signal differential voltage amplification§ | R _L = 10 kΩ | | 25°C | 4 | 12 | | 5 | 14.3 | V/mV |
| | | | 0°C | 3 | 11.1 | | 4 | 13.5 | |
| | | | 70°C | 4 | 13.3 | | 5 | 15.2 | |
| r _i Input resistance | | | 25°C | 10 ¹² | | 10 ¹² | | Ω | |
| c _i Input capacitance | | | 25°C | 5 | | 14 | | pF | |
| CMRR Common-mode rejection ratio | V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω | | 25°C | 70 | 87 | | 75 | 94 | dB |
| | | | 0°C | 70 | 87 | | 75 | 94 | |
| | | | 70°C | 70 | 87 | | 75 | 94 | |
| k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO}) | V _O = 0, R _S = 50 Ω | | 25°C | 75 | 96 | | 75 | 96 | dB |
| | | | 0°C | 75 | 96 | | 75 | 96 | |
| | | | 70°C | 75 | 96 | | 75 | 96 | |

† Full range is 0°C to 70°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V_{CC±} = ±5 V, V_O = ±2.3 V; at V_{CC±} = ±15 V, V_O = ±10 V



TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL034C and TL034AC electrical characteristics at specified free-air temperature (continued)

| PARAMETER | TEST CONDITIONS | T _A | TL034C, TL034AC | | | | | | UNIT |
|----------------------------------|--|-----------------------------|-------------------------|------|-----|--------------------------|------|------|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| P _D | Total power dissipation (two amplifiers) | V _O = 0, No load | 25°C | 7.7 | 10 | | 26 | 34 | mW |
| | | | 0°C | 7.4 | 10 | | 25.3 | 34 | |
| | | | 70°C | 7.6 | 10 | | 25.2 | 34 | |
| I _{CC} | Supply current (four amplifiers) | V _O = 0, No load | 25°C | 0.77 | 1 | | 0.87 | 1.12 | mA |
| | | | 0°C | 0.74 | 1 | | 0.85 | 1.12 | |
| | | | 70°C | 0.76 | 1 | | 0.84 | 1.12 | |
| V _{O1} /V _{O2} | Crosstalk attenuation | A _{VD} = 100 | 25°C | 120 | | | 120 | | dB |

TL034C and TL034AC operating characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | T _A | TL034C, TL034AC | | | | | | UNIT | |
|------------------|-----------------------------------|---|---------------------------------------|-----------|-----|--------------------------|---------|-----|--------|--------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| SR ₊ | Positive slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | 2 | | | 1.5 2.9 | | V/μs | |
| | | | 0°C | 1.8 | | | 1 2.6 | | | |
| | | | 70°C | 2.2 | | | 1.5 3.2 | | | |
| SR ₋ | Negative slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | 3.9 | | | 1.5 5.1 | | V/μs | |
| | | | 0°C | 3.7 | | | 1.5 5 | | | |
| | | | 70°C | 4 | | | 1.5 5 | | | |
| t _r | Rise time | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | 138 | | | 132 | | ns | |
| | | | 0°C | 134 | | | 127 | | | |
| | | | 70°C | 150 | | | 142 | | | |
| t _f | Fall time | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | 138 | | | 132 | | ns | |
| | | | 0°C | 134 | | | 127 | | | |
| | | | 70°C | 150 | | | 142 | | | |
| Overshoot factor | | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | 11% | | | 5% | | | |
| | | | 0°C | 10% | | | 4% | | | |
| | | | 70°C | 12% | | | 6% | | | |
| V _n | Equivalent input noise voltage | TL034C | R _S = 20 Ω See Figure 3 | f = 10 Hz | 83 | | | 83 | | nV/√Hz |
| | | | | f = 1 kHz | 43 | | | 43 | | |
| | | TL034AC | f = 10 Hz | 83 | | | 83 | | | |
| | | | f = 1 kHz | 43 | | | 43 60 | | | |
| I _n | Equivalent input noise current | f = 1 kHz | 25°C | 0.003 | | | 0.003 | | pA/√Hz | |
| B ₁ | Unity-gain bandwidth | V _I = 10 mV R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | 1 | | | 1.1 | | MHz | |
| | | | 0°C | 1 | | | 1.1 | | | |
| | | | 70°C | 1 | | | 1 | | | |
| φ _m | Phase margin at unity gain | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | 61° | | | 65° | | | |
| | | | 0°C | 61° | | | 65° | | | |
| | | | 70°C | 60° | | | 64° | | | |

† For V_{CC±} = ±5 V, V_{I(PP)} = ±1 V; for V_{CC±} = ±15 V, V_{I(PP)} = ±5 V



TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL034I and TL034AI electrical characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | | T _A | TL034I, TL034AI | | | | | | UNIT |
|--|---|---------|----------------|-------------------------|------------------|------|--------------------------|---------------|-------|------|
| | | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{IO} Input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL034I | 25°C | 0.91 | 3.6 | | 0.79 | 4 | mV | |
| | | | Full range† | | | 9.3 | | 7.3 | | |
| | | TL034AI | 25°C | | 0.7 | 3.5 | | 0.58 | | 1.5 |
| | | | Full range† | | | 6.8 | | 4.8 | | |
| α _{V_{IO}} Temperature coefficient of input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL034I | 25°C to 85°C | | 11.5 | | 11.6 | | μV/°C | |
| | | TL034AI | 25°C to 85°C | | 11.5 | | 11.6 | 25 | | |
| Input offset voltage long-term drift‡ | V _O = 0, V _{IC} = 0, R _S = 50 Ω | | 25°C | | 0.04 | | 0.04 | | μV/mo | |
| I _{IO} Input offset current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | | 1 | 100 | 1 | 100 | pA | |
| | | | 85°C | | 0.02 | 0.45 | 0.02 | 0.45 | nA | |
| I _{IB} Input bias current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | | 2 | 200 | 2 | 200 | pA | |
| | | | 85°C | | 0.2 | 0.9 | 0.3 | 0.9 | nA | |
| V _{ICR} Common-mode input voltage range | | | 25°C | -1.5 to 4 | -3.4 to 5.4 | | -11.5 to 14 | -13.4 to 15.4 | V | |
| | | | Full range† | -1.5 to 4 | | | -11.5 to 14 | | | |
| V _{OM+} Maximum positive peak output voltage swing | R _L = 10 kΩ | | 25°C | 3 | 4.3 | | 13 | 14 | V | |
| | | | -40°C | 3 | 4.1 | | 13 | 14 | | |
| | | | 85°C | 3 | 4.4 | | 13 | 14 | | |
| V _{OM-} Maximum negative peak output voltage swing | R _L = 10 kΩ | | 25°C | -3 | -4.2 | | -12.5 | -13.9 | V | |
| | | | -40°C | -3 | -4.1 | | -12.5 | -13.8 | | |
| | | | 85°C | -3 | -4.2 | | -12.5 | -14 | | |
| A _{VD} Large-signal differential voltage amplification§ | R _L = 10 kΩ | | -40°C | 4 | 12 | | 5 | 14.3 | V/mV | |
| | | | 85°C | 3 | 8.4 | | 4 | 11.6 | | |
| r _i Input resistance | | | 25°C | | 10 ¹² | | 10 ¹² | Ω | | |
| c _i Input capacitance | | | 25°C | | 5 | | 4 | pF | | |
| CMRR Common-mode rejection ratio | V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω | | 25°C | 70 | 87 | | 75 | 94 | dB | |
| | | | -40°C | 70 | 87 | | 75 | 94 | | |
| | | | 85°C | 70 | 87 | | 75 | 94 | | |
| k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO}) | V _O = 0, R _S = 50 Ω | | 25°C | 75 | 96 | | 75 | 96 | dB | |
| | | | -40°C | 75 | 96 | | 75 | 96 | | |
| | | | 85°C | 75 | 96 | | 75 | 96 | | |

† Full range is -40°C to 85°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V_{CC±} = ±5 V, V_O = ±2.3 V; at V_{CC±} = ±15 V, V_O = ±10 V



TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL034I and TL034AI electrical characteristics at specified free-air temperature (continued)

| PARAMETER | TEST CONDITIONS | T _A | TL034I, TL034AI | | | | | | UNIT |
|----------------------------------|--|-----------------------|-------------------------|------|-----|--------------------------|------|------|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| P _D | Total power dissipation (four amplifiers) V _O = 0, No load | 25°C | | 7.7 | 10 | | 26 | 34 | mW |
| | | -40°C | | 5.8 | 10 | | 21.7 | 34 | |
| | | 85°C | | 7.4 | 10 | | 24.8 | 34 | |
| I _{CC} | Supply current (four amplifiers) V _O = 0, No load | 25°C | | 0.77 | 1 | | 0.87 | 1.12 | mA |
| | | -40°C | | 0.58 | 1 | | 0.72 | 1.12 | |
| | | 85°C | | 0.74 | 1 | | 0.83 | 1.12 | |
| V _{O1} /V _{O2} | Crosstalk attenuation | A _{VD} = 100 | 25°C | | 120 | | 120 | | dB |

TL034I and TL034AI operating characteristics

| PARAMETER | TEST CONDITIONS | T _A | TL034I, TL034AI | | | | | | UNIT |
|------------------|---|---------------------------------------|-------------------------|------|-------|--------------------------|-------|--------|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| SR ₊ | Positive slew rate at unity gain† R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 2 | | 1.5 | 2.9 | V/μs | |
| | | -40°C | | 1.6 | | 1 | 2.1 | | |
| | | 85°C | | 2.3 | | 1.5 | 3.3 | | |
| SR ₋ | Negative slew rate at unity gain† R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | | 3.9 | | 1.5 | 5.1 | V/μs | |
| | | -40°C | | 3.3 | | 1.5 | 4.8 | | |
| | | 85°C | | 4.1 | | 1.5 | 4.9 | | |
| t _r | Rise time V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 138 | | 132 | ns | | |
| | | -40°C | | 132 | | 123 | | | |
| | | 85°C | | 154 | | 146 | | | |
| t _f | Fall time V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 138 | | 132 | ns | | |
| | | -40°C | | 132 | | 123 | | | |
| | | 85°C | | 154 | | 146 | | | |
| Overshoot factor | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | | 11% | | 5% | | | |
| | | -40°C | | 12% | | 5% | | | |
| | | 85°C | | 13% | | 7% | | | |
| V _n | Equivalent input noise voltage TL034I TL034AI | R _S = 20 Ω See Figure 3 | f = 10 Hz | 25°C | | 83 | | nV/√Hz | |
| | | | f = 1 kHz | 25°C | | 43 | | | 43 |
| | | f = 10 Hz | 25°C | | 83 | | 83 | | |
| | | | f = 1 kHz | 25°C | | 43 | | | 43 |
| I _n | Equivalent input noise current | f = 1 kHz | 25°C | | 0.003 | | 0.003 | pA/√Hz | |
| B ₁ | Unity-gain bandwidth V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 1 | | 1.1 | MHz | | |
| | | -40°C | | 1 | | 1.1 | | | |
| | | 85°C | | 0.9 | | 1 | | | |
| φ _m | Phase margin at unity gain V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | | 61° | | 65° | | | |
| | | -40°C | | 61° | | 65° | | | |
| | | 85°C | | 60° | | 64° | | | |

† For V_{CC±} = ±5 V, V_{I(PP)} = ±1 V; for V_{CC±} = ±15 V, V_{I(PP)} = ±5 V



TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL034M and TL034AM electrical characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | | T _A | TL034M, TL034AM | | | | | | UNIT |
|--|--|---------|----------------|-------------------------|-------------|-----|--------------------------|---------------|-------|------|
| | | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| V _{IO} Input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL034M | 25°C | 0.91 | 3.6 | | 0.78 | 4 | mV | |
| | | | Full range† | | 11 | | | 9 | | |
| | | TL034AM | 25°C | 0.7 | 3.5 | | 0.58 | 1.5 | | |
| | | | Full range† | | 8.5 | | | 6.5 | | |
| α _{V_{IO}} Temperature coefficient of input offset voltage | V _O = 0, V _{IC} = 0, R _S = 50 Ω | TL034M | 25°C to 125°C | 10.6 | | | 10.9 | | μV/°C | |
| | | TL034AM | 25°C to 125°C | 10.6 | | | 10.9 | | | |
| Input offset voltage long-term drift‡ | V _O = 0, V _{IC} = 0, R _S = 50 Ω | | 25°C | 0.04 | | | 0.04 | | μV/mo | |
| I _{IO} Input offset current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 1 | 100 | | 1 | 100 | pA | |
| | | | 125°C | 0.2 | 10 | | 0.2 | 10 | nA | |
| I _{IB} Input bias current | V _O = 0, V _{IC} = 0 See Figure 5 | | 25°C | 2 | 200 | | 2 | 200 | pA | |
| | | | 125°C | 7 | 20 | | 8 | 20 | nA | |
| V _{ICR} Common-mode input voltage range | | | 25°C | -1.5 to 4 | -3.4 to 5.4 | | -11.5 to 14 | -13.4 to 15.4 | V | |
| | | | Full range† | -1.5 to 4 | | | -11.5 to 14 | | | |
| V _{OM+} Maximum positive peak output voltage swing | R _L = 10 kΩ | | 25°C | 3 | 4.3 | | 13 | 14 | V | |
| | | | -55°C | 3 | 4.1 | | 13 | 14 | | |
| | | | 125°C | 3 | 4.4 | | 13 | 14 | | |
| V _{OM-} Maximum negative peak output voltage swing | R _L = 10 kΩ | | 25°C | -3 | -4.2 | | -12.5 | -13.9 | V | |
| | | | -55°C | -3 | -4 | | -12.5 | -13.8 | | |
| | | | 125°C | -3 | -4.3 | | -12.5 | -14 | | |
| A _{VD} Large-signal differential voltage amplification§ | R _L = 10 kΩ | | 25°C | 4 | 12 | | 5 | 14.3 | V/mV | |
| | | | -55°C | 3 | 7.1 | | 4 | 10.4 | | |
| | | | 125°C | 3 | 12.9 | | 4 | 15 | | |
| r _i Input resistance | | | 25°C | 10 ¹² | | | 10 ¹² | | Ω | |
| c _i Input capacitance | | | 25°C | 5 | | | 4 | | pF | |
| CMRR Common-mode rejection ratio | V _{IC} = V _{ICRmin} , V _O = 0, R _S = 50 Ω | | 25°C | 70 | 87 | | 75 | 94 | dB | |
| | | | -55°C | 70 | 87 | | 70 | 94 | | |
| | | | 125°C | 70 | 87 | | 70 | 94 | | |
| k _{SVR} Supply-voltage rejection ratio (ΔV _{CC±} /ΔV _{IO}) | V _O = 0, R _S = 50 Ω | | 25°C | 75 | 96 | | 75 | 96 | dB | |
| | | | -55°C | 75 | 95 | | 75 | 95 | | |
| | | | 125°C | 75 | 96 | | 75 | 96 | | |

† Full range is -55°C to 125°C.

‡ Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

§ At V_{CC±} = ±5 V, V_O = ±2.3 V; at V_{CC±} = ±15 V, V_O = ±10 V



TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TL034M and TL034AM electrical characteristics at specified free-air temperature (continued)

| PARAMETER | TEST CONDITIONS | T _A | TL034M, TL034AM | | | | | | UNIT |
|----------------------------------|--|-----------------------------|-------------------------|------|-----|--------------------------|------|------|------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| P _D | Total power dissipation (two amplifiers) | V _O = 0, No load | 25°C | 7.7 | 10 | | 26 | 34 | mW |
| | | | -55°C | 4.6 | 12 | | 18.7 | 45 | |
| | | | 125°C | 7.1 | 12 | | 23.6 | 45 | |
| I _{CC} | Supply current (two amplifiers) | V _O = 0, No load | 25°C | 0.77 | 1 | | 0.87 | 1.12 | mA |
| | | | -55°C | 0.46 | 1.2 | | 0.62 | 1.5 | |
| | | | 125°C | 0.71 | 1.2 | | 0.79 | 1.5 | |
| V _{O1} /V _{O2} | Crosstalk attenuation | A _{VD} = 100 | 25°C | 120 | | | 120 | | dB |

TL034M and TL034AM operating characteristics at specified free-air temperature

| PARAMETER | TEST CONDITIONS | T _A | TL034M, TL034AM | | | | | | UNIT | | |
|------------------|-----------------------------------|---|---------------------------------------|-----------|------|--------------------------|---------|-----|------|--------|--------|
| | | | V _{CC±} = ±5 V | | | V _{CC±} = ±15 V | | | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | | | |
| SR ₊ | Positive slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | 2 | | | 1.5 2.9 | | | V/μs | |
| | | | -55°C | 1.4 | | | 1 1.9 | | | | |
| | | | 125°C | 2.4 | | | 1 3.5 | | | | |
| SR ₋ | Negative slew rate at unity gain† | R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | 3.9 | | | 1.5 5.1 | | | V/μs | |
| | | | -55°C | 3.2 | | | 1 4.6 | | | | |
| | | | 125°C | 4.1 | | | 1 4.7 | | | | |
| t _r | Rise time | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | 138 | | | 132 | | | ns | |
| | | | -55°C | 142 | | | 123 | | | | |
| | | | 125°C | 166 | | | 58 | | | | |
| t _f | Fall time | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figure 1 | 25°C | 138 | | | 132 | | | ns | |
| | | | -55°C | 142 | | | 123 | | | | |
| | | | 125°C | 166 | | | 158 | | | | |
| Overshoot factor | | V _{I(PP)} = ±10 V, R _L = 10 kΩ, C _L = 100 pF See Figures 1 and 2 | 25°C | 11% | | | 5% | | | | |
| | | | -55°C | 16% | | | 6% | | | | |
| | | | 125°C | 14% | | | 8% | | | | |
| V _n | Equivalent input noise voltage | TL034M | R _S = 20 Ω See Figure 3 | f = 10 Hz | 25°C | | | 83 | | | nV/√Hz |
| | | | | f = 1 kHz | 25°C | | | 43 | | | |
| | | TL034AM | | f = 10 Hz | 25°C | | | 83 | | | |
| | | | | f = 1 kHz | 25°C | | | 43 | | | |
| I _n | Equivalent input noise current | f = 1 kHz | 25°C | 0.003 | | | 0.003 | | | pA/√Hz | |
| B1 | Unity-gain bandwidth | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | 1 | | | 1.1 | | | MHz | |
| | | | -55°C | 1 | | | 1.1 | | | | |
| | | | 125°C | 0.9 | | | 0.9 | | | | |
| φ _m | Phase margin at unity gain | V _I = 10 mV, R _L = 10 kΩ, C _L = 25 pF See Figure 4 | 25°C | 61° | | | 65° | | | | |
| | | | -55°C | 57° | | | 64° | | | | |
| | | | 125°C | 59° | | | 62° | | | | |

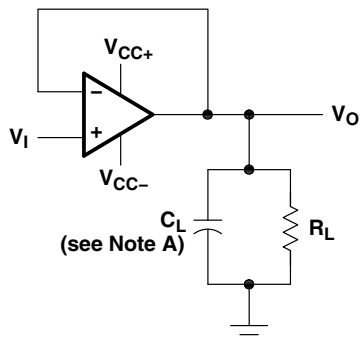
† For V_{CC±} = ±5 V, V_{I(PP)} = ±1 V; for V_{CC±} = ±15 V, V_{I(PP)} = ±5 V



TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes fixture capacitance.

Figure 1. Slew-Rate and Overshoot Test Circuit

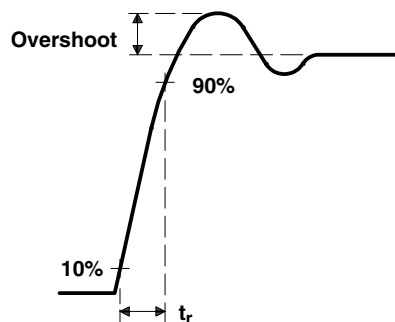


Figure 2. Rise Time and Overshoot Waveform

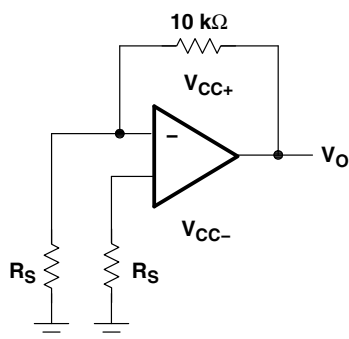
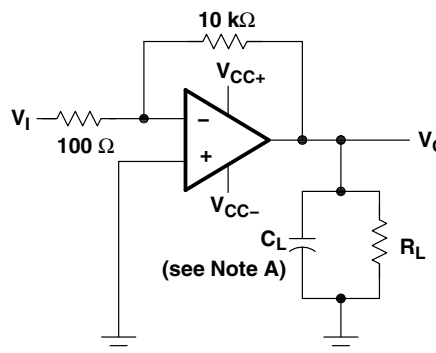


Figure 3. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 4. Unity-Gain Bandwidth and Phase-Margin Test Circuit

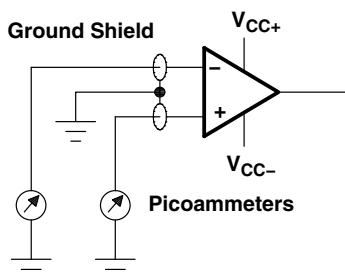


Figure 5. Input-Bias and Offset-Current Test Circuit

PARAMETER MEASUREMENT INFORMATION

typical values

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

input bias and offset current

At the picoampere bias current level typical of the TL03x and TL03xA, accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test-socket leakages easily can exceed the actual device bias currents. To accurately measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted into the socket and a second test that measures both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

noise

With the increasing emphasis on low noise levels in many of today's applications, the input noise voltage density is performed at $f = 1$ kHz, unless otherwise noted.

TL03x, TL03xA
ENHANCED-JFET LOW-POWER LOW-OFFSET
OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TYPICAL CHARACTERISTICS

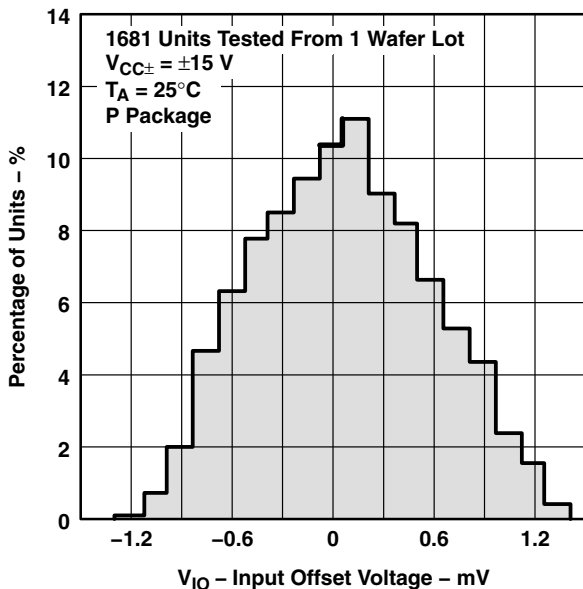
Table of Graphs

| | FIGURE |
|--|---------------|
| Distribution of TL03x input offset voltage | 6–11 |
| Distribution of TL03x input offset-voltage temperature coefficient | 12–14 |
| Input bias current vs Common-mode input voltage | 15 |
| Input bias current and input offset current vs Free-air temperature | 16 |
| Common-mode input voltage vs Supply voltage | 17 |
| Common-mode input voltage vs Free-air temperature | 18 |
| Output voltage vs Differential input voltage | 19, 20 |
| Maximum peak output voltage vs Supply voltage | 21 |
| Maximum peak-to-peak output voltage vs Frequency | 22 |
| Maximum peak output voltage vs Output current | 23, 24 |
| Maximum peak output voltage vs Free-air temperature | 25, 26 |
| Large-signal differential voltage amplification vs Load resistance | 27 |
| Large-signal differential voltage amplification and Phase shift vs Frequency | 28 |
| Large-signal differential voltage amplification vs Free-air temperature | 29 |
| Output impedance vs Frequency | 30 |
| Common-mode rejection ratio vs Frequency | 31, 32 |
| Common-mode rejection ratio vs Free-air temperature | 33 |
| Supply-voltage rejection ratio vs Free-air temperature | 34 |
| Short-circuit output current vs Supply voltage | 35 |
| Short-circuit output current vs Time | 36 |
| Short-circuit output current vs Free-air temperature | 37 |
| Equivalent input noise voltage vs Frequency (TL031 and TL031A) | 38 |
| Equivalent input noise voltage vs Frequency (TL032 and TL032A) | 39 |
| Equivalent input noise voltage vs Frequency (TL034 and TL034A) | 40 |
| Supply current vs Supply voltage (TL031 and TL031A) | 41 |
| Supply current vs Supply voltage (TL032 and TL032A) | 42 |
| Supply current vs Supply voltage (TL034 and TL034A) | 43 |
| Supply current vs Free-air temperature (TL031 and TL031A) | 44 |
| Supply current vs Free-air temperature (TL032 and TL032A) | 45 |
| Supply current vs Free-air temperature (TL034 and TL034A) | 46 |
| Slew rate vs Load resistance | 47, 48 |
| Slew rate vs Free-air temperature | 49, 50 |
| Overshoot factor vs Load capacitance | 51 |
| Total harmonic distortion vs Frequency | 52 |
| Unity-gain bandwidth vs Supply voltage | 53 |
| Unity-gain bandwidth vs Free-air temperature | 54 |
| Phase margin vs Supply voltage | 55 |
| Phase margin vs Load capacitance | 56 |
| Phase margin vs Free-air temperature | 57 |
| Voltage-follower small-signal pulse response | 58 |
| Voltage-follower large-signal pulse response | 59, 60 |

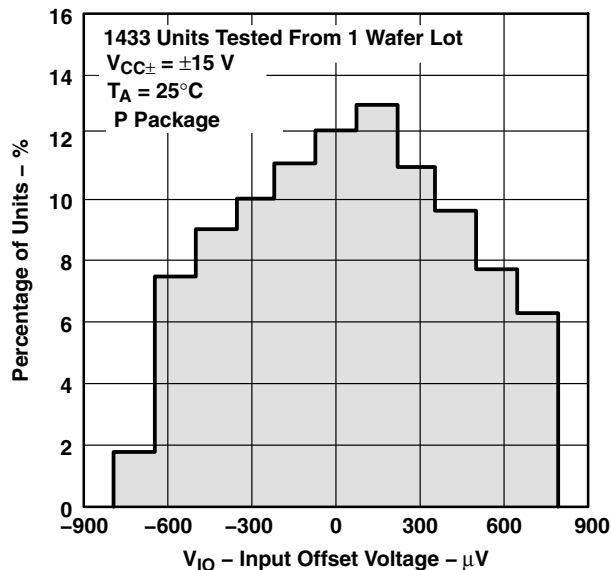


TYPICAL CHARACTERISTICS

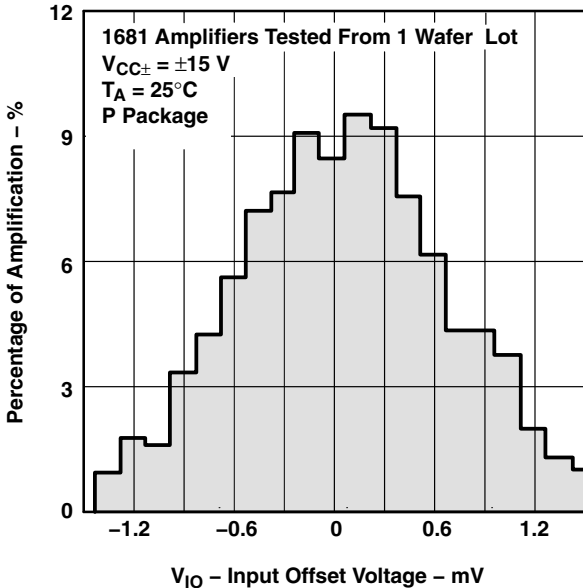
**DISTRIBUTION OF TL031
 INPUT OFFSET VOLTAGE**



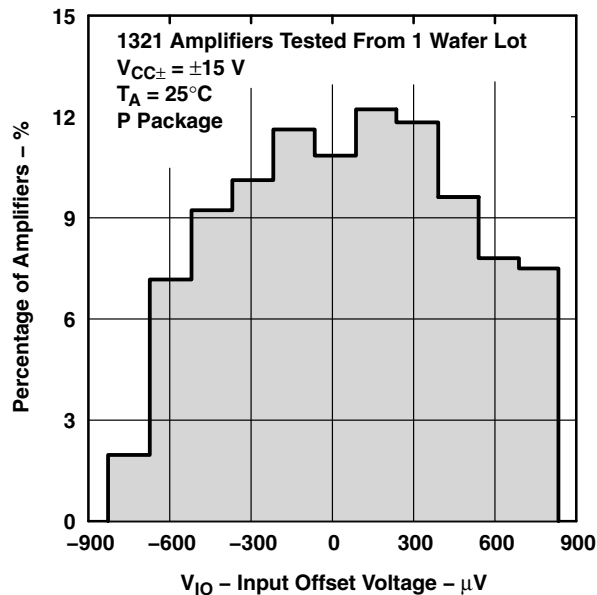
**DISTRIBUTION OF TL031A
 INPUT OFFSET VOLTAGE**



**DISTRIBUTION OF TL032
 INPUT OFFSET VOLTAGE**



**DISTRIBUTION OF TL032A
 INPUT OFFSET VOLTAGE**



TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TL034
INPUT OFFSET VOLTAGE**

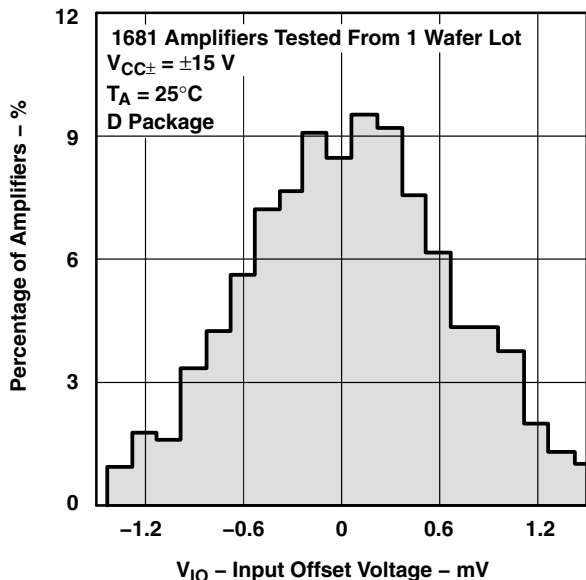


Figure 10

**DISTRIBUTION OF TL034A
INPUT OFFSET VOLTAGE**

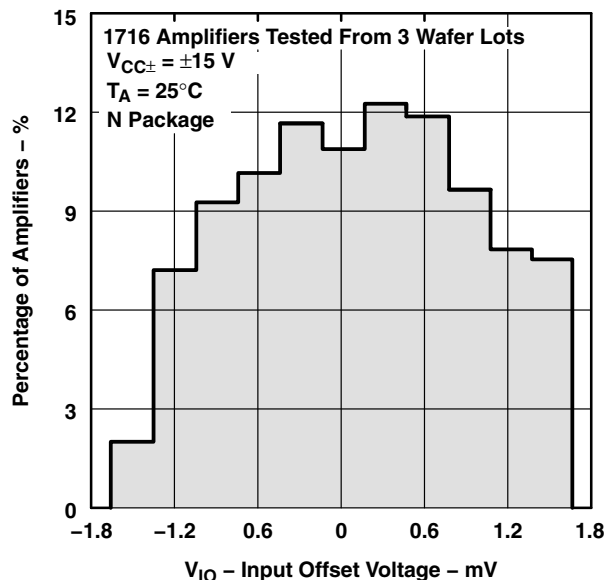


Figure 11

**DISTRIBUTION OF TL031
INPUT OFFSET-VOLTAGE
TEMPERATURE COEFFICIENT**

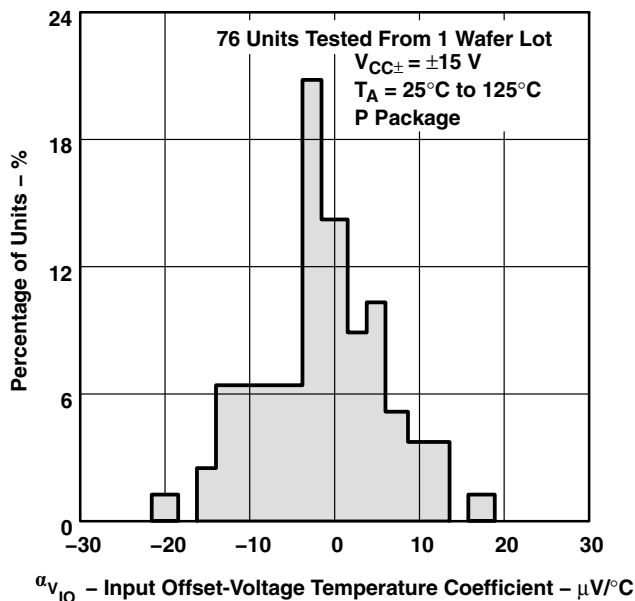


Figure 12

**DISTRIBUTION OF TL032
INPUT OFFSET-VOLTAGE
TEMPERATURE COEFFICIENT**

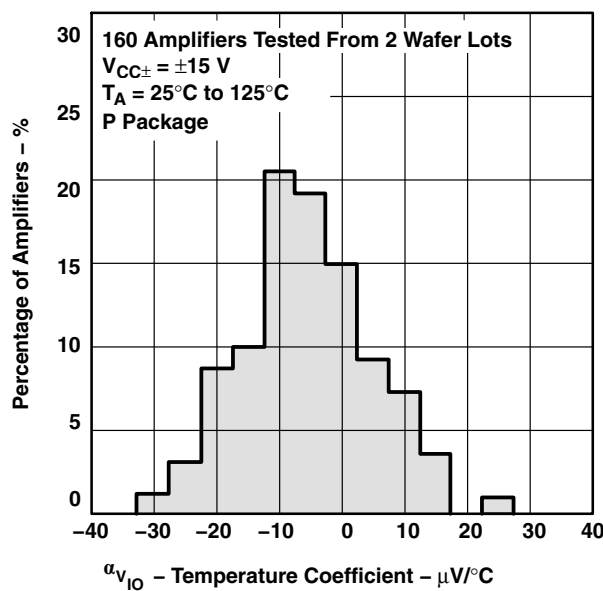


Figure 13

TYPICAL CHARACTERISTICS

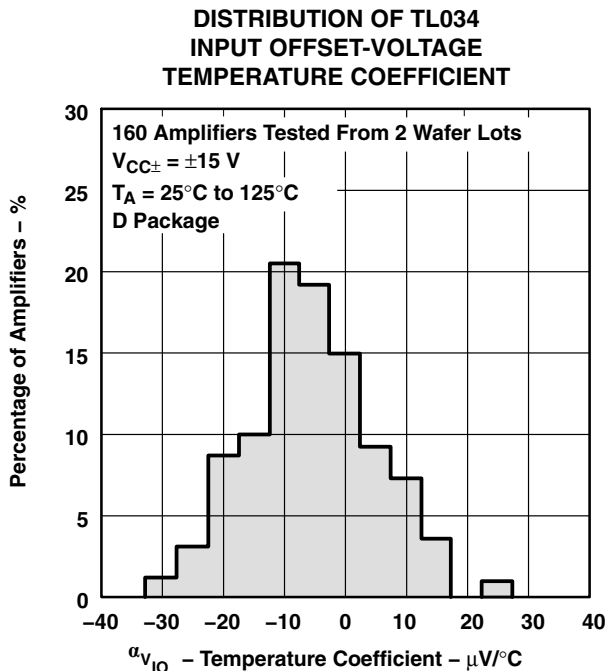


Figure 14

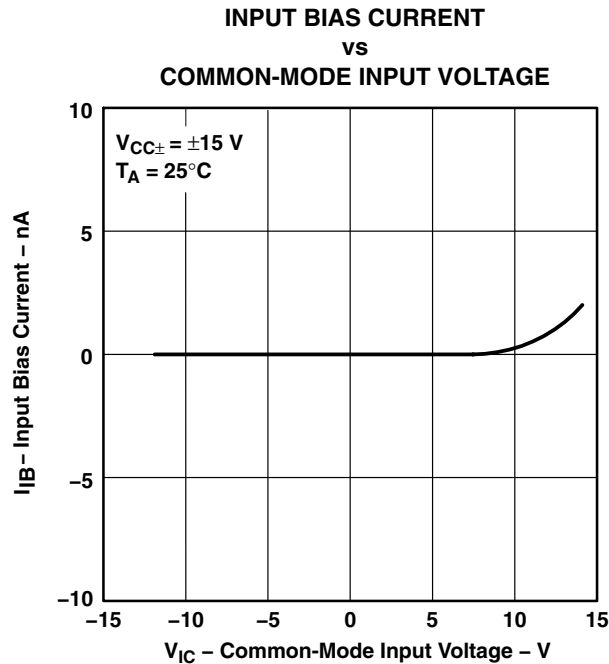


Figure 15

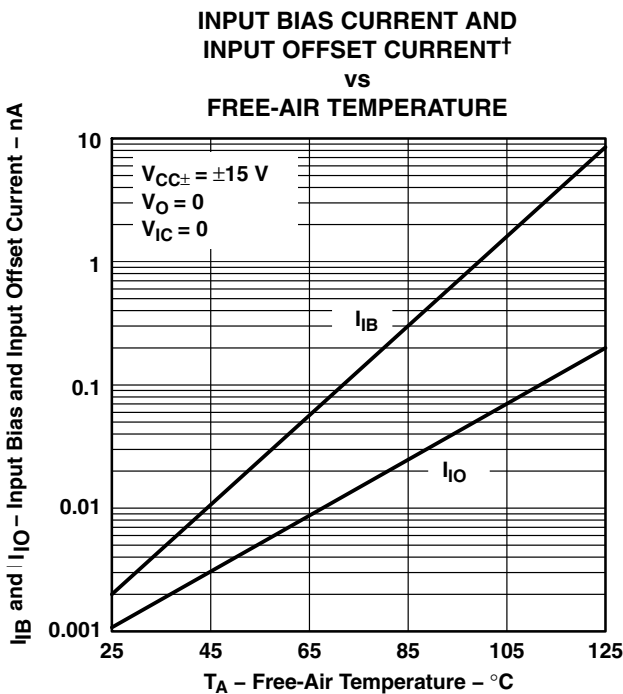


Figure 16

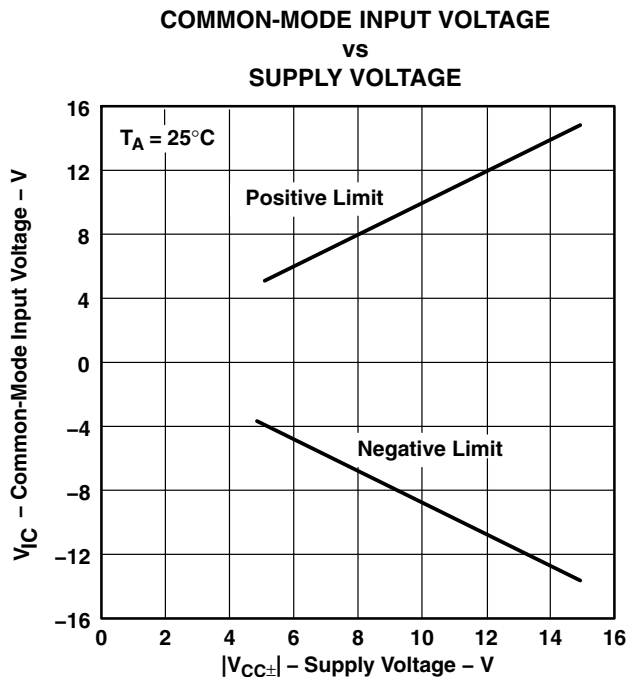


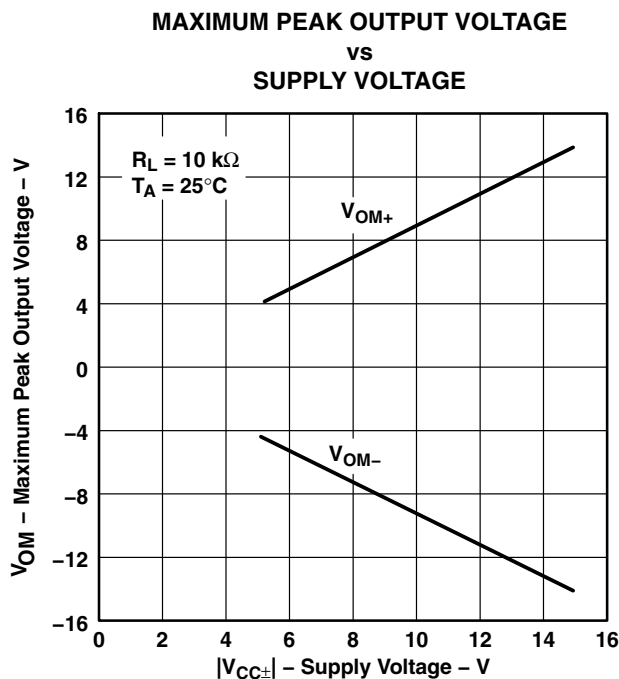
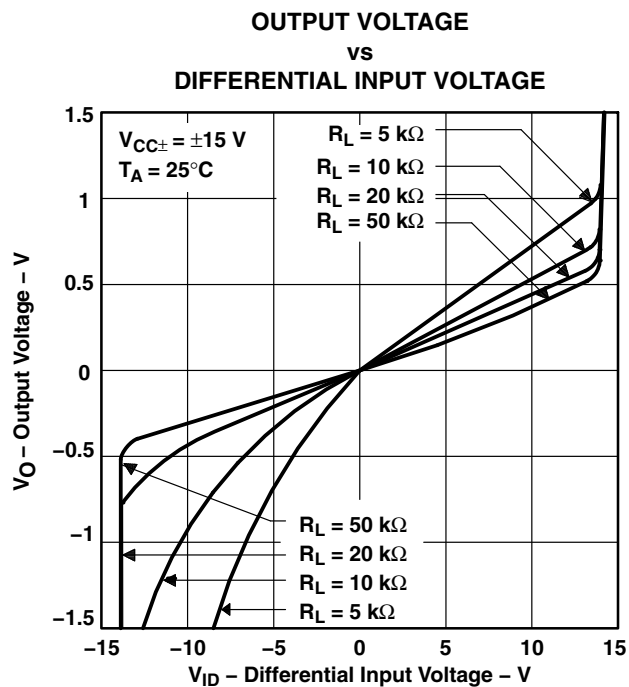
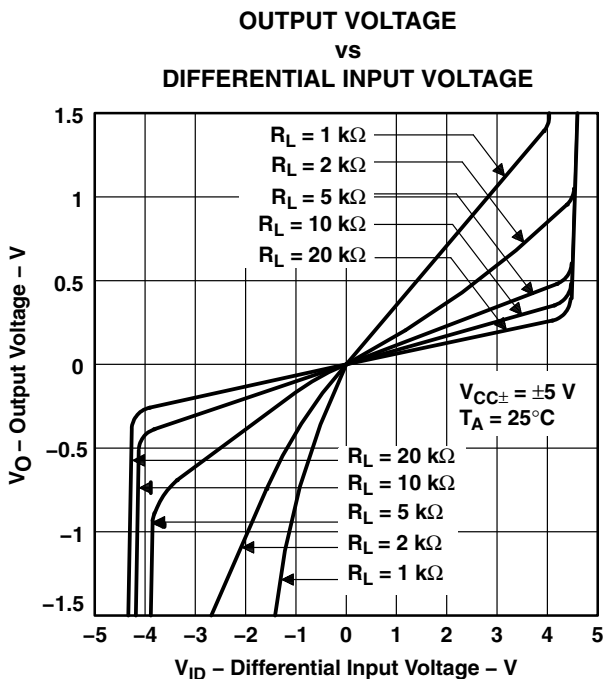
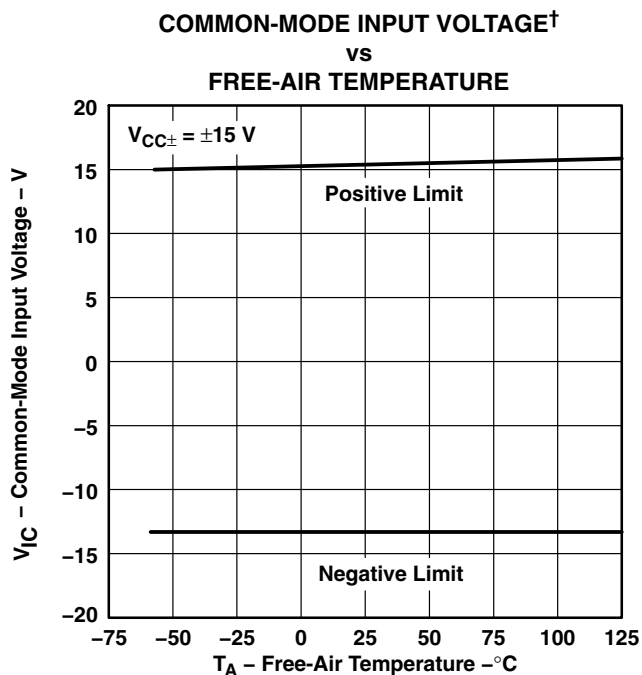
Figure 17

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE†
vs
FREQUENCY**

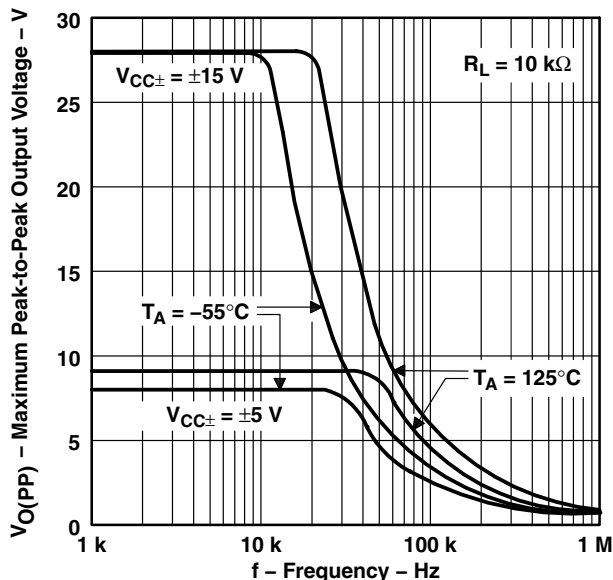


Figure 22

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

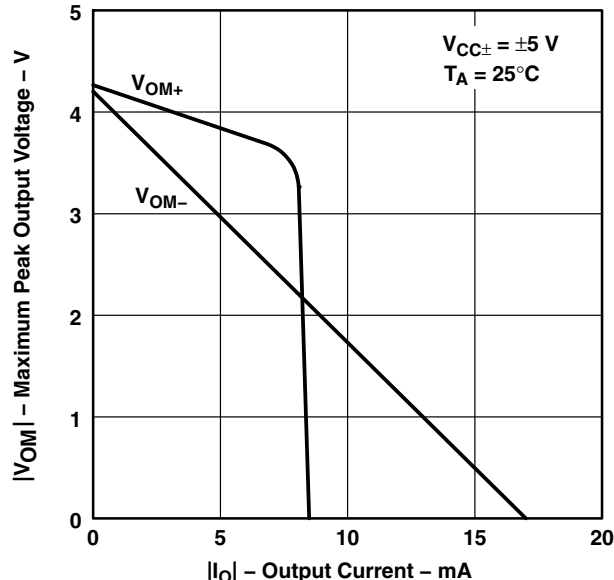


Figure 23

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
OUTPUT CURRENT**

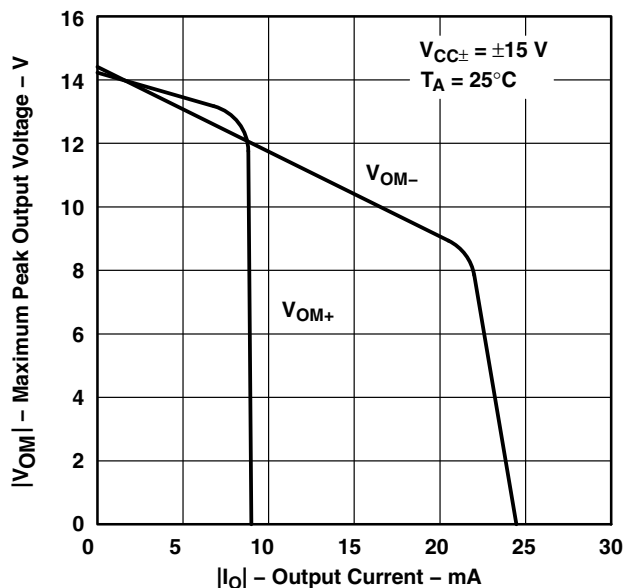


Figure 24

**MAXIMUM PEAK OUTPUT VOLTAGE†
vs
FREE-AIR TEMPERATURE**

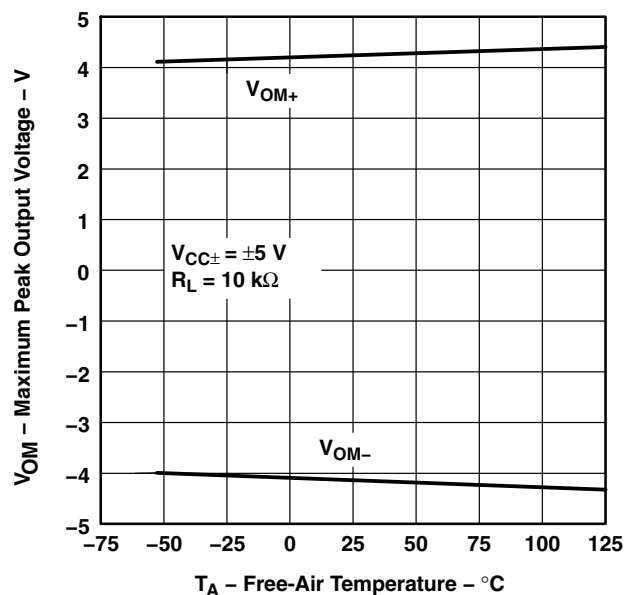


Figure 25

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TYPICAL CHARACTERISTICS

MAXIMUM PEAK OUTPUT VOLTAGE†
vs
FREE-AIR TEMPERATURE

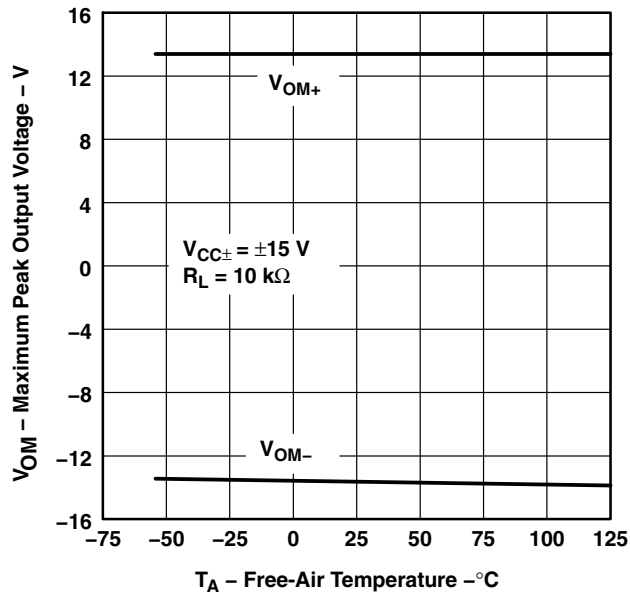


Figure 26

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION
vs
LOAD RESISTANCE

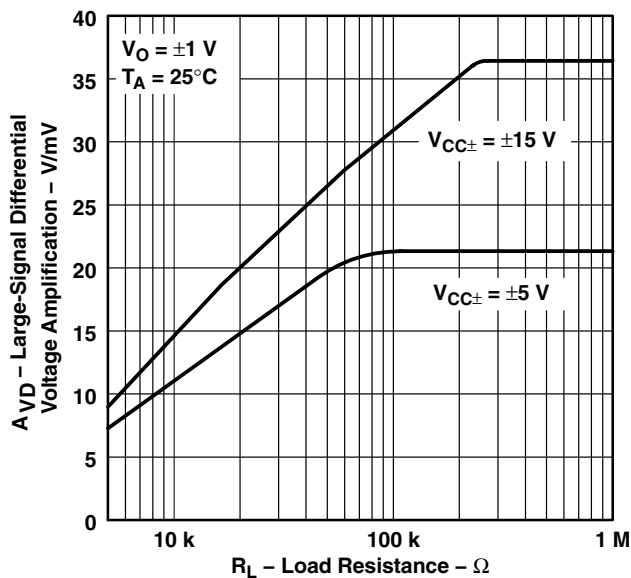


Figure 27

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

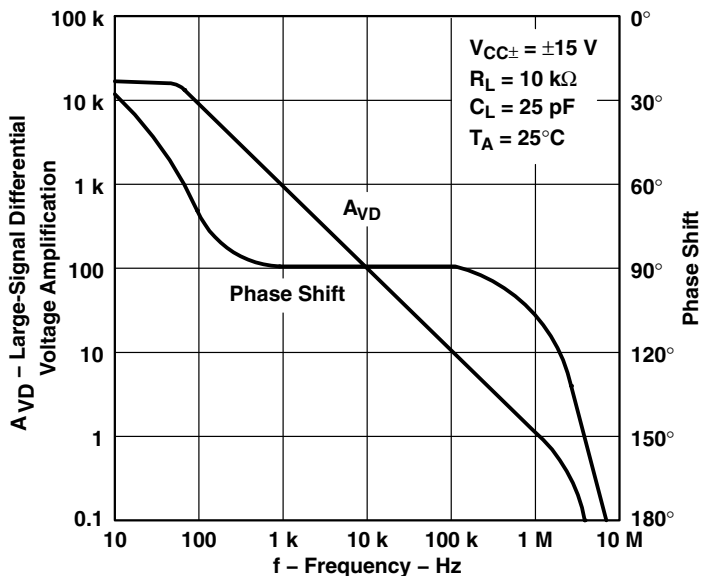


Figure 28

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

**LARGE-SIGNAL DIFFERENTIAL
 VOLTAGE AMPLIFICATION†
 vs
 FREE-AIR TEMPERATURE**

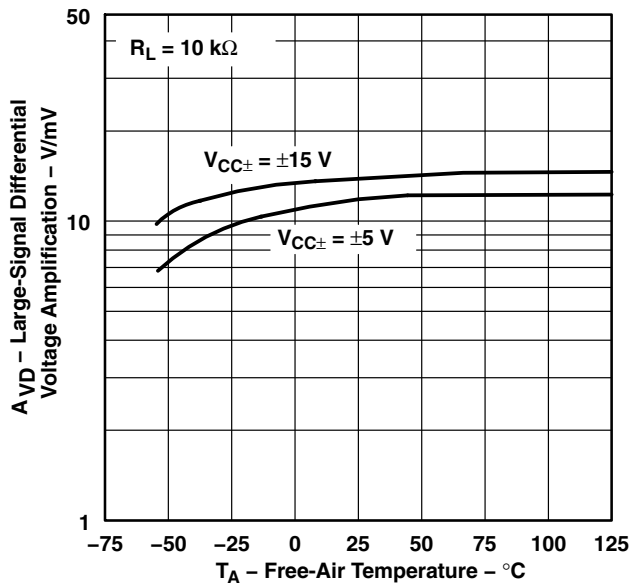


Figure 29

**OUTPUT IMPEDANCE
 vs
 FREQUENCY**

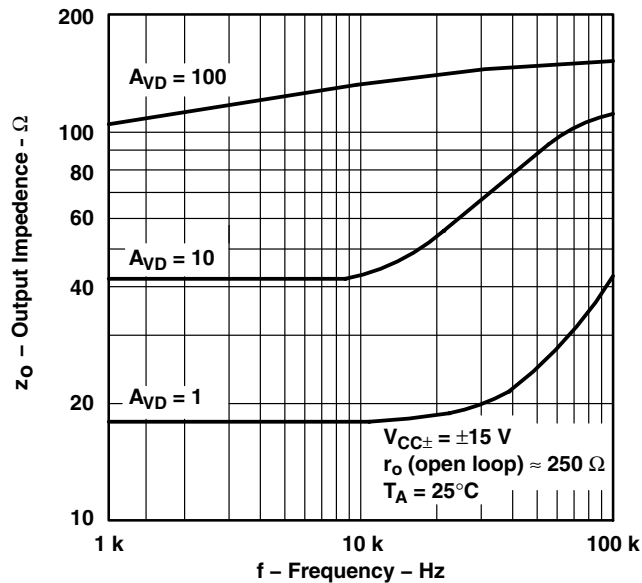


Figure 30

**COMMON-MODE REJECTION RATIO
 vs
 FREQUENCY**

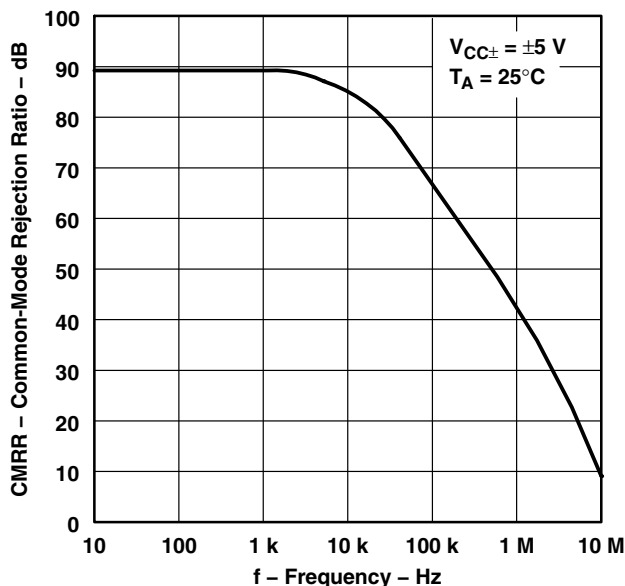


Figure 31

**COMMON-MODE REJECTION RATIO
 vs
 FREQUENCY**

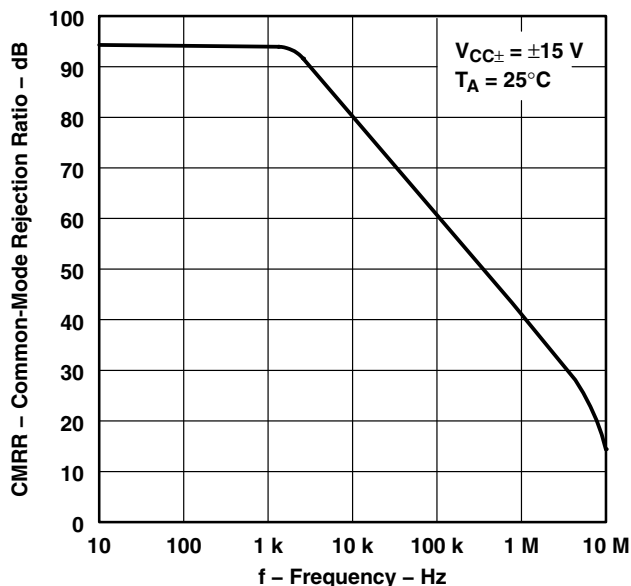


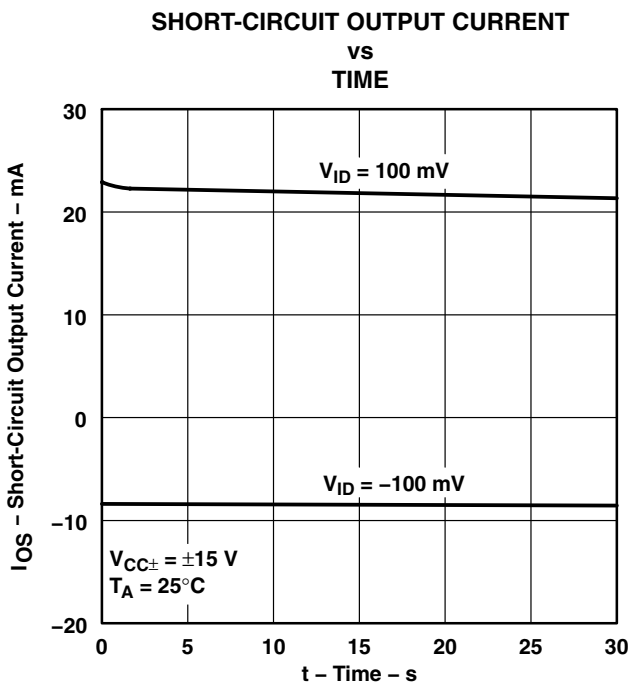
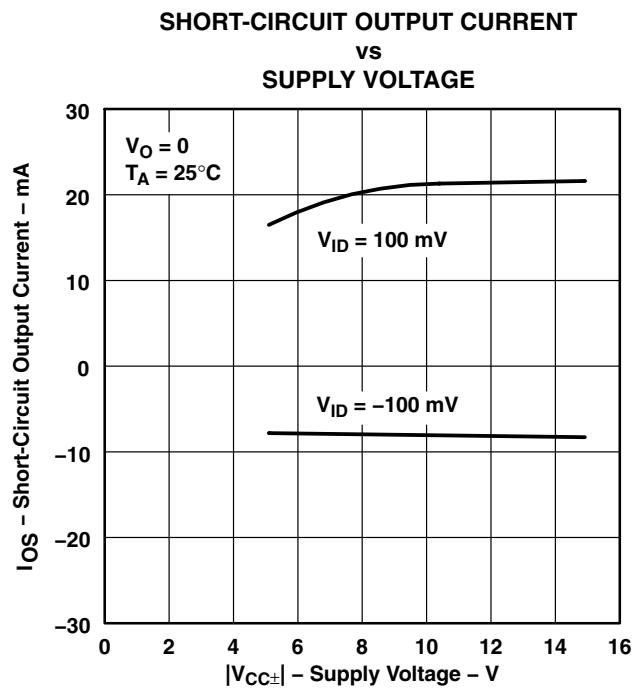
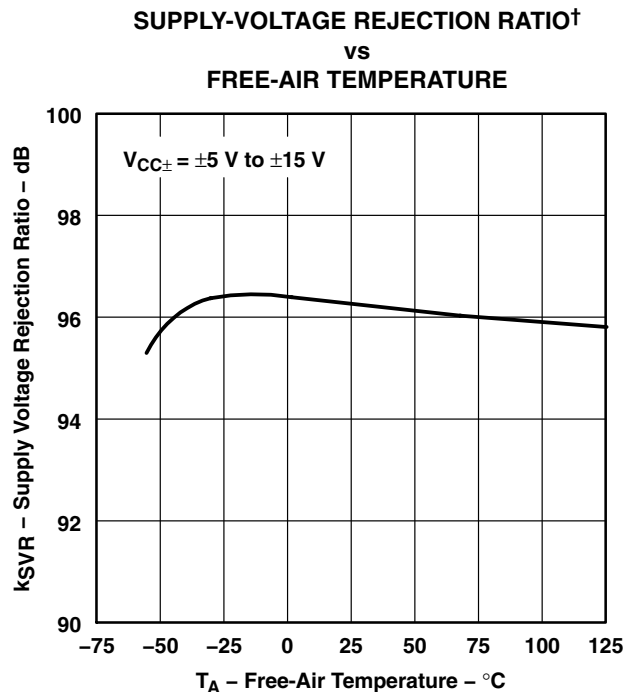
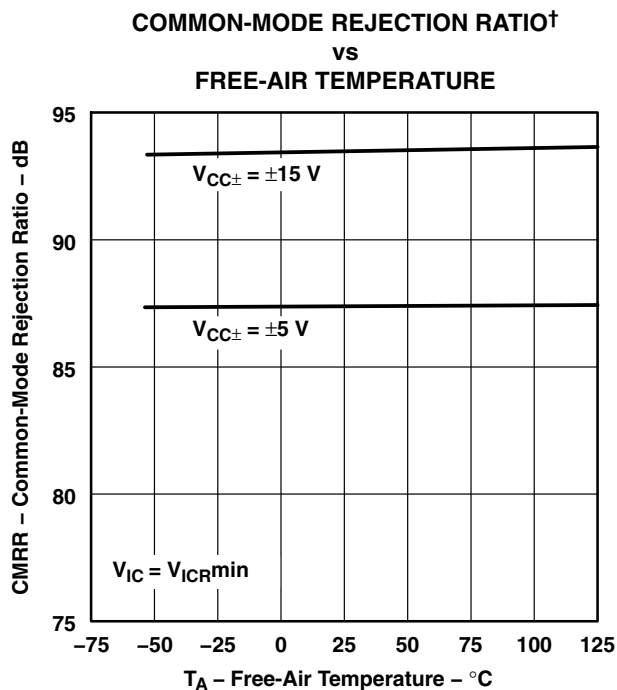
Figure 32

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

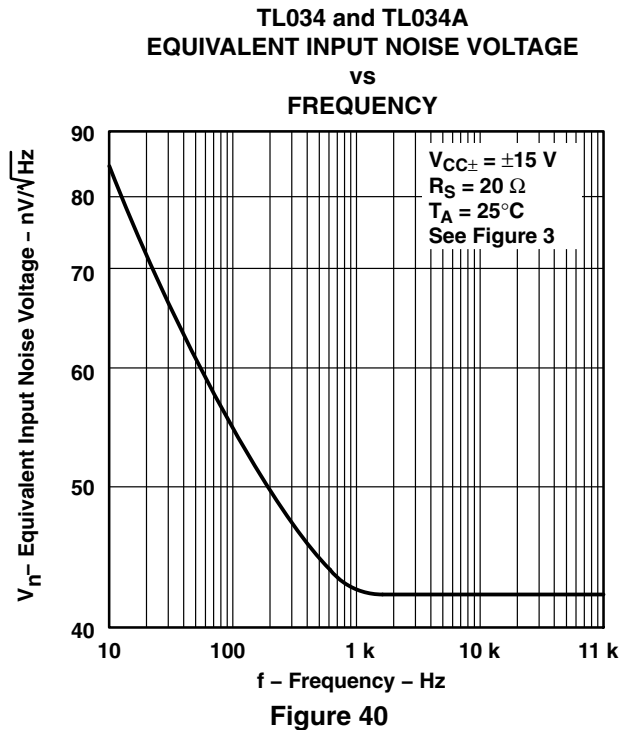
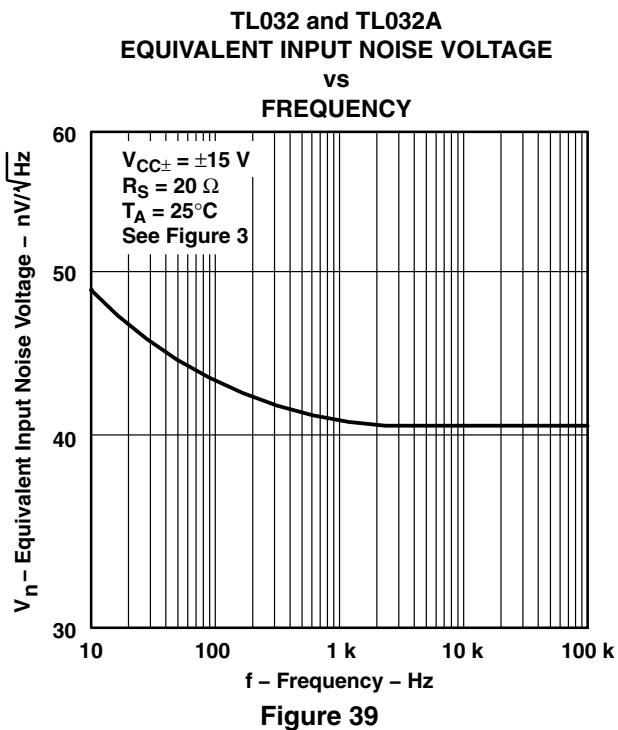
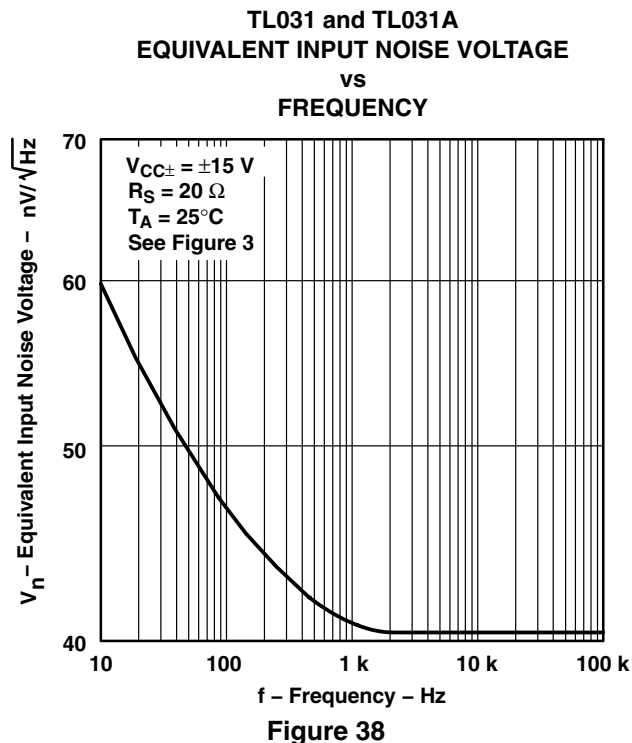
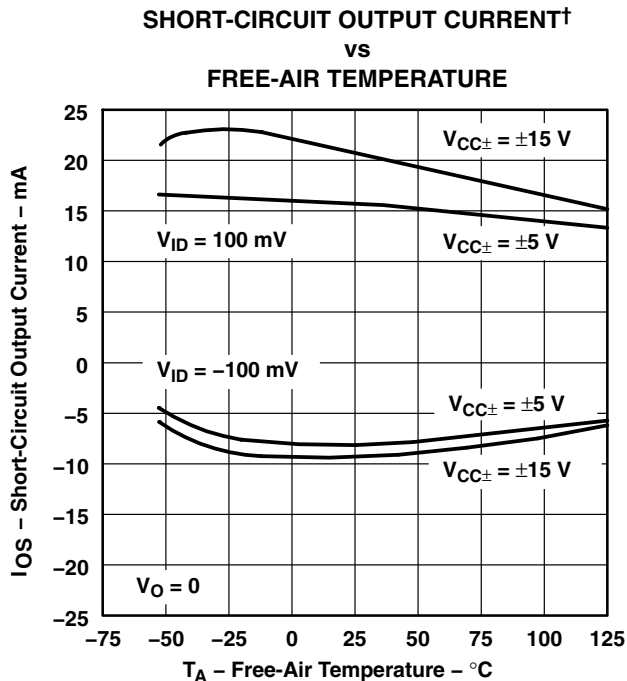
SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TYPICAL CHARACTERISTICS

TL031 and TL031A
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

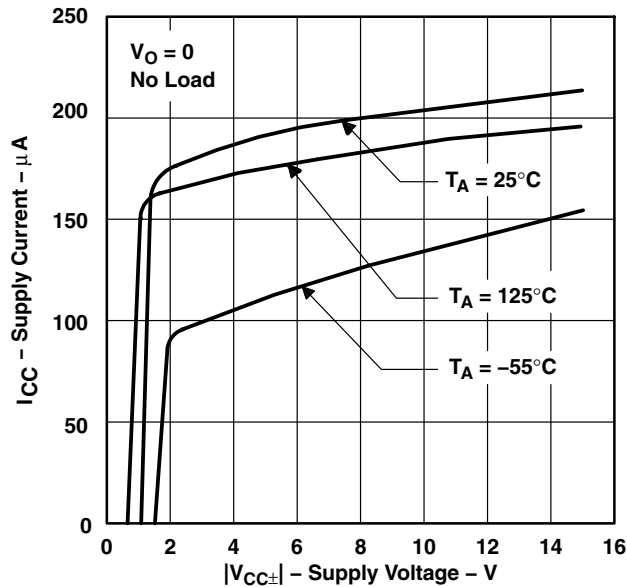


Figure 41

TL032 and TL032A
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

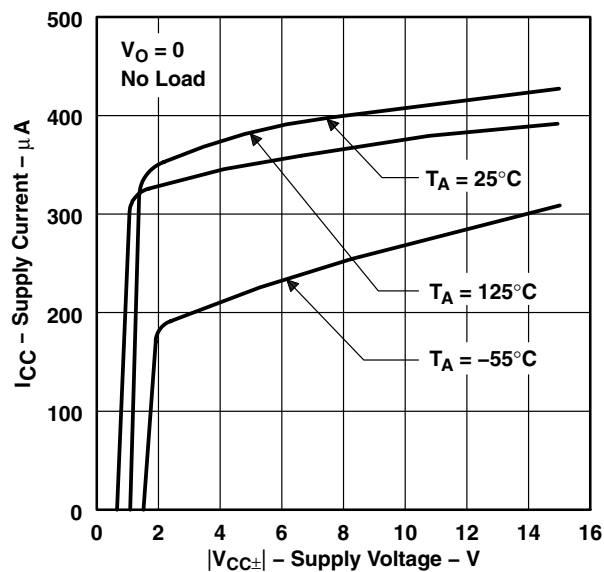


Figure 42

TL034 and TL034A
SUPPLY CURRENT†
vs
SUPPLY VOLTAGE

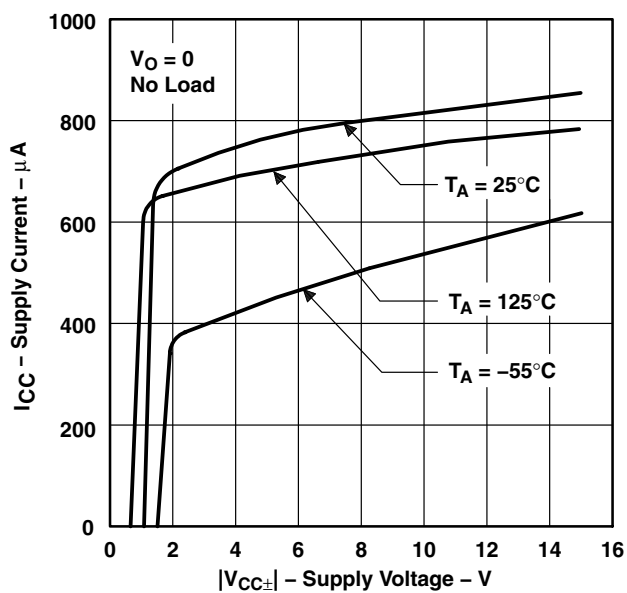


Figure 43

TL031 and TL031A
SUPPLY CURRENT†
vs
FREE-AIR TEMPERATURE

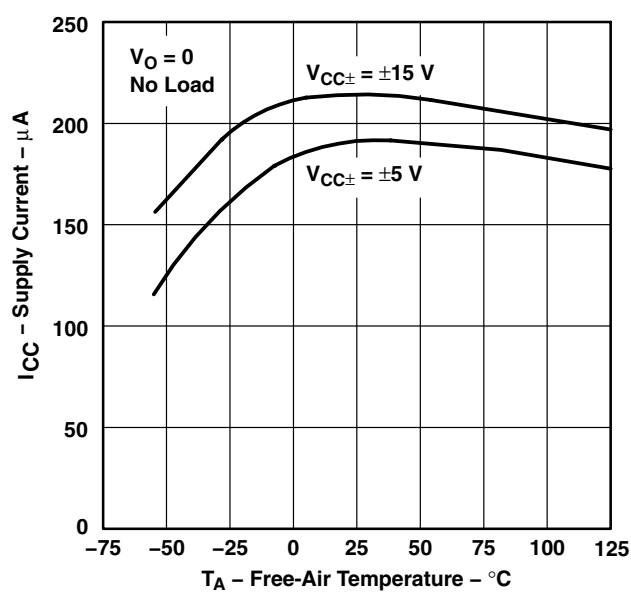
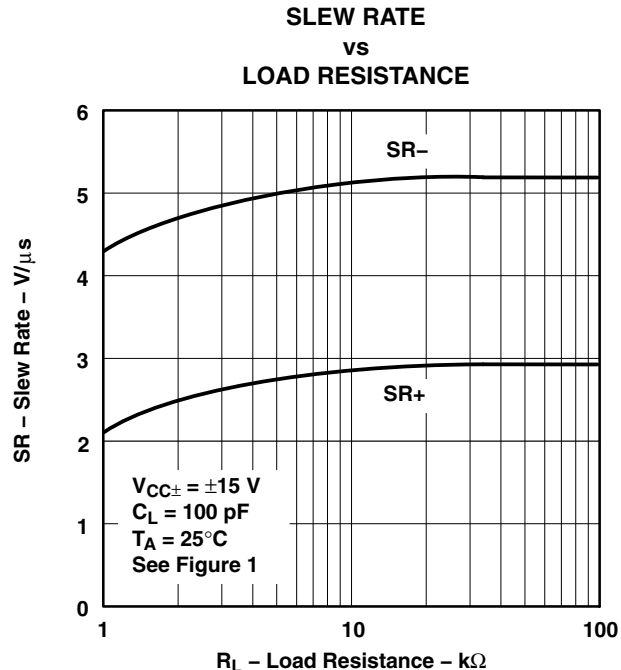
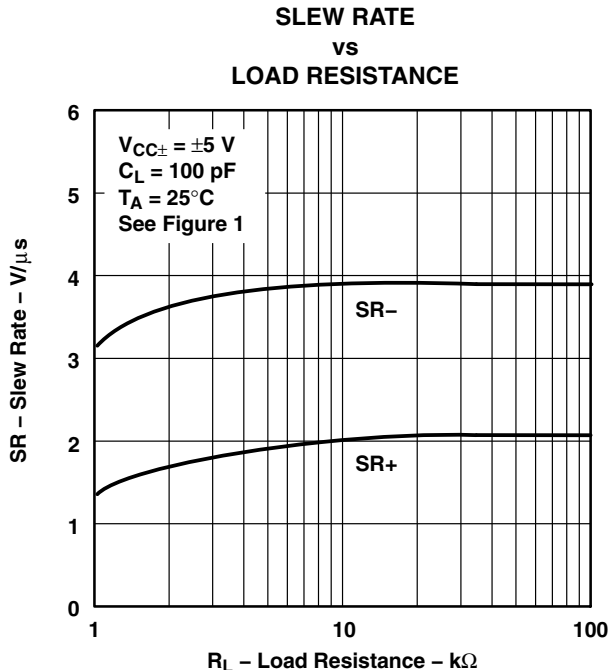
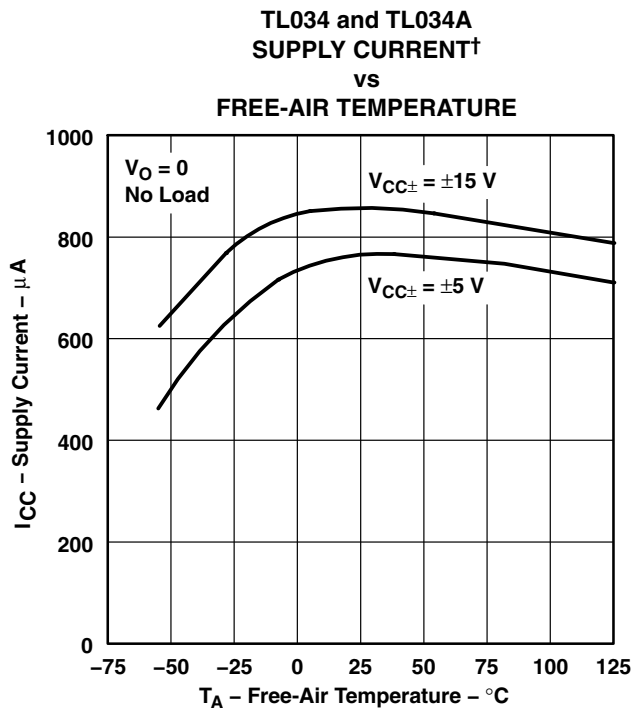
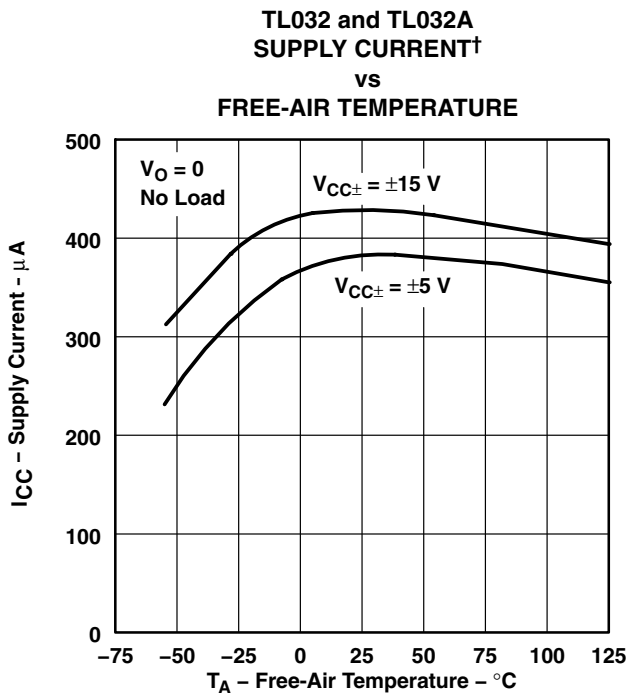


Figure 44

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TYPICAL CHARACTERISTICS

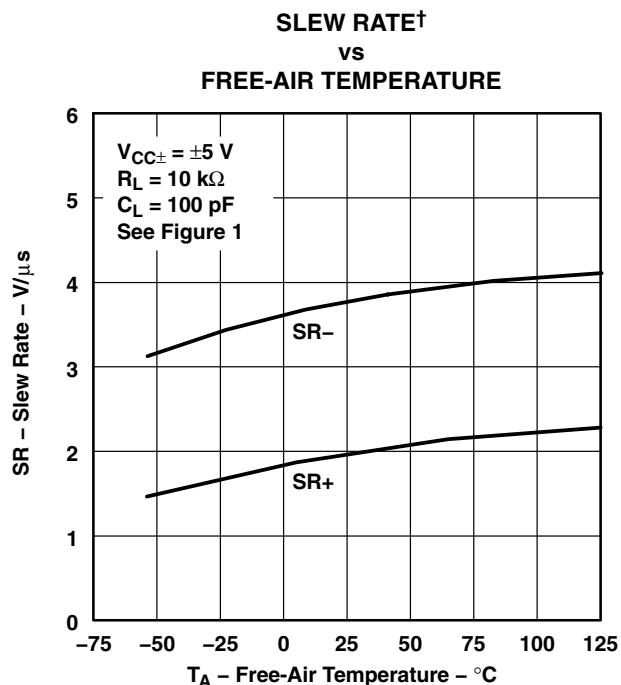


Figure 49

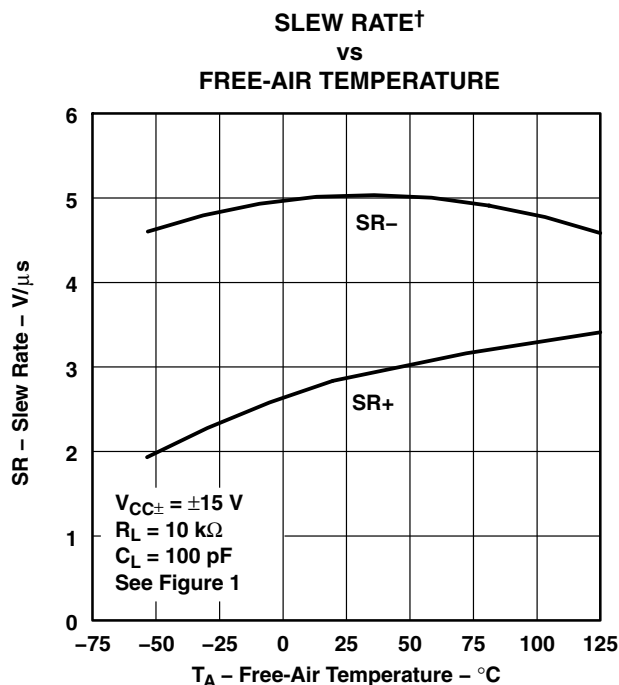


Figure 50

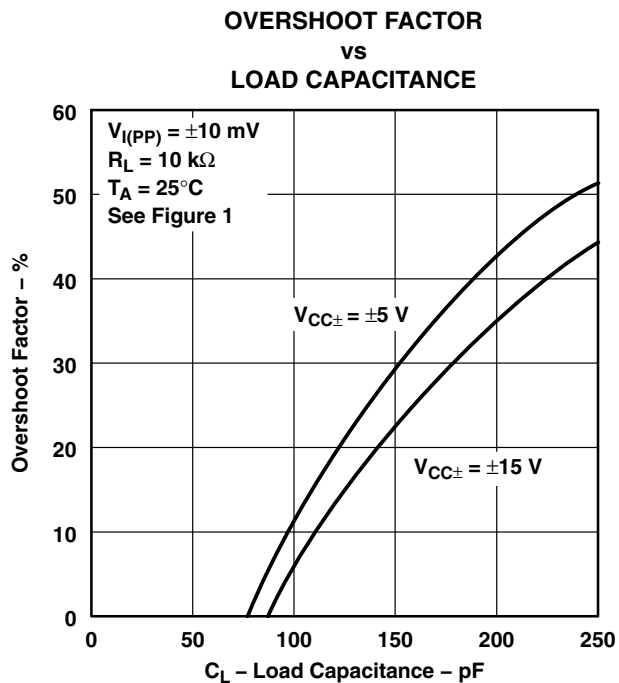


Figure 51

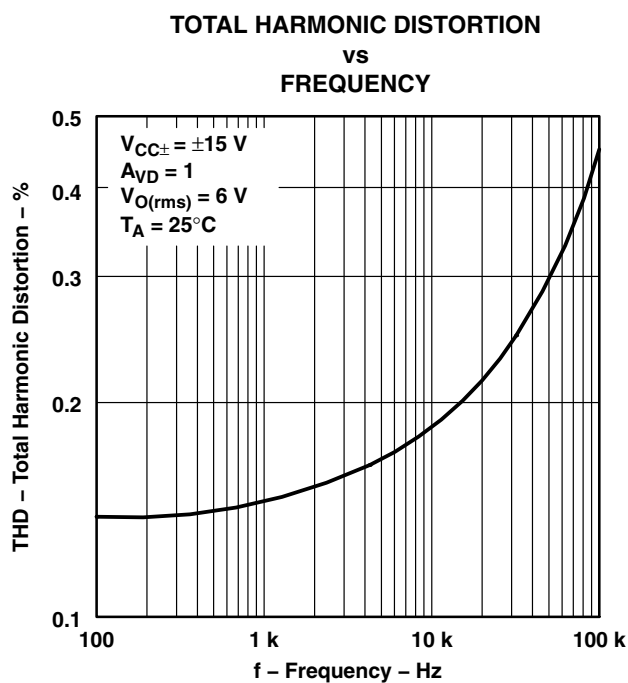


Figure 52

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

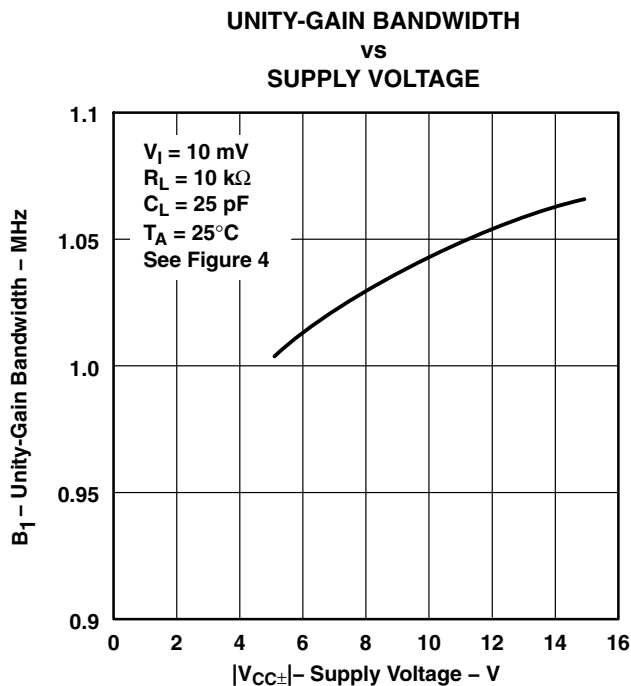


Figure 53

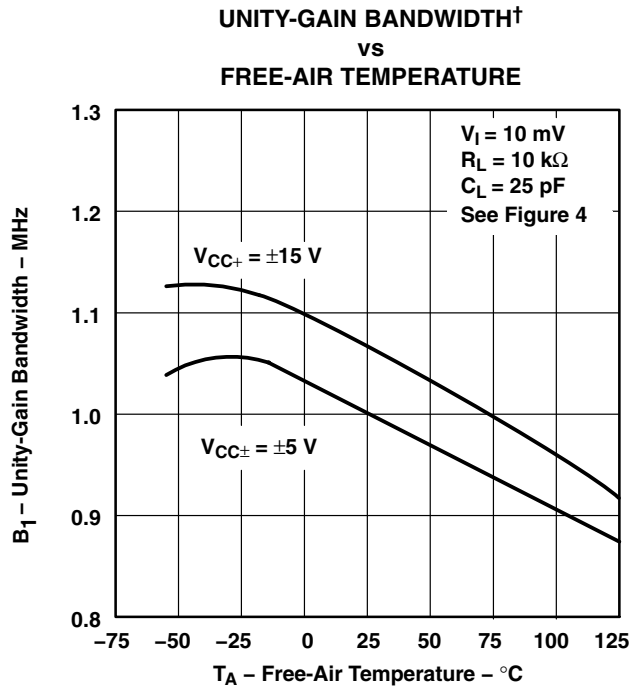


Figure 54

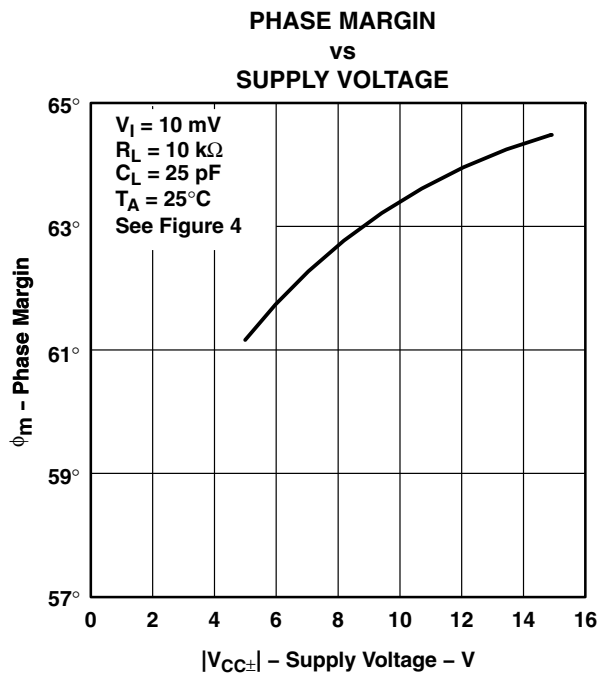
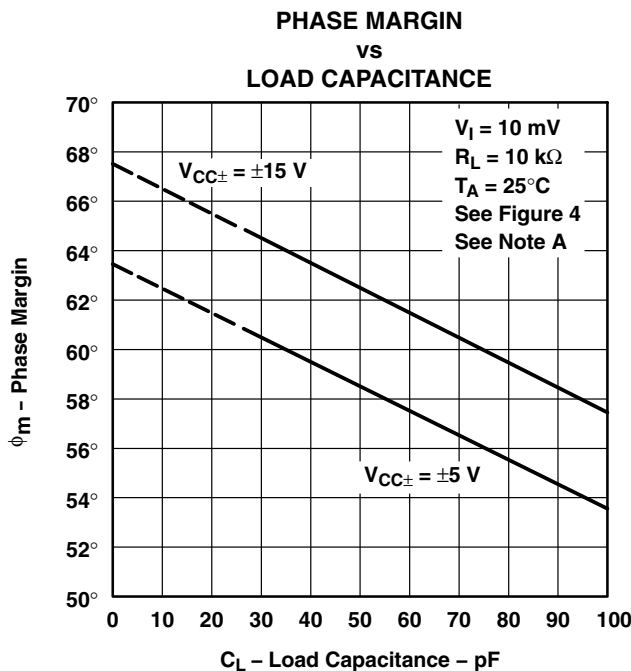


Figure 55



NOTE A: Values of phase margin below a load capacitance of 25 pF were estimated.

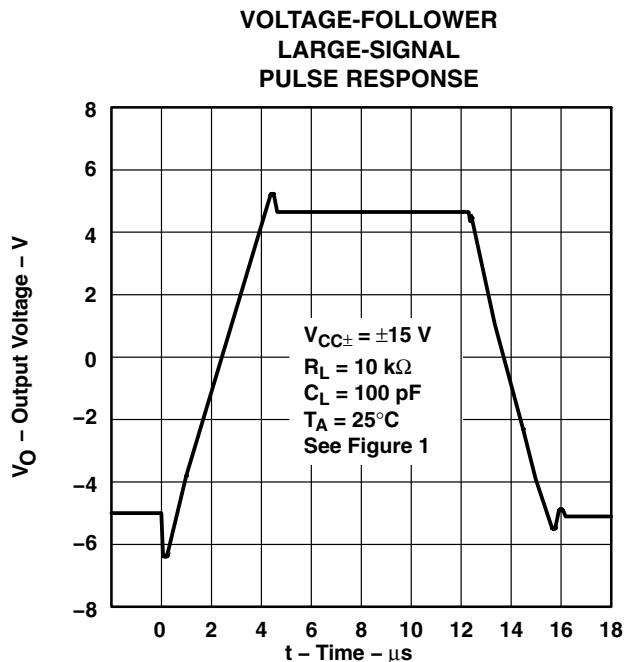
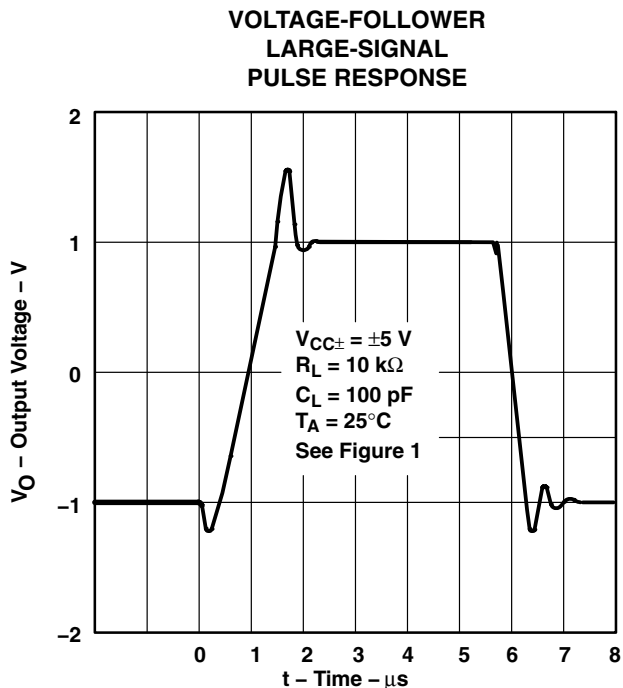
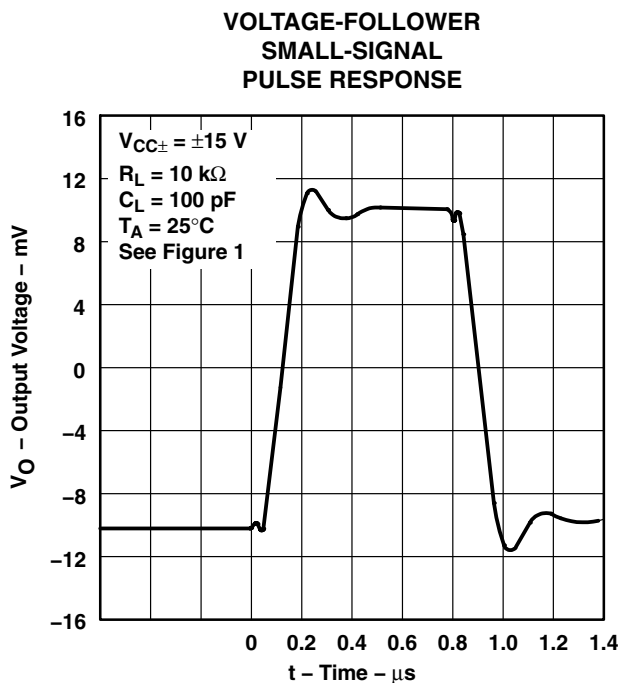
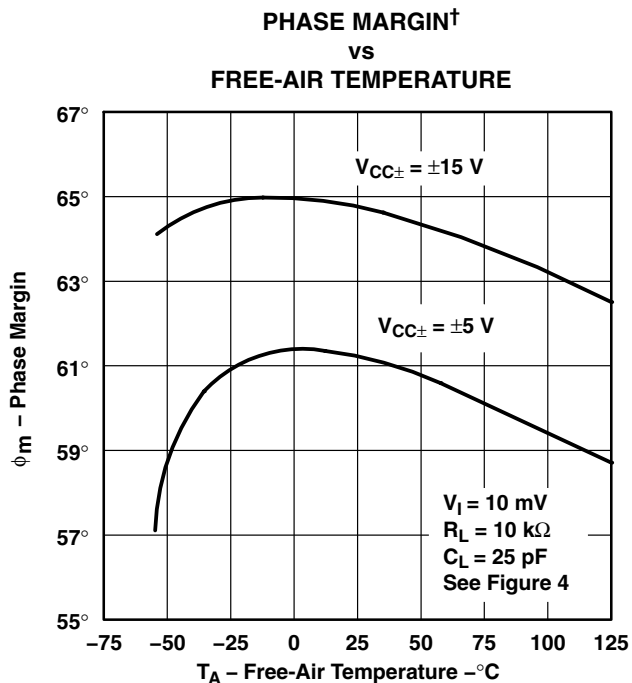
Figure 56

† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the recommended operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

input characteristics

The TL03x and TL03xA are specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction.

Due to the extremely high input impedance and resulting low bias-current requirements, the TL03x and TL03xA are well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets easily can exceed bias-current requirements and cause degradation in system performance. It is a good practice to include guard rings around inputs (see Figure 61). These guard rings should be driven from a low-impedance source at the same voltage level as the common-mode input.

Unused amplifiers should be connected as grounded unity-gain followers to avoid oscillation.

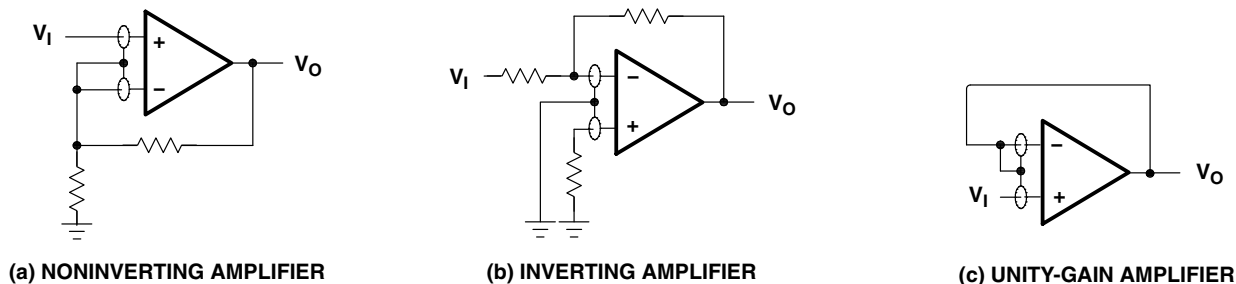


Figure 61. Use of Guard Rings

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

APPLICATION INFORMATION

output characteristics

All operating characteristics (except bandwidth and phase margin) are specified with 100-pF load capacitance. The TL03x and TL03xA drive higher capacitive loads; however, as the load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation. The value of the load capacitance at which oscillation occurs varies with production lots. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem (see Figure 63). Capacitive loads of 1000 pF and larger can be driven if enough resistance is added in series with the output (see Figure 62).

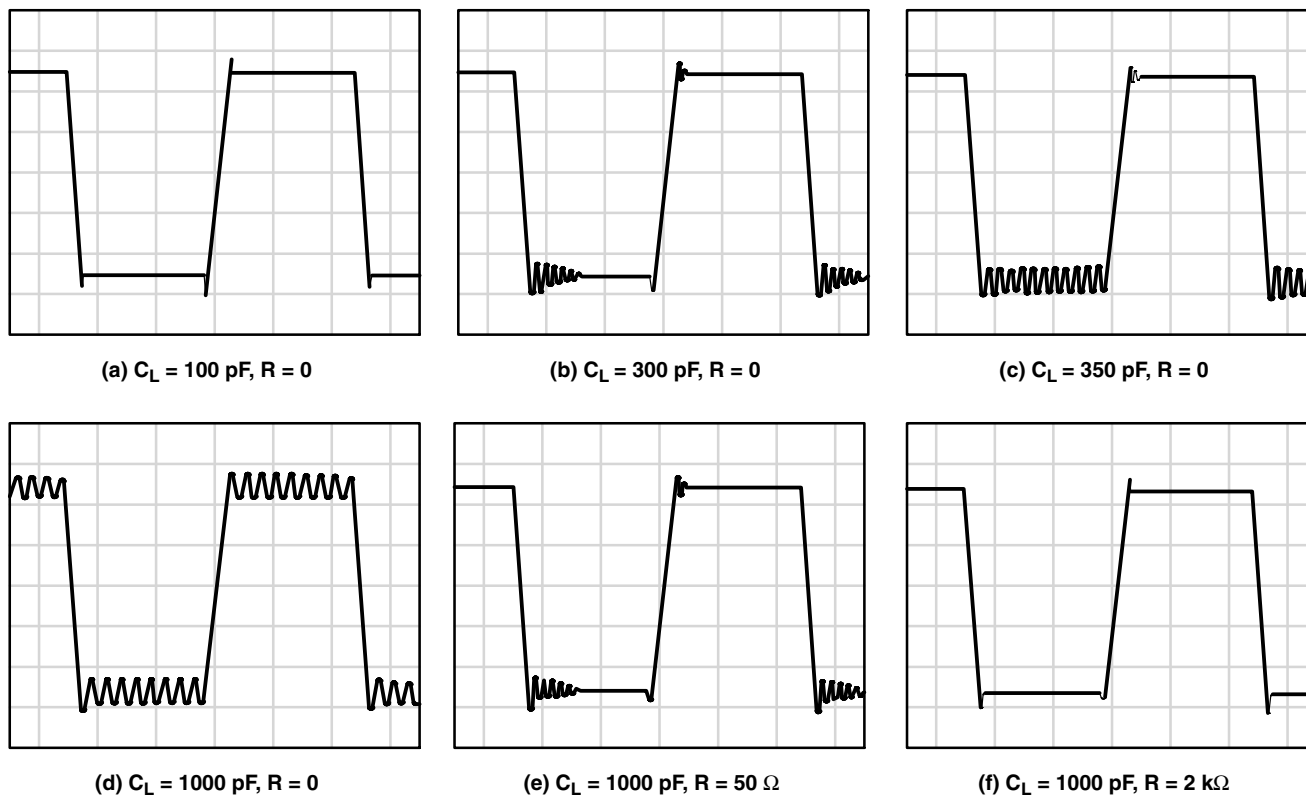


Figure 62. Effect of Capacitive Loads

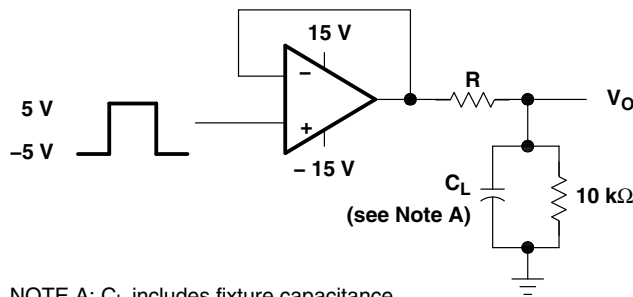


Figure 63. Test Circuit for Output Characteristics

APPLICATION INFORMATION

high-Q notch filter

In general, Texas Instruments enhanced-JFET operational amplifiers serve as excellent filters. The circuit in Figure 64 provides a narrow notch at a specific frequency. Notch filters are designed to eliminate frequencies that are interfering with the operation of an application. For this filter, the center frequency can be calculated as:

$$f_0 = \frac{1}{2\pi \times R1 \times C1}$$

With the resistors and capacitors shown in Figure 64, the center frequency is 1 kHz. $C1 = C3 = C2 + 2$ and $R1 = R3 = 2 \times R2$. The center frequency can be modified by varying these values. When adjusting the center frequency, ensure that the operational amplifier has sufficient gain at the frequency required.

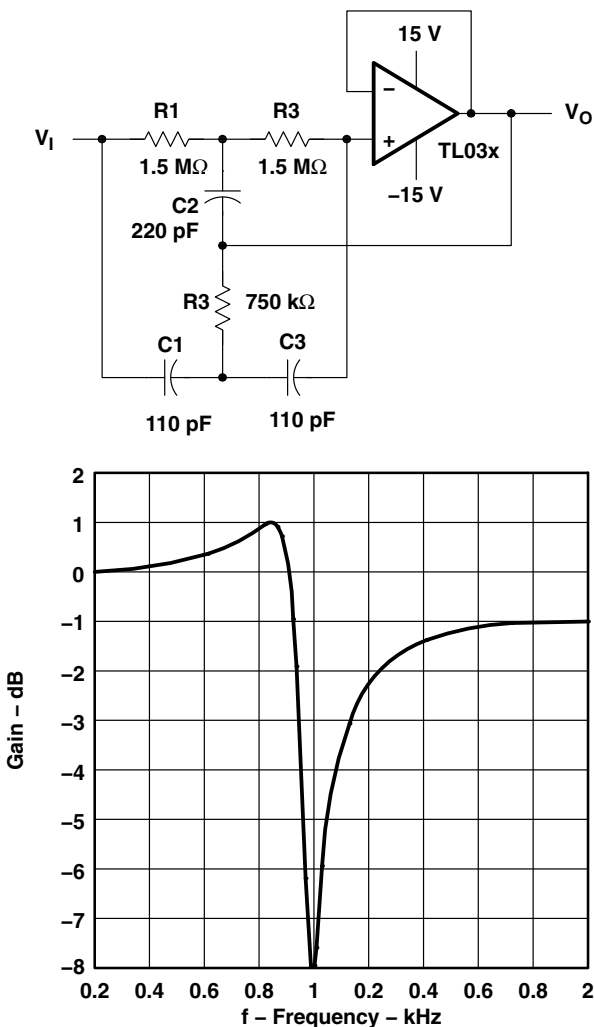


Figure 64. High-Q Notch Filter

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

APPLICATION INFORMATION

transimpedance amplifier

The low-power precision TL03x allows accurate measurement of low currents. The high input impedance and low offset voltage of the TL03xA greatly simplify the design of a transimpedance amplifier. At room temperature, this design achieves 10-bit accuracy with an error of less than 1/2 LSB.

Assuming that R2 is much less than R1 and ignoring error terms, the output voltage can be expressed as:

$$V_O = -I_{IN} \times R_F \left(\frac{R_1 + R_2}{R_2} \right)$$

Using the resistor values shown in the schematic for a 1-nA input current, the output voltage equals -0.1 V. If the V_O limit for the TL03xA is measured at ± 12 V, the maximum input current for these resistor values is ± 120 nA. Similarly, one LSB on a 10-bit scale corresponds to 12 mV of output voltage, or 120 pA of input current.

The following equation shows the effect of input offset voltage and input bias current on the output voltage:

$$V_O = - \left[V_{IO} + R_F (I_{IO} + I_{IB}) \right] \left(\frac{R_1 + R_2}{R_2} \right)$$

If the application requires input protection for the transimpedance amplifier, do not use standard PN diodes. Instead, use low-leakage Siliconix SN4117 JFETs (or equivalent) connected as diodes across the TL03xA inputs (see Figure 65).

As with all precision applications, special care must be taken to eliminate external sources of leakage and interference. Other precautions include using high-quality insulation, cleaning insulating surfaces to remove fluxes and other residue, and enclosing the application within a protective box.

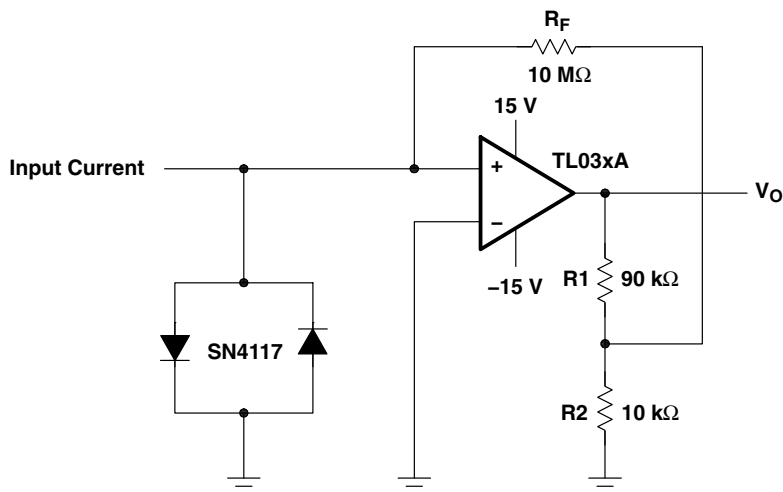


Figure 65. Transimpedance Amplifier

APPLICATION INFORMATION

4-mA to 20-mA current loops

Often, information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The following circuits give two variations of low-power current loops. The circuit in Figure 66 requires three wires from the transmitting to receiving circuitry, while the second variation in Figure 67 requires only two wires, but includes an extra integrated circuit. Both circuits benefit from the high input impedance of the TL03xA because many inexpensive sensors do not have low output impedance.

Assuming that the voltage at the noninverting input of the TL03xA is zero, the following equation determines the output current:

$$I_O = V_I \left(\frac{R_3}{R_1 \times R_S} \right) + 5V \left(\frac{R_3}{R_2 \times R_S} \right) = 0.16 \times V_I + 4\text{mA}$$

The circuits presently provide 4-mA to 20-mA output current for an input voltage of 0 to 100 mV. By modifying R1, R2, and R3, the input voltage range or the output current range can be adjusted.

Including the offset voltage of the operational amplifier in the above equation clearly illustrates why the low offset TL03xA was chosen:

$$\begin{aligned} I_O &= V_I \left(\frac{R_3}{R_1 \times R_S} \right) + 5V \left(\frac{R_3}{R_2 \times R_S} \right) - V_I \left(\frac{R_3}{R_1 \times R_S} + \frac{R_3}{R_2 \times R_S} + \frac{R_1}{R_S} \right) \\ &= 0.16 \times V_I + 4\text{mA} - 0.17 \times V_I \end{aligned}$$

For example, an offset voltage of 1 mV decreases the output current by 0.17 mA.

Due to the low power consumption of the TL03xA, both circuits have at least 2 mA available to drive the actual sensor from the 5-V reference node.

TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

APPLICATION INFORMATION

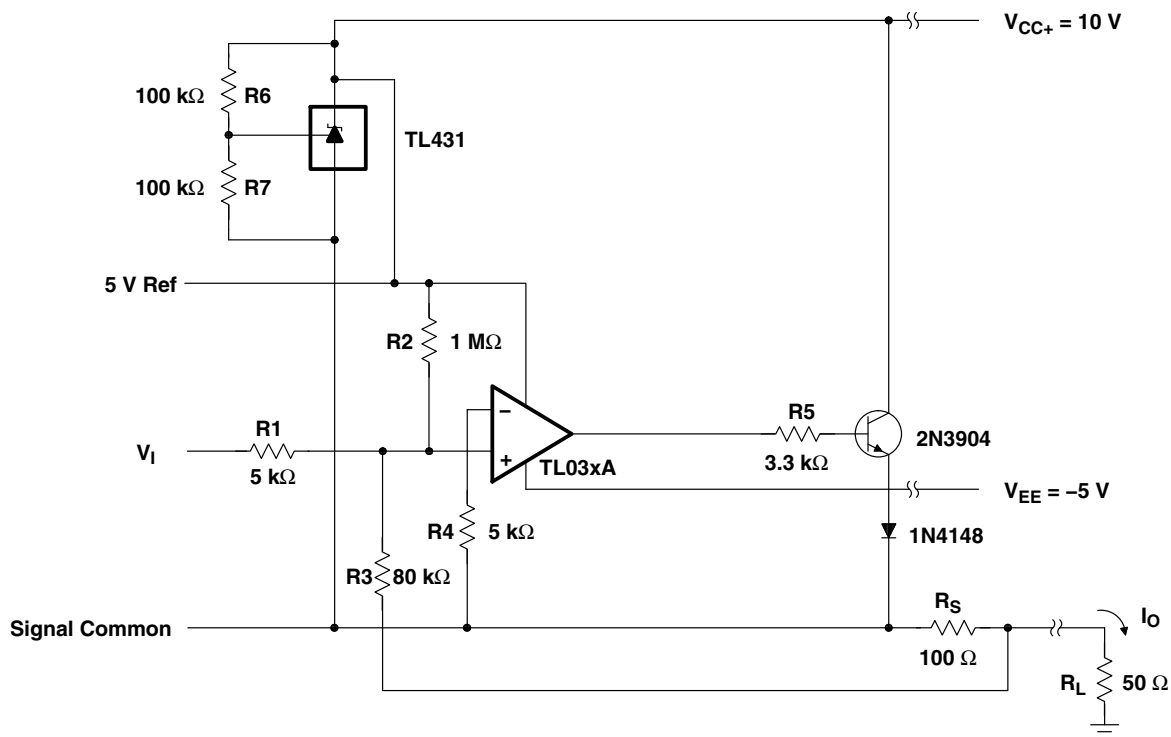


Figure 66. Three-Wire 4-mA to 20-mA Current Loop

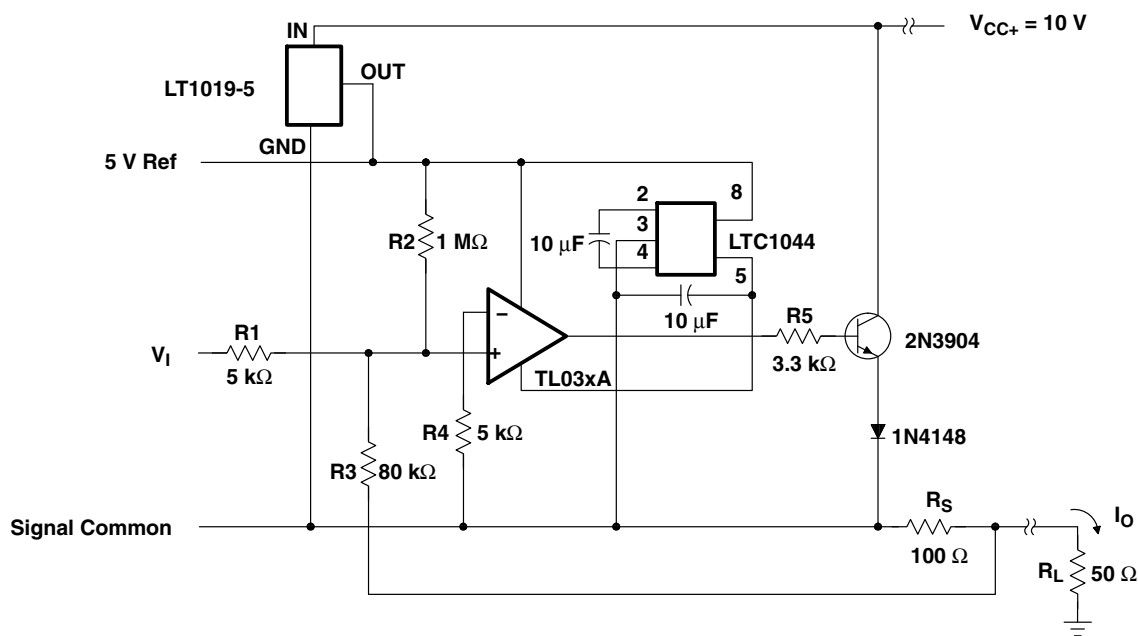


Figure 67. Two-Wire 4-mA to 20-mA Current Loop

APPLICATION INFORMATION

low-level light-detector preamplifier

Applications that need to detect small currents require high input-impedance operational amplifiers; otherwise, the bias currents of the operational amplifier camouflage the current being monitored. Phototransistors provide a current that is proportional to the light reaching the transistor. The TL03x allows even the small currents resulting from low-level light to be detected.

In Figure 68, if there is no light, the phototransistor is off and the output is high. As light is detected, the operational amplifier output begins pulling low. Adjusting R4 both compensates for offset voltage of the amplifier and adjusts the point of light detection by the amplifier.

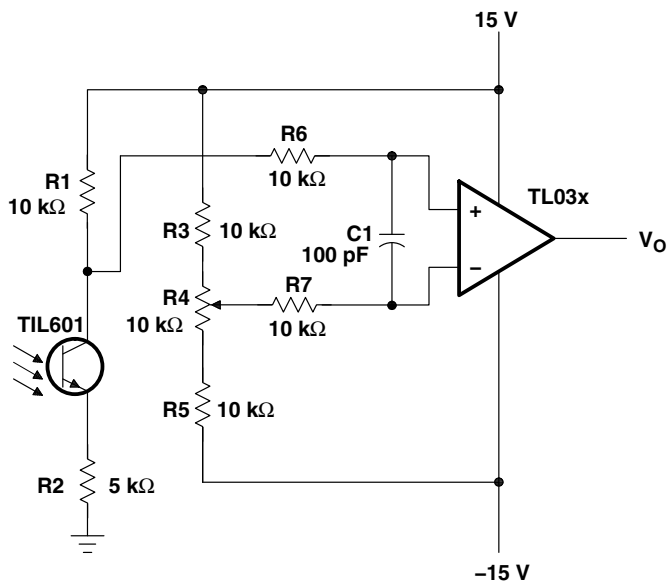


Figure 68. Low-Level Light-Detector Preamplifier

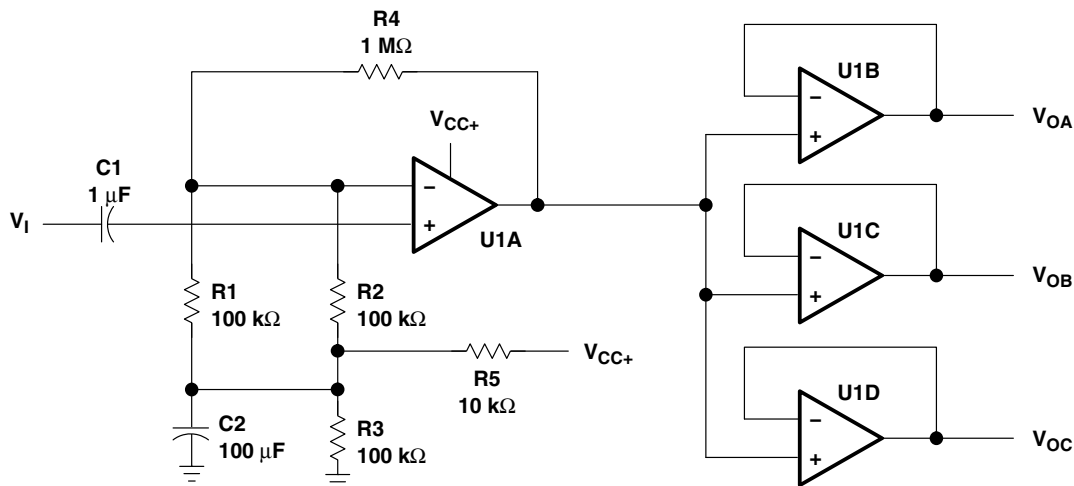
TL03x, TL03xA ENHANCED-JFET LOW-POWER LOW-OFFSET OPERATIONAL AMPLIFIERS

SLOS180C – FEBRUARY 1997 – REVISED DECEMBER 2001

APPLICATION INFORMATION

audio-distribution amplifier

This audio-distribution amplifier (see Figure 69) feeds the input signal to three separate output channels. U1A amplifies the input signal with a gain of 10, while U1B, U1C, and U1D serve as buffers to the output channels. The gain response of this circuit is very flat from 20 Hz to 20 kHz. The TL03x allows quick response to the input signal while maintaining low power consumption.



NOTE A: U1A through U1D = TL03x; $V_{CC+} = 5\text{ V}$

Figure 69. Audio-Distribution Amplifier Circuit

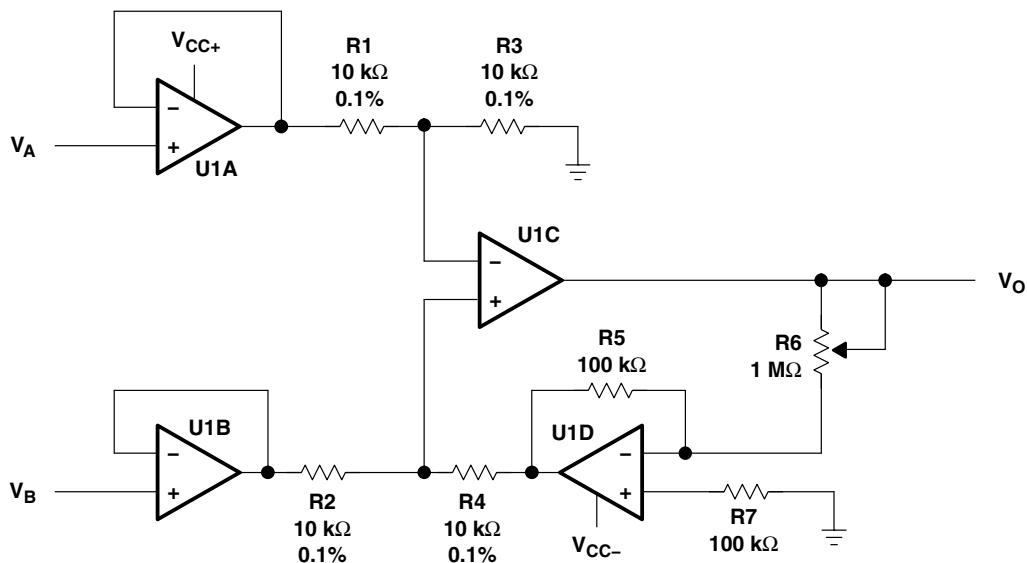
APPLICATION INFORMATION

instrumentation amplifier with linear gain adjust

The low offset voltage and low power consumption of the TL03x provide an accurate but inexpensive instrumentation amplifier (see Figure 70). This particular configuration offers the advantage that the gain can be linearly set by one resistor:

$$V_O = \frac{R6}{R5} \times (V_B - V_A)$$

Adjusting R6 varies the gain. The value of R6 always should be greater than, or equal to, the value of R5 to ensure stability. The disadvantage of this instrumentation amplifier topology is the high degree of CMRR degradation resulting from mismatches between R1, R2, R3, and R4. For this reason, these four resistors should be 0.1%-tolerance resistors.



NOTE A: U1A through U1D = TL03x; $V_{CC\pm} = \pm 15$ V

Figure 70. Instrumentation Amplifier With Linear Gain-Adjust Circuit

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TL031CD | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL031C | |
| TL031CDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL031C | Samples |
| TL031CP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL031CP | Samples |
| TL031ID | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL031I | |
| TL031IDG4 | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL031I | |
| TL031IP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL031IP | Samples |
| TL032ACD | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 032AC | |
| TL032ACDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 032AC | Samples |
| TL032ACP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL032ACP | Samples |
| TL032AID | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 032AI | |
| TL032AIDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 032AI | Samples |
| TL032AIP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL032AIP | Samples |
| TL032CD | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL032C | |
| TL032CDE4 | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL032C | |
| TL032CDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL032C | Samples |
| TL032CP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL032CP | Samples |
| TL032CPE4 | ACTIVE | PDIP | P | 8 | 50 | TBD | Call TI | Call TI | 0 to 70 | | Samples |
| TL032CPSR | LIFEBUY | SO | PS | 8 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T032 | |
| TL032ID | LIFEBUY | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL032I | |
| TL032IDR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL032I | Samples |
| TL032IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| TL032IP | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL032IP | Samples |
| TL034ACD | LIFEBUY | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL034AC | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TL034ACDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL034AC | Samples |
| TL034ACN | LIFEBUY | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL034ACN | |
| TL034AID | LIFEBUY | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL034AI | |
| TL034AIDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL034AI | Samples |
| TL034AIN | LIFEBUY | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL034AIN | |
| TL034CD | LIFEBUY | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL034C | |
| TL034CDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL034C | Samples |
| TL034CN | LIFEBUY | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | TL034CN | |
| TL034CNSR | LIFEBUY | SO | NS | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TL034 | |
| TL034CPW | LIFEBUY | TSSOP | PW | 14 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T034 | |
| TL034CPWR | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | T034 | Samples |
| TL034ID | LIFEBUY | SOIC | D | 14 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL034I | |
| TL034IDR | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TL034I | Samples |
| TL034IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| TL034IN | LIFEBUY | PDIP | N | 14 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | TL034IN | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL031CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL032ACDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL032AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL032CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL032CPSR | SO | PS | 8 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| TL032IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL034ACDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL034AIDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL034CDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TL034CNSR | SO | NS | 14 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TL034CPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TL034IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL031CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL032ACDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL032AIDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL032CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL032CPSR | SO | PS | 8 | 2000 | 356.0 | 356.0 | 35.0 |
| TL032IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL034ACDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL034AIDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL034CDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |
| TL034CNSR | SO | NS | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TL034CPWR | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| TL034IDR | SOIC | D | 14 | 2500 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TL031CD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL031CP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL031ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL031IDG4 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL031IP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL032ACD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL032ACP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL032AID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL032AIP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL032CD | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL032CDE4 | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL032CP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL032ID | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| TL032IP | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| TL034ACD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL034ACN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL034AID | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL034AIN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL034CD | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL034CN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| TL034CPW | PW | TSSOP | 14 | 90 | 530 | 10.2 | 3600 | 3.5 |
| TL034ID | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| TL034IN | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



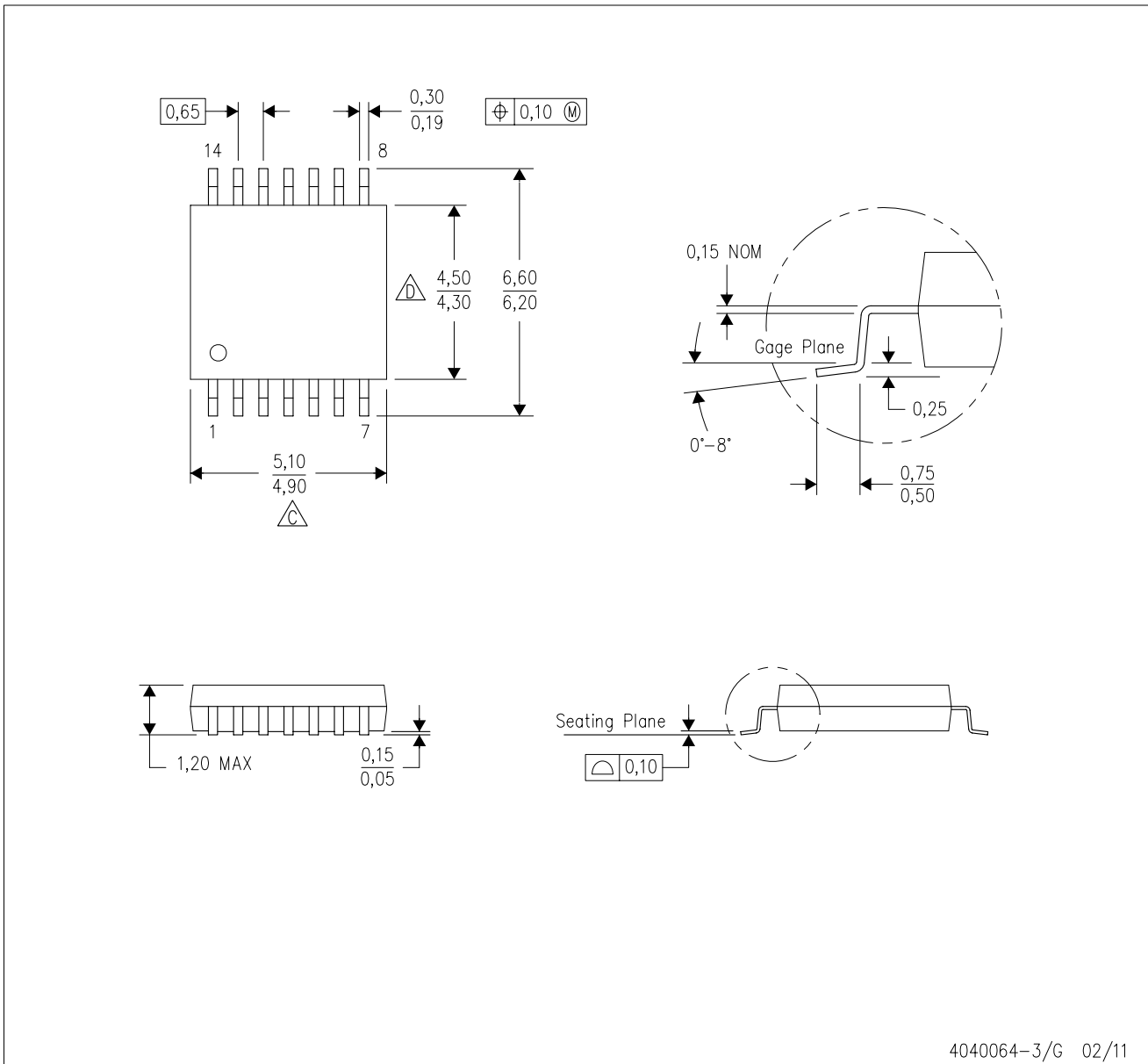
4211283-3/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

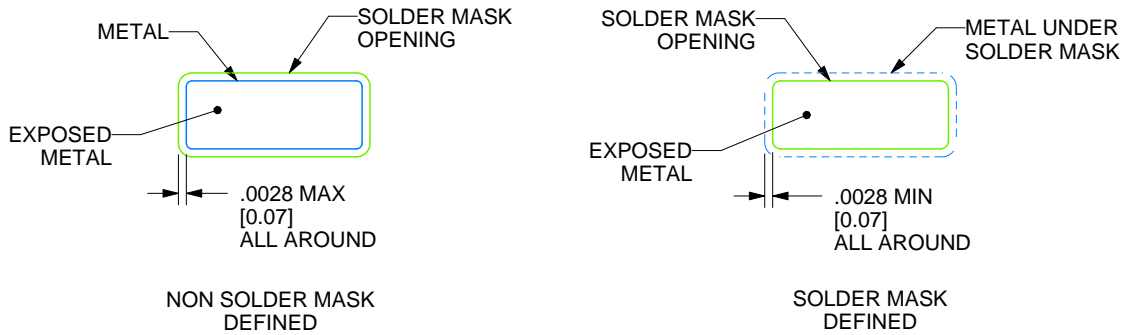
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated