SN74AHCT1G86Q-Q1 Automotive Single 2-Input Exclusive-OR Gate

1 Features

- Qualified for automotive applications
- Operating range of 4.5 V to 5.5 V
- Max t_{pd} of 8 ns at 5 V
- Low power consumption, 10-µA max I_{CC}
- ±8-mA output drive at 5 V
- Inputs are TTL-voltage compatible

2 Applications

- Enable or disable a digital signal
- Controlling an indicator LED
- Translation between communication modules and system controllers

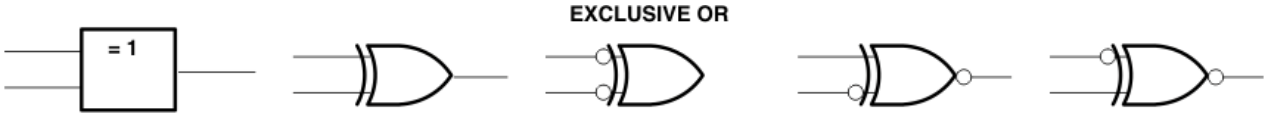
3 Description

The SN74AHCT1G86Q-Q1 is a single 2-input exclusive-OR gate. The device performs the Boolean function $Y = A \oplus B$ or $Y = \overline{A}B + A\overline{B}$ in positive logic.

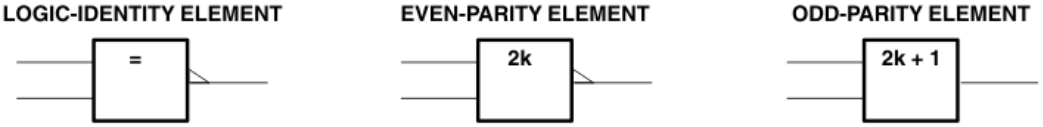
Table 3-1. Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE(3)
SN74AHCT1G86Q-Q1	DCK (SC-70, 5)	2 mm x 2.1 mm	2 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



These five equivalent exclusive-OR symbols are valid for an SN74AHCT1G86 gate in positive logic; negation may be shown at any two ports.



The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

Exclusive-OR Logic

Table of Contents

4 Revision History

Changes from Revision * (December 2010) to Revision A (October 2023)	Page
• Added *Applications* section, *Package Information* table, *Pin Functions* table, *Thermal Information* table, *Device Functional Modes, Application and Implementation* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Updated RθJA values: DCK = 252 to 289.2, all values in °C/W	4

5 Pin Configuration and Functions

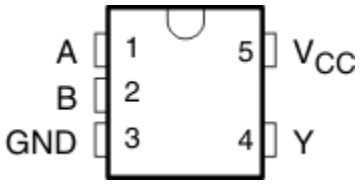


Figure 5-1. DCK Package (Top View)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	A	I	A input
2	B	I	B input
3	GND	–	Ground pin
4	Y	O	Output
5	Vcc	–	Power pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

6 Specifications

6.1 Absolute Maximum Ratings

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I (1)	Input voltage		–0.5	7	V
V_O (1)	Output voltage range applied in the high- or low-state		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 V		–20	V
I_{OK}	Output clamp current	V_O < 0 V or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 V to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		–8	mA
I_{OL}	Low-level output current		8	mA
Δt/ΔV	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	–40	125	°C

6.3 Thermal Information

THERMAL METRIC(1)		DCK (SC-70)	UNIT
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	289.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA		4.5 V	4.4	4.5		4.4		V
	I_{OH} = –8 mA			3.94			3.8		
V_{OL}	I_{OL} = 50 µA		4.5 V			0.1		0.1	V
	I_{OL} = 8 mA					0.36		0.44	
I_I	V_I = 5.5 V or GND		0 V to 5.5 V			±0.1		±1	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0 A	5.5 V			1		10	µA
ΔI_{CC} (1)	One input at 3.4 V,	Other inputs at GND or V_{CC}	5.5 V			1.35		1.5	mA
C_I	V_I = V_{CC} or GND		5 V			10		10	pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.

6.5 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V, T_A = –40°C to 125°C, see Load Circuit and Voltage Waveforms

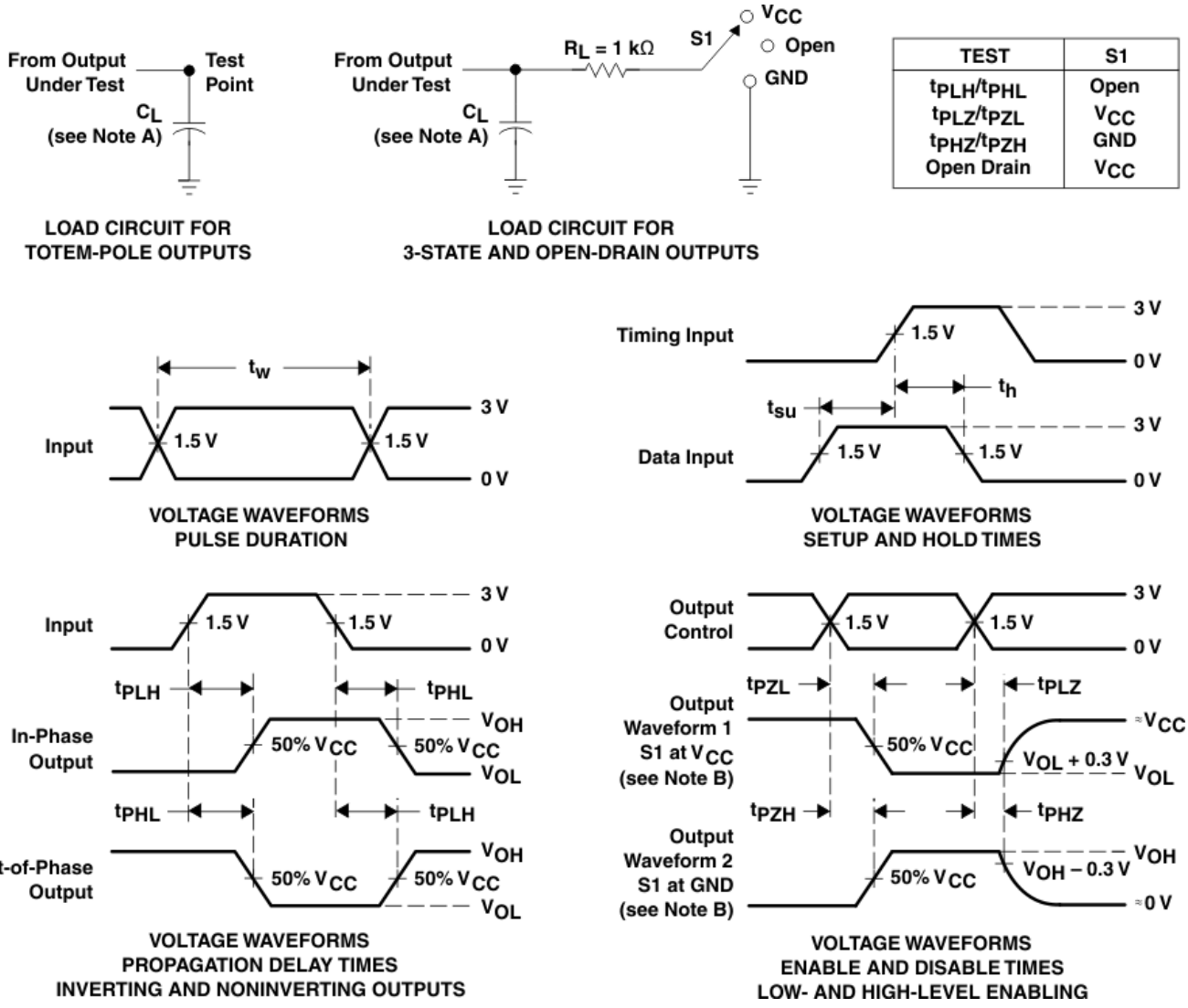
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A or B	Y	C_L = 50 pF		5.5	7.9	1	9	ns
t_{PHL}					5.5	7.9	1	9	

6.6 Operating Characteristics

V_{CC} = 5 V ±0.5 V, T_A = –40°C to 125°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, f = 1 MHz	18	pF

7 Parameter Measurement Information



A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤3 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AHCT1G86Q-Q1 contains four independent 2-input AND Gates with Schmitt-trigger inputs. Each gate performs the Boolean function Y = A × B in positive logic. The output level is referenced to the supply voltage (V_{CC}) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

8.2 Functional Block Diagram

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

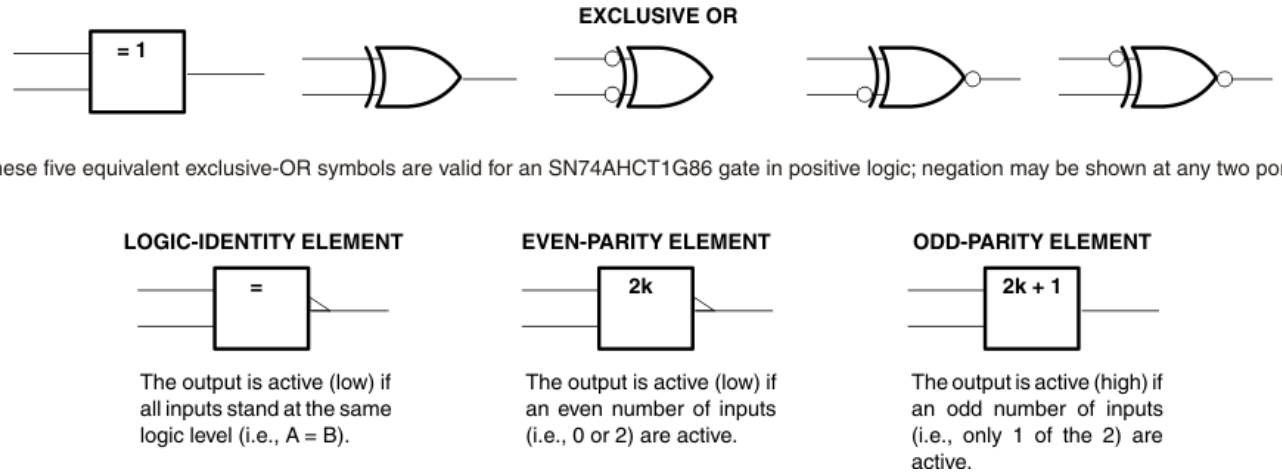


Figure 8-1. Exclusive-OR Logic

8.3 Feature Description

8.3.1 TTL-Compatible CMOS Inputs

This device includes TTL-compatible CMOS inputs. These inputs are specifically designed to interface with TTL logic devices by having a reduced input voltage threshold.

TTL-compatible CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law (R = V ÷ I).

TTL-compatible CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave TTL-compatible CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

8.3.2 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.3 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in Figure 8-2.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

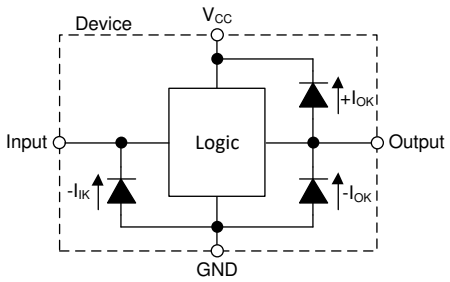


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

Functional Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74AHCT1G86 is a Low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V V_{IL} and 2-V V_{IH}. This feature makes it Ideal for translating up from 3.3 V to 5 V.

9.2 Typical Application

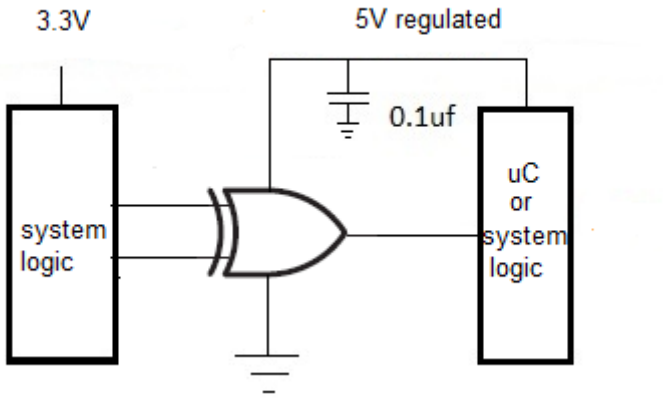


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHCT1G86Q-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74AHCT1G86Q-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74AHCT1G86Q-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross to be considered a logic LOW, and to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHCT1G86Q-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; it will, however, ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHCT1G86Q-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than (V_{CC} / $I_{O(max)}$) Ω, so that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

9.2.3 Application Curves

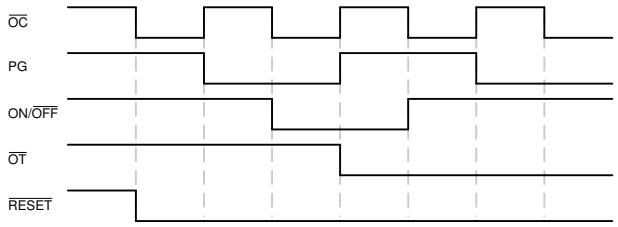


Figure 9-2. Application Timing Diagram

9.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Section 6.2*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-µF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01-µF or 0.022-µF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

9.4 Layout

9.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

9.4.1.1 Layout Example

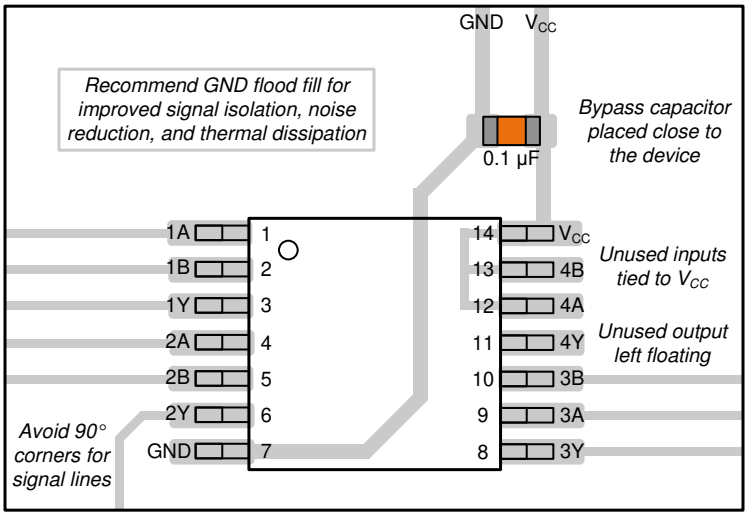


Figure 9-3. Example Layout for the SN74AHCT1G86Q-Q1

10 Device and Documentation Support

10.1 Documentation Support (Analog)

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAHCT1G86QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	B5S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74AHCT1G86-Q1 :

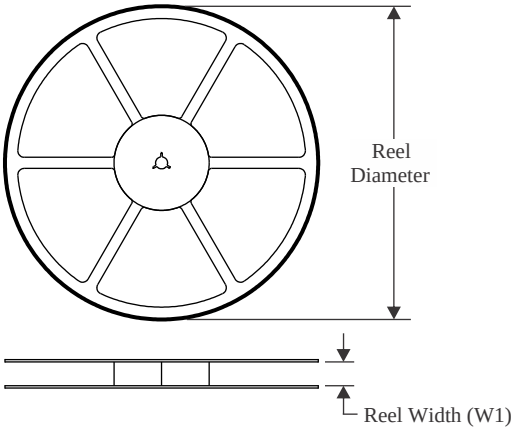
- Catalog : SN74AHCT1G86

NOTE: Qualified Version Definitions:

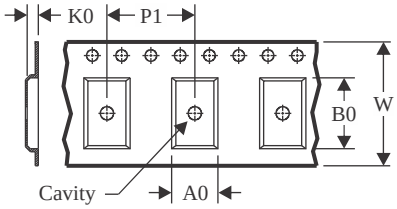
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

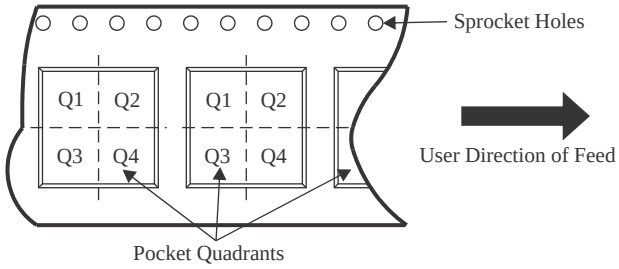


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

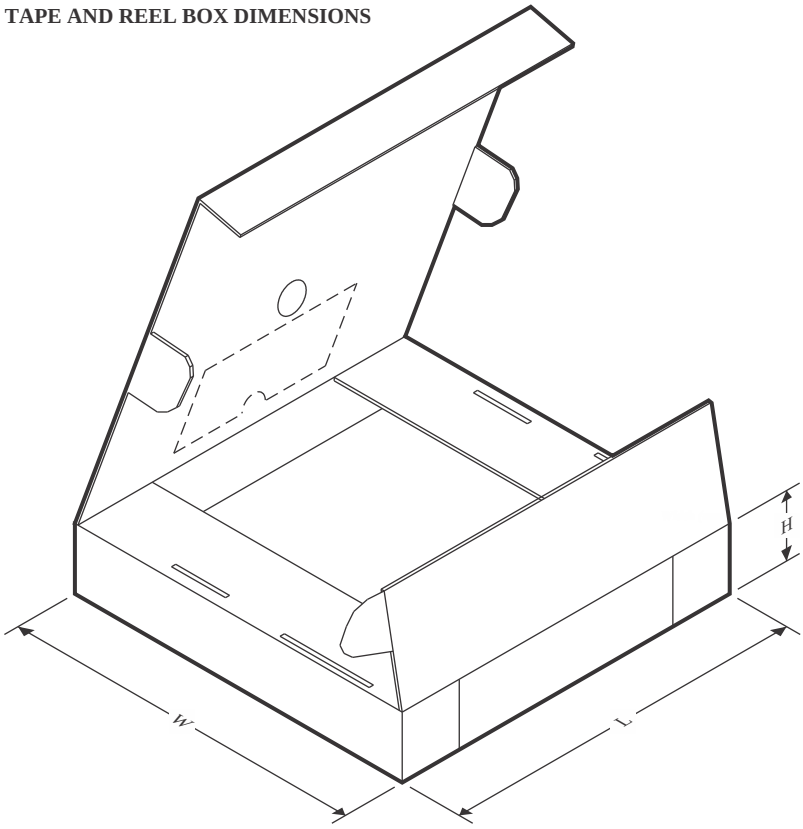
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAHCT1G86QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

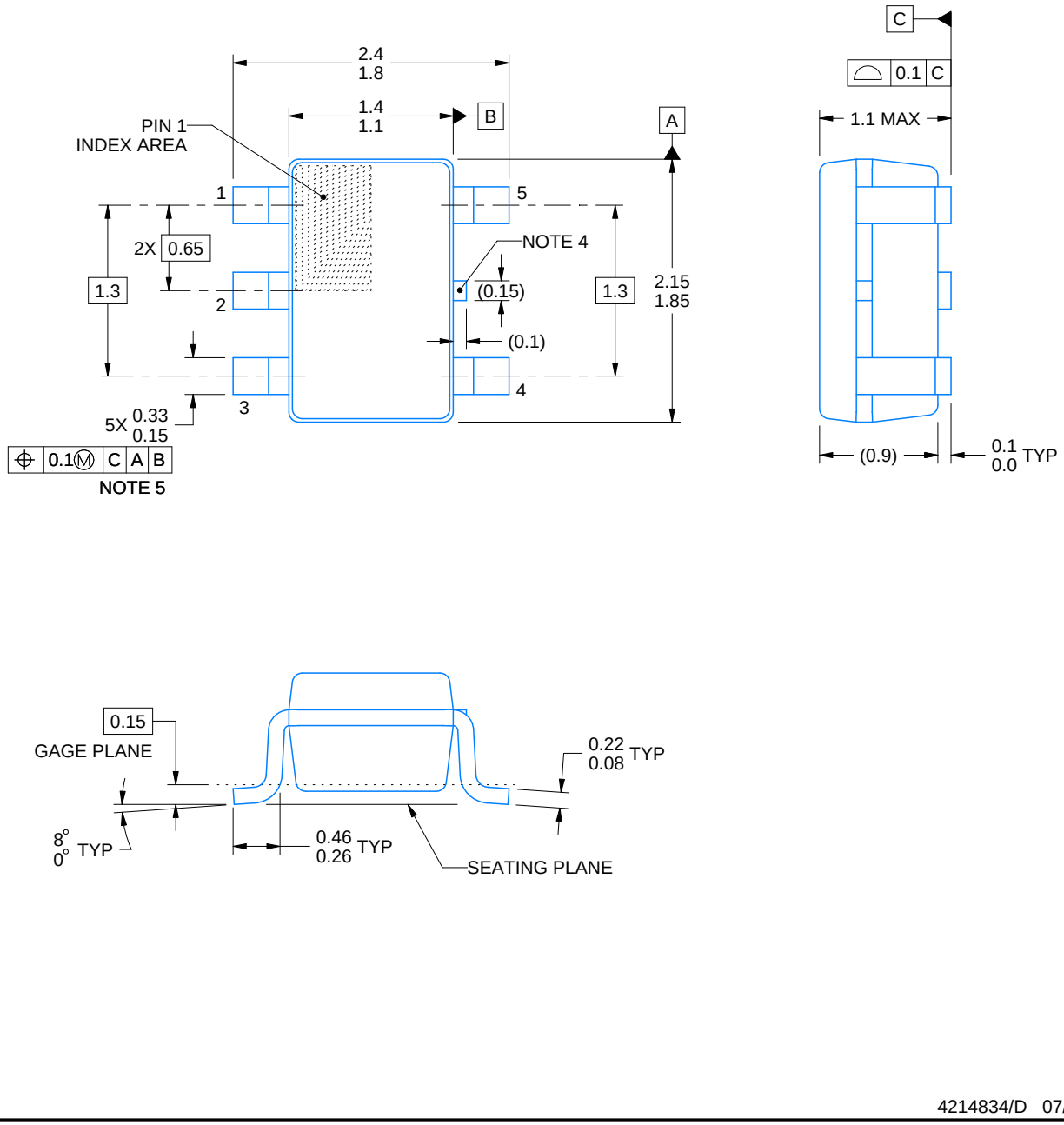
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAHCT1G86QDCKRQ1	SC70	DCK	5	3000	202.0	201.0	28.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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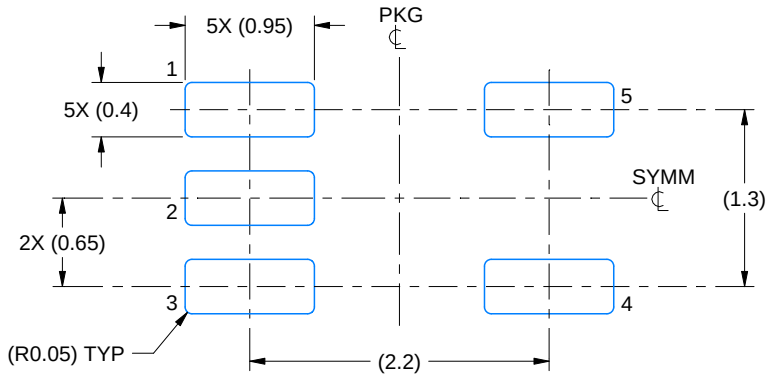
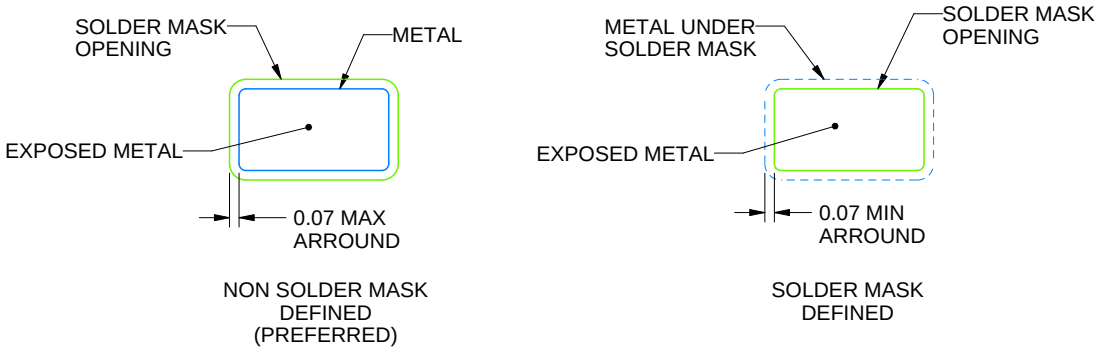
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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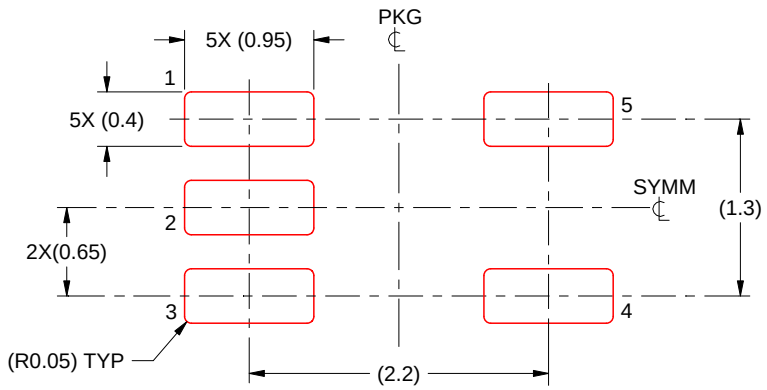
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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