

INA131

Precision $G = 100$ INSTRUMENTATION AMPLIFIER

FEATURES

- **LOW OFFSET VOLTAGE:** $50\mu\text{V}$ max
- **LOW DRIFT:** $0.25\mu\text{V}/^\circ\text{C}$ max
- **LOW INPUT BIAS CURRENT:** 2nA max
- **HIGH COMMON-MODE REJECTION:** 110dB min
- **INPUT OVERVOLTAGE PROTECTION:** $\pm 40\text{V}$
- **WIDE SUPPLY RANGE:** ± 2.25 to $\pm 18\text{V}$
- **LOW QUIESCENT CURRENT:** 3mA
- **8-PIN PLASTIC DIP**

DESCRIPTION

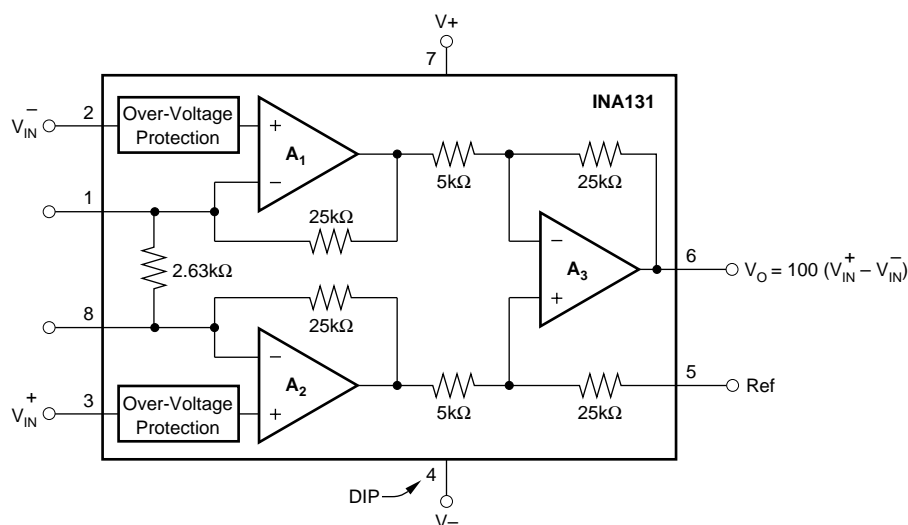
The INA131 is a low cost, general purpose $G = 100$ instrumentation amplifier offering excellent accuracy. Its 3-op amp design and small size make it ideal for a wide range of applications.

On-chip laser trimmed resistors accurately set a fixed gain of 100. The INA131 is laser trimmed to achieve very low offset voltage ($50\mu\text{V}$ max), drift ($0.25\mu\text{V}/^\circ\text{C}$ max), and high CMR (110dB min). Internal input protection can withstand up to $\pm 40\text{V}$ inputs without damage.

The INA131 is available in a 8-pin plastic DIP. They are specified over the -40°C to $+85^\circ\text{C}$ temperature range.

APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION



SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $R_L = 2\text{k}\Omega$, unless otherwise noted.

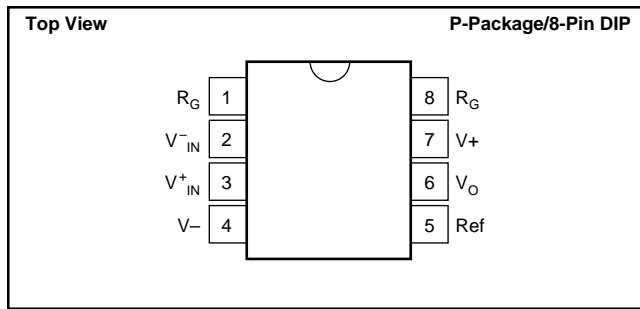
PARAMETER	CONDITIONS	INA131BP			INA131AP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT								
Offset Voltage, RTI	$T_A = +25^\circ\text{C}$ $T_A = T_{\text{MIN}}$ to T_{MAX} $V_S = \pm 2.25\text{V}$ to $\pm 18\text{V}$		± 10	± 50		± 25	± 125	μV
Initial			± 0.1	± 0.25		± 0.25	± 1	$\mu\text{V}/^\circ\text{C}$
vs Temperature			0.5	3		*	*	$\mu\text{V}/\text{V}$
vs Power Supply			0.2			*	*	$\mu\text{V}/\text{mo}$
Long-Term Stability			$10^{10} \parallel 6$			*	*	$\Omega \parallel \text{pF}$
Impedance, Differential			$10^{10} \parallel 6$			*	*	$\Omega \parallel \text{pF}$
Common-Mode			± 11		*	*	V	
Input Common-Mode Range				± 40			*	V
Safe Input Voltage								dB
Common-Mode Rejection	$V_{\text{CM}} = \pm 10\text{V}$, $\Delta R_S = 1\text{k}\Omega$	110	120		106	110		
BIAS CURRENT			± 0.5	± 2		*	± 5	nA
vs Temperature			± 8			*		$\text{pA}/^\circ\text{C}$
OFFSET CURRENT			± 0.5	± 2		*	± 5	nA
vs Temperature			± 8			*		$\text{pA}/^\circ\text{C}$
NOISE VOLTAGE, RTI	$R_S = 0\Omega$							
f = 10Hz			16			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 100Hz			12			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 1kHz			12			*		$\text{nV}/\sqrt{\text{Hz}}$
f = 10kHz			12			*		$\text{nV}/\sqrt{\text{Hz}}$
$f_B = 0.1\text{Hz}$ to 10Hz			0.4			*		$\mu\text{Vp-p}$
Noise Current								
f = 10Hz			0.4			*		$\text{pA}/\sqrt{\text{Hz}}$
f = 1kHz			0.2			*		$\text{pA}/\sqrt{\text{Hz}}$
$f_B = 0.1\text{Hz}$ to 100Hz			18			*		pAp-p
GAIN								
Gain Error ⁽¹⁾			± 0.01	± 0.024		*	± 0.1	%
Resistor Value ⁽²⁾			± 10	± 40		*	*	%
Gain vs Temperature			± 5	± 10		*	± 20	$\text{ppm}/^\circ\text{C}$
Nonlinearity			± 0.0003	± 0.002		*	± 0.004	% of FSR
OUTPUT								
Voltage	$I_O = 5\text{mA}$, T_{MIN} to T_{MAX} $V_S = \pm 11.4\text{V}$, $R_L = 2\text{k}\Omega$ $V_S = \pm 2.25\text{V}$, $R_L = 2\text{k}\Omega$ Stable Operation	± 13.5	± 13.7		*	*		V
		± 10	10.5		*	*		V
		± 1	1.5		*	*		V
			1000		*	*		pF
Load Capacitance, max								mA
Short Circuit Current				$+20/-15$		*		
FREQUENCY RESPONSE								
Bandwidth, -3dB	$V_O = \pm 10\text{V}$		70			*		kHz
Slew Rate		0.3	0.7		*	*		$\text{V}/\mu\text{s}$
Settling Time, 0.01%			100		*	*		μs
Overload Recovery		50% Overdrive		20		*	*	μs
POWER SUPPLY								
Voltage Range	$V_{\text{IN}} = 0\text{V}$	± 2.25	± 15	± 18	*	*	*	V
Current			± 2.2	± 3	*	*	*	mA
TEMPERATURE RANGE								
Specification		-40		85	*		*	$^\circ\text{C}$
Operating		-40		125	*		*	$^\circ\text{C}$
θ_{JA}			100			*		$^\circ\text{C}/\text{W}$

* Specification same as INA131BP.

NOTES: (1) $R_L = 10\text{k}\Omega$. (2) Absolute value of internal gain-setting resistors. (Gain depends on resistor ratios.)

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

PIN CONFIGURATION



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
INA131AP	8-Pin Plastic DIP	006	-40°C to +85°C
INA131BP	8-Pin Plastic DIP	006	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage	±18V
Input Voltage Range	±40V
Output Short Circuit (to ground)	Continuous
Operating Temperature	-40°C to +125°C
Storage Temperature	-40°C to +125°C
Junction Temperature	+150°C
Lead Temperature (soldering -10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage.



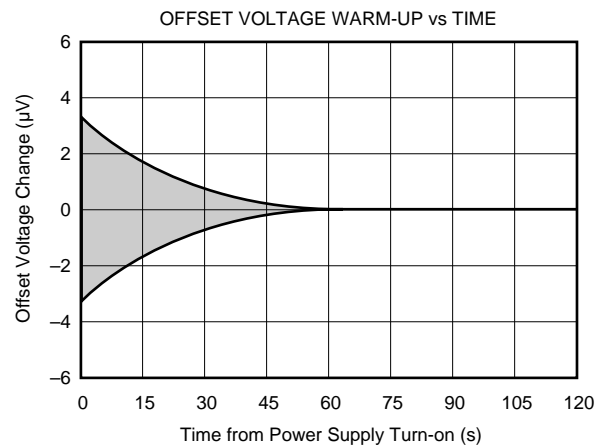
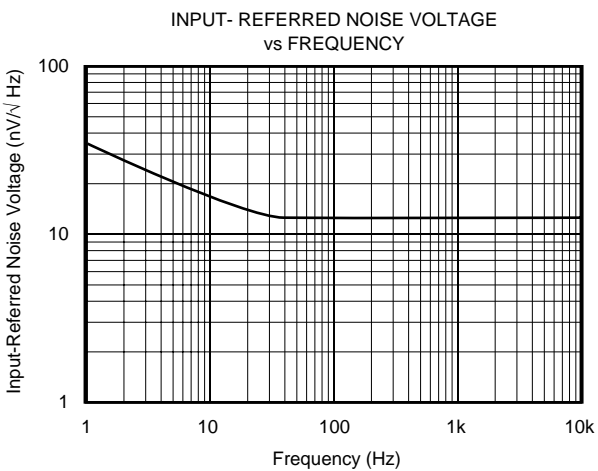
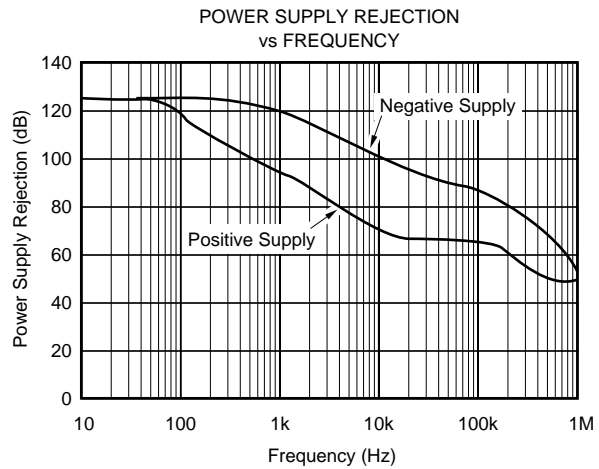
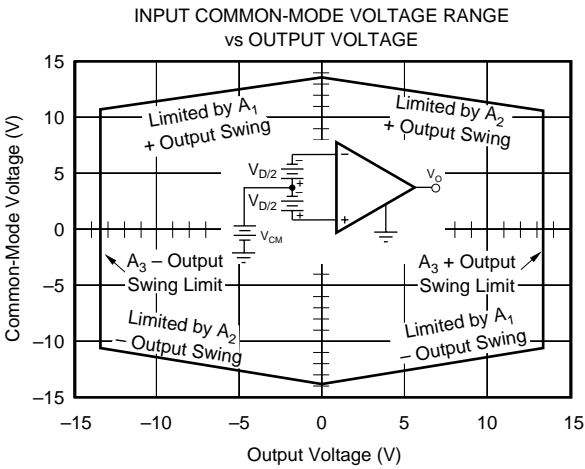
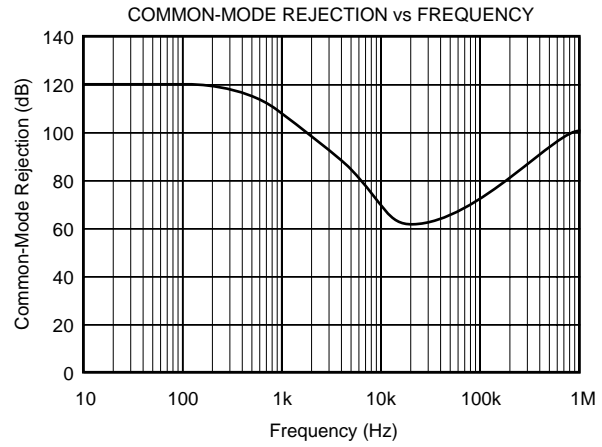
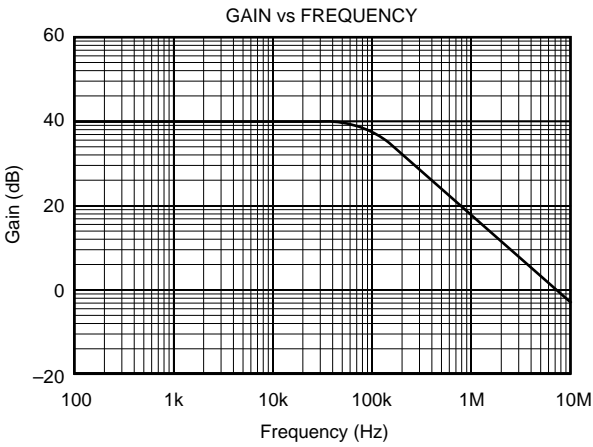
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

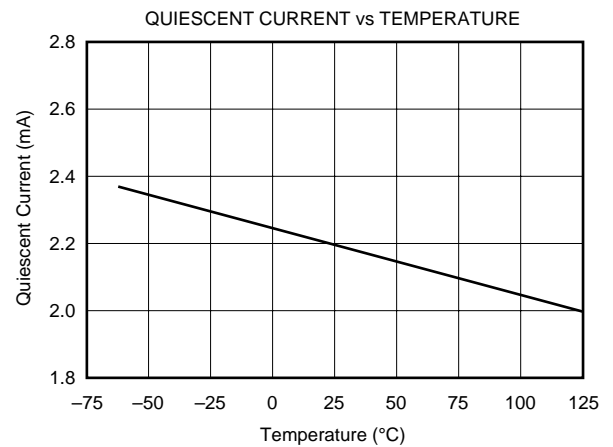
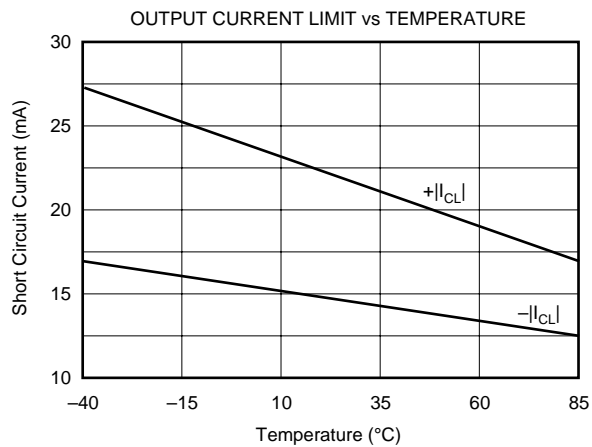
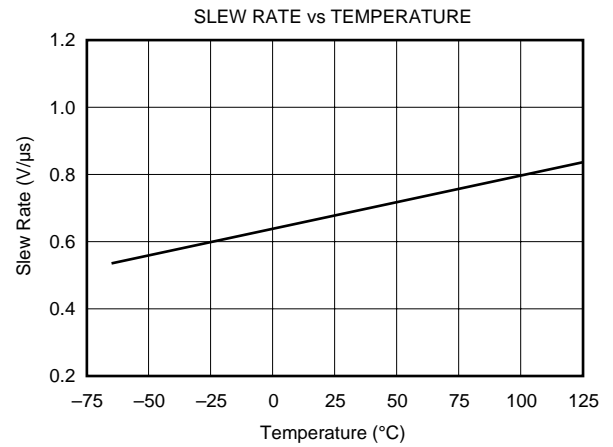
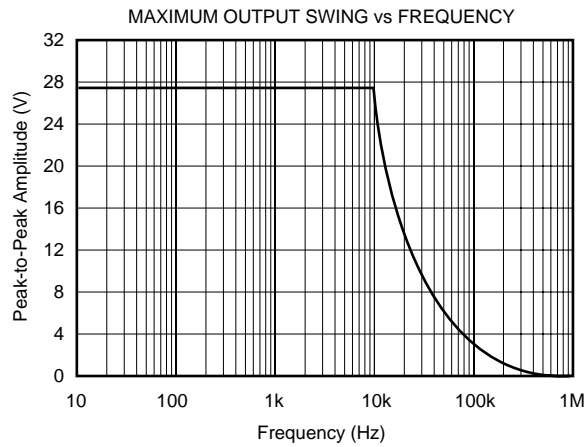
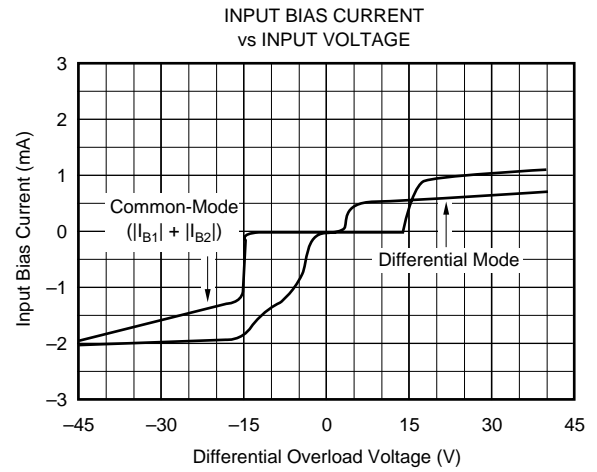
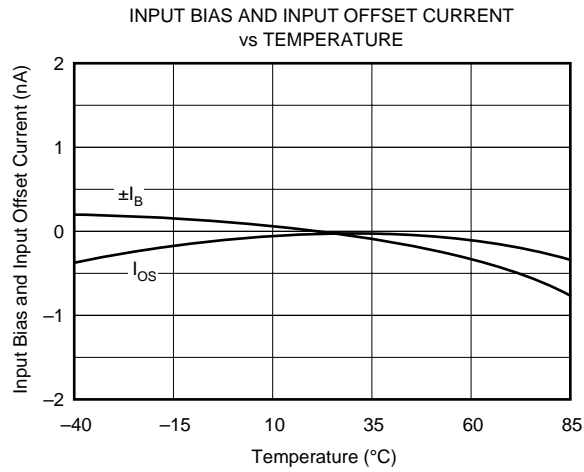
TYPICAL PERFORMANCE CURVES

At 25°C, $V_S = \pm 15V$, unless otherwise noted.



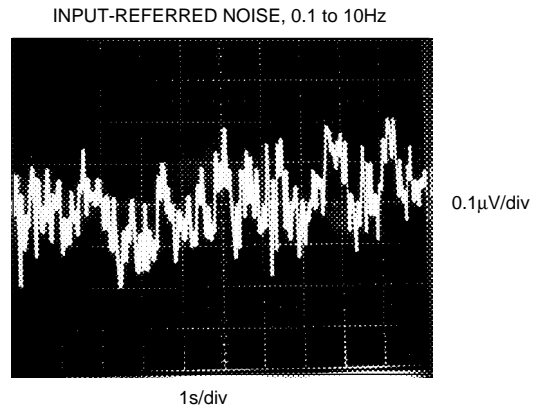
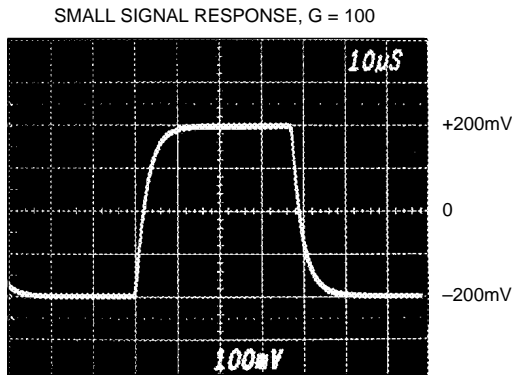
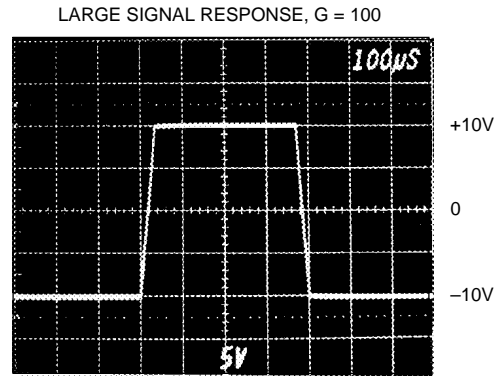
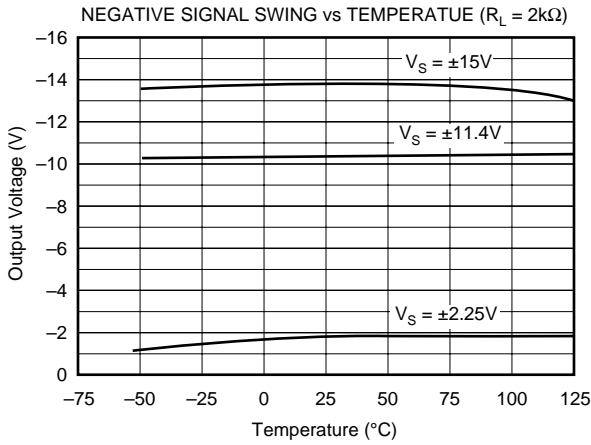
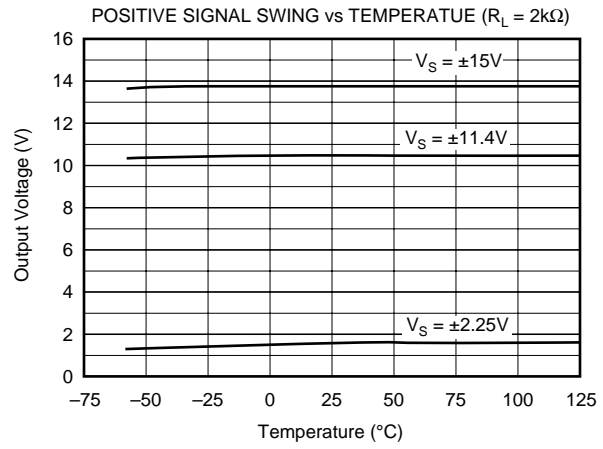
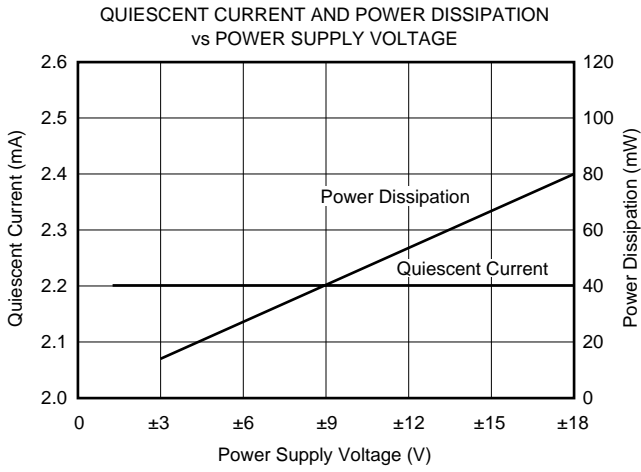
TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, $V_S = \pm 15V$, unless otherwise noted.



TYPICAL PERFORMANCE CURVES (CONT)

At 25°C, $V_S = \pm 15V$, unless otherwise noted.



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA131. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a device with 110dB CMR to degrade to approximately 106dB CMR.

SETTING THE GAIN

No external resistors are required for $G = 100$. On-chip laser-trimmed resistors set the gain, providing excellent gain accuracy and temperature stability. Gain is distributed between the input and output stages of the INA131. Bandwidth is increased by approximately five times (compared to the INA114 in $G = 100$). Input common-mode range is also improved (see “Input Common-Mode Range”).

Although the INA131 is primarily intended for fixed $G = 100$ applications, the gain can be increased by connecting an external resistor to the R_G pins. The internal resistors are trimmed for precise ratios, not to absolute values, so the influence of an external resistor will vary from device to

device. Absolute accuracy of the internal values is $\pm 40\%$. The nominal gain with an external R_G resistor can be calculated by:

$$G = 100 + \frac{250 \text{ k}\Omega}{R_G} \quad (1)$$

Where: R_G is the external gain resistor.

Accuracy of the 250kΩ term is $\pm 40\%$.

The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. R_G 's contribution to gain accuracy and drift can be directly inferred from the gain equation (1).

NOISE PERFORMANCE

The INA131 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-Input Instrumentation Amplifier may provide lower noise.

Low frequency noise of the INA131 is approximately 0.4μVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of state-of-the-art chopper-stabilized amplifiers.

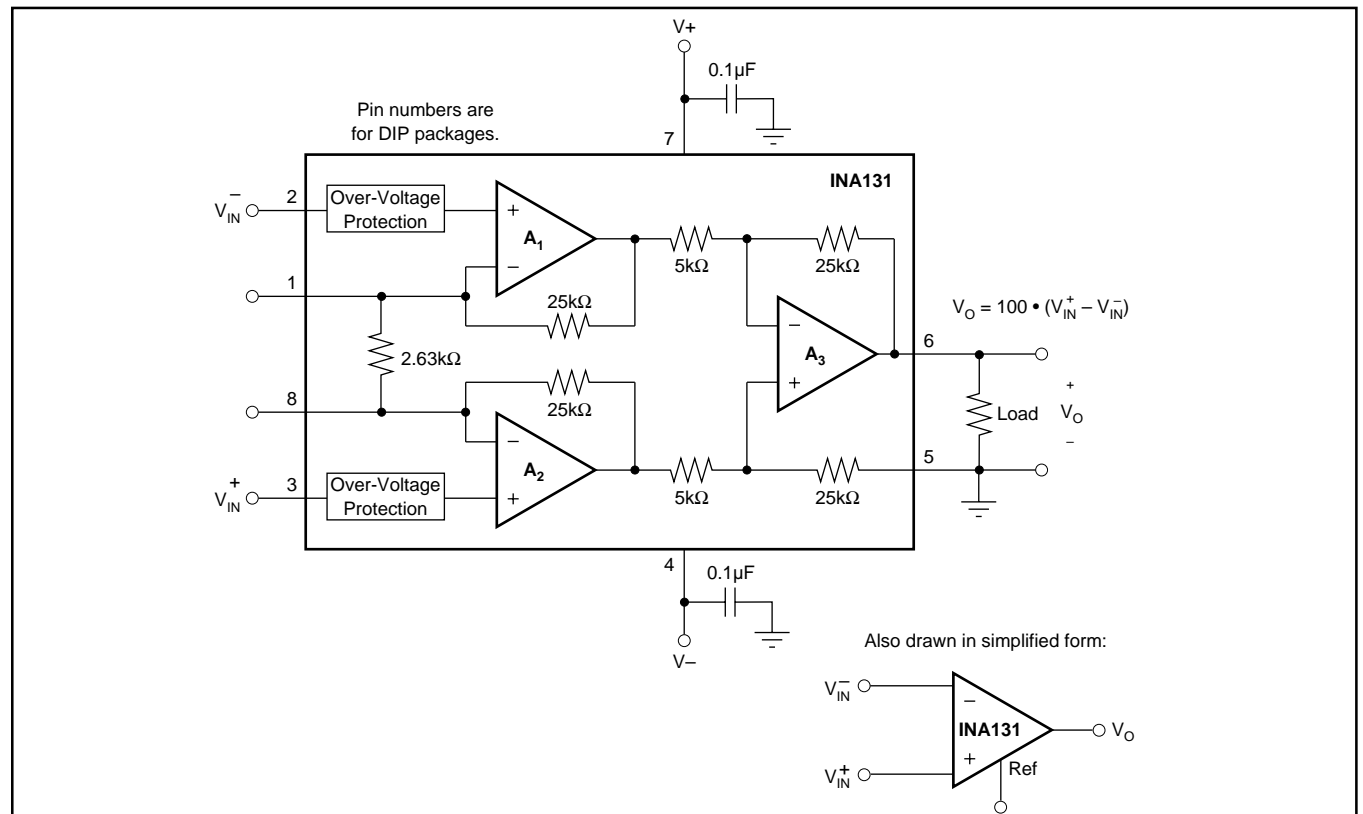


FIGURE 1. Basic Connections.

OFFSET TRIMMING

The INA131 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering trim voltage with an op amp as shown.

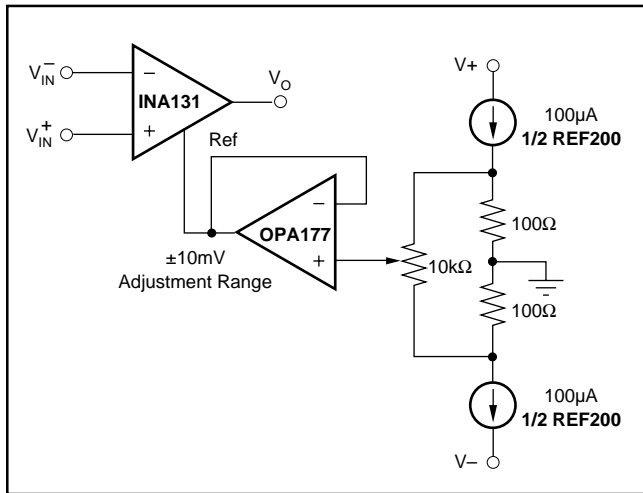


FIGURE 2. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA131 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than $\pm 1\text{nA}$ (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA131 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA131 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA131 is approximately $\pm 13.75\text{V}$ (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range is limited by the output voltage swing of the input amplifiers, A_1 and A_2 . The 5V/V output stage gain of the INA131 reduces this effect. Compared to the

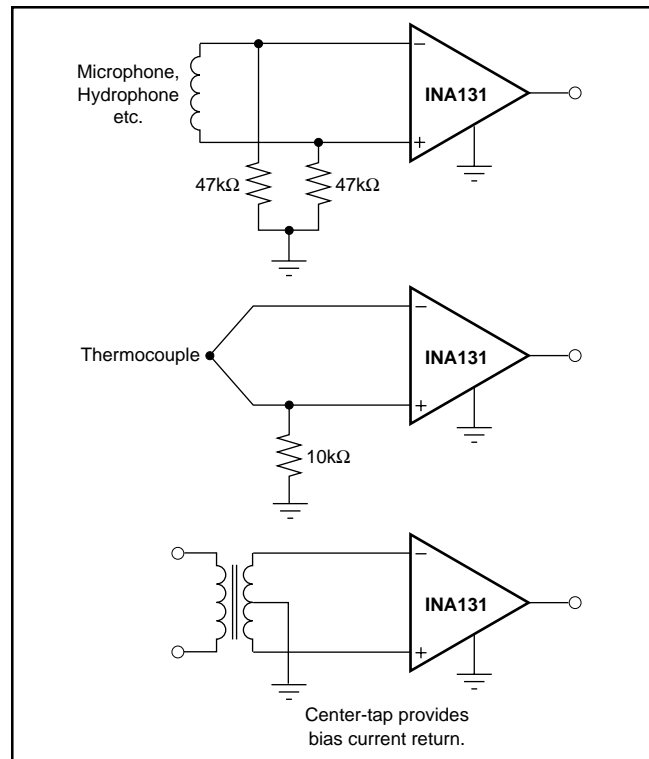


FIGURE 3. Providing an Input Common-Mode Current Path.

INA114 and other unity output gain instrumentation amplifiers, the INA131 provides several additional volts of input common-mode range with full output voltage swing. See the typical performance curve “Input Common-Mode Range vs Output Voltage”.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of $+20\text{V}$ on one input and $+40\text{V}$ on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to the nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA131 will be near 0V even though both inputs are overloaded.

INPUT PROTECTION

The inputs of the INA131 are individually protected for voltages up to $\pm 40\text{V}$. For example, a condition of -40V on one input and $+40\text{V}$ on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve “Input Bias Current vs Input Voltage” shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

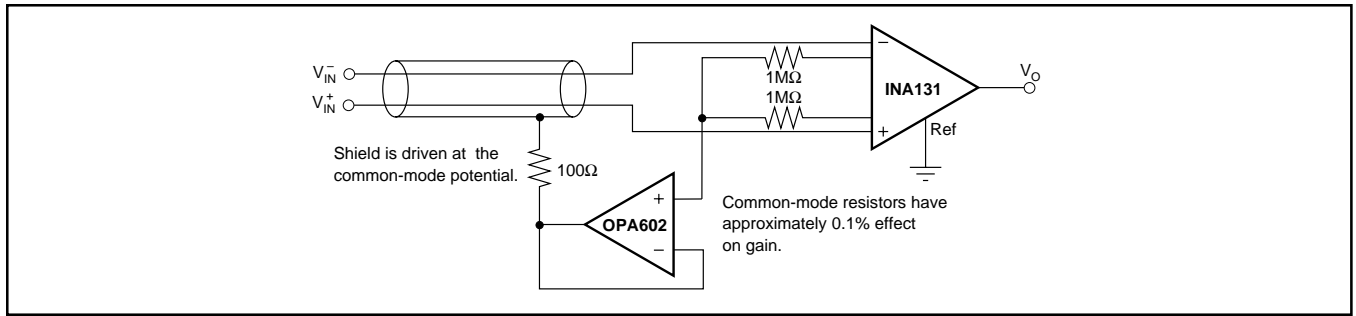


FIGURE 4. Shield Driver Circuit.

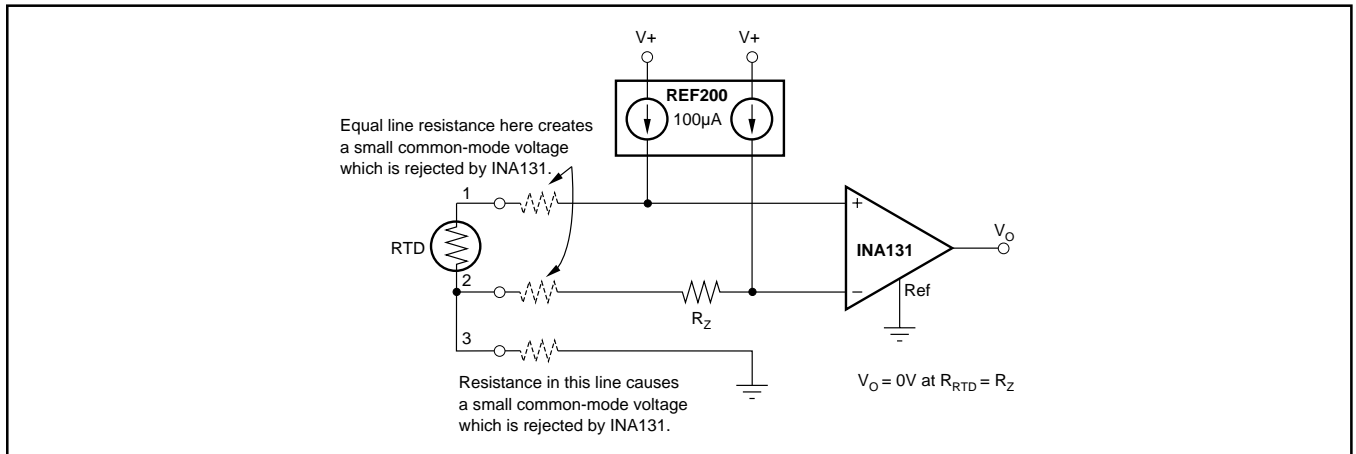


FIGURE 5. RTD Temperature Measurement Circuit.

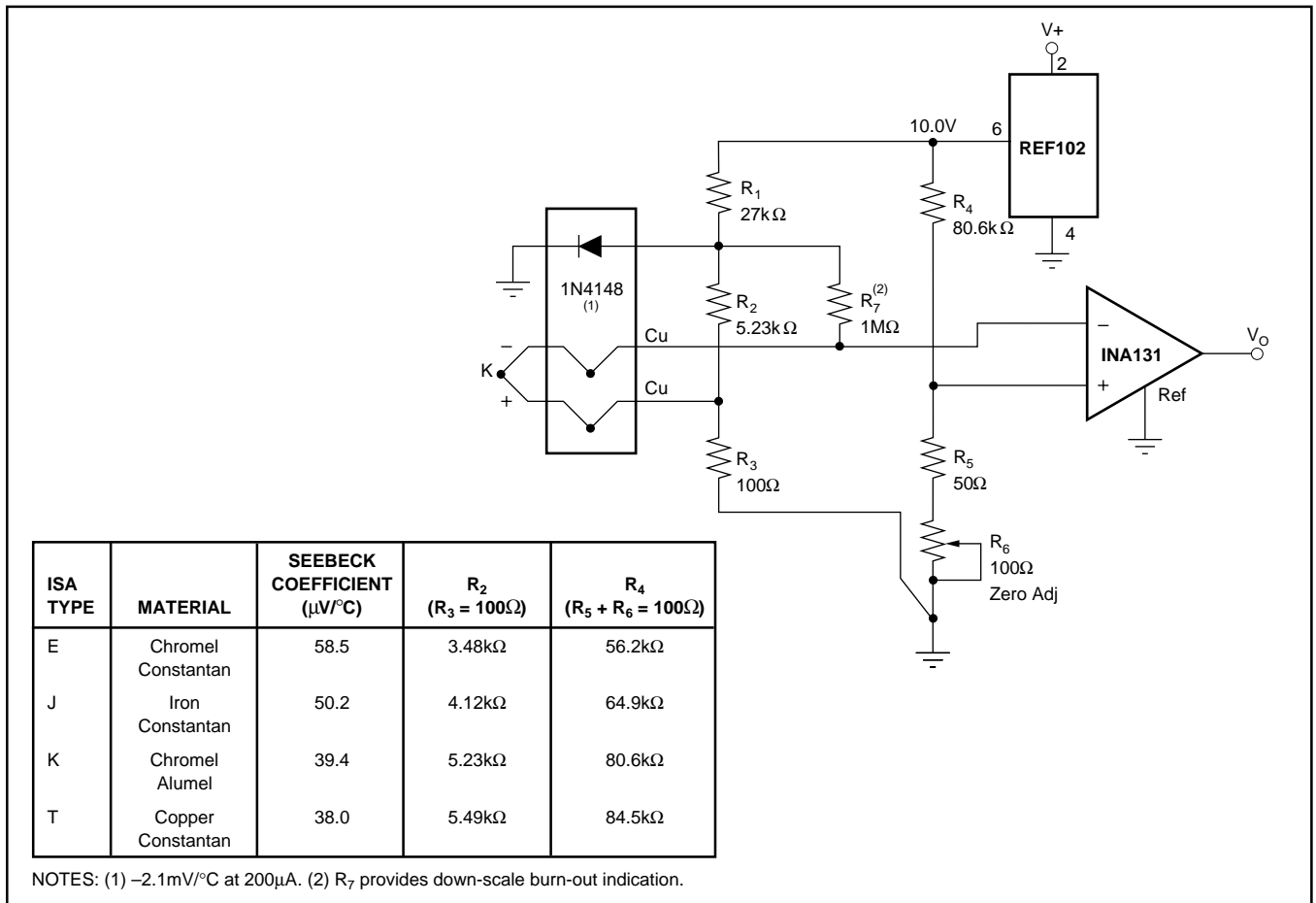


FIGURE 6. Thermocouple Amplifier with Cold Junction Compensation.

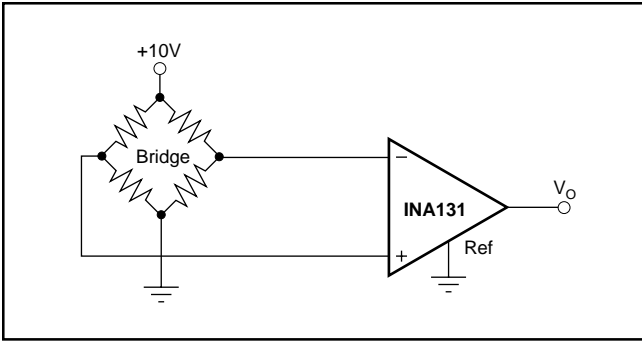


FIGURE 7. Bridge Transducer Amplifier.

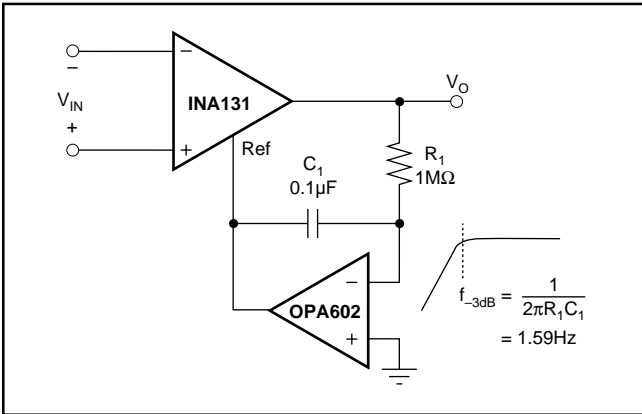


FIGURE 8. AC-Coupled Instrumentation Amplifier.

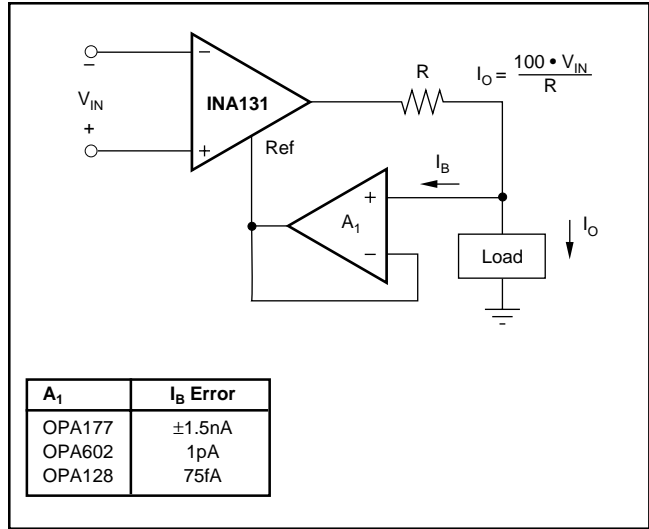


FIGURE 9. Differential Voltage to Current Converter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA131AP	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type	-40 to 85	INA131AP	Samples
INA131BP	ACTIVE	PDIP	P	8	50	RoHS & Green	Call TI	N / A for Pkg Type		INA131BP	Samples
INA131BPG4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
INA131AP	P	PDIP	8	50	506	13.97	11230	4.32
INA131BP	P	PDIP	8	50	506	13.97	11230	4.32

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated