TPS22906 Ultra-Small, Low-Input Voltage, Low r_{ON} Load Switch

1 Features

- Low-Input Voltage: 1.0 V to 3.6 V
- Ultra-Low ON-State Resistance
  - r_{ON} = 90 mΩ at V_{IN} = 3.6 V
  - r_{ON} = 100 mΩ at V_{IN} = 2.5 V
  - r_{ON} = 114 mΩ at V_{IN} = 1.8 V
  - r_{ON} = 172 mΩ at V_{IN} = 1.2 V
- 500-mA Maximum Continuous Switch Current
- Ultra-Low Quiescent Current: 82 nA at 1.8 V
- Ultra-Low Shutdown Current: 44 nA at 1.8 V
- Low Control Input Thresholds Enable Use of 1.2-V/1.8-V/2.5-V/3.3-V Logic
- Controlled Slew Rate to Avoid Inrush Current: 220 µs t_r
- ESD Performance Tested Per JESD 22
  - 2000-V Human Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Four-Terminal Wafer-Chip-Scale Package (WCSP)
  - 0.9 mm × 0.9 mm, 0.5-mm Pitch, 0.5-mm Height

2 Applications

- Personal Digital Assistants (PDAs)
- Cellular Phones
- GPS Devices
- MP3 Players
- Digital Cameras
- Peripheral Ports
- Portable Instrumentation
- RF Modules

3 Description

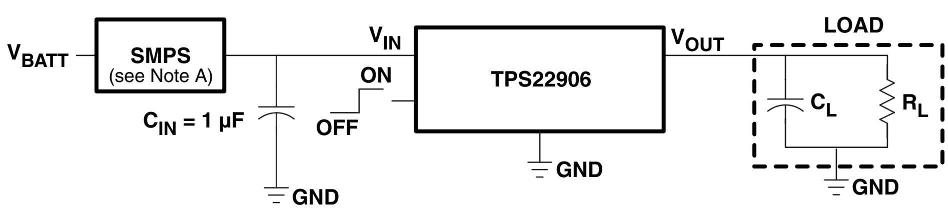
TPS22906 device is an ultra-small, low ON-state resistance (r_{ON}) load switch with controlled turn on. The device contains a P-channel MOSFET that operates over an input voltage range of 1.0 V to 3.6 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. A 120-Ω on-chip load resistor is added for output quick discharge when the switch is turned off. TPS22906 is available in a space-saving 4-terminal WCSP with 0.5-mm pitch (YZV). The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22906	DSBGA (4)	0.90 mm × 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2009) to Revision A	**Page**
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted Ordering Information table.	1

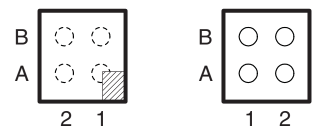
5 Device Options

DEVICE	r_{ON} at 1.8 V (TYP)	SLEW RATE (TYP at 1.8 V)	QUICK OUTPUT DISCHARGE (1)	MAX OUTPUT CURRENT	ENABLE
TPS22906	114 mΩ	220 µs	Yes	500 mA	Active high

(1) This feature discharges the output of the switch to ground through a 120-Ω resistor, preventing the output from floating.

6 Pin Configuration and Functions

YZV Package
4 Pins DSBGA
Top View



Laser Marking View **Bump View**

Pin Assignments

B	ON	GND
A	V_{IN}	V_{OUT}
	2	**1**

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{OUT}	A1	O	Switch output
V_{IN}	A2	I	Switch input, bypass this input with a ceramic capacitor to ground
GND	B1	—	Ground
ON	B2	I	Switch control input, active high

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	4	V
V_{OUT}	Output voltage		V_{IN} + 0.3	V
V_{ON}	Input voltage	–0.3	4	V
P_D	Power dissipation at T_A = 25°C		0.48	W
I_{MAX}	Maximum continuous switch current		500	mA
T_A	Operating free-air temperature range	–40	85	°C
Maximum lead temperature (10-s soldering time), T_{lead}			300	°C
Storage temperature, T_{stg}		-45	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage range	1	3.6	V
V_{OUT}	Output voltage range		V_{IN}	V
V_{IH}	High-level input voltage, ON	0.85	3.6	V
V_{IL}	Low-level input voltage, ON		0.4	V
C_{IN}	Input capacitor	1		μF

7.4 Thermal Information

THERMAL METRIC (1)		TPS2206	UNIT
		YZV (DSBGA)	
		4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 1.0 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
I_{IN}	Quiescent current	I_{OUT} = 0, V_{IN} = V_{ON}	V_{IN} = 1.1 V	Full		37	120	nA
			V_{IN} = 1.8 V	Full		82	235	
			V_{IN} = 3.6 V	Full		204	880	
$I_{IN(OFF)}$	OFF-state supply current	V_{ON} = GND, OUT = Open	V_{IN} = 1.1 V	Full		22	210	nA
			V_{IN} = 1.8 V	Full		44	260	
			V_{IN} = 3.6 V	Full		137	700	
$I_{IN(LEAKAGE)}$	OFF-state switch current	V_{ON} = GND, V_{OUT} = 0	V_{IN} = 1.1 V	Full		22	140	nA
			V_{IN} = 1.8 V	Full		45	230	
			V_{IN} = 3.6 V	Full		137	610	

Electrical Characteristics (continued)

V_{IN} = 1.0 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
r_{ON}	ON-state resistance	I_{OUT} = - 200 mA	V_{IN} = 3.6 V	25°C		90	108	mΩ
				Full			125	
			V_{IN} = 2.5 V	25°C		100	120	
				Full			140	
			V_{IN} = 1.8 V	25°C		114	138	
				Full			160	
			V_{IN} = 1.2 V	25°C		172	210	
				Full			235	
			V_{IN} = 1.1 V	25°C		204	330	
				Full			330	
r_{PD}	Output pulldown resistance	V_{IN} = 3.3 V, V_{ON} = 0, I_{OUT} = 30 mA		25°C		88	120	Ω
I_{ON}	ON input leakage current	V_{ON} = 1.1 V to 3.6 V or GND		Full			25	nA

7.6 Switching Characteristics – V_{IN} = 1.1 V

T_A = 25°C , RL_CHIP = 120 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		531		µs
			C_L = 1 µF		596		
			C_L = 3.3 µF		659		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		11		µs
			C_L = 1 µF		67		
			C_L = 3.3 µF		225		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		365		µs
			C_L = 1 µF		367		
			C_L = 3.3 µF		395		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		21		µs
			C_L = 1 µF		189		
			C_L = 3.3 µF		565		

7.7 Switching Characteristics – V_{IN} = 1.2 V

T_A = 25°C , RL_CHIP = 120 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		471		µs
			C_L = 1 µF		527		
			C_L = 3.3 µF		587		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		10		µs
			C_L = 1 µF		61		
			C_L = 3.3 µF		199		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		324		µs
			C_L = 1 µF		325		
			C_L = 3.3 µF		350		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		20		µs
			C_L = 1 µF		175		
			C_L = 3.3 µF		523		

7.8 Switching Characteristics – V_{IN} = 1.8 V

T_A = 25°C , RL_CHIP = 120 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		302		µs
			C_L = 1 µF		335		
			C_L = 3.3 µF		367		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		8		µs
			C_L = 1 µF		49		
			C_L = 3.3 µF		167		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		220		µs
			C_L = 1 µF		220		
			C_L = 3.3 µF		235		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		15		µs
			C_L = 1 µF		159		
			C_L = 3.3 µF		481		

7.9 Switching Characteristics – V_{IN} = 2.5 V

T_A = 25°C , RL_CHIP = 120 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		223		µs
			C_L = 1 µF		246		
			C_L = 3.3 µF		268		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		7		µs
			C_L = 1 µF		47		
			C_L = 3.3 µF		158		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		175		µs
			C_L = 1 µF		175		
			C_L = 3.3 µF		187		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		18		µs
			C_L = 1 µF		185		
			C_L = 3.3 µF		471		

7.10 Switching Characteristics – V_{IN} = 3 V

T_A = 25°C , RL_CHIP = 120 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		191		µs
			C_L = 1 µF		211		
			C_L = 3.3 µF		231		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		7		µs
			C_L = 1 µF		46		
			C_L = 3.3 µF		156		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		159		µs
			C_L = 1 µF		160		
			C_L = 3.3 µF		170		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		17		µs
			C_L = 1 µF		160		
			C_L = 3.3 µF		473		

7.11 Switching Characteristics – V_{IN} = 3.6 V

T_A = 25°C , RL_CHIP = 120 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω	C_L = 0.1 µF		166		µs
			C_L = 1 µF		183		
			C_L = 3.3 µF		201		
t_{OFF}	Turnoff time	R_L = 500 Ω	C_L = 0.1 µF		7		µs
			C_L = 1 µF		45		
			C_L = 3.3 µF		155		
t_r	V_{OUT} rise time	R_L = 500 Ω	C_L = 0.1 µF		146		µs
			C_L = 1 µF		146		
			C_L = 3.3 µF		156		
t_f	V_{OUT} fall time	R_L = 500 Ω	C_L = 0.1 µF		17		µs
			C_L = 1 µF		161		
			C_L = 3.3 µF		475		

7.12 Typical Characteristics

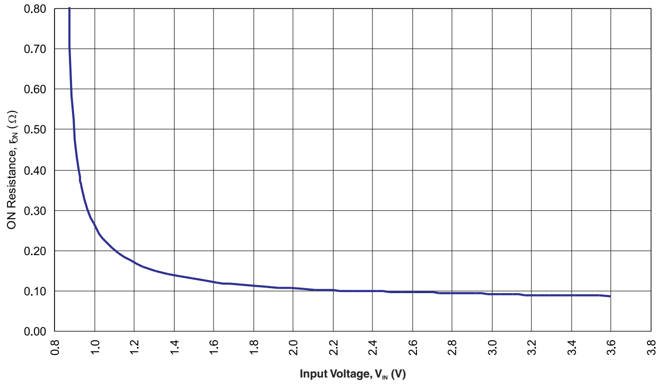


Figure 1. r_{ON} vs V_{IN}

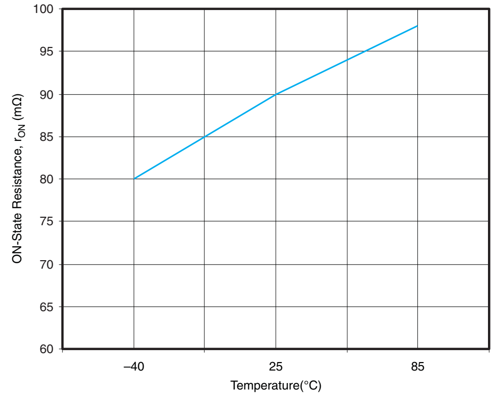


Figure 2. r_{ON} vs Temperature (V_{IN} = 3.3 V)

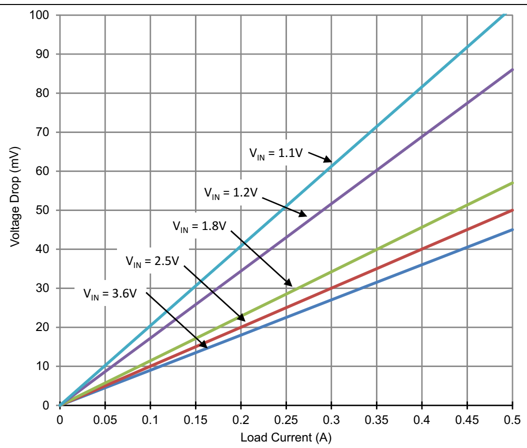


Figure 3. Voltage Drop vs Load Current

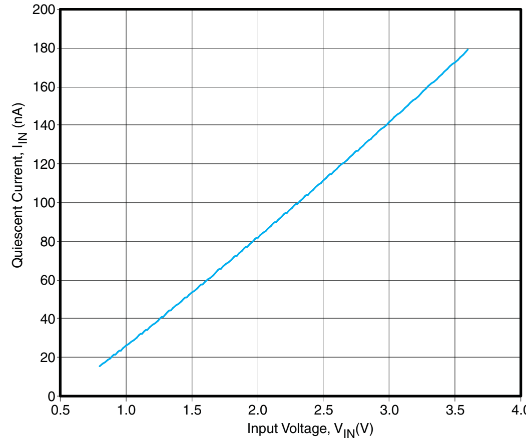


Figure 4. Quiescent Current vs V_{IN} (V_{ON} = V_{IN}, I_{OUT} = 0)

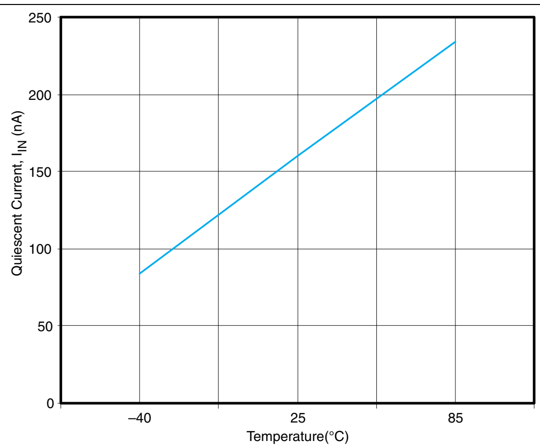


Figure 5. Quiescent Current vs Temperature (V_{IN} = 3.3 V, I_{OUT} = 0)

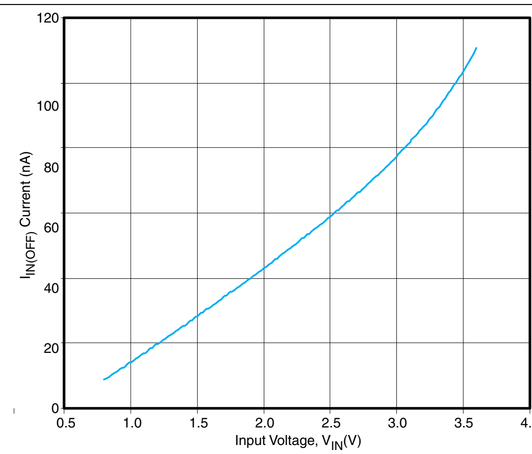


Figure 6. $I_{IN(OFF)}$ vs V_{IN} (V_{ON} = 0 V)

Typical Characteristics (continued)

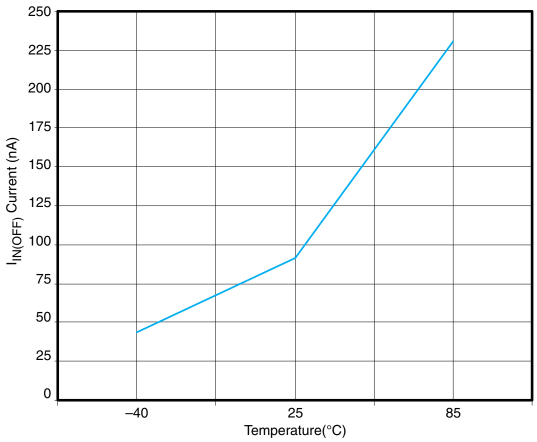


Figure 7. $I_{IN(OFF)}$ vs Temperature (V_{IN} = 3.3 V)

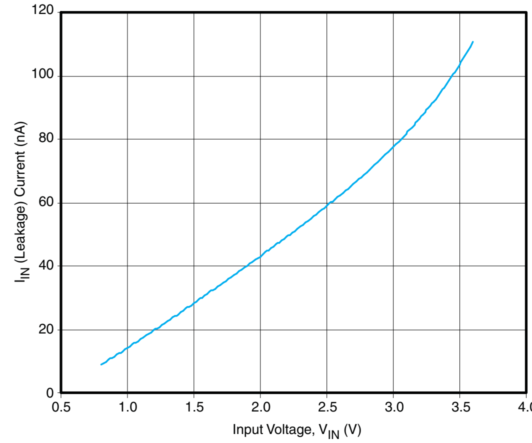


Figure 8. I_{IN}(Leakage) vs V_{IN} (I_{OUT} = 0)

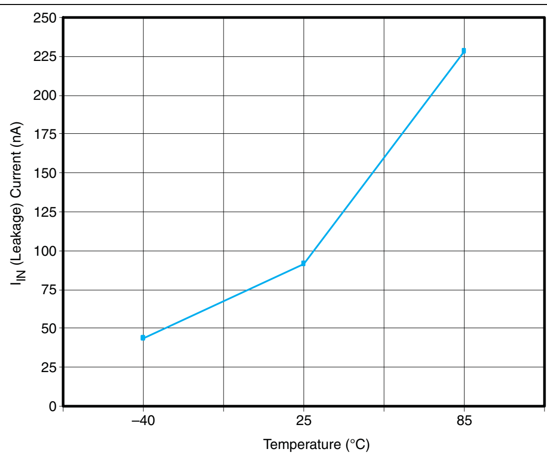


Figure 9. I_{IN} (Leakage) vs Temperature (V_{IN} = 3.3 V)

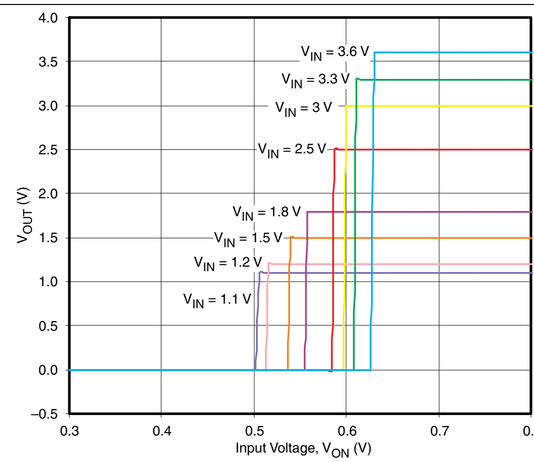


Figure 10. ON-Input Threshold

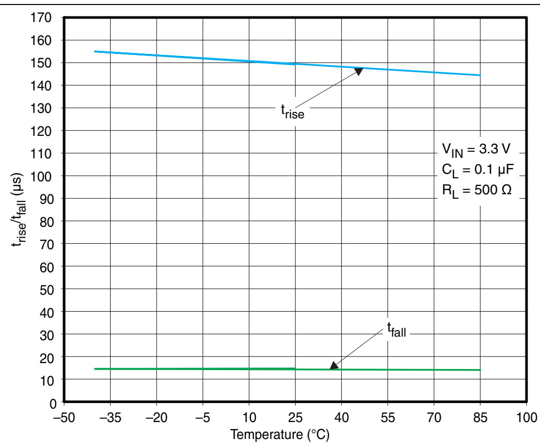


Figure 11. t_{rise}/t_{fall} vs Temperature

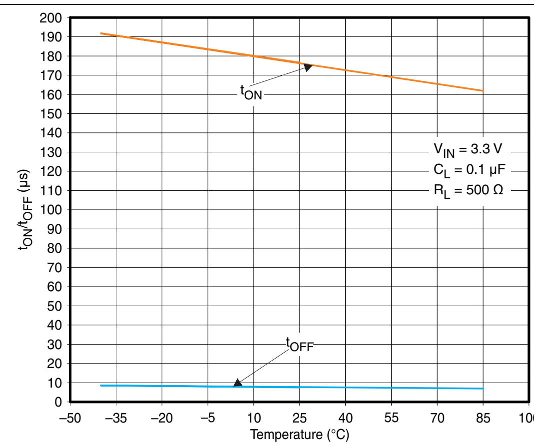


Figure 12. t_{ON}/t_{OFF} vs Temperature

Typical Characteristics (continued)

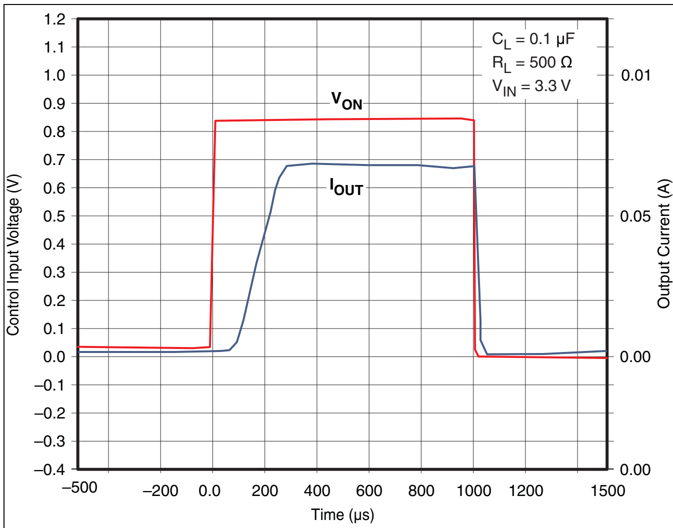


Figure 13. t_{ON} Response

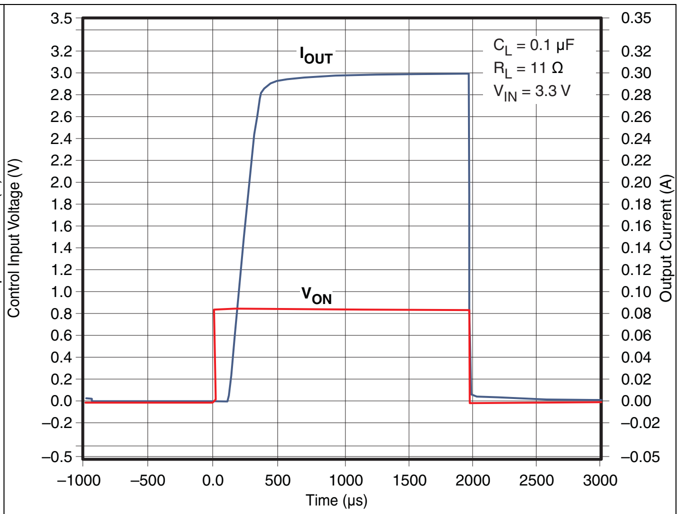


Figure 14. t_{ON} Response

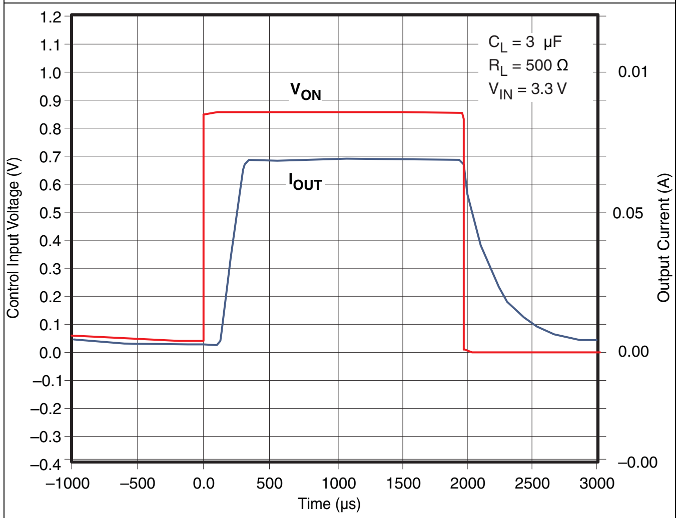


Figure 15. t_{ON} Response

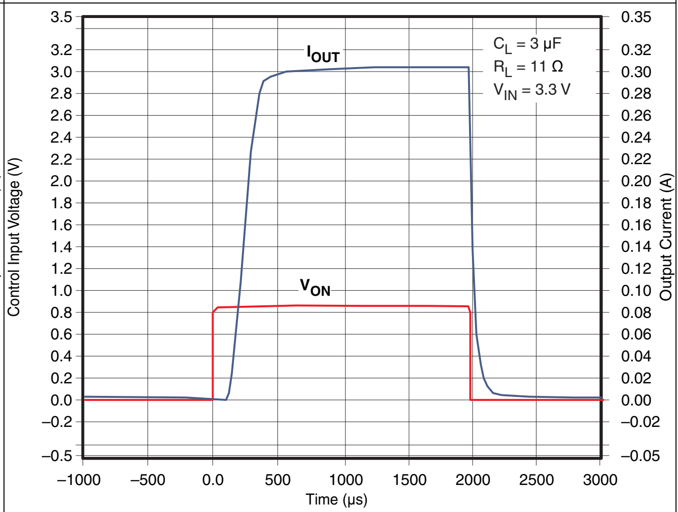


Figure 16. t_{ON} Response

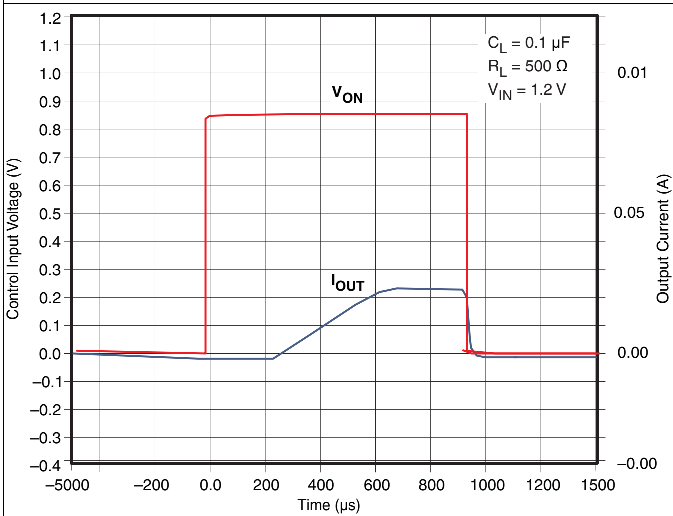


Figure 17. t_{ON} Response

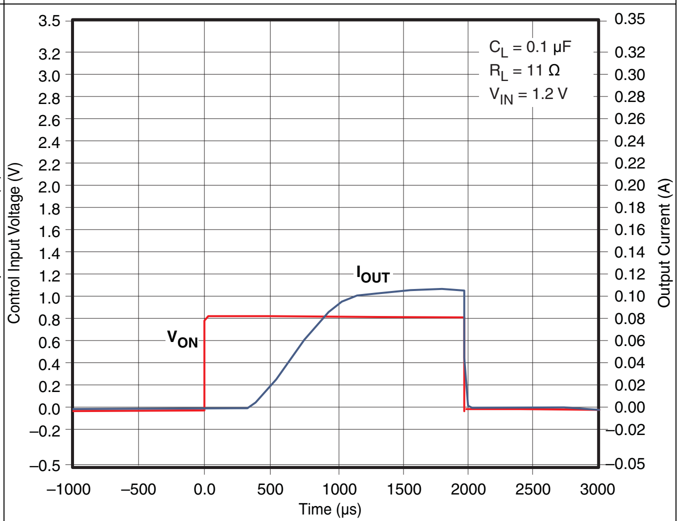


Figure 18. t_{ON} Response

Typical Characteristics (continued)

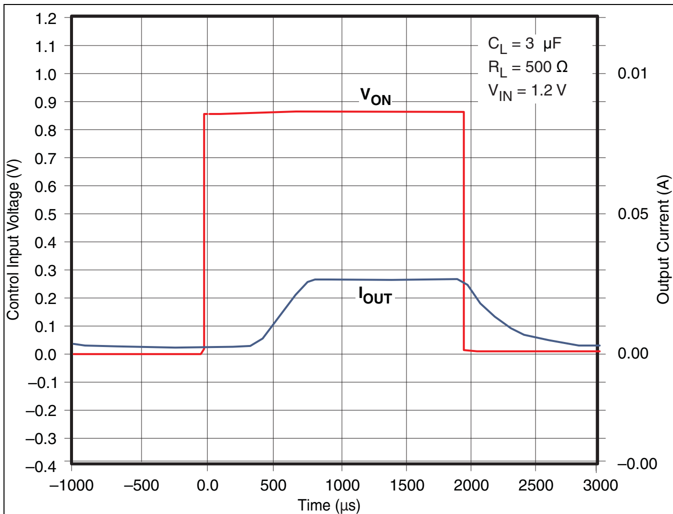


Figure 19. t_{ON} Response

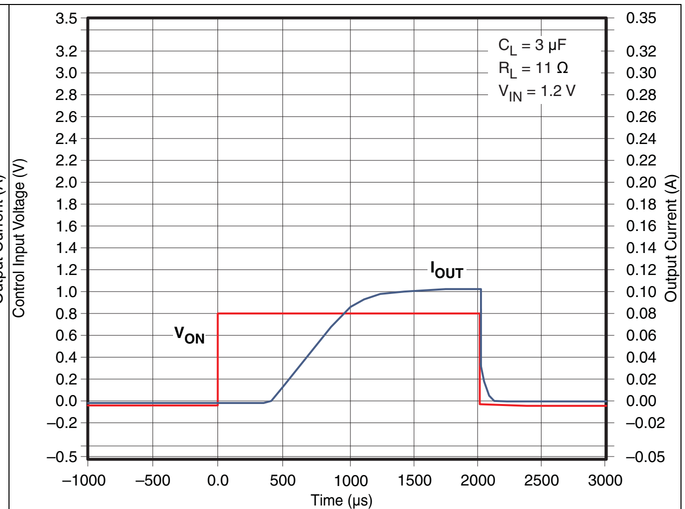


Figure 20. t_{ON} Response

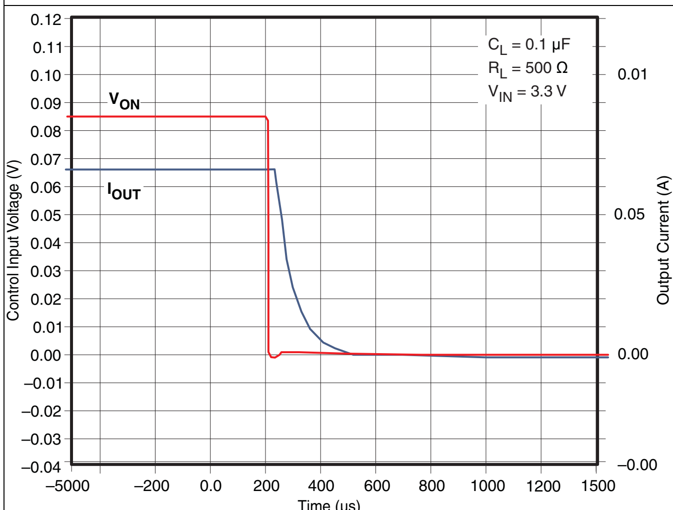


Figure 21. t_{OFF} Response

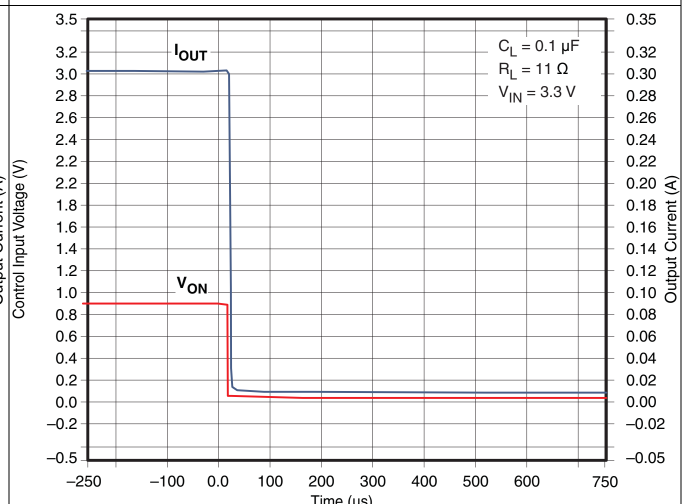


Figure 22. t_{OFF} Response

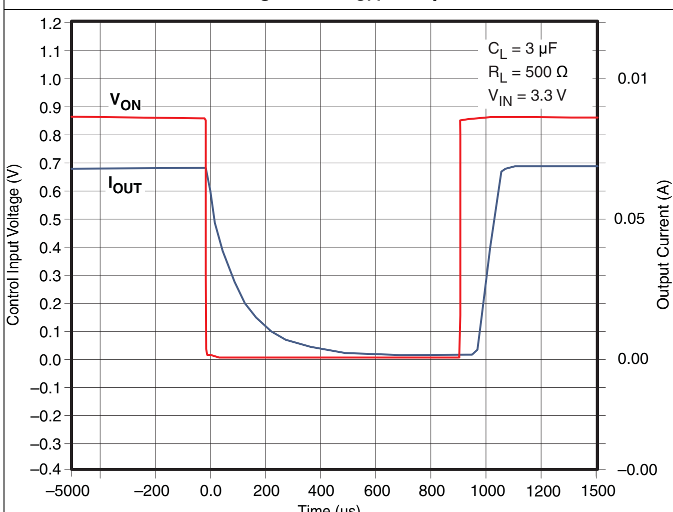


Figure 23. t_{OFF} Response

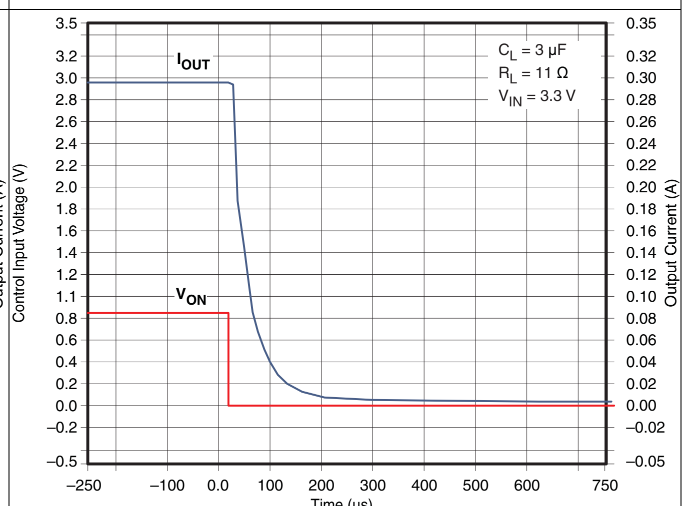


Figure 24. t_{OFF} Response

Typical Characteristics (continued)

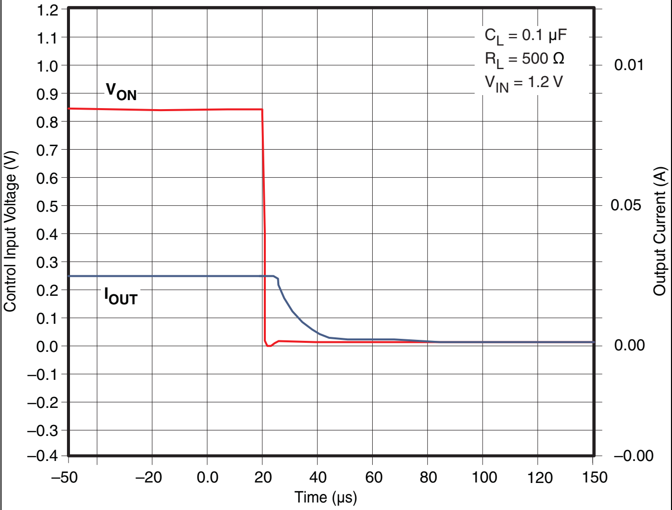


Figure 25. t_{OFF} Response

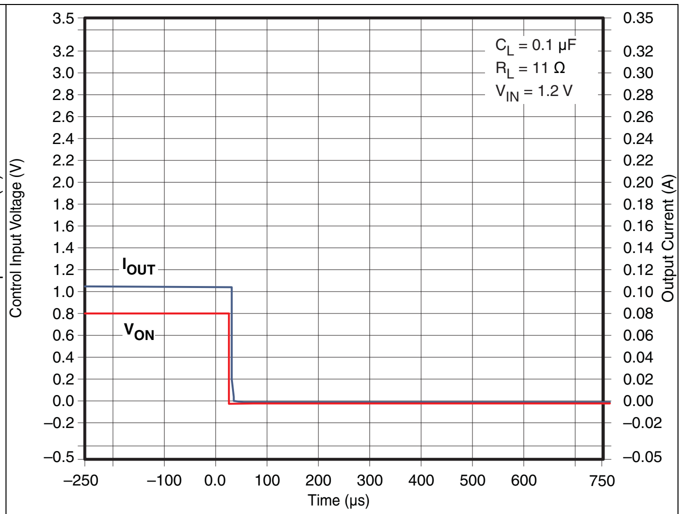


Figure 26. t_{OFF} Response

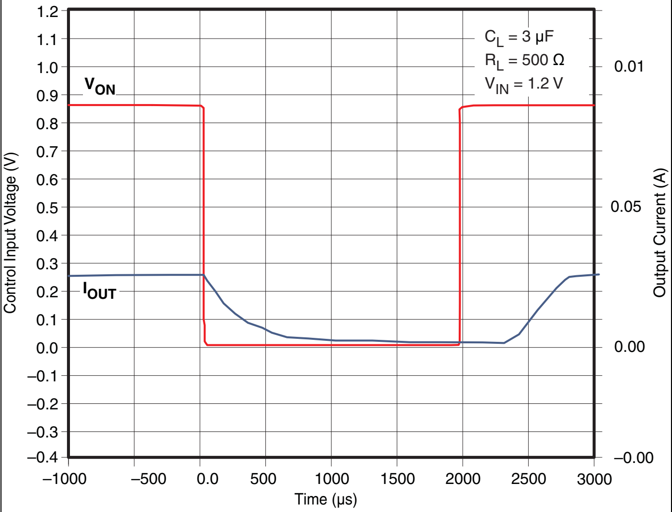


Figure 27. t_{OFF} Response

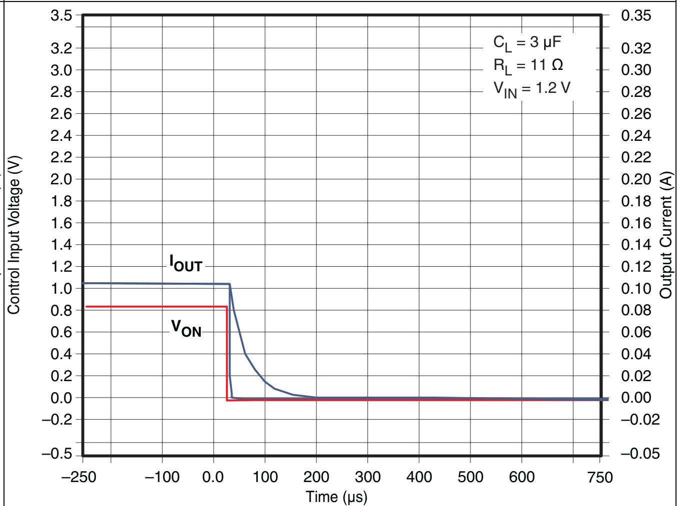
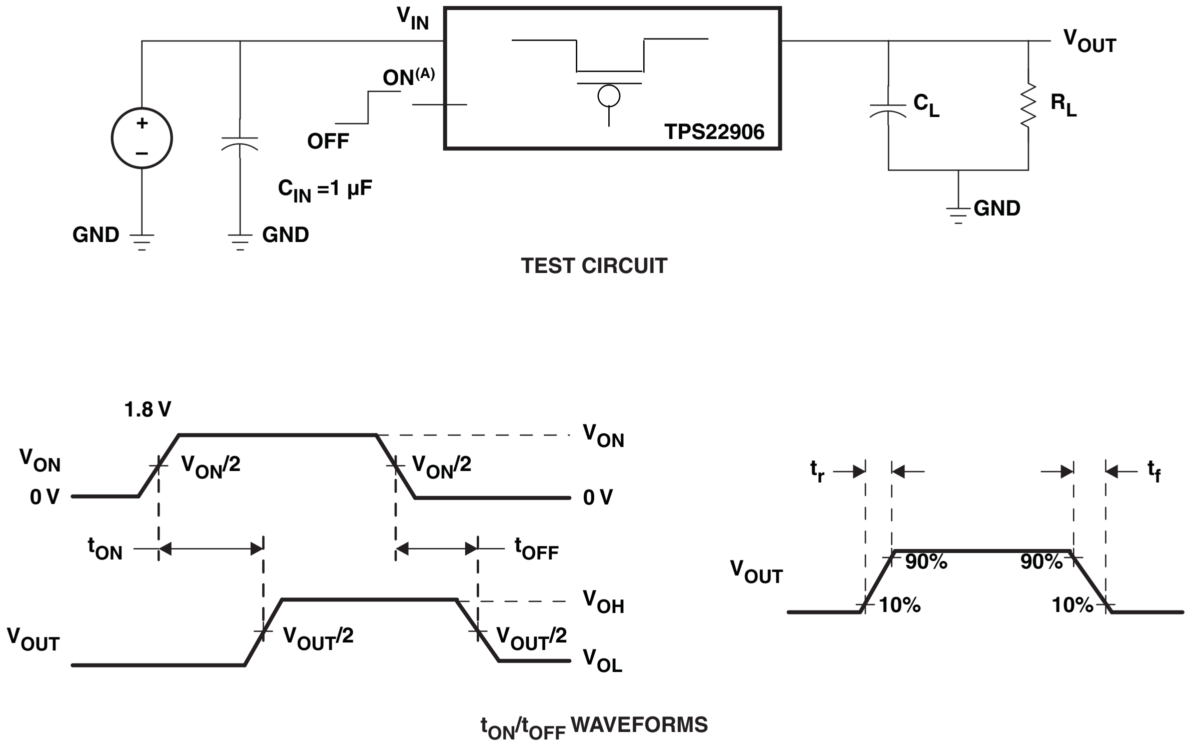


Figure 28. t_{OFF} Response

8 Parameter Measurement Information



A. t_{rise} and t_{fall} of the control signal is 100 ns.

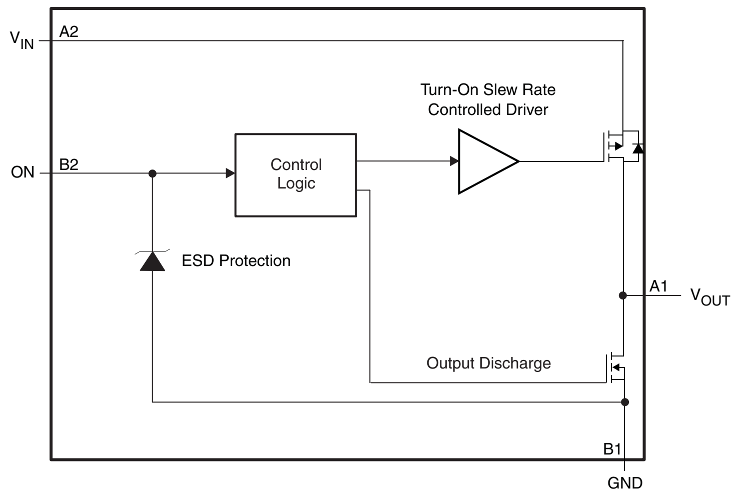
Figure 29. Test Circuit and t_{ON}/t_{OFF} Waveforms

9 Detailed Description

9.1 Overview

TPS22906 is a low ON-state resistance (r_{ON}) load switch with controlled turnon. The device contains a P-channel MOSFET that operates over an input voltage range of 1.0 V to 3.6 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. A 120-Ω on-chip load resistor is added for output quick discharge when the switch is turned off.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 ON/OFF Control

The ON pin controls the state of the switch. Activating ON continuously holds the switch in the on state so long as there is no fault. ON is active HI and has a low threshold making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, or 3.3-V GPIOs.

9.4 Device Functional Modes

Table 1 lists the functional modes of the TPS22906.

Table 1. Function Table

ON (CONTROL INPUT)	V_{IN} TO V_{OUT}	V_{OUT} TO GND
L	OFF	ON
H	ON	OFF

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

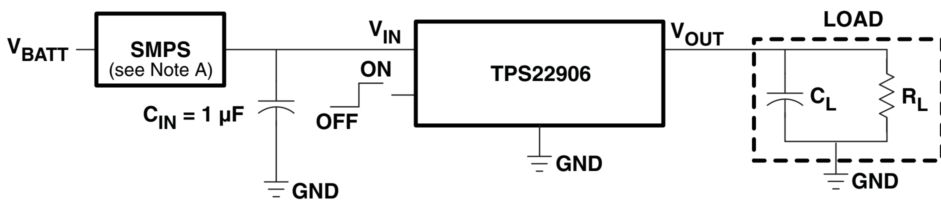
10.1.1 Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1-μF ceramic capacitor, C_{IN}, place close to the pins is usually sufficient. Higher values of C_{IN} can be use to further reduce the voltage drop during high current application. When switching heavy loads, it is recommended to have an input capacitor approximately 10 times higher than the output capacitor to avoid excessive voltage drop.

10.1.2 Output Capacitor

Due to the integral body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

10.2 Typical Application



A. Switched mode power supply

Figure 30. Powering a Downstream Module

10.2.1 Design Requirements

Table 2 lists the design parameters for the TPS22906 device.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	1.8 V
Load Current	0.3 A
Ambient Temperature	25°C

10.2.2 Detailed Design Procedure

10.2.2.1 V_{IN} to V_{OUT} Voltage Drop

The voltage drop from V_{IN} to V_{OUT} is determined by the ON-resistance of the device and the load current. The r_{ON} can be found in *Electrical Characteristics* and is dependent on temperature. When the value of r_{ON} is found, Equation 1 can be used to calculate the voltage drop across the device:

$$\Delta V = I_{LOAD} \times r_{ON}$$

where

- ΔV = Voltage drop across the device
- I_{LOAD} = Load current

- r_{ON} = ON-resistance of the device (1)

At V_{IN} = 1.8 V, the TPS22906 has a r_{ON} value of 114 mΩ. Using this value and the defined load current, the above equation can be evaluated:

$\Delta V = 0.30\ A \times 114\ m\Omega$

where

- ΔV = 34 mV (2)

Therefore, the voltage drop across the device will be 34 mV.

10.2.3 Application Curve

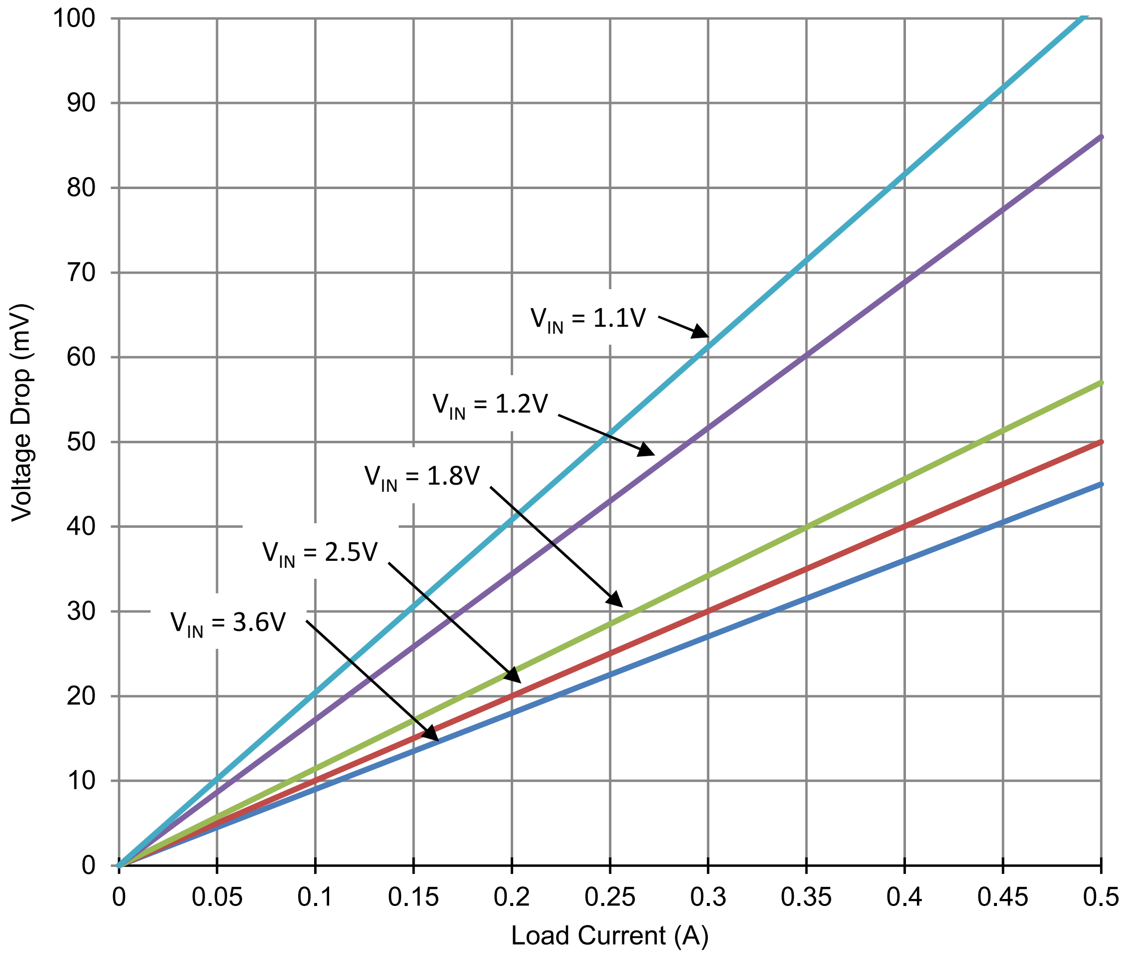


Figure 31. Voltage Drop Vs Load Current

11 Power Supply Recommendations

The device is designed to operate with a V_{IN} range of 1.1 V to 3.6 V. This supply must be well regulated and placed as close to the device terminals as possible. It must also be able to withstand all transient and load currents, using a recommended input capacitance of 1 µF if necessary. If the supply is more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

12 Layout

12.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short circuit operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

12.2 Layout Example

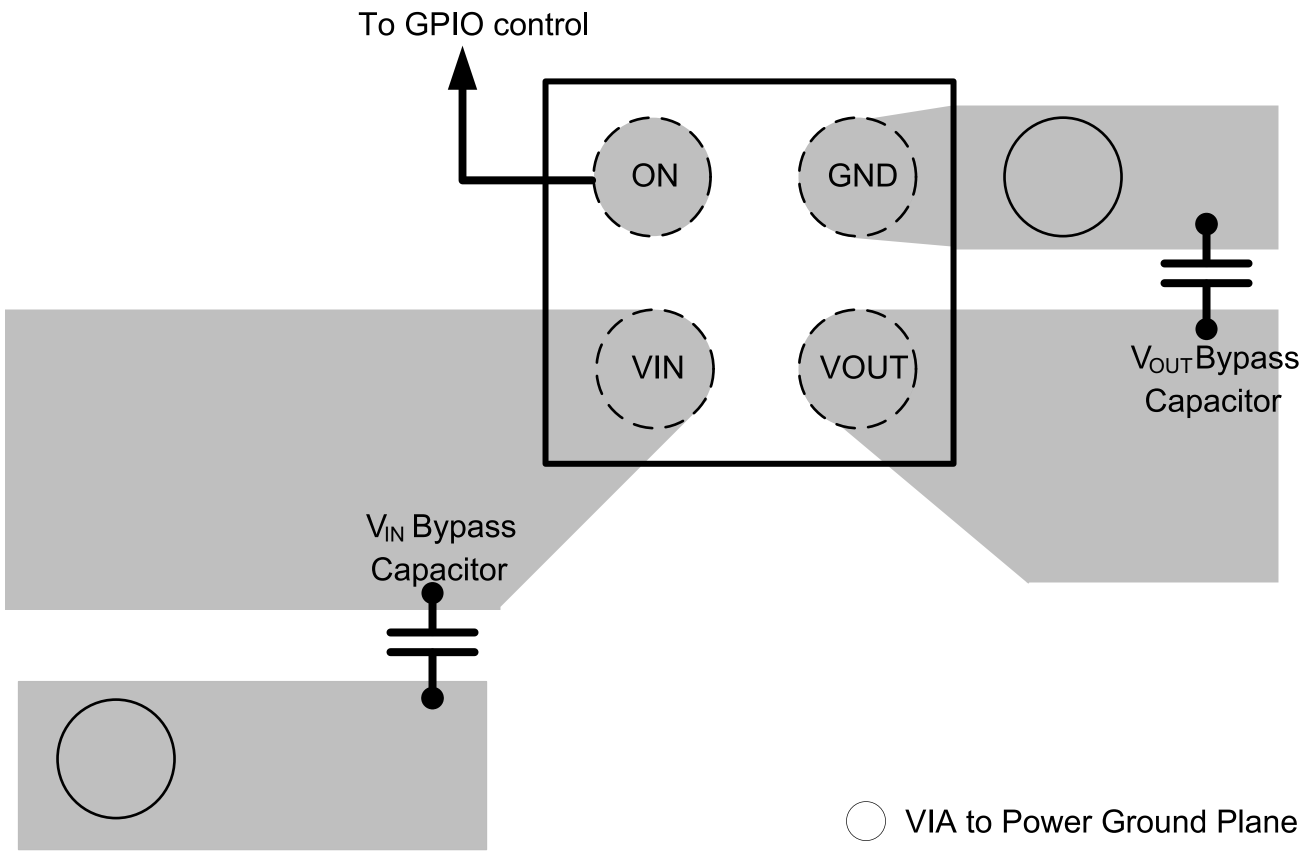


Figure 32. Recommended Board Layout

13 Device and Documentation Support

13.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.2 Trademarks

E2E is a trademark of Texas Instruments.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22906YZVR	NRND	DSBGA	YZV	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5D (3, 5)	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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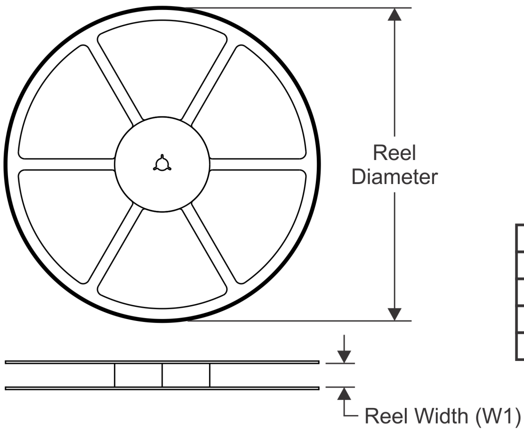
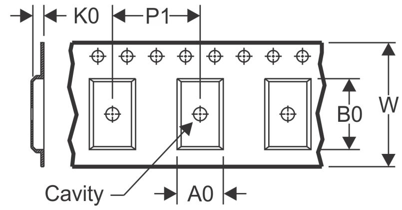
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

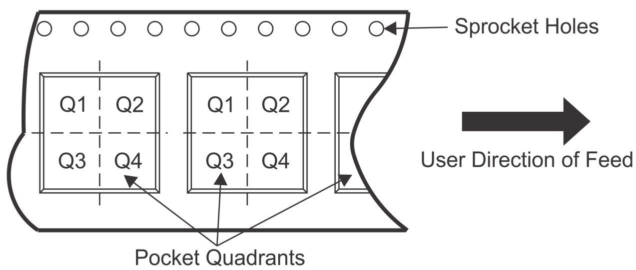


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

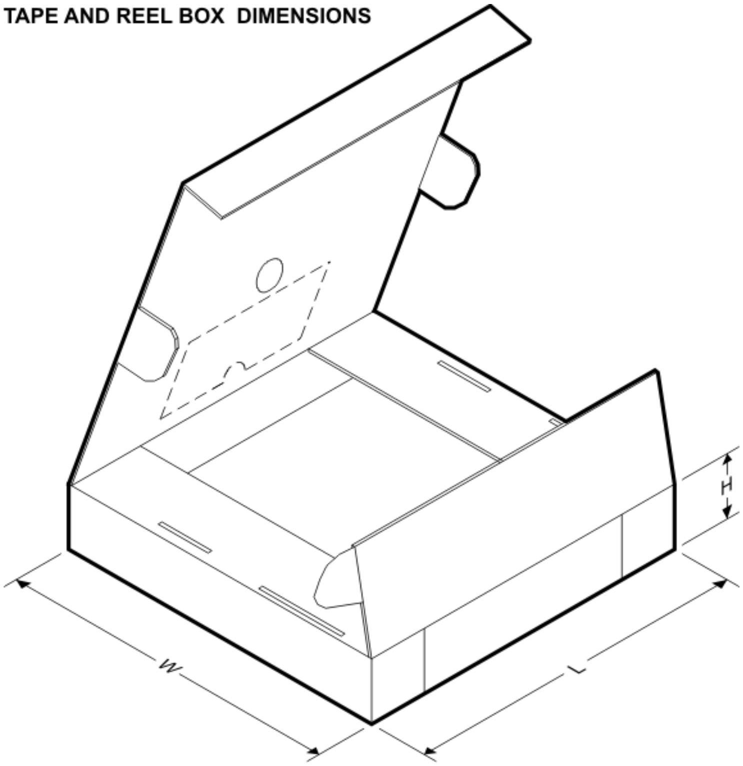
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22906YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

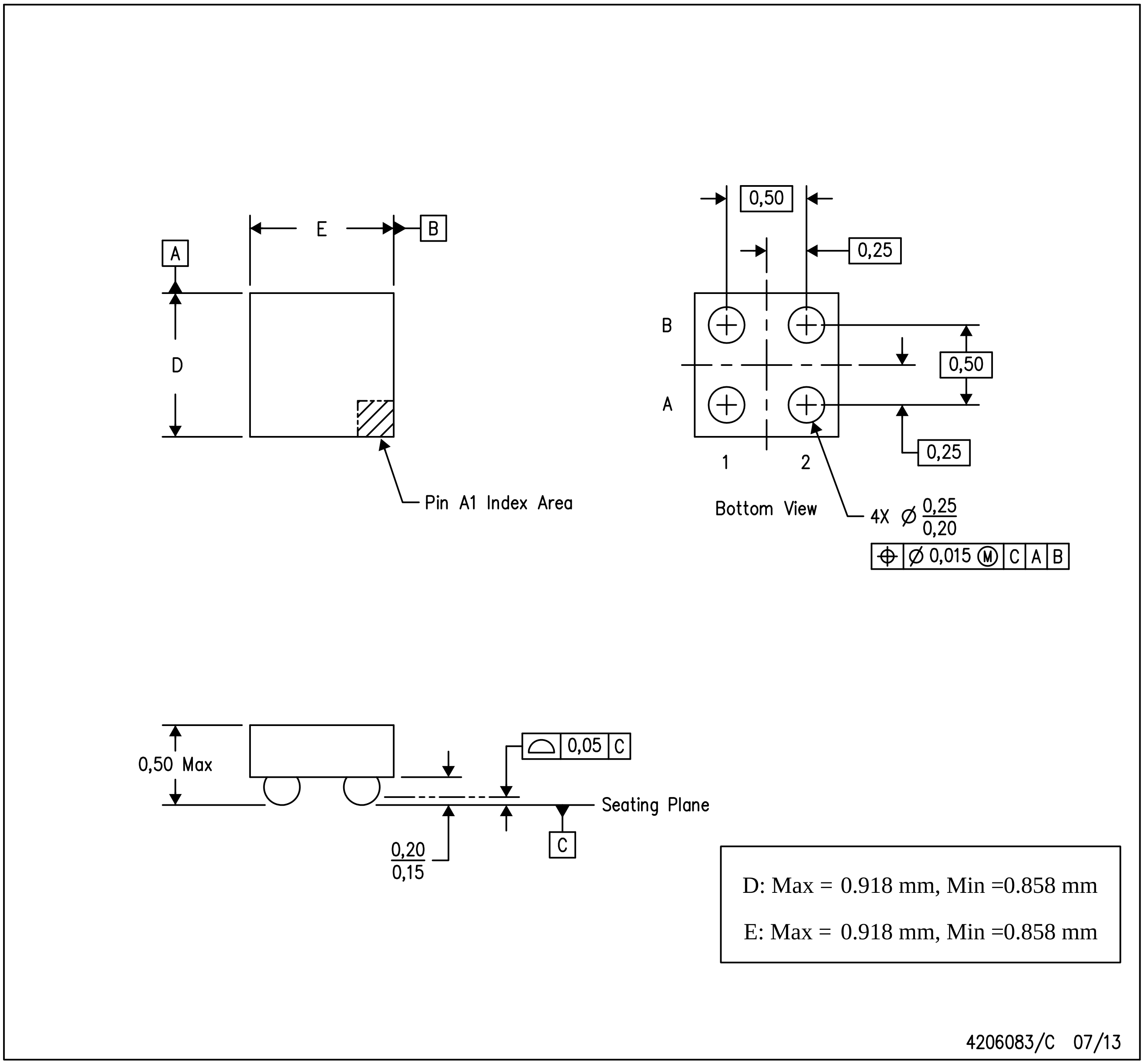
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22906YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.