TPS40180 Single Phase Stackable Controller

1 Features

- Stackable to 8 Phases, Multiple Controllers Can Occupy Any Phase
- 2-V to 40-V Power Stage Operation Range
- eTrim™ in System Reference Voltage Trim to Tighten Overall Output Voltage Tolerance, Reference is Better Than 0.75% Untrimmed
- VDD From 4.5 V to 15 V, With Internal 5-V Regulator
- Supports Output Voltage From 0.7 V to 5.8 V
- Supports Prebiased Outputs
- 10-µA Shutdown Current
- Programmable Switching Frequency up to 1-MHz per Phase
- Current Feedback Control With Forced Current Sharing (Patents Pending)
- Resistive Divider Sets Input Undervoltage Lockout and Hysteresis
- True Remote Sensing Differential Amplifier
- Resistive or Inductor's DCR Current Sensing

2 Applications

- Graphic Cards
- Servers
- Networking Equipment
- Telecommunications Equipment
- Distributed DC Power Systems

3 Description

The TPS40180 is a stackable single-phase synchronous buck controller. Stacking allows a modular power supply design where multiple modules can be connected in parallel to achieve higher power capability. Stacked modules can be configured at the same switching frequency with interleaved phase shift to reduce input and output ripple current. Stacked modules can also be configured to generate separate output rails at the same time as different phase shift to reduce input ripple current.

The TPS40180 is optimized for low-output voltage (from 0.7-V to 5.8-V), high-output current applications powered from a 2-V to 40-V supply.

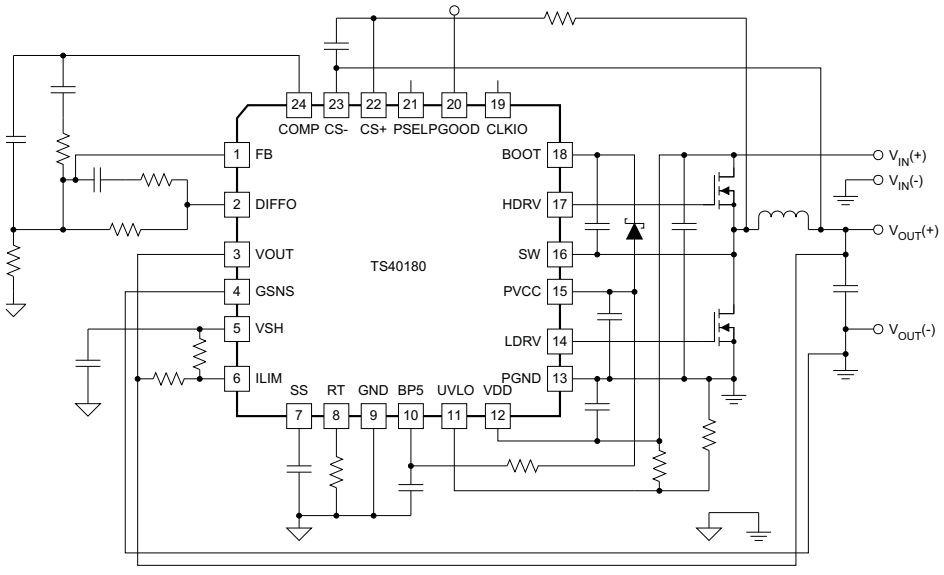
With eTrim™, the TPS40180 gives the user the capability to trim the reference voltage on the device to compensate for external component tolerances, tightening the overall system accuracy and allowing tighter specifications for output voltage of the converter.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS40180	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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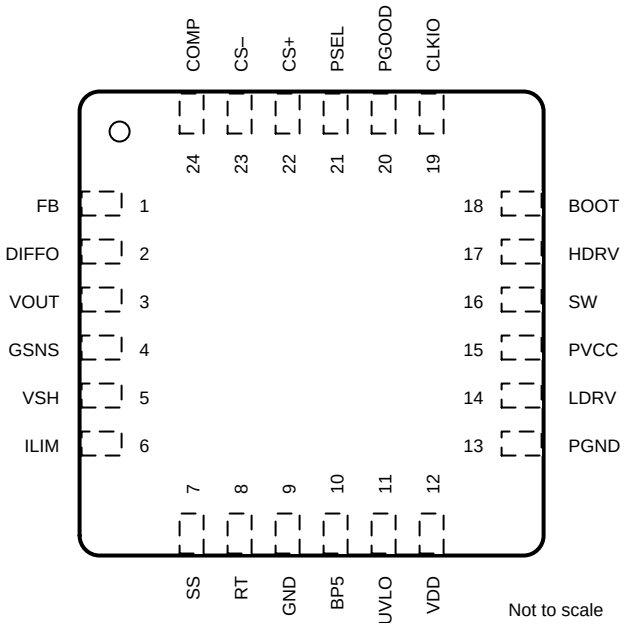
4 Revision History

Changes from Revision B (November 2007) to Revision C **Page**

- Added *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	FB	I	Inverting input to the internal error amplifier. Normally this pin is at the reference voltage of 700 mV.
2	DIFFO	O	Output of the remote sense amplifier. Amplifier is fixed gain of 1 differential mode and is used for output voltage sensing at the load to eliminate distribution drops.
3	VOUT	I	Positive input to the remote sense amplifier. Amplifier is fixed gain of 1 differential mode and is used for output voltage sensing at the load to eliminate distribution drops.
4	GSNS	I	Negative input to the remote sense amplifier. Amplifier is fixed gain of 1 differential mode and is used for output voltage sensing at the load to eliminate distribution drops.
5	VSH	I/O	Pin is either an input or an output. If the chip is configured as a voltage loop master the valley voltage is output on this pin and is distributed to the slave devices. If configured as a voltage loop slave, the master VSH pin is connected here and the device uses the master valley voltage reference to improve current sharing.
6	ILIM	I	Programs the overcurrent limit of the device. Connecting a resistor from this pin to VSH and another to VOUT on the voltage loop master sets a voltage above VSH. COMP is not allowed to exceed this voltage. If the load current requirements force COMP to this level for seven clock cycles, an overcurrent event is declared, and the system shuts down and enter a hiccup fault recovery mode. The controller attempts to restart after a time period given by seven soft-start cycles.
7	SS	I	Soft-start input. This pin determines the startup ramp time for the converter as well as overcurrent and other fault recovery timing. The voltage at this pin is applied as a reference to the error amplifier. While this voltage is below the precision 700 mV reference, it acts as the dominant reference to the error amp providing a closed loop startup. After it rises above the 700 mV precision reference, the 700 mV precision reference dominates and the output regulates at the programmed level. In case of an overcurrent event, the converter attempts to restart after a period of time defined by seven soft-start cycles. Additionally this pin is used to configure the chip as a voltage loop master or slave. If the pin is tied to VDD or PVCC at power up, the device is in voltage loop slave mode. Otherwise, the device is a voltage loop master.
8	RT	I	Frequency programming pin. Connecting a resistor from this pin to GND sets the switching frequency of the device. If this pin is connected to VDD or PVCC, the device is a clock slave and gets its time base from CLKIO of the clock master device. Phase addressing is done on PSEL.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
9	GND	—	Signal level ground connection for the device. All low level signals at the device should be referenced to this pin. No power level current should be allowed to flow through the GND pin copper areas on the board. Connect to the thermal pad area, and from there to the PGND copper area.
10	BP5	I	Electrically quiet 5-V supply for the internal circuitry inside the device. If VDD is above 5 V, connect a 20-Ω resistor from PVCC to this pin and a 100-nF capacitor from this pin to GND. For VDD at 5 V, this pin can be tied directly to VDD or through a 20-Ω resistor with a 100-nF decoupling capacitor to reduce internal noise.
11	UVLO	I	UVLO input for the device. A resistor divider from VDD sets the turn on voltage for the device. Below this voltage, the device is in a low quiescent current state. Pulling this pin to ground shuts down the device, and is used as a system shutdown method.
12	VDD	I	Power input for the LDO on the device.
13	PGND	—	Common connection for the power circuits on the device. This pin should be electrically close to the source of the FET connected to LDRV. Connected to GND only at the thermal pad for best results.
14	LDRV	O	Gate drive output for the low-side or rectifier FET.
15	PVCC	O	Output of the on board LDO. This is the power input for the drivers and bootstrap circuit. The 5.3-V output on this pin is used for external circuitry as long as the total current required to drive the gates of the switching FETs and external loads is less than 50 mA. Connect a 1-µF capacitor from this pin to GND.
16	SW	O	This pin is connected to the source of the high-side or *switch* FET and is the return path for the floating high-side driver.
17	HDRV	O	Gate drive output for the high-side FET. High-side FET turn-on time must not be greater than minimum on-time. See electrical characteristics table for the minimum on time of the pulse width modulator.
18	BOOT	I	Bootstrap pin for the high-side driver. A 100-nF capacitor is connected from this pin to SW and provides power to the high-side driver when the high-side FET is turned on.
19	CLKIO	I/O	Clock and phase timing output while the device is configured as a clock master. In clock slave mode, the master CLKIO pin is connected to the slave CLKIO pin to provide time base information to the slave.
20	PGOOD	O	Power good output. This open drain output pulls low when the device is in any state other than in normal regulation. Active soft start, UVLO, overcurrent, undervoltage, overvoltage or overtemperature warning (115°C junction) causes this output to pull low.
21	PSEL	I	Phase select pin. For a clock master, a resistor from this pin to GND determines the CLKIO output. When configured as a clock slave, a resistor from the pin to GND selects the phase relationship that the slave has with the master. Allowing this pin to float causes the slave to drop off line to shed the phase when current demands are light for improved overall efficiency. See *Detailed Description* for more details.
22	CS+	I	Positive input to the current sense amplifier.
23	CS–	I	Negative input to the current sense amplifier.
24	COMP	O	Output of the error amplifier.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage, V_I	VDD, UVLO, RT, SS	–0.3	16	V
	FB, VOUT, GSNS, VSH, ILIM, BP5, PSEL, CS+, CS–, VS+, VS–	–0.3	6	
Output voltage, V_O	BOOT – HDRV	–0.3	6	V
	SW, HDRV	–1	44	
	SW, HDRV, transient (<50 ns)	–5	44	
	DIFFO, LDRV, PVCC, CLKIO, PGOOD, COMP	–0.3	6	
	PGOOD (eTrim™ usage only)	–0.3	22	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_I	Input voltage	VDD, UVLO	4.5		15	V
		SW	–1		40	
		BOOT – SW		5.5		
		All other pins	0		5.8	
	RT				25	µA
	PSEL				150	µA
T_J	Operating junction temperature		–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS40180 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{VDD} = 12 V, V_{BP5} = 15 V, V_{PVCC} = 5 V, –40°C ≤ T_J ≤ 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD INPUT SUPPLY						
V_{VDD}	Operating voltage range		4.5	12	15	V
I_{VDDSD}	Shutdown current	V_{UVLO} < 0.5 V			50	µA
BP5 INPUT SUPPLY						
V_{BP5}	Operating voltage range		4.3	5	5.5	V
I_{BP5}	Operating current		2	3	5	mA
V_{BP5UV}	Rising undervoltage turn on threshold		4	4.25	4.5	V
V_{BP5UVH}	BP5 UVLO hysteresis			225		mV
PVCC REGULATOR						
V_{PVCC}	Output voltage	4.5 V < V_{DD} < 15 V	4.3	5	5.5	V
I_{PVCC}	Output current		0		50	mA
OSCILLATOR						
F_{OSC}	Oscillator frequency	R_{RT} = 64.9 kΩ	360	415	454	kHz
	Oscillator frequency range		150		1000	
V_{RMP}	Ramp voltage(1)		420	500	525	mV
$V_{RTCKLSLV}$	RT pin clock slave voltage threshold				2	V
DIGITAL CLOCK SIGNAL (CLKIO)						
R_{CLKH}	Pull up resistance(1)			27		Ω
R_{CLKL}	Pull down resistance(1)			27		Ω
$I_{CLKIOLK}$	Leakage current in high impedance state(1)	V_{RT} < 2 V, V_{PSEL} = 5 V			1	µA
UVLO PIN						
$V_{UVLO(on)}$	PVCC regulator enabled		0.8	0.9	1.5	V
	PWM switching enabled		1.9	2	2.1	
I_{UVLO}	Hysteresis bias current		9	12	15	µA
PULSE WIDTH MODULATOR						
D_{MAX}	Maximum duty cycle	8 phase CLK scheme		87.5%		
		6 phase CLK scheme		83%		
$t_{ON(min)}$	Minimum pulse width(1)			75		ns
VSHARE						
V_{VSH}	Current share reference; ramp valley voltage	R_{LOAD} = 20 kΩ	1.7	1.8	1.9	V
ERROR AMPLIFIER						
I_{IB}	Input bias current at FB pin	V_{FB} = 0.7 V	–200	0	200	nA
V_{REF}	Trimmed FB control voltage	Includes differential sense amp offset	695	700	705	mV
I_{OH}	COMP source current	V_{COMP} = 1.1 V, V_{FB} = 0.6 V	1	2		mA
I_{OL}	COMP sink current	V_{COMP} = 1.1 V, V_{FB} = 0.8 V	1	2		mA
EA_{GBWP}	Gain bandwidth product(1)		8	12		MHz
A_{OL}	Open loop gain(1)		60	90		dB
SOFTSTART						
I_{SS1}	Charging current (before first PWM pulse)	Device enabled, during hiccup fault recovery	6.5	7.5	8.2	µA
I_{SS2}	Charging current (after first PWM pulse)		12	15	17	µA
V_{SS_FE}	Fault enable threshold			0.8		V

(1) Specified by design. Not production tested.

Electrical Characteristics (continued)

V_{VDD} = 12 V, V_{BP5} = 15 V, V_{PVCC} = 5 V, –40°C ≤ T_J ≤ 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SSSLV}	Voltage loop slave mode threshold voltage	V_{BP5} = 5 V			V_{BP5} – 0.75	V
CURRENT LIMIT						
I_{ILIM}	Threshold setting current		21.5	23.5	25.5	µA
CURRENT SENSE AMPLIFIER						
V_{ISOFST}	Input offset voltage		–2.5	0	2.5	mV
I_{IS_CS}	Input bias current			100		nA
G_{CS}	Gain at PWM input	0.2 V ≤ V_{ICM} ≤ 5.8 V	11.25	12.5	13.75	V/V
V_{ICM}	Input common mode range		0		5.8	V
V_{DIFFMX}	Maximum differential input voltage		–60		60	mV
DIFFERENTIAL REMOVE VOLTAGE SENSE AMPLIFIER						
GRVS	Gain	0.7 V < $V_{(VOUT)}$ – $V_{(GSNS)}$ < 5.8 V	0.995	1	1.005	V/V
I_{DIFFOH}	DIFFO source current	$V_{(VOUT)}$ – $V_{(GSNS)}$ = 2 V, $V_{(DIFFO)}$ > 1.98 V, $V_{(VDD)}$ – $V_{(VOUT)}$ > 2 V			2	mA
		$V_{(VOUT)}$ – $V_{(GSNS)}$ = 5.8 V, $V_{(DIFFO)}$ > 5.6 V, $V_{(VDD)}$ – $V_{(VOUT)}$ > 1 V			1	
I_{DIFFOL}	DIFFO sink current	$V_{(VOUT)}$ – $V_{(GSNS)}$ = 2 V, $V_{(DIFFO)}$ > 2.02 V			2	mA
BW_{DIFFA}	Unity gain bandwidth[1]		5	8		MHz
$R_{INDIFFA}$	Input resistance	Inverting, DIFFO to GSNS		60		kΩ
		Noninverting, OUT to GND		60		
PSEL PIN						
I_{ISEL}	Bias current		21.5	23.5	25.5	µA
V_{MNCLK}	Master mode	No output on CLKIO	0	0	0.5	V
V_{M8PH}		8 phase CLKIO	0.5	0.7	0.9	
V_{M6PH}		6 phase CLKIO	0.9			
V_{SSTDBY}	Slave mode, standby state		3.4			V
V_{S45}	Clock slave mode, 45° phase slot[1]	8 phase CLKIO	0	0	0.2	V
V_{S90}	Clock slave mode, 90° phase slot[1]	8 phase CLKIO	0.2	0.35	0.5	V
V_{S135}	Clock slave mode, 135° phase slot[1]	8 phase CLKIO	0.5	0.7	0.9	V
V_{S180}	Clock slave mode, 180° phase slot[1]	8 phase CLKIO	0.9	1.1	1.3	V
V_{S225}	Clock slave mode, 225° phase slot[1]	8 phase CLKIO	1.3	1.6	1.9	V
V_{S270}	Clock slave mode, 270° phase slot[1]	8 phase CLKIO	1.9	2.25	2.6	V
V_{S315}	Clock slave mode, 315° phase slot[1]	8 phase CLKIO	2.6	3	3.4	V
V_{S0}	Clock slave mode, 0 phase slot[1]	6 phase CLKIO	1.9	2.25	2.6	V
V_{S60}	Clock slave mode, 60° phase slot[1]	6 phase CLKIO	0	0	0.2	V
V_{S120}	Clock slave mode, 120° phase slot[1]	6 phase CLKIO	0.2	0.35	0.5	V
V_{S180}	Clock slave mode, 180° phase slot[1]	6 phase CLKIO	0.5	0.7	0.9	V

Electrical Characteristics (continued)

V_{VDD} = 12 V, V_{BP5} = 15 V, V_{PVCC} = 5 V, –40°C ≤ T_J ≤ 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{S240}	Clock slave mode, 240° phase slot(1)	6 phase CLKIO	0.9	1.1	1.3	V
V_{S300}	Clock slave mode, 300° phase slot(1)	6 phase CLKIO	1.3	1.6	1.9	V
GATE DRIVERS						
$R_{HDRV(on)}$	HDRV pull up resistance	V_{BOOT} = 5 V, $V_{(SW)}$ = 0 V, I_{HDRV} = 100 mA	1	2	3	Ω
$R_{HDRV(off)}$	HDRV pull down resistance	V_{BOOT} = 5 V, $V_{(SW)}$ = 0 V, I_{HDRV} = 100 mA	0.5	1	2	Ω
$R_{LDRV(on)}$	LDRV pull up resistance	V_{PVCC} = 5 V, I_{LDRV} = 100 mA	1	2	3.5	Ω
$R_{LDRV(off)}$	LDRV pull down resistance	V_{PVCC} = 5 V, I_{LDRV} = 100 mA	0.3	0.75	1.5	Ω
$t_{HDRV(r)}$	HDRV rise time(1)	C_{LOAD} = 3.3 nF		25	75	ns
$t_{HDRV(f)}$	HDRV fall time(1)	C_{LOAD} = 3.3 nF		25	75	ns
$t_{LDRV(r)}$	LDRV rise time(1)	C_{LOAD} = 3.3 nF		25	75	ns
$t_{LDRV(f)}$	LDRV fall time(1)	C_{LOAD} = 3.3 nF		10	60	ns
POWER GOOD						
V_{FBPG_H}	Power good high FB voltage threshold		764	787	798	mV
V_{FBPG_L}	Power good low FB voltage threshold		591	611	626	mV
$V_{FBPG(hyst)}$	Power good threshold hysteresis		30		60	mV
T_{PGDLY}	Power good delay time(1)			10		µs
V_{PGL}	Power good low level output voltage	I_{PG} = 2 mA		0.35	0.4	V
I_{PGLK}	Power good leakage current	V_{PG} = 5 V		1		µA
OVERVOLTAGE AND UNDERVOLTAGE						
V_{FB_U}	FB pin under voltage threshold		565	580	595	mV
V_{FB_O}	FB pin over voltage threshold		792	810	828	mV
THERMAL SHUTDOWN						
T_{TSD}	Shutdown temperature(1)		126	135	144	°C
$T_{TSD(hyst)}$	Hysteresis(1)			40		°C
T_{WRN}	Warning temperature(1)		106	115	124	°C
$T_{WR(hyst)}$	Hysteresis(1)			10		°C

6.6 Typical Characteristics

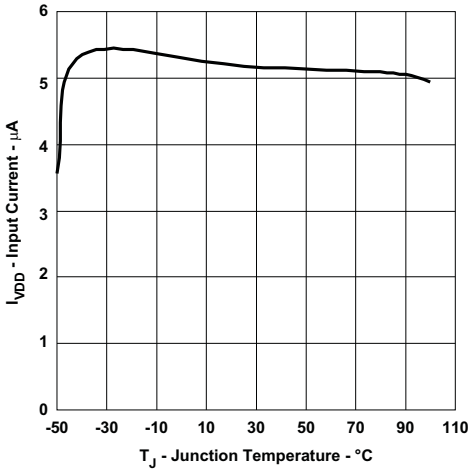


Figure 1. Input Shutdown Current vs Junction Temperature

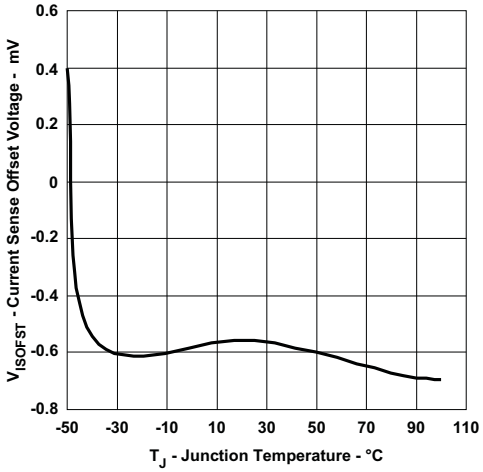


Figure 2. Current Sense Amplifier Offset Voltage vs Junction Temperature

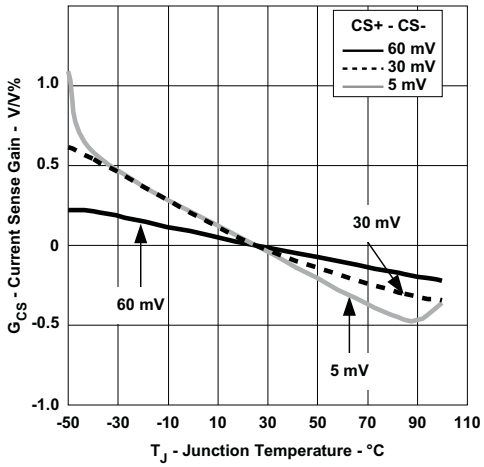


Figure 3. Relative Current Sense Gain vs Junction Temperature

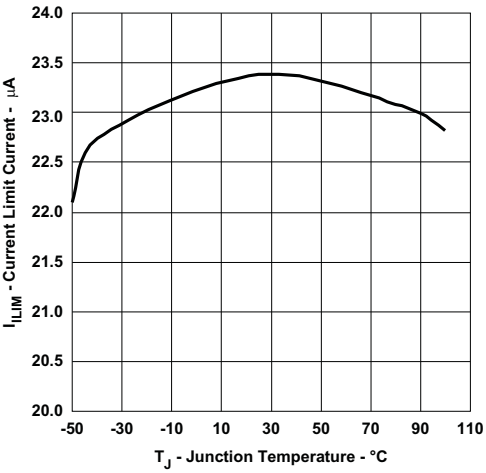


Figure 4. Current Limit vs Junction Temperature

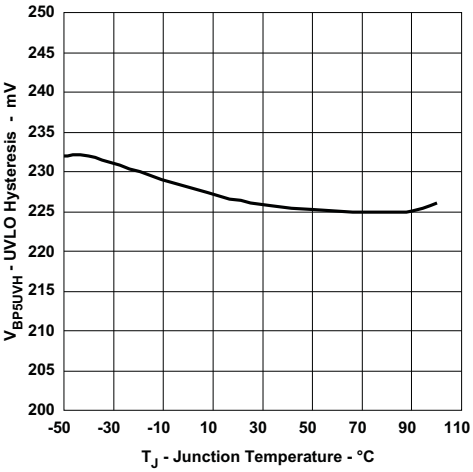


Figure 5. UVLO Hysteresis vs Junction Temperature

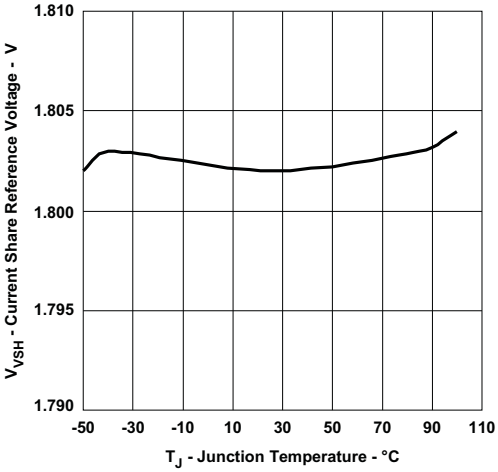


Figure 6. Current Share RE Voltage vs Junction Temperature

Typical Characteristics (continued)

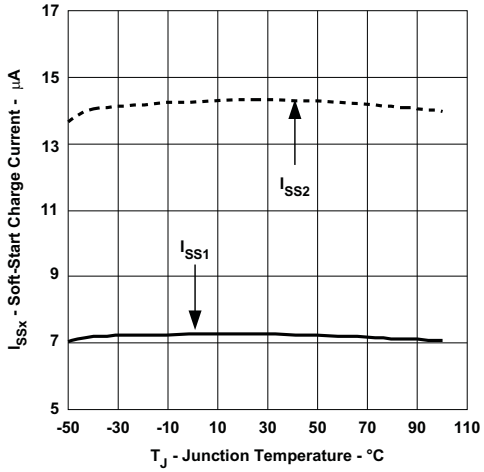


Figure 7. Soft-Start Charge Current vs Junction Temperature

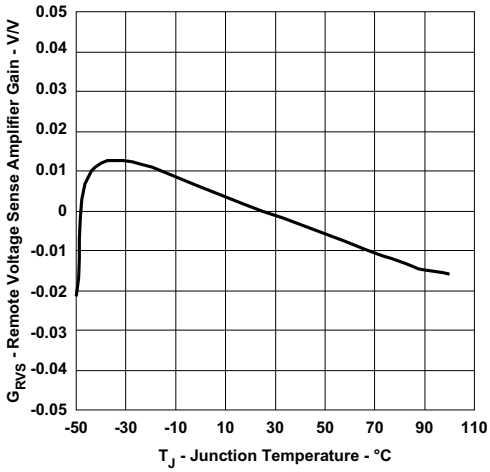


Figure 8. Remote Voltage Sense Amplifier vs Junction Temperature

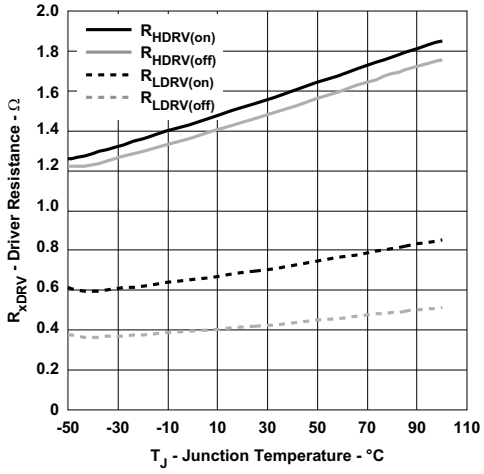


Figure 9. Driver Resistance vs Junction Temperature

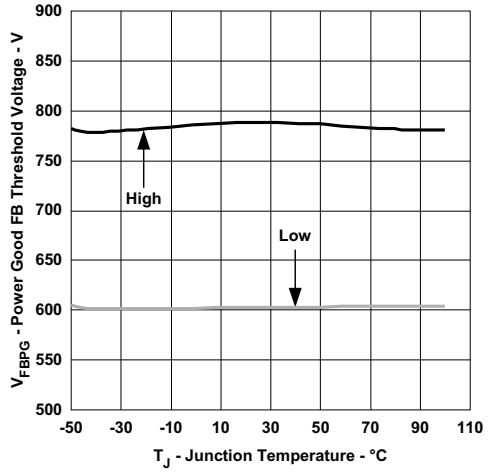


Figure 10. Power Good Threshold Voltage vs Junction Temperature

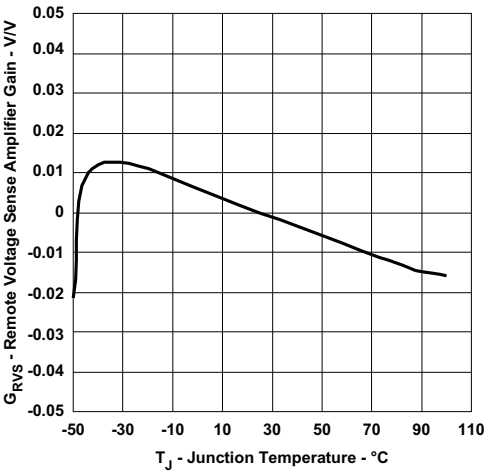


Figure 11. Power Good Low Threshold Voltage vs Junction Temperature

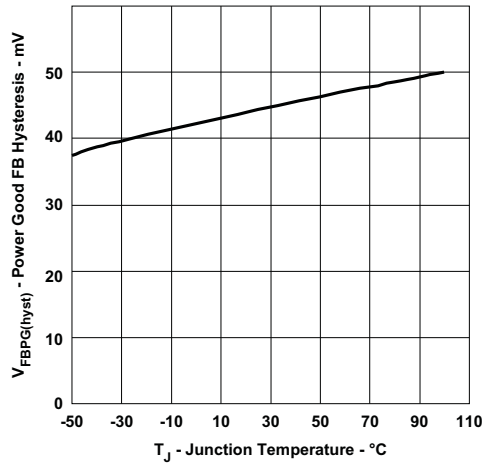


Figure 12. Power Good FB Hysteresis vs Junction Temperature

Typical Characteristics (continued)

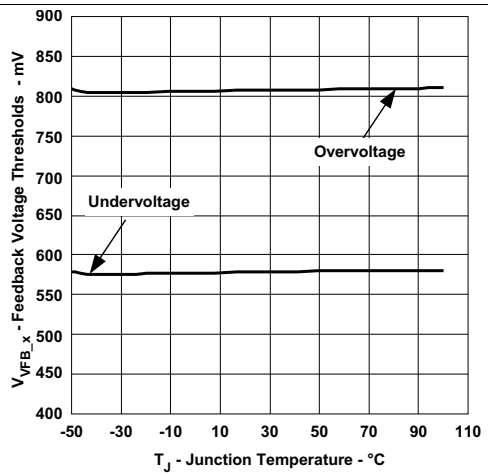


Figure 13. Undervoltage and Overvoltage Threshold vs Junction Temperature

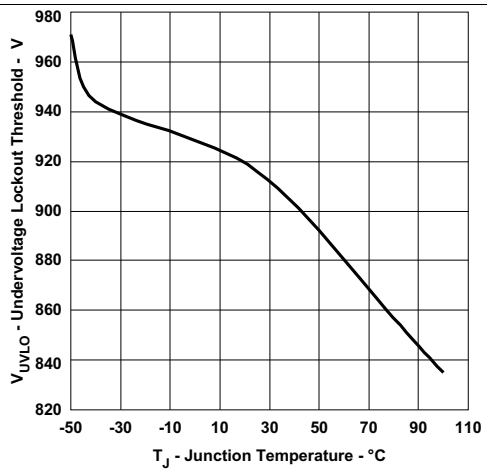


Figure 14. UVLO Enable Threshold vs Junction Temperature

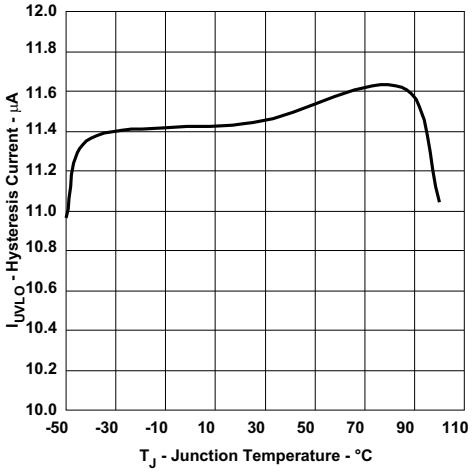


Figure 15. UVLO Hysteresis Current vs Junction Temperature

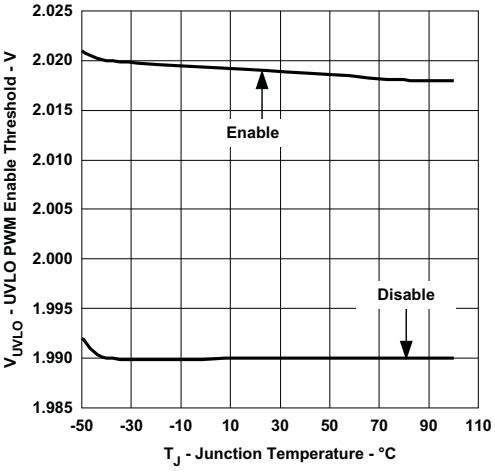


Figure 16. UVLO PWM Enable Threshold Voltage vs Junction Temperature

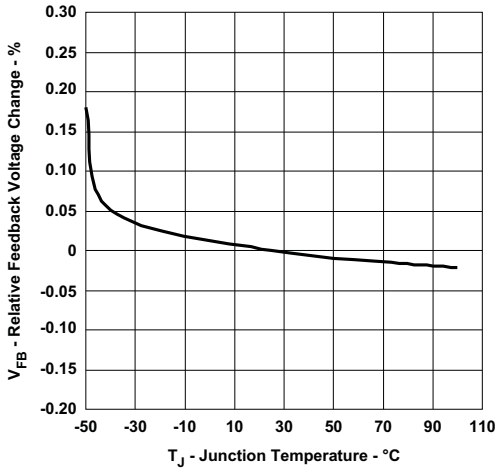


Figure 17. Relative Feedback Reference Voltage Change vs Junction Temperature

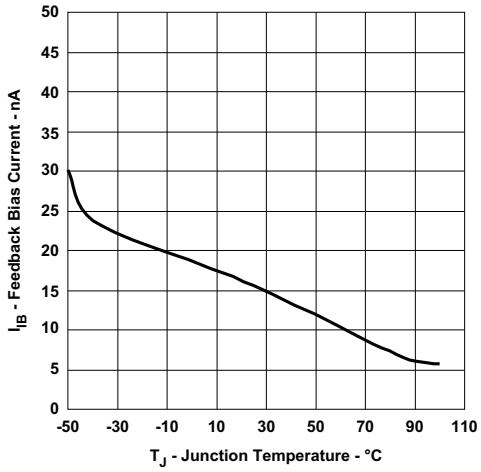


Figure 18. Feedback Bias Current vs Junction Temperature

Typical Characteristics (continued)

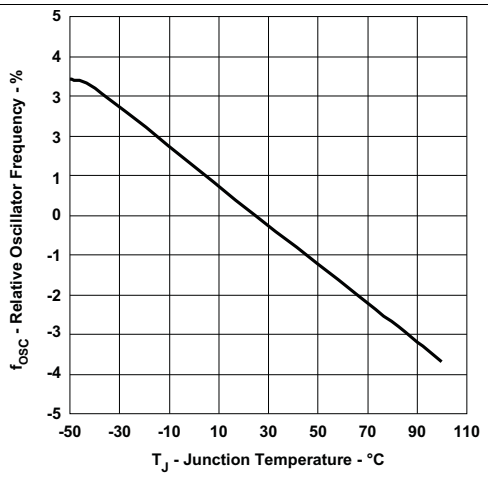


Figure 19. Relative Oscillator Frequency vs Junction Temperature

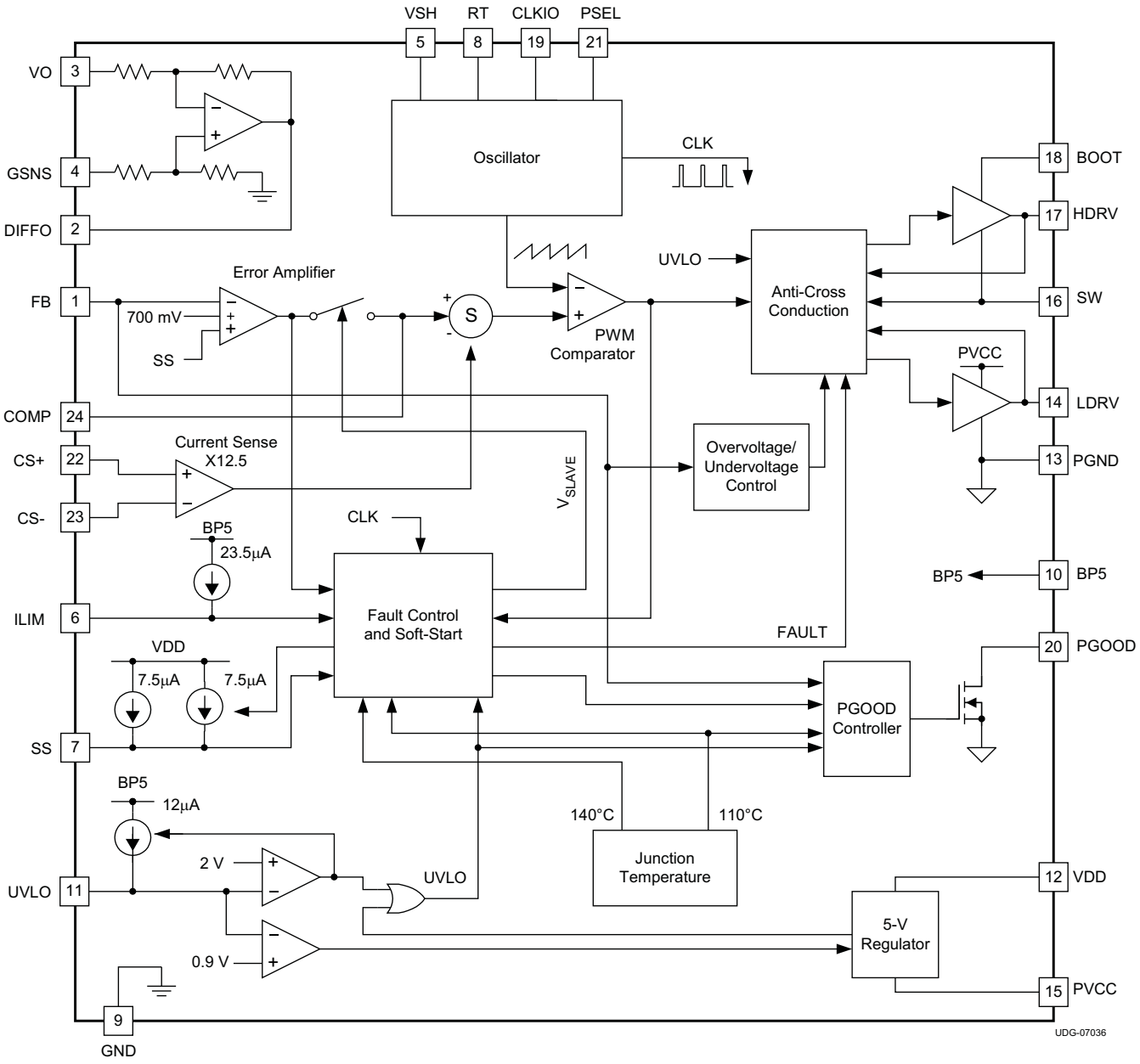
7 Detailed Description

7.1 Overview

The TPS40180 is a versatile single-phase controller that can be used as a building block for a more complex power system, or as a stand-alone power supply controller. In either system, the TPS40180 provides an excellent power conversion solution and supports such features as prebias start-up, intelligent fault handling capability with graceful shutdown and restart even with multiple modules sharing a common load. Remote load voltage sense for improved load regulation where it counts, at the load, thermal shutdown, remote enable and power good indication features help solve the problems faced by the power supply designer. To ease application to a specific task, there are several user programmable features including closed loop soft-start time, operating frequency and current limit level.

More complex power solutions are readily supported by the TPS40180. The device can be configured to run in a master/slave configuration where a master can control several slaves. Several options are possible including a single output multiple phase supply sharing phase timing information to reduce input and output ripple, a multiple output supply that shares phase switching timing information to reduce input ripple currents, and a combination approach that has multiple outputs sharing phase information where each output can use multiple phases. Phase information in all cases comes from a single device designated the clock master. Current sharing information is passed from the device designated voltage loop master for each output to the slaves for that particular output rail by connecting the COMP pin of the master to the COMP pin of the slaves. The clock master is also the voltage loop master in one of the rails of a multiple output supply; whereas, the other rails are controlled by a voltage loop master that is a clock slave to the single clock master device.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Current Sensing and Overcurrent Detection

The TPS40180 uses the current sensing architecture shown in Figure 20.

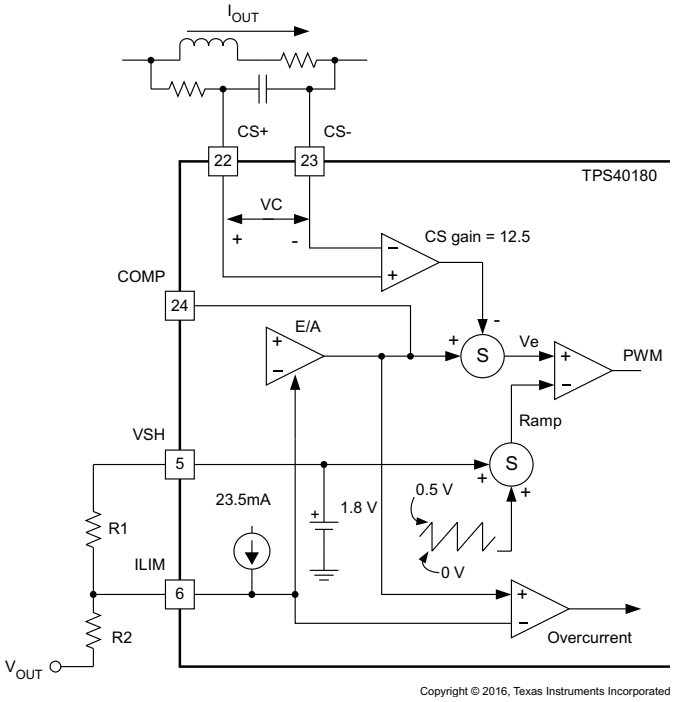


Figure 20. Current Sense Architecture

The sense resistor can either be a resistor between the inductor and the output capacitor(s) or an R-C filter across the inductor.

Overcurrent protection for the TPS40180 is set by connecting a resistor from the ILIM pin to the VSH pin. A current source of 23.5 µA out of the ILIM pin sets a voltage level on the ILIM pin and the COMP pin is not allowed to rise above this level. Since the device uses current mode control and COMP cannot rise above this level, an effective maximum output current is defined. The second resistor on the ILIM pin, R2, is optional and if used is connected to the output voltage. This resistor provides compensation of the overcurrent level for changes in output voltage, such as would be seen at start-up. If not used, the overcurrent threshold level is higher at output voltages lower than the designed target.

The output current, flows through the inductor resistance and develops a voltage, VC across it, representative of the output current. This resistance voltage is extracted from the total inductor voltage by the R-C network placed across the inductor. This voltage is amplified with a gain of 12.5 and then subtracted from the error amplifier output, COMP, to generate the Ve voltage. The Ve signal is compared to the slope-compensation RAMP signal to generate the PWM signal that is used to control the FET drivers. As the output current is increased, the amplified VC causes the Ve signal to decrease. In order to maintain the proper duty cycle, the COMP signal must increase. Therefore, the magnitude of the COMP signal contains the output current information as shown in Equation 1 through Equation 3.

$$COMP = V_e + (I_{pk} \times R_L) \times 12.5 \quad (1)$$

$$I_{RIPPLE} = \left(\frac{(V_{IN} - V_{OUT})}{L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f_{SW}}\right) \quad (2)$$

$$I_{PK} = \left(\frac{I_{RIPPLE}}{2}\right) + I_{OUT} \quad (3)$$

In order to satisfy the input-output voltage relationship, Equation 4 must hold.

Feature Description (continued)

$$Ve = V_{RMP} \times \frac{V_{OUT}}{V_{IN}} + V_{VSH} \quad (4)$$

Combining Equation 1 and Equation 4 and solving for the COMP voltage gives Equation 5.

$$COMP = V_{RMP} \times \left(\frac{V_{OUT}}{V_{IN}} \right) + V_{VSH} + (I_{PK} \times R_L) \times 12.5 \quad (5)$$

Since COMP and ILIM are of equal voltage when at the current limit condition, setting ILIM to the expected COMP voltage at maximum current is how the current limit threshold is set. To calculate the resistors R1 and R2 from Figure 20, use Equation 6 through Equation 9.

$$\alpha = \left(\frac{V_{RMP}}{V_{IN}} \right) \quad (6)$$

$$\beta = R_L \times 12.5 \times I_{PK} + \left(\frac{V_{RMP}}{(2 \times N_{ph})} \right) \quad (7)$$

$$R1 = \frac{\beta + \alpha \times V_{VSH}}{(1 - \alpha) \times I_{ILIM}} \quad (8)$$

$$R2 = \frac{\alpha + \beta \times V_{VSH}}{\alpha \times I_{ILIM}}$$

where (for Equation 1 through Equation 9)

- COMP is the voltage on the COMP pin
- V_{RMP} is the ramp amplitude, 500 mV
- V_{OUT} is the output voltage of the converter
- I_{OUT} is the dc output current of the converter
- V_{IN} is the input voltage of the converter
- V_{VSH} is the valley voltage of the ramp, 1.8 V
- I_{PK} is the peak current in the inductor
- R_L is the DC resistance of the inductor
- L is the inductance of the inductor
- 12.5 is the gain of the current sense amplifier network inside the device
- N_{ph} is the number of phase that the master clock is set to, either 6 or 8
- I_{ILIM} is the bias current out of the ILIM pin, 23.5 µA typical (9)

The TPS40180 architecture inherently allows multiple modules to start simultaneously into a load without problems with overcurrent tripping. The reason this is the case is the master device in a group of devices configured as a multiphase power supply is the only device that retains overcurrent control. The slave devices do not have the ability to initiate an overcurrent event but rely on the master to handle this function. For this reason, when setting the overcurrent threshold for a multiple converter system, the previous equations should be used to set the threshold on a per-converter basis. For example, if four converters are being used to generate a supply that has a 60-A current limit, the current limit to use for calculating the resistors would be 15 A.

NOTE

The above equations indicate that the overcurrent threshold is dependent on input voltage. Consequently, as the input voltage increases, the overcurrent threshold also rises.

7.3.2 Hiccup Fault Recovery

To reduce the input current and component dissipation during on overcurrent event, a hiccup mode is implemented. Hiccup mode refers to a sequence of 7 soft-start cycles where no MOSFET switching occurs, and then a re-start is attempted. If the fault has cleared, the re-start results in returning to normal operation and regulation. This is shown in Figure 21.

Feature Description (continued)

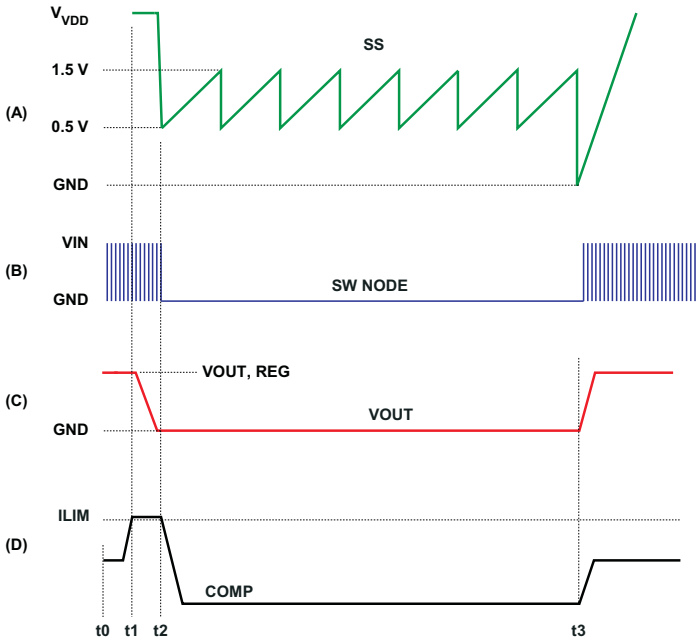


Figure 21. Hiccup Recovery From Faults

Normal operation is occurring between t0 and t1 as shown by VOUT at the regulated voltage, (C) and normal switching on the SW NODE (B) and COMP at its nominal level, (D). At t1, an overcurrent load is experienced. The increased current forces COMP to increase to the ILIM level as shown in (D). If the COMP voltage is above the ILIM voltage for 7 switching cycles, the controller enters a hiccup mode at t2. During this time the controller is not switching and the power MOSFETs are turned off. The SS pin goes through 7 cycles of charging and discharging the soft-start capacitor. At the end of the 7 cycles the controller attempts another normal re-start. If the fault has been cleared, the output voltage comes up to the regulation level as shown at time t3. If the fault has not cleared, the COMP voltage again rises above the ILIM voltage and a fresh hiccup cycle starts. This condition may continue indefinitely.

The prebias circuitry is reset at this time and the restart does not discharge an output prebias condition if it exists.

7.3.3 Selecting Current Sense Network Components

Some consideration must be given to selecting the components that are used to sense current in the converter. If an R-C filter across the inductor is used, the R-C time constant should match the natural time constant of the inductor. Equation 10 and Figure 22 describe the relationship.

$$R_{CS} \times C_{CS} = \left(\frac{L}{R_L} \right) \tag{10}$$

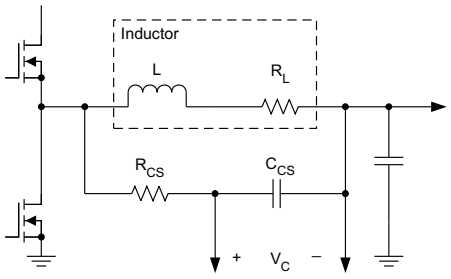


Figure 22. Current Sense Network

Feature Description (continued)

The amplitude of the V_C voltage must also be considered. If the V_C voltage is expected to rise above 60 mV at the desired overcurrent threshold, an attenuator should be used to keep the voltage to a maximum of 60 mV. To implement the divider, place a resistor in parallel with C_{CS}. The time constant of the whole network should remain the same as the L/R time constant of the inductor.

High-ripple current applications can also cause problems under certain conditions. When the sensing network is matched to the inductor, the ripple voltage on the capacitor C_{CS} is the same as the ripple voltage produced on the effective inductor resistance. If this ripple component is too great, subharmonic instability can result and the PWM exhibits excessive jitter or give a long pulse, short pulse type of output. To minimize this effect, the slope of the signal presented to the current sense amplifier must be less than a maximum value. This places a minimum limit on what the inductor L/R time constant can be for a given application as shown in Equation 11. If the chosen inductor and other application parameters fall outside these recommendations, it is necessary to attenuate the current feedback signal with an extra resistor.

$$\left(\frac{L}{R_L}\right) > \frac{G_{CS(max)} \times (V_{IN} + (2 \times V_{OUT}))}{f_{SW}} \quad (11)$$

where

- L is the inductance in H
- R_L is the equivalent series resistance of the inductor in Ω
- $G_{CS(max)}$ is the maximum gain of the current sense amplifier, 13.75
- V_{IN} is the input voltage in V
- V_{OUT} is the output voltage in V
- f_{SW} is the switching frequency in Hz

7.3.4 PGOOD Functionality

PGOOD functions as a normal, open-drain power good output on an device configured as a master. This is an open-drain signal and pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include:

- FB pin more that ±15% from nominal
- Soft start is active
- A UVLO condition exists for the TPS40180
- The TPS40180 has detected a short-circuit condition
- The TPS40180 die is over warning temperature threshold (115°C)

If the device is configured as a voltage loop slave, PGOOD pulls low the following conditions only:

- A UVLO condition exists for the TPS40180
- The TPS40180 die is over warning temperature threshold (115°C)

Note that when there is no power to the device, PGOOD is not able to pull close to GND if an auxiliary supply is used for the power good indication.

7.3.5 Output Overvoltage and Undervoltage Protection

If the output voltage is sensed to be too low, the TPS40180 turns off the power FETs, and initiates a hiccup restart sequence just as if a fault condition had occurred. The sensing of the output voltage is done using the FB pin and the undervoltage threshold voltage for the FB pin is 580-mV typical. The prebias circuitry is reset at this time and the restart does not discharge an output prebias condition if it exists.

The TPS40180 also includes an output overvoltage protection mechanism. This mechanism is designed to turn on the low-side FET when the FB pin voltages exceeds the overvoltage protection threshold of 810-mV (typical). The high-side FET turns off and the low-side FET turns on and stays on until the voltage on the FB drops below the undervoltage threshold. At this point, the controller enters a hiccup recovery cycle as in the undervoltage case. The output overvoltage protection scheme is active at all times. If at any time when the controller is enabled, the FB pin voltage exceeds the overvoltage threshold, the low-side FET turns on until the FB pin voltage falls below the undervoltage threshold.

Feature Description (continued)

7.3.6 Overtemperature Protection

When the TPS40180 die temperature exceeds 115°C, the PG pin is pulled low as a warning that temperatures are becoming excessive. Systems can act on this indication as appropriate.

The TPS40180 shuts down if the die temperature is sensed to be more than 135°C. The die must cool to less than the warning level reset of 105°C before the device restarts. The device restarts automatically after the die cools to this level.

7.3.7 eTRIM™

The TPS40180 incorporates an innovative new feature that allows the user to trim the reference voltage in system. This allows the user to tighten overall output tolerances by trimming out errors caused by resistor divider and other system tolerances. The reference has been designed so that it may be trimmed without affecting temperature drift so that the user can perform system level trims without worrying about creating a situation where the reference temperature drift becomes a problem. Trimming in the TPS40180 is done with a small bank of EEPROM. Changing bit values in this EEPROM causes parameters, like reference voltage, inside the device to change. Once trim is accomplished, there is no need to trim again, the change is permanent (but can be overwritten by subsequent trimming operations). The eTrim™ trimming mechanism has been designed so that the user can only program the reference voltage so that any errors in the programming sequence does not affect other factory set trims such as current feedback gain for example. This provides a secure environment for the user to use and eliminates the possibility that other parameters could inadvertently changed.

The adjustment range is ±14 mV from the untrimmed level. The reference is pre-trimmed at the factory to ±0.5% of nominal so further trim is not necessary unless it is desired to further reduce total system errors. This factory trim uses the same eTrim™ mechanism that can be used at the system or converter level and changes the same bits that the user changes if using eTrim™. Consequently, not all of the trim range may be available to make adjustments in system as the factory trim sets the bits to the value that provides the correct nominal reference voltage. Typically, the trim has at least 3 steps remaining in any direction to allow for user system level trim.

There are several steps required to use the eTrim™ feature. A typical trim sequence would flow as follows:

1. Power up the system and wait for the system to stabilize in steady state
2. Program the TPS40180 reference trim to a default setting (overwriting factory trim)
3. Measure the system output voltage
4. Calculate a correction factor to be applied to the output voltage
5. Program the EEPROM inside the TPS40180 with the new trim code
6. Measure the new system output voltage
7. Repeat from step 4 if required

The TPS40180 provides 4 trim bits available for user programming. The bits and their effect on the untrimmed reference value are given in Table 1.

Table 1. eTrim Bit Codes and Effect

eTrim™ REFERENCE BIT CODE				REFERENCE CHANGE (mV)
b3	b2	b1	b0	
1	0	0	0	+14
1	0	0	1	+12
1	0	1	0	+10
1	0	1	1	+8
1	1	0	0	+6
1	1	0	1	+4
1	1	1	0	+2
1	1	1	1	0(1)
0	0	0	0	0
0	0	0	1	–2

(1) Default setting

Table 1. eTrim Bit Codes and Effect (continued)

eTrim™ REFERENCE BIT CODE				REFERENCE CHANGE (mV)
b3	b2	b1	b0	
0	0	1	0	–4
0	0	1	1	–6
0	1	0	0	–8
0	1	0	1	–10
0	1	1	0	–12
0	1	1	1	–14

The process of writing to the on chip trim EEPROM is as follows. With power applied to the system and the system in steady state:

1. Force the input voltage to the device, V_{VDD}, to a level of 7 V (this eases stresses on the UVLO pin).
2. Raise the UVLO pin to a level 2 V above V_{VDD} and PGOOD to 20 V
3. Apply a pulse of V_{VDD} + 4 V for a minimum of 10 µs to UVLO
4. Bring UVLO to V_{VDD} + 2 V for at least 8 µs
5. The UVLO pin is then pulsed to V_{VDD} + 4 V seven times (six address bits and one data bit) for each bit that is to be written. The pulse period is typically 1 µs and the width of the pulse determines whether the pulse is interpreted as a 1 or as a 0 by the EEPROM circuitry.
6. Data has been placed in a buffer. To finalize the writing, pull PGOOD to 20 V and the UVLO pin to V_{VDD} + 4 V for at least 15 ms.

Figure 23 shows a typical sequence.

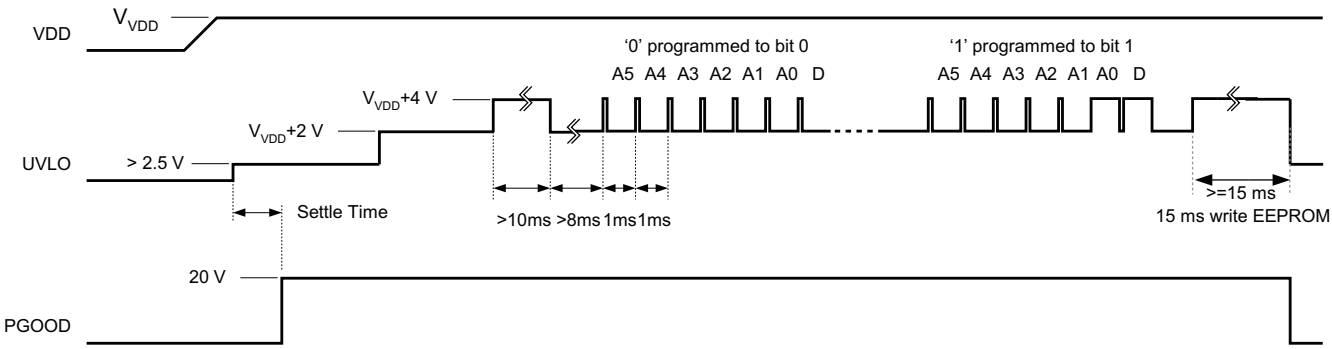


Figure 23. eTrim™ EEPROM Programming Sequence

The pulses from V_{VDD} + 2 V to V_{VDD} + 4 V on UVLO are governed by the timing shown in Figure 24.

There are six address bits in the sequence to write to a single EEPROM bit. To write to the eTrim™ accessible bits, the address sequence must be correct for all six bits or else the write attempt has no effect. To write to eTrim™ accessible bits the first four address bits must be zero. Anything else is not accepted. Address bits A1 and A0 select which eTrim™ accessible EEPROM bit is written. For example, to write a 1 to bit 3 of the eTrim™ accessible bits, the data pulse sequence would look like Figure 25.

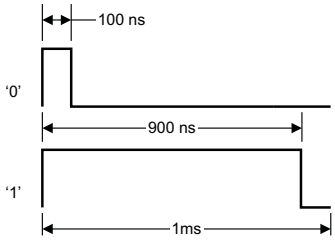


Figure 24. eTrim™ Bit Pulse Timing

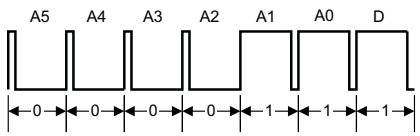


Figure 25. Write 1 to Bit 3

As data is clocked into the device, the reference voltage reflects the updates without writing the data buffer to the actual EEPROM. System measurements can be made after a suitable system dependent settling time has elapsed after changing the bits in the buffer. When satisfied with the results, the EEPROM may be written by pulling PGOOD to 20 V and UVLO to V_{VDD} + 4 V for at least 15 ms. For best reliability, the EEPROM should only be written to by pulling PGOOD to 20 V and UVLO to V_{VDD} + 4 V a maximum of three times during the product lifetime. This writing only needs to be done once during the entire trimming cycle, after the optimal trim values are found since data clocked in will affect the output without performing the actual write. Until written, changes are not permanent and will be lost after power cycling the device.

7.3.8 Connections Between Controllers for Stacking

One of the main benefits of using the TPS40180 is the ability to parallel output power stages to achieve higher output currents and to scale or stack on controllers as needed. Phasing information is also shared among the controllers to minimize input ripple and RMS current in the input stage capacitors. Figure 26 shows the connections among the controller devices and the controller configuration connections to implement a single output stacked configuration. Up to 7 slave controllers can be connected to the master controller in this manner with unique phasing for each controller. More than 7 controllers can also be connected as long as some of them are programmed to operate at the same phase relationship with respect to the master. Not shown are the power stage portions of the schematics. The outputs of the individual converters inductors are simply connected together and then to a common output capacitor bank. All other connections would be as for a single device used as a converter.

In Figure 26, the master controller is configured as a CLK master and as a voltage control loop master (SS and RT pin connections). The slave controllers are configured as CLK slaves (RT pin tied to PVCC) and as voltage control loop slaves (SS pin tied to PVCC).

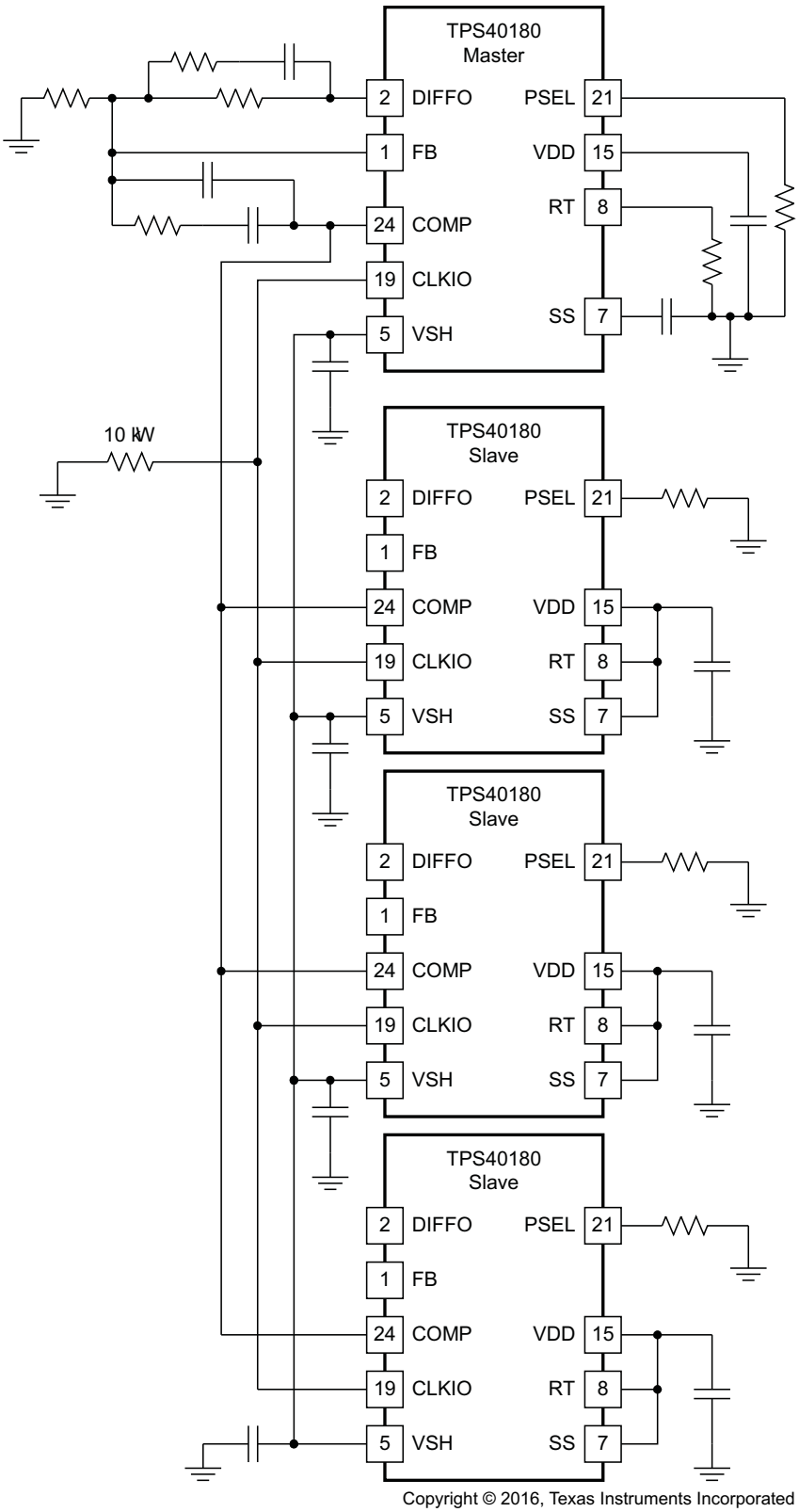


Figure 26. Single-Output Stacked Configuration

The 10-kΩ resistor connected from the CLKIO line to GND is required to ensure that the CLKIO line falls to GND quickly when the master device is shutdown or powers off. The master CLKIO pin goes to a high impedance state at these times and if the CLKIO line was high, there is no other active discharge part. The slave controllers look at the CLKIO line to determine if the system is supposed to be running or not. A level below 0.5 V on CLKIO is required for this purpose. If the CLKIO line remains high after that master is shut down, the slaves continue to operate. This is seen as the slave LDRV signal remaining high for a period of time after the master is shut down and results in output voltage excursions that are not controlled.

NOTE

In any system configured to have a CLK master and CLK slaves, a 10-kΩ resistor connected from CLKIO to GND is required.

For simplicity of design, the compensation components shown on the master, as well as the components connected to the RT and SS pins may be present on the slaves. This prevents separate designs being necessary for master and slave circuits. The RT and SS pins can have jumper option to tie them to VDD to program an individual device as a slave. These components were omitted in Figure 26.

Selection of the PSEL pin resistors is simple. First determine if the master should generate a CLK signal that is suitable for 60 or 45 spacing of the phases. Select the appropriate PSEL connection option from Table 3. For the slaves, determine the desired firing angle for each one and pick the appropriate resistor from either Table 4 or Table 5 depending on the clock scheme chosen for the master.

Design Note: When used in a master/slave relationship and an overvoltage event occurs, only the control loop master turns on the low-side FET to pull down the output voltage. This results in the master phase low-side FET sinking all of the combined maximum current for the slaves. For example, if the per phase current limit is 10 A and there are 4 phases, the master low-side FET could be required to pass 30 A for a brief time. The master error amplifier is still active during this time and tries to have the slaves regulate the output voltage. As the master COMP pin rises to the ILIM point, a fault event is sensed and the converter shuts down, and then initiate a hiccup restart. Size the master low-side FET to handle the appropriate amount of surge current for 7 clock cycles of the converter.

A connection diagram for several controllers sharing phase information and synchronized to each other but having different output voltages is shown in Figure 27. This is similar to the previous example but here the controllers are all control loop masters (SS not pulled to VDD) and control their own output voltages independently. One device is configured as a CLK master (RT not tied to VDD) and is the clock generator for the CLK slaves. Picking the PSEL resistors is the same as before. overcurrent in this configuration depends on which controller senses the overcurrent event. If one of the CLK slaves experiences a fault, that converter only shuts down, and enter the hiccup restart mode. If the CLK master controller senses an overcurrent, it stops sending CLKIO pulses to the slaves, causing them to stop. The master then enters a hiccup recovery mode.

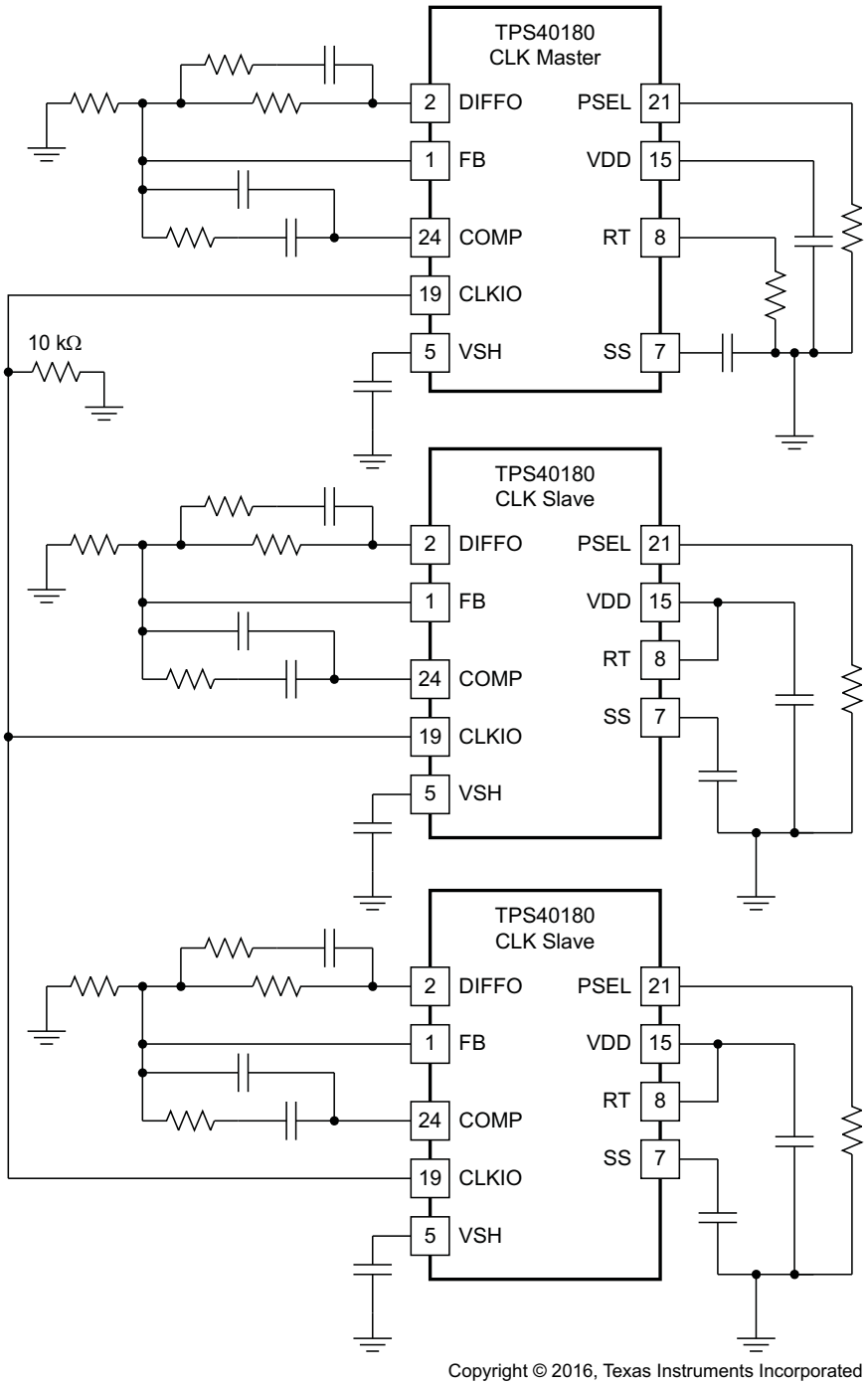


Figure 27. Phase Share Multiple Output Configuration

Finally, a configuration diagram for multiple multiphase converters is shown in Figure 28. This is just a combination of the two previous examples and should follow intuitively once those are understood. It is the example of Figure 26 with a CLK slave but control loop master added to create a second output voltage while sharing phasing information with the first converter group. A slave has been added to the second control loop master controller in this case as well creating a grouping of controllers that provide a second output voltage. This can have a significant impact on the required input filter capacitance if all the converters are located close to one another.

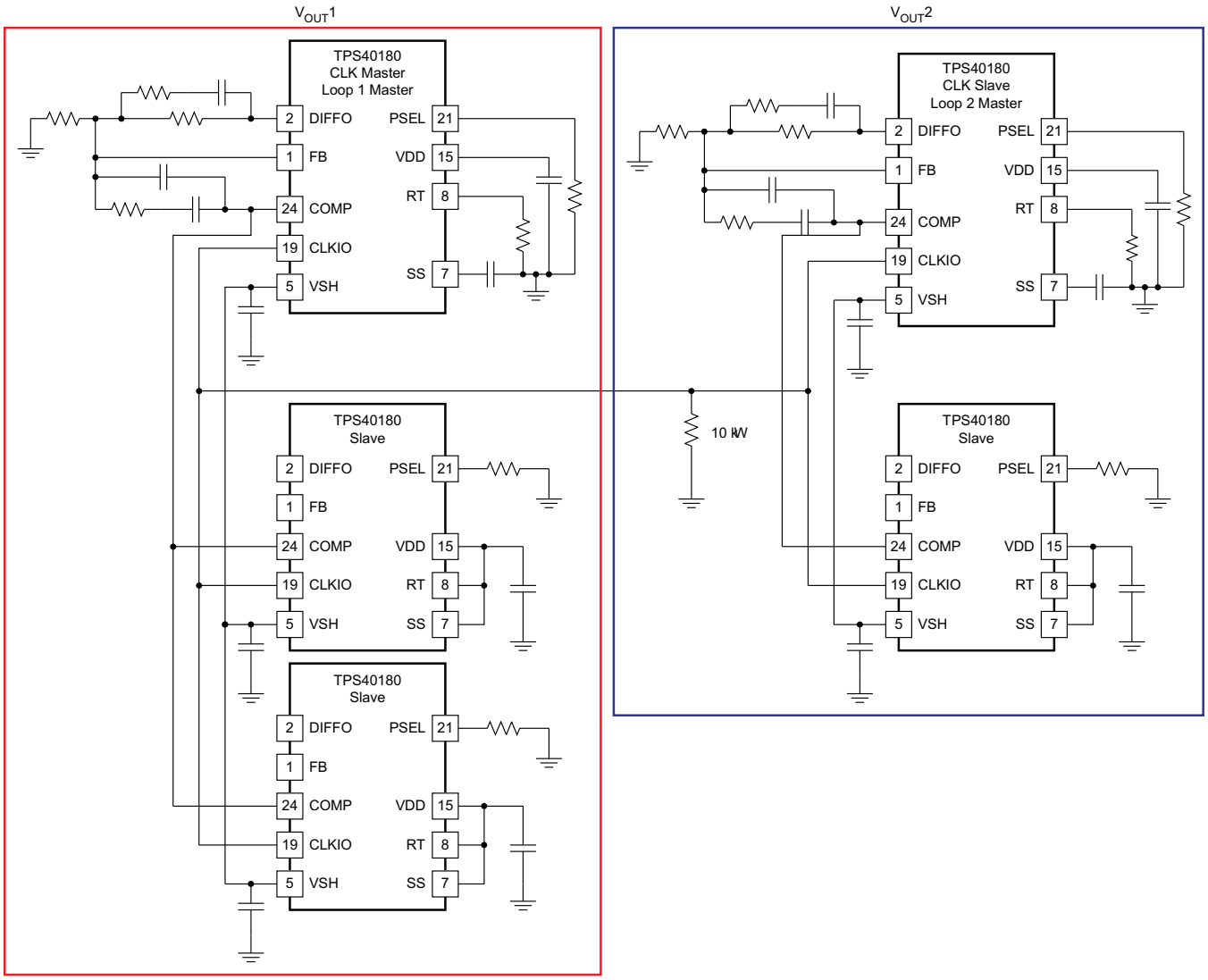


Figure 28. Multiple Multiphase Configuration

7.3.9 VSH Line in the Multiphase

The examples in Figure 26, Figure 27, and Figure 28 show the VSH line distributed among the various controllers comprising a single-output voltage grouping. This is the recommended practice for best results. However, if the ground potential difference between the controllers is not great (no more that 10 mV), distribution of VSH among the controllers in a particular output voltage group may not be necessary. VSH is the valley voltage of the controller and distributing it provides a known current reference signal among the controllers that when compared with the distributed COMP signal from the master, serves to better balance the current among the modules. If the ground potential between modules in the same output voltage grouping is small enough, there error contributed by not distributing the VSH signal becomes on the order of systematic errors already present and its usefulness is diminished. A decision must be made on an individual application basis.

7.4 Device Functional Modes

7.4.1 Tracking

The TPS40180 can function in a tracking mode, where the output tracks some other voltage. To do this, a voltage divider is connected from the voltage to be tracked to GND, with the tap of the divider connected to the SS pin of the TPS40180 (see Figure 29). The capacitors C1 and C2 are required for two purposes. First they provide a means for timing of overcurrent restart attempts. Second, they provide for matching output voltage ramp up rate of the TPS40180 to the controlling external supply.

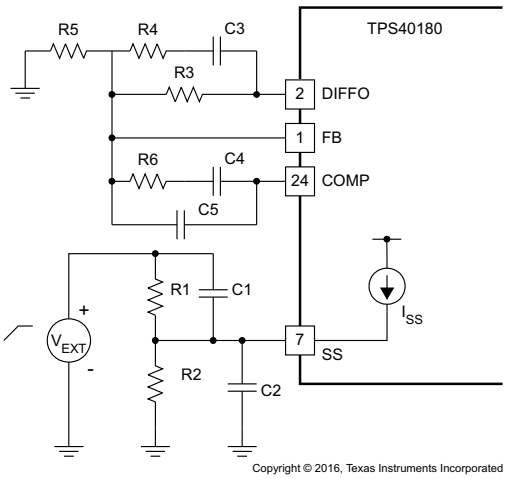


Figure 29. Tracking Setup

When choosing component values, the SS pin current (I_{SS}) must be accounted for in order to prevent an offset in the output of the TPS40180 converter and the tracked supply.

$$R1 = \left(\frac{R3}{R5}\right) \times R2 \times \left(\frac{V_{REF}}{V_{REF} - (I_{SS} \times R2)}\right)$$

where

- R1, R2, R3, and R5 are in Ω
- V_{REF} is the reference voltage fo the TPS40180, 700 mV
- $I_{(SS)}$ is the SS pin current, 15 µA typical (12)

To use Equation 12, R3 and R5 must be known from the design of the compensation network and nominal converter output voltage. R2 is then chosen arbitrarily. A value between 1 kΩ and 10 kΩ is suggested. Too large a value and the tracking error is greater. Too small, and the requirements for C2 and C2 become excessive. Once R1 and R2 have been chosen, C1 and C2 can be chosen. The R1-C1 time constant and the R2 C2 time constant should match as in Equation 13.

$$R1 \times C1 = R2 \times C2 \quad (13)$$

Absolute matching of the time constants is not necessary for Equation 13. The nearest standard values of capacitor provides satisfactory results. Pick a value for C1 or C2 and find the closest corresponding standard value for the other capacitor.

7.5 Programming

7.5.1 Programming the Operating Frequency

A resistor is connected from the RT pin to GND to select the operating frequency of the converter. The relationship between the desired operating frequency and the timing resistance is given by Equation 14.

$$R_{RT} = \frac{3.675 \times 10^5}{(f_{SW})^2} + \frac{2.824 \times 10^4}{f_{SW}} - 5.355$$

Programming (continued)

where

- R_{RT} is the timing resistance in kΩ
- f_{SW} is the desired switching frequency in kHz (14)

If this is a clock master, the switching frequency above is the per-phase switching frequency.

7.5.2 Programming the Soft-Start Time

The soft-start time is programmable by connecting a capacitor from the SS pin to GND. An internal current source charges this capacitor providing a linear ramp voltage. This ramp voltage is the effective reference to the error amplifier while it is less that the 700-mV internal reference. The time required for the SS pin to ramp from GND to 700 mV is the soft-start time. For outputs that are not prebiased, that time is given in Equation 15.

$$T_{SS} = \frac{V_{REF} \times C_{SS}}{I_{SS}}$$

where

- t_{SS} is the soft-start time in seconds
- C_{SS} is the capacitor from SS to GND in µF
- I_{SS} is the soft-start current in µA, 15-µA typical (15)

If the output of the converter has a pre-existing voltage on it, the soft start occurs a little differently. The SS pin current is held to a lower value than normal until the PWM becomes active. This occurs as the SS pin voltage exceeds the FB pin voltage and the COMP pin moves up into the ramp range, causing the first pulse. At that point, the SS pin current is shifted to 15 µA nominal. Figure 30 and Figure 31 illustrate this.

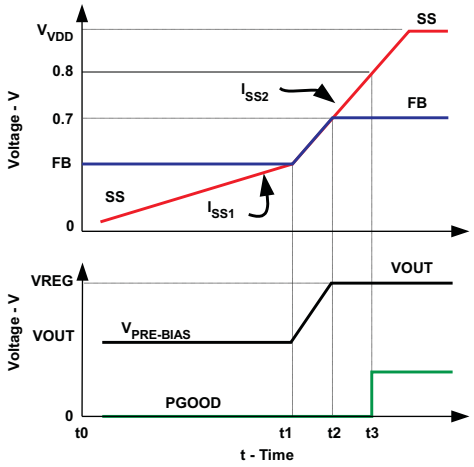


Figure 30. Soft-Start Waveform for Prebiased Outputs

Programming (continued)

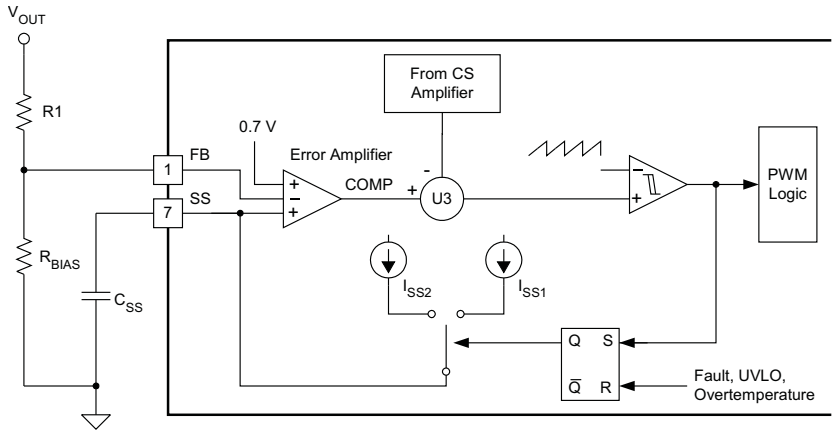


Figure 31. Soft-Start Implementation

Using Figure 30 provides Equation 16, Equation 17, and Equation 18.

$$t1 = \frac{C_{SS}}{I_{SS1}} \times \left(\frac{V_{PREBIAS} \times R_{BAIS}}{R1 + R_{BIAS}} \right) \quad (16)$$

$$t2 = \frac{C_{SS}}{I_{SS2}} \times \left(V_{REF} - \left(\frac{V_{PREBIAS} \times R_{BAIS}}{R1 + R_{BIAS}} \right) \right) \quad (17)$$

$$T_{SS} = t1 + t2 \quad (18)$$

where

- t_1 is the time to the first PWM pulse in seconds
- t_2 is the time from the first PWM pulse until regulation in seconds
- $C_{(SS)}$ is the SS pin capacitor in µF
- $I_{(SS1)}$ is the SS1 pin charging current in µA, 7.5 µA
- $I_{(SS2)}$ is the SS2 pin charging current in µA, 15 µA
- T_{SS} is the total soft-start time

7.5.3 Using the Device for Clock Master/Slave Operation

The TPS40180 can be operated as either a master clock source or a slave to a master clock as seen in Table 2.

Table 2. RT Voltage and Clock Master/Slave

RT VOLTAGE (V_{RT})	CLOCK MODE
< 0.5 V	Master (or single converter)
> 2 V (tied to PVCC or VDD)	Slave

In the clock master mode, the master clock frequency is set by connecting a resistor from the RT pin to GND. In the clock master mode, the PSEL pin selects the CLKIO operating mode for the device. There are three possible states defined in Table 3.

Table 3. PSEL Pin Modes for Clock Master

PSEL RESISTANCE TO GND (kΩ)	MODE
0	No CLKIO, CLKIO does not send out pulses
OPEN	8 phase CLKIO, CLKIO send out a pulse train for interleaving with 45° phase separation
29.4	6 phase CLKIO, CLKIO send out a pulse train for interleaving with 60° phase separation

In the clock slave mode, the CLKIO pin is an input. The controller fires in a fixed relationship to the master determined by the resistance placed from PSEL to GND, or is turned off to improve efficiency at light load. The actual result depends on how the master CLKIO is programmed in either Table 4 or Table 5.

Table 4. PSEL Phase Programming for Slave With 8 Phase Master Clock

PHASE ANGLE (°)	PSEL RESISTANCE TO GND (kΩ)
Standby	OPEN
45	0
90	14.7
135	29.4
180	47
225	68
270	95.3
315	127

Table 5. PSEL Phase Programming for Slave With 6 Phase Master Clock

PHASE ANGLE (°)	PSEL RESISTANCE TO GND (kΩ)
Standby	OPEN
0	95.3
60	0
120	14.7
180	29.4
240	47
300	68

When a slave senses any level change on the PSEL pin that would indicate a change in firing angle, it momentarily goes into standby mode. When a slave leaves standby mode, it starts supplying current after 64 clock cycles have elapsed if the status of the PSEL pin has not changed from when the device entered standby mode. In this way, a slave can have its firing angle dynamically changed depending on operating conditions. A slave can be held in standby mode by allowing the PSEL pin to float.

7.5.4 Using the TPS40180 for Voltage Control Loop Master or Slave Operation

The TPS40180 can function as a voltage loop master or as a voltage loop slave. As a voltage loop master, the TPS40180 behaves like a standard control device in that it regulates its output using its internal error amplifier and reference. As a voltage loop slave, the TPS40180 takes the VSH and COMP signals from a voltage loop master and the slave converter becomes an output current booster to the master converter. Current is shared between the master and slave since both the current command reference (VSH) and the current command (COMP) are being distributed form the master controller and used by the slave to set its output current. The error amplifier in the master is responsible for overall voltage regulation. The error amplifier on the slave is disconnected when configured as a voltage control loop slave.

To configure a TPS40180 as a voltage loop slave, connect the SS pin to VDD or PVCC. It is important that the SS pin not fall more than 1 V below the PVCC voltage when starting up as a slave. If this condition is no met, the controller may not start. For this reason, it is not recommended to tie SS to BP5 to configure the converter as a voltage control loop slave.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The first design example describes the design process and component selection for a single-phase, synchronous buck, DC/DC converter using the TPS40180 device. The design process and component selection for a two-phase design are provided as well.

8.2 Typical Applications

8.2.1 Single Output Synchronous Buck Converter

Figure 32 illustrates the design process and component selection for a single output synchronous buck converter using TPS40180. The design goal parameters are given in Table 6. A list of symbol definitions is found in *Device Nomenclature*.

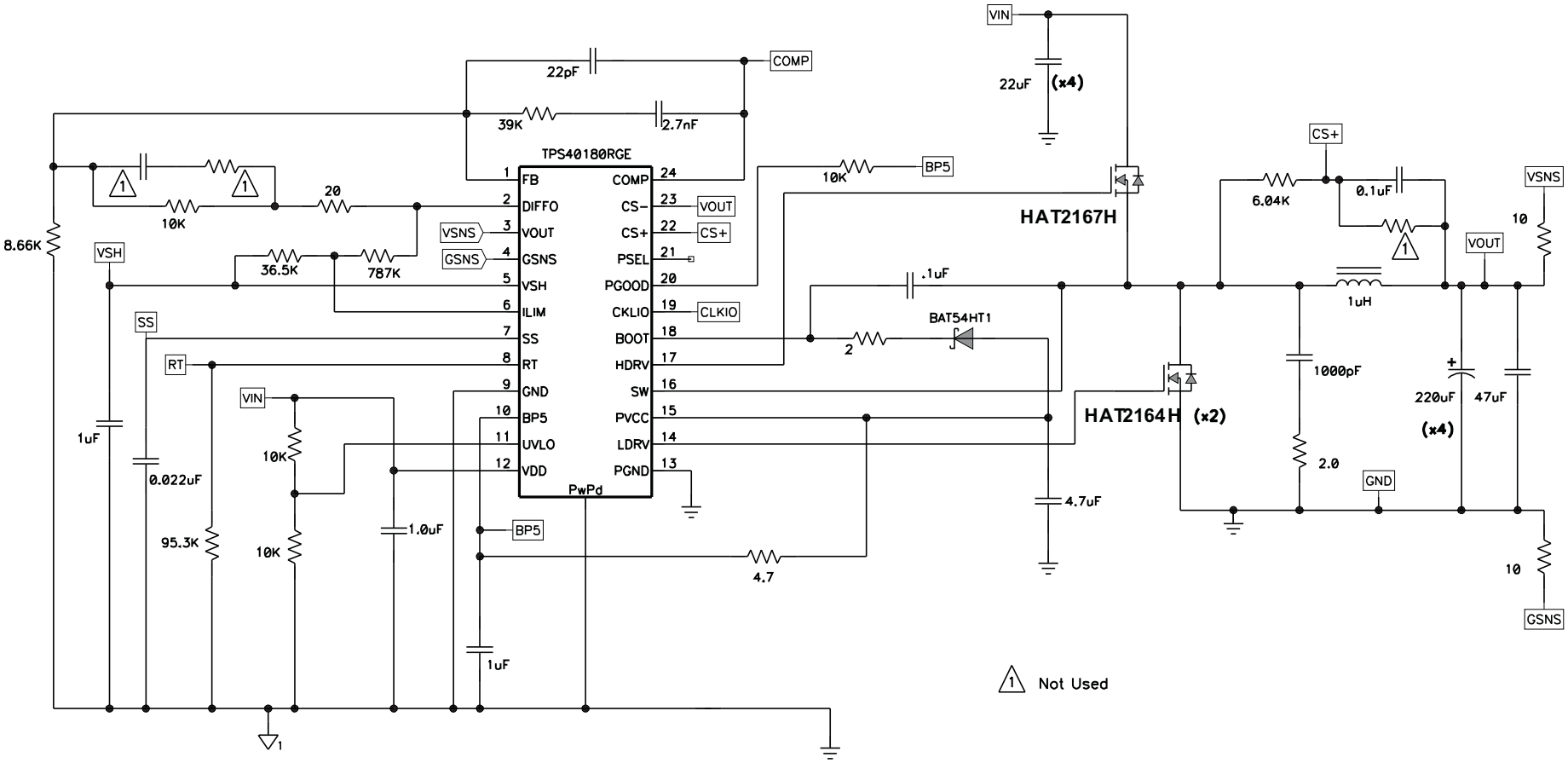


Figure 32. Single-Output Converter Schematic

8.2.1.1 Design Requirements

Table 6 lists the design parameters for the single output configuration from 12-V to 1.5-V DC-to-DC converter using a TPS40180.

Table 6. Design Goal Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		10.8	12	13.2	V
V_{OUT}	Output voltage			1.5		V
V_{RIPPLE}	Output ripple	I_{OUT} = 20 A		30		mV
I_{OUT}	Output current			20		A
f_{SW}	Switching frequency			280		kHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Inductor Selection

The inductor is determined by the desired ripple current. The required inductor is calculated by Equation 19.

$$L = \frac{V_{IN(max)} - V_{OUT}}{I_{RIPPLE}} \times \frac{VO_{UT}}{V_{IN(max)}} \times \frac{1}{f_{SW}} \quad (19)$$

Typically the peak-to-peak inductor current I_{RIPPLE} is selected to be around 25% of the rated output current. In this design, I_{RIPPLE} is targeted at 25% of I_{OUT}. The calculated inductor is 0.95 µH and in practical a 1-µH inductor with 1.7-mΩ DCR from Vishay is selected. The real inductor ripple current is 4.7 A.

8.2.1.2.2 Output Capacitor Selection

The output capacitor is typically selected by the output load transient response requirement. Equation 20 estimates the minimum capacitor to reach the undervoltage requirement with load step-up. Equation 21 estimates the minimum capacitor for over voltage requirement with load step-down. When $V_{IN(min)} < 2 \times V_{OUT}$, the minimum output capacitance can be calculated using Equation 20. Otherwise, Equation 21 is used.

$$C_{OUT}(MIN) = \frac{I^2_{TRAN(MAX)} \times L}{2 \times (V_{IN(MIN)} - V_{OUT}) \times V_{UNDER}} \quad (20)$$

$$C_{OUT}(MIN) = \frac{I^2_{TRAN(MAX)} \times L}{2 \times V_{OUT} \times V_{OVER}} \quad (21)$$

In this design, $V_{IN(min)}$ is much larger than 2 × V_{OUT}, so Equation 21 is used to determine the minimum capacitance. Based on a 8-A load transient with a maximum of 60-mV deviation, a minimum 356-µF output capacitor is required. Considering the capacitance variation and derating, four 220-µF, 4-V, SP capacitor are selected in the design to achieve sufficient margin. Each capacitor has an ESR of 5 mΩ.

Another criterion for capacitor selection is the output ripple voltage. The output ripple is determined mainly by the capacitance and the ESR. With an 880-µF output capacitance, the ripple voltage at the capacitor is calculated to be 1.5 mV. In the specification, the output ripple voltage should be less than 30 mV, so based on Equation 22, the required maximum ESR is 9.4 mΩ. The selected capacitors can meet this requirement.

$$ESR_{Co} = \frac{V_{RIPPLE(TotOUT)} - V_{RIPPLE(COUT)}}{I_{RIPPLE}} = \frac{V_{RIPPLE(TotOUT)} - \left(\frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}\right)}{I_{RIPPLE}} \quad (22)$$

8.2.1.2.3 Input Capacitor Selection

The input voltage ripple depends on input capacitance and ESR. The minimum capacitor and the maximum ESR can be estimated by Equation 23 and Equation 24.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{RIPPLE(Cin)} \times V_{IN} \times f_{SW}} \quad (23)$$

$$ESR_{Cin} = \frac{V_{RIPPLE(CinESR)}}{I_{OUT} + 1/2 I_{RIPPLE}} \quad (24)$$

For this design, assume $V_{RIPPLE(Cin)}$ is 100 mV and $V_{RIPPLE(CinESR)}$ is 50 mV, so the calculated minimum capacitance is 89 µF and the maximum ESR is 2.3 mΩ. Choosing four 22-µF, 16-V, 2-mΩ ESR ceramic capacitors meets this requirement.

Another important thing for the input capacitor is the RMS ripple current rating. The RMS current in the input capacitor is estimated with Equation 25.

$$I_{RMS\_CIN} = \sqrt{D \times (1-D)} \times I_{OUT} \quad (25)$$

where

- D is the duty cycle

The calculated RMS current is 6.6 A. Each selected ceramic capacitor has a RMS current rating of 4.3 A, so it is sufficient to reach this requirement.

8.2.1.2.4 MOSFET Selection

The MOSFET selection determines the converter efficiency. In this design, the duty cycle is very small so that the high-side MOSFET is dominated with switching losses and the low-side MOSFET is dominated with conduction loss. To optimize the efficiency, choose smaller gate charge for the high-side MOSFET and smaller $R_{DS(on)}$ for the low-side MOSFET. RENESAS HAT2167H and HAT2164H are selected as the high-side and low-side MOSFET respectively. The power losses in the high-side MOSFET is calculated with the following equations.

The RMS current in the high-side MOSFET is Equation 26.

$$ISW_{rms} = \sqrt{D \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12} \right)} = 7.08A \quad (26)$$

The $R_{DS(on)(sw)}$ is 9.3 mΩ when the MOSFET gate voltage is 4.5 V. The conduction loss is Equation 27.

$$P_{SW(cond)} = (I_{SWrms})2 \times R_{DS(on)(sw)} = 0.47\ W \quad (27)$$

The switching loss is Equation 28.

$$P_{SW(sw)} = \frac{I_{PK} \times V_{IN} \times f_{SW} \times R_{DRV} \times (Qgd_{SW} + Qgs_{SW})}{Vgtdrv} = 0.35\ W \quad (28)$$

The calculated total loss is the high-side MOSFET is Equation 29.

$$P_{SW(tot)} = P_{SW(cond)} + P_{SW(SW)} = 0.82\ W \quad (29)$$

The RMS current in the low-side MOSFET is Equation 30.

$$I_{SRrms} = \sqrt{(1-D) \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}^2}{12} \right)} = 18.7A \quad (30)$$

The $R_{DS(on)(sr)}$ of each HAT2164 is 4.4 mΩ when the gate voltage is 4.5 V. Two HAT2164 FETs are used in this design.

The conduction loss in the low-side MOSFETs is Equation 31.

$$P_{SR(cond)} = (I_{SRrms})^2 \times \left(\frac{R_{DS(on)(sr)}}{2} \right) = 0.77\ W \quad (31)$$

The total power loss in the body diode is Equation 32.

$$P_{DIODE} = 2 \times I_{OUT} \times t_D \times V_f \times f_{SW} = 0.39\ W \quad (32)$$

Therefore, the calculated total loss in the SR MOSFETs is Equation 33.

$$P_{DIODE} = P_{SR(cond)} + P_{DIODE} = 1.16\ W \quad (33)$$

8.2.1.2.5 Peripheral Component Design

8.2.1.2.5.1 Switching Frequency Setting (RT)

$$R_T = \frac{3.675 \times 10^5}{(f_{SW})^2} + \frac{2.824 \times 10^4}{f_{SW}} - 5.355 = 100\ k\Omega \quad (34)$$

In the design, a 95.3 kΩ resistor is selected. The actual switching frequency is 280 kHz.

8.2.1.2.5.2 Output Voltage Setting (FB)

Substitute the top resistor R1 with 10 kΩ in Equation 35, and then calculate the bottom bias resistor.

$$R_{BIAS} = 0.7 \times \frac{R1}{V_{OUT} - 0.7} = 8.66\ k\Omega \quad (35)$$

8.2.1.2.5.3 Current Sensing Network Design (CS+, CS–)

Choosing C1 a value for 0.1 µF, and calculating R with Equation 36.

$$R = \frac{L}{DCR \times C1} = 6\ k\Omega \quad (36)$$

8.2.1.2.5.4 Overcurrent Protection (ILIM)

ILIM pin is connected to VSH and VOUT pins with R1 and R2 respectively. Equation 8 and Equation 9 are used to calculate the overcurrent setting resistors. The DC over current rating is set at 28 A. The calculated values are 41 kΩ and 830 kΩ for R1 and R2 respectively. In the final design, R1 and R2 are chosen as 36.5 kΩ and 787 kΩ for temperature and other tolerances compensation.

8.2.1.2.5.5 V_{REG} (PVCC)

A 4.7-µF capacitor is recommended to filter noise.

8.2.1.2.5.6 BP5

A 4.7-Ω resistor and 1-µF capacitor is placed between V REG and BP5 as a low-pass filter.

8.2.1.2.5.7 Phase Select (PSEL)

If the board is configured as a clock master for a multiphase application, an 8-phase CLKIO signal is generated if PSEL pin is open, and a 6-phase CLKIO signal is generated if PSEL is tied to ground with a 29.4-kΩ resistor. If the board is stacked as a slave for a multiphase application, a different resistor value is selected. The PSEL resistor selection is illustrated in the previous datasheet section.

8.2.1.2.5.8 VSHARE (VSH)

A 1-µF capacitor is tied from VSHARE to GND.

8.2.1.2.5.9 Powergood (PGOOD)

The PGOOD pin is tied to BP5 with a 10-kΩ resistor.

8.2.1.2.5.10 Undervoltage Lockout (UVLO)

UVLO is connected to the input voltage with a resistor divider. The two resistors have the same value of 10 kΩ. When the input voltage is higher than 2 V, the internal linear regulator is enabled.

8.2.1.2.5.11 Clock Synchronization (CLKIO)

CLKIO is floating as no clock synchronization required for single output configuration.

8.2.1.2.5.12 Bootstrap Capacitor

A bootstrap capacitor is connected between the BOOT and SW pin. The bootstrap capacitor depends on the total gate charge of the high-side MOSFET and the amount of droop allowed on the bootstrap capacitor (see Equation 37).

$$C_{BOOT} = \frac{Qg}{\Delta V} = 55\ nF \tag{37}$$

Qg is 11 nC and is 0.2 V in the calculation. For this application, a 0.1-µF capacitor is selected.

8.2.1.2.5.13 Soft Start (SS)

To get about 1-ms soft-start time, a 22-nF capacitor is tied to SS pin (see Equation 38).

$$C_{SS} = \frac{I_{SS} \times T_{SS}}{V_{REF}} = 22\ nF \tag{38}$$

I_{SS} is the soft-start current which is 15-µA typically. V_{REF} is the reference voltage, 0.7 V.

8.2.1.2.5.14 Remote Sense

VOUT and GSNS are connected to the remote sensing output connector. DIFFO is connected to the output voltage setting resistor divider. If the differential amplifier is not used, VOUT and GSNS are suggested to be grounded, and DIFFO is left open.

8.2.1.2.5.15 Feedback Compensator Design

Peak current mode control method is employed in the controller. A small signal model is developed from the COMP signal to the output (see Equation 39).

$$G_{VC(s)} = \frac{1}{DCR \times A_C} \times \frac{1}{s \times t_s + 1} \times \frac{(s \times C_{OUT} \times ESR + 1) \times R_{OUT}}{s \times C_{OUT} \times R_{OUT} + 1} \tag{39}$$

The time constant is defined by Equation 40.

$$T_S = \frac{T}{\ln\left(\frac{\left(\frac{V_{RAMP}}{T}\right) - \left(\frac{V_{OUT}}{L}\right) \times DCR \times A_C}{\left(\frac{V_{RAMP}}{T}\right) - \left(\frac{V_{IN} - V_{OUT}}{L}\right) \times DCR \times A_C - \left(\frac{2 \times V_{OUT}}{L}\right) \times DCR \times A_C}\right)} \tag{40}$$

Equation 40 is applied when the PWM pulse width is shorter than the current loop delay. The current loop delay is typically 100 ns.

$$T_S = \frac{T}{\ln\left(\frac{\left(\frac{V_{RAMP}}{T}\right) + \left(\frac{V_{IN} - V_{OUT}}{L}\right) \times DCR \times A_C}{\left(\frac{V_{RAMP}}{T}\right) - \left(\frac{V_{OUT}}{L}\right) \times DCR \times A_C}\right)} \tag{41}$$

Equation 41 is applied when the PWM pulse width is longer than the current loop delay. The current loop delay is typically 100 ns. Equation 42 is used in this design because the PWM pulse width is much larger than the current loop delay. The low frequency pole is calculated by Equation 42.

$$f_{VCP1} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{OUT}} = 2.36\ kHz \tag{42}$$

The ESR zero is calculated by Equation 43.

$$f_{ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times ESR} = 176.8\ kHz \tag{43}$$

In this design, at Type II compensator (Figure 33) is employed to compensate the loop.

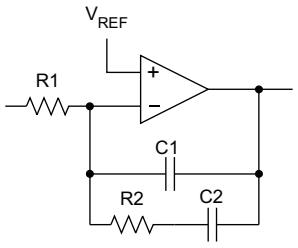


Figure 33. Type II Compensator

The compensator transfer function is Equation 44.

$$Gc(s) = \frac{1}{R1 \times (C1 + C2)} \times \frac{s \times R2 \times C2 \times +1}{s \times \left(s \times R2 \times \left(\frac{(C1 \times C2)}{(C1 + C2)} \right) + 1 \right)} \quad (44)$$

The loop gain function is Equation 45.

$$T_{V(s)} = G_{C(s)} \times G_{VC(s)} \quad (45)$$

Assume the desired crossover frequency is 25 kHz, then set the compensator zero about 1/10 of the crossover frequency and the compensator pole equal to the ESR zero. The compensator gain is then calculated to achieve the desired bandwidth. In this design, the compensator gain, pole and zero are selected using Equation 46 through Equation 49.

$$f_P = \frac{1}{2 \times \pi \times R2 \times \left(\frac{(C1 \times C2)}{(C1 + C2)} \right)} = 176.8 \text{ kHz} \quad (46)$$

$$f_Z = \frac{1}{2 \times \pi \times R2 \times C2} = 2.5 \text{ kHz} \quad (47)$$

$$\left| T_V (j \times 2 \times \pi \times f_C) \right| = 1 \quad (48)$$

From Equation 48, the compensator gain is solved as 4.5×10^5.

$$A_{CM} = \frac{1}{R1 \times (C1 + C2)} = 6.29 \times 10^4 \quad (49)$$

Set R1 equal to 10 kΩ, and then calculate all the other components.

- R2 = 40 kΩ
- C1 = 22 pF
- C2 = 1.6 nF

In the real laboratory practice, the final components are selected as following to increase the phase margin and reduce PWM jitter.

- R1 = 10 kΩ
- R2 = 39 kΩ
- C1 = 22 pF
- C2 = 2.7 nF

8.2.1.3 Application Curves

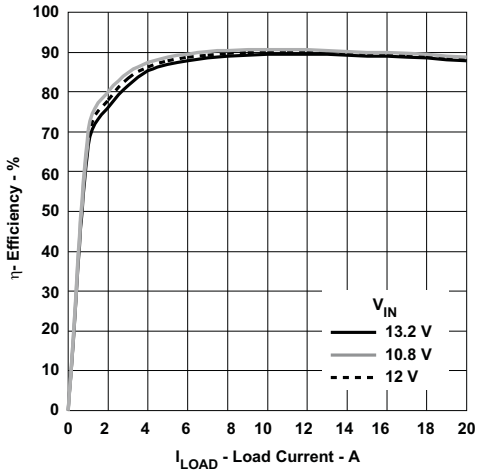


Figure 34. Efficiency Curve

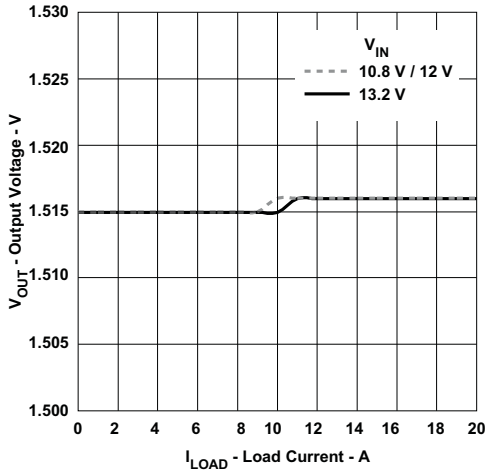


Figure 35. Output Load Regulation

8.2.2 Simultaneous Tracking With TPS40180 Devices

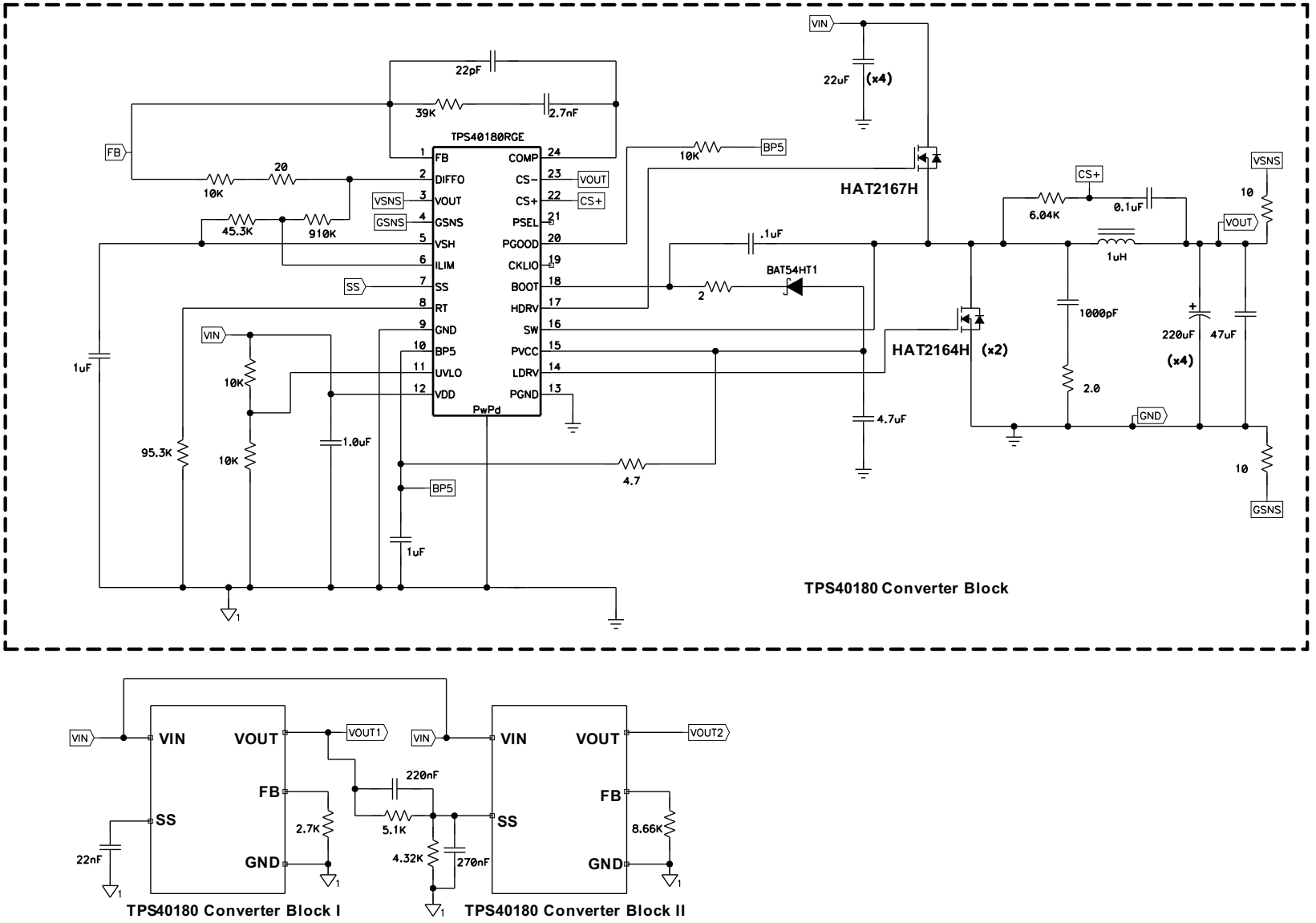


Figure 36. Simultaneous Tracking With TPS40180

8.2.2.1 Design Requirements

The TPS40180 can function in a tracking mode, where the output tracks some other voltage. In the simultaneous tracking design, the output voltages of two TPS40180 blocks needs to rise up and fall down with the same slew rate.

8.2.2.2 Detailed Design Procedure

In Figure 36, the SS pin of Block II is connected to the output voltage of Block I via voltage divider. A value between 1 kΩ and 10 kΩ is suggested for the bottom. Here a 4.32-kΩ resistor is selected for bottom resistor. From Equation 12, the top resistor is calculated as 5.1 kΩ.

From Equation 13, a 220-nF capacitor is selected in parallel with the top resistor, and a 270-nF capacitor is selected in parallel with bottom resistor.

8.2.2.3 Application Curves

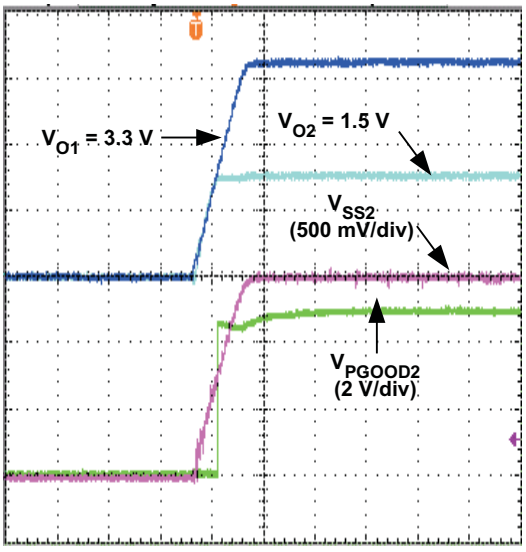


Figure 37. Simultaneously Tracking Up

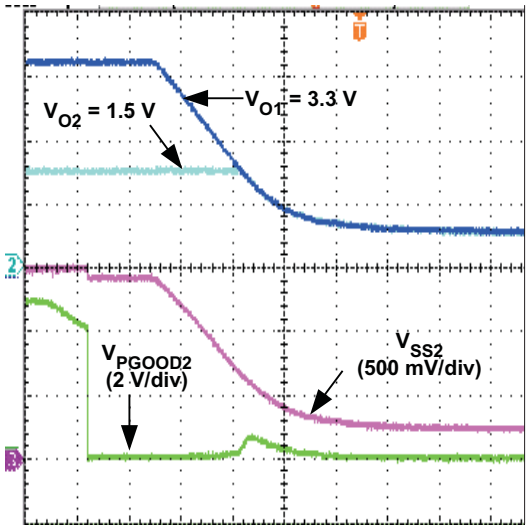


Figure 38. Simultaneously Tracking Down

8.2.3 2-Phase Single Output With TPS40180

In Figure 39, Block I and Block II are configured as master and slave respectively.

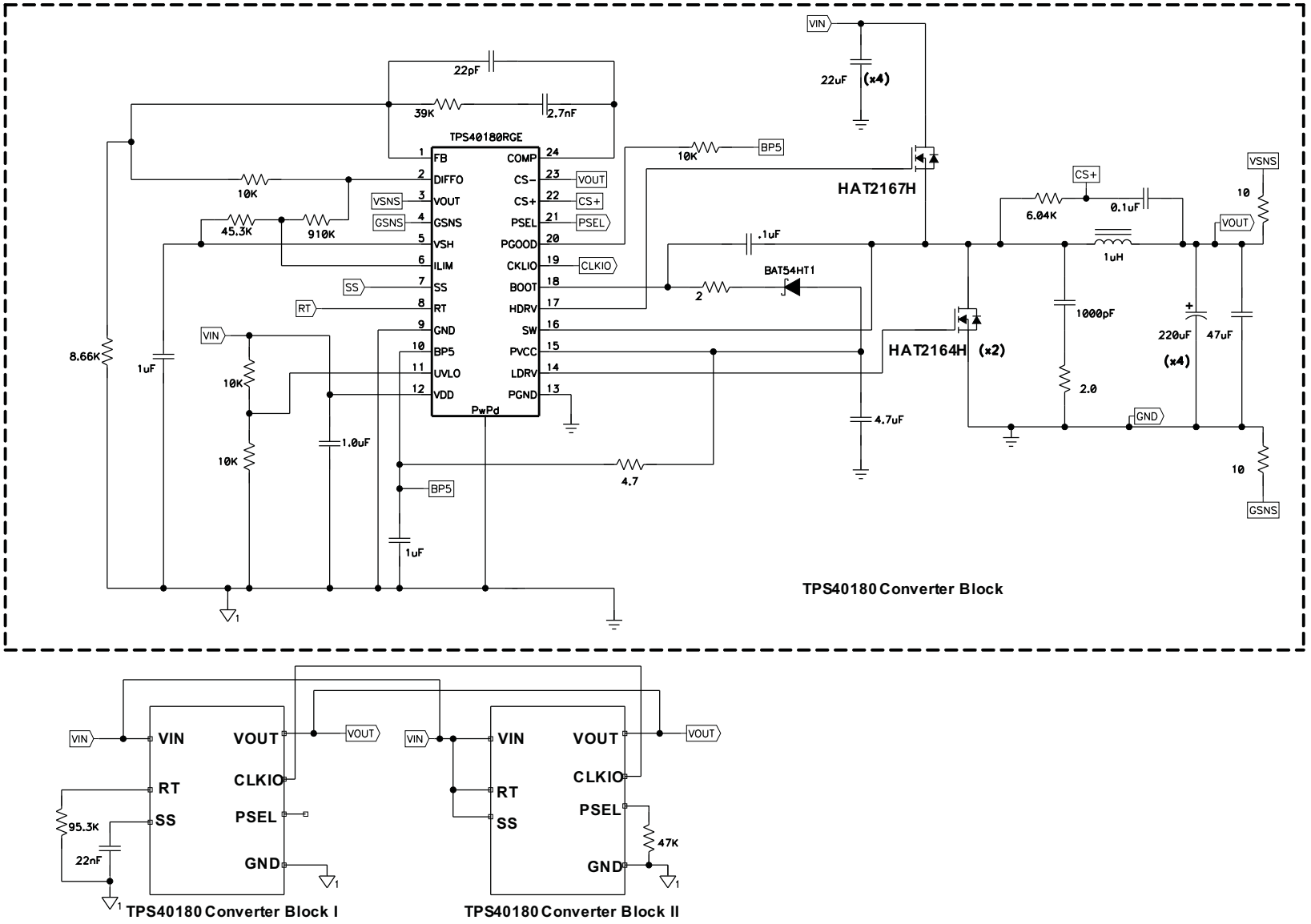


Figure 39. 2-Phase Single Output Schematic with TPS40180
V_{IN} = 12 V, V_{OUT} = 1.5 V, I_{OUT} = 40 A

8.2.3.1 Design Requirements

Table 7 lists the design parameters for this example application.

Table 7. Design Goal Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		10.8	12	13.2	V
V_{OUT}	Output voltage			1.5		V
V_{RIPPLE}	Output ripple	I_{OUT} = 40 A		30		mV
I_{OUT}	Output current			40		A
f_{SW}	Switching frequency			280		kHz

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 Inductor Selection

The inductor is determined by the desired inductor ripple current. Use Equation 19 to calculate the inductor value. In this design, I_{RIPPLE} is targeted at 25% of phase current. The calculated inductor is 0.95 µH and in practical a 1-µH inductor with 1.7-mΩ DCR is selected. The real inductor ripple current is 4.7 A.

8.2.3.2.2 Output Capacitor Selection

The output capacitor is typically selected by the output load transient response requirement. Equation 21 in the single-phase design example is used. The inductor L in the equation is equal to the phase inductance divided by number of phases.

Based on a 40-A load transient with a maximum of 30 mV deviation, a minimum 711-µF output capacitor is required. Considering the capacitance variation and derating, eight 220-µF SP capacitors are selected in the design with sufficient margin. Each capacitor has an ESR of 5 mΩ.

Another criterion for capacitor selection is the output ripple voltage that is determined mainly by the capacitance and the ESR.

Due to the interleaving of channels, the total output ripple current is smaller than the ripple current from a single phase. The ripple cancellation factor is expressed in Equation 50. In this design, the ripple cancellation factor is 0.857.

$$I_{RIP\_NORN} = \frac{N_{PH} \times (D - \frac{m}{N_{PH}}) \times (\frac{m+1}{N_{PH}} - D)}{D \times (1 - D)}$$

where

- D is the duty cycle for a single phase
- N_{PH} is the number of active phases, here it is equal to 2
- m = floor (N_{PH} × D) is the maximum integer that does not exceed the (N_{PH} × D), here m is 0 (50)

The output ripple current is then calculated in Equation 51. The maximum output ripple is with maximum input voltage. In this design, the maximum output ripple is calculated as 4.03 A.

$$I_{RIPPLE} = \frac{V_{OUT} \times (1 - D)}{L \times f_{SW}} \times I_{RIP\_NORM} \quad (51)$$

With 1.76-mF output capacitance, the ripple voltage from the capacitance is 1 mV. In the specification, the output ripple voltage should be less than 30 mV, so based on Equation 22, the required maximum ESR is 7.2 mΩ. The selected capacitors must meet this requirement.

8.2.3.2.3 Input Capacitor Selection

The input voltage ripple depends on the input capacitance and ESR. The minimum capacitor and the maximum ESR can be estimated by Equation 23 and Equation 24 in the single phase design example. The phase current should be used in the calculation.

8.2.3.2.4 Peripheral Component Design

8.2.3.2.4.1 PSEL Pin

Use Table 3 and Table 4 to configure PSEL pin. In this design, the PSEL pin of master controller is open to set 8 phase CLKIO. The CLKIO pin sends out a pulse train for interleaving with 45° phase separation. The PSEL pin of slave controller is connected to GND through 47-kΩ resistor to set 180° phase angle.

8.2.3.2.4.2 CLKIO Pin

The CLKIO pins of master and slave controllers must be connected together. A 10-kΩ resistor is connected from the CLKIO line to GND to ensure that the CLKIO line falls to GND quickly when the master controller is shutdown or powers off.

8.2.3.2.4.3 RT Pin

In this design, the RT pin of master controller is connected to GND through 95.3-kΩ resistor to set switching frequency at 280 kHz per phase. The RT pin of slave controller is connected to VDD.

8.2.3.2.4.4 SS Pin

The SS pin of master controller is connected to GND through 22-nF capacitor to get about 1-ms soft-start time. The SS pin of slave parts to VDD pin is connected to VDD pin.

8.2.3.2.4.5 DIFFO Pin and FB Pin

The DIFFO pin and FB pin of master controller are connected to feedback and compensation network. The DIFFO pin and FB pin of slave controller are open.

8.2.3.2.4.6 COMP Pin

The COMP pins of master and slave controller must be connected together.

8.2.3.2.4.7 VSH Pin

An individual VSH bypass capacitor is required by master and slave controller. The VSH pins of master and slave controllers must be connected together.

8.2.3.2.4.8 Other Pins

Follow the design procedure of single-phase design for other peripheral components design.

8.2.3.3 Application Curves

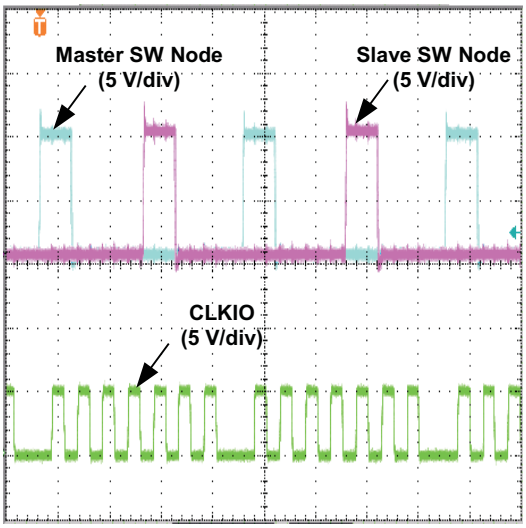


Figure 40. Switch Node and CLKIO Waveforms

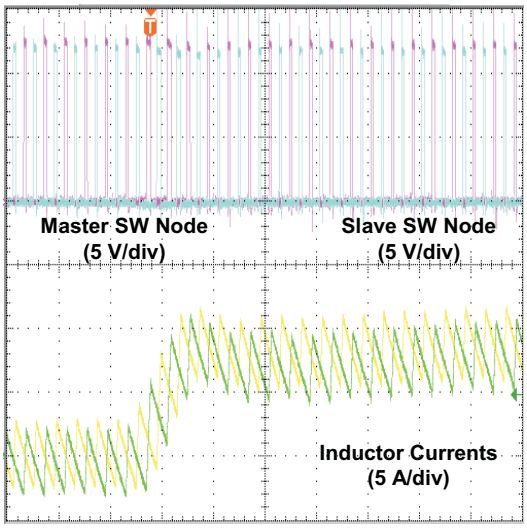


Figure 41. Current Balance at 0-A to 16-A Load Step-Up, 2.5-A/µs Slew Rate

9 Power Supply Recommendations

The TPS40180 VDD is designed from voltage supply range from 5 V to 15 V. Good regulation of this input supply is essential. The power stage input voltage range is from 2 V to 40 V. If the input supply is more distant than a few inches from the power stage, the circuit may requires bulk capacitance in addition to ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

10.1.1 Power Stage

A synchronous BUCK power stage has two primary current loops. One is the input current loop which carries high AC discontinuous current adn the other is the output current loop carrying a high DC continuous current.

The input current loop includes the input capacitors, the main switching MOSFET, the inductor, the output capacitors and the ground path back to the input capacitors. To keep this loop as small as possible, it is generally good practice to place some ceramic capacitance directly between the drain of the main switching MOSFET and the source of the synchronous rectifier (SR) through a power ground plane directly under the MOSFETs.

The output current loop includes the SR MOSFET, the inductor, the output capacitors, and the ground return between the output capacitors and the source of the SR MOSFET. As with the input current loop, the ground return between the output capacitor ground and the source of the SR MOSFET should be routed under the inductor and SR MOSFET to minimize the power loop area.

The SW node area should be as small as possible to reduce the parasitic capacitance and minimize the radiated emissions.

The gate drive loop impedance (HDRV-gate-source-SW and LDRV-gate-source-GND) should be kept to as low as possible. The HDRV and LDRV connections should widen to 20 mils as soon as possible out from the IC pin.

10.1.2 Device Peripheral

The TPS40180 provides separate signal ground (GND) and power ground (PGND) pins. It is required to separate properly the circuit grounds. The return path for the pins associated with the power stage should be through PGND. The other pins especially for those sensitive pins such as FB, RT and ILIM should be through the low noise GND. The GND and PGND plane are suggested to be connected at the output capacitor with single 20 mil trace.

A minimum 0.1-µF ceramic capacitor must be placed as close to the VDD pin and AGND as possible with at least 15-mil wide trace from the bypass capacitor to the GND.

A 4.7-µF ceramic capacitor should be placed as close to the PVCC pin and PGND as possible.

BP5 is the filtered input from the PVCC pin. A 4.7-Ω resistor should be connected between PVCC and BP5 and a 1-µF ceramic capacitor should be connected from BP5 to GND. Both components should be as close to BP5 pin as possible.

When a DCR sensing method is applied, the sensing resistor is placed close to the SW node. It is connected to the inductor with Kelvin connection. The sensing traces from the power stage to the chip should be away from the switching components. The sensing capacitor should be placed very close to the CS+ and CS– pins. The frequency setting resistor should be placed as close to RT pin and GND as possible. The VOUT and GSNS pins should be directly connected to the point of load where the voltage regulation is required.

A parallel pair of 10-mil traces connects the regulated voltage back to the chip. They should be away from the switching components. The PowerPAD should be electrically connected to GND.

Layout Guidelines (continued)

10.1.3 PowerPad Layout™

The PowerPAD™ package provides low thermal impedance for heat removal from the device. The PowerPAD™ derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depend on the size of the PowerPAD™ package. Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter plus 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to PowerPAD™ Thermally Enhanced Package for more information on the PowerPAD™ package.

10.2 Layout Example

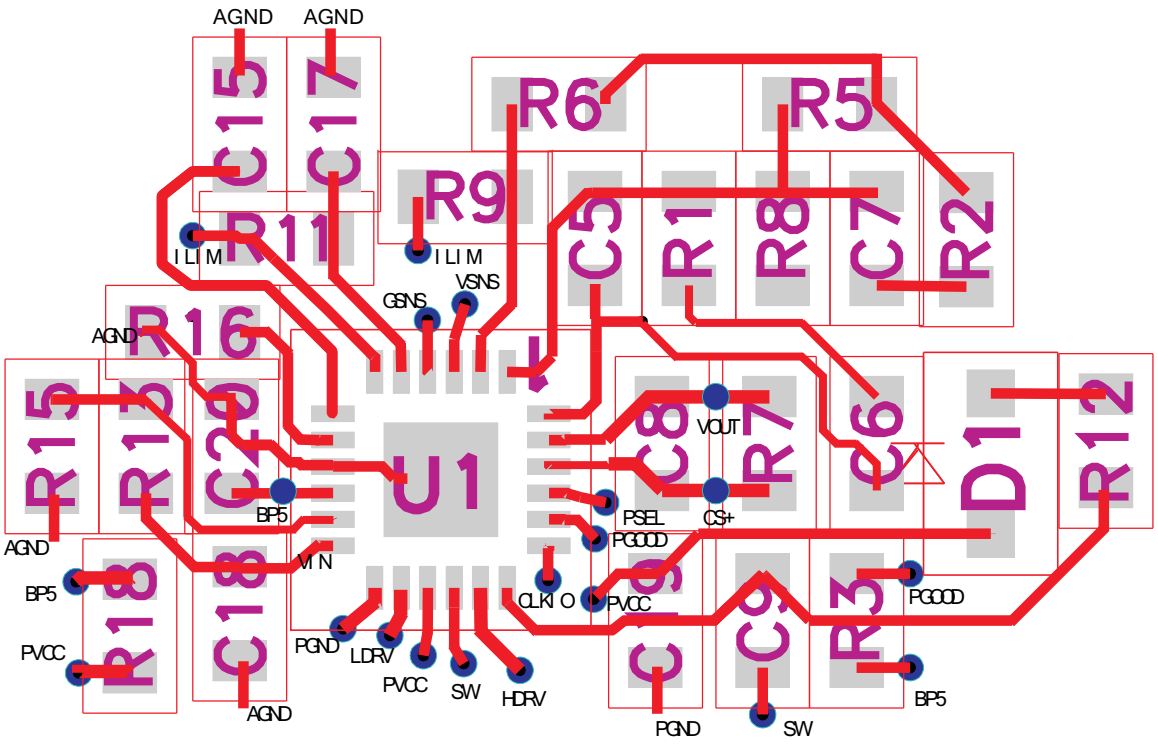


Figure 42. TPS40180 Recommended Layout for Peripheral Components

Layout Example (continued)

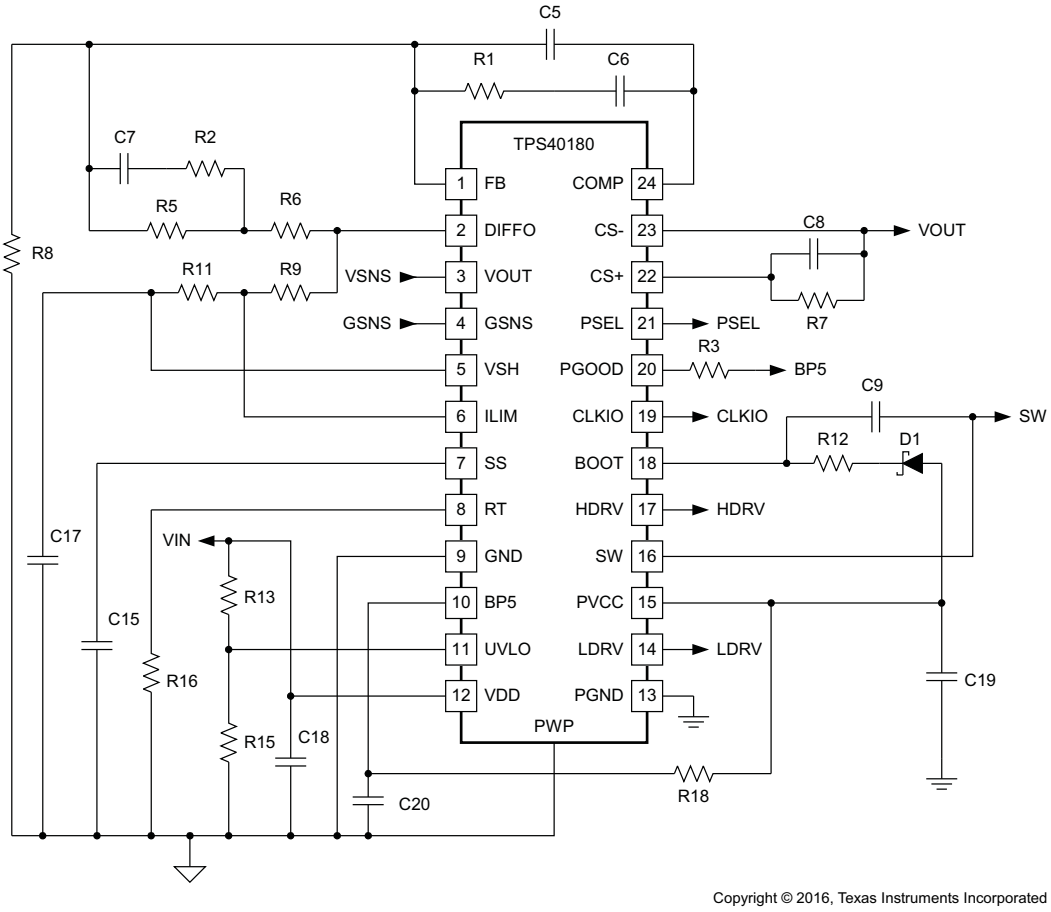


Figure 43. TPS40180 Peripheral Schematic

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Device Nomenclature

$V_{IN(min)}$	Minimum operating input voltage
$V_{IN(max)}$	Maximum operating input voltage
V_{OUT}	Output voltage
I_{RIPPLE}	Inductor peak-peak ripple current
$I_{TRAN(max)}$	Maximum load transient
V_{UNDER}	Output voltage undershot
V_{OVER}	Output voltage overshot
$V_{RIPPLE(totOUT)}$	Total output ripple
$V_{RIPPLE(COUT)}$	Output voltage ripple due to output capacitance
$V_{RIPPLE(CIN)}$	Input voltage ripple due to input capacitance
$V_{RIPPLE(CinESR)}$	Input voltage ripple due to the ESR of input capacitance
$P_{SW(cond)}$	High side MOSFET switching loss
I_{SWrms}	RMS current in the high side MOSFET
$R_{DS(on)(SW)}$	*ON* drain-source resistance of the high side MOSFET
$P_{SW(sw)}$	High side MOSFET switching loss
I_{PK}	Peak current through the high side MOSFET
R_{DRV}	Driver resistance of the high side MOSFET
Qgd_{SW}	Gate to drain charge of the high side MOSFET
Qgs_{SW}	Gate to source charge of the high side MOSFET
V_{GSW}	Gate drive voltage of the high side MOSFET
$P_{SW(gate)}$	Gate drive loss of the high side MOSFET
Qg_{SW}	Gate charge of the high side MOSFET
$P_{SW(tot)}$	Total losses of the high side MOSFET
$P_{SR(cond)}$	Low side MOSFET conduction loss
I_{SRrms}	RMS current in the low side MOSFET
$R_{DS(on)(SR)}$	*ON* drain-source resistance of the low side MOSFET
$P_{SR(gate)}$	Gate drive loss of the low side MOSFET
Qg_{SR}	Gate charge of the low side MOSFET
Vg_{SR}	Gate drive voltage of the low side MOSFET
P_{DIODE}	Power loss in the diode
t_D	Dead time between the condiction of high and low side MOSFET

Device Support (continued)

Vf	Forward voltage drop of the body diode of the low side MOSFET
$P_{SR(tot)}$	Total losses of the low side MOSFET
DCR	Inductor DC resistance
A_C	Gain of the current sensing amplifier, typically it is 13
R_{OUT}	Output load resistance
V_{RAMP}	Ramp amplitude, typically it is 0.5 V
T	Switching period
$G_{VC(s)}$	Control to output transfer function
$G_{C(s)}$	Compensator transfer function
$T_{V(s)}$	Loop gain transfer function
A_{CM}	Gain of the compensator
f_P	The pole frequency of the compensator
f_Z	The zero frequency of the compensator

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40180RGER	NRND	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 40180	
TPS40180RGET	NRND	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 40180	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

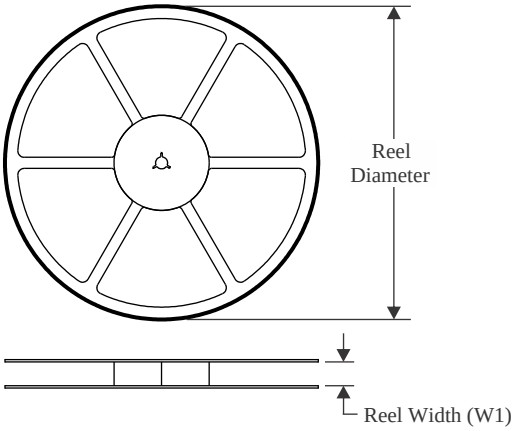
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

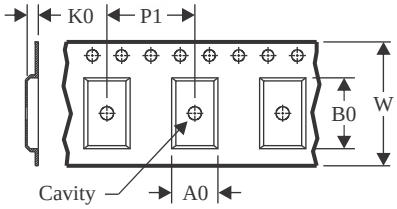
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

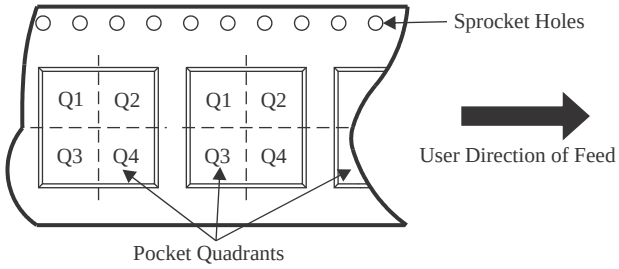


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

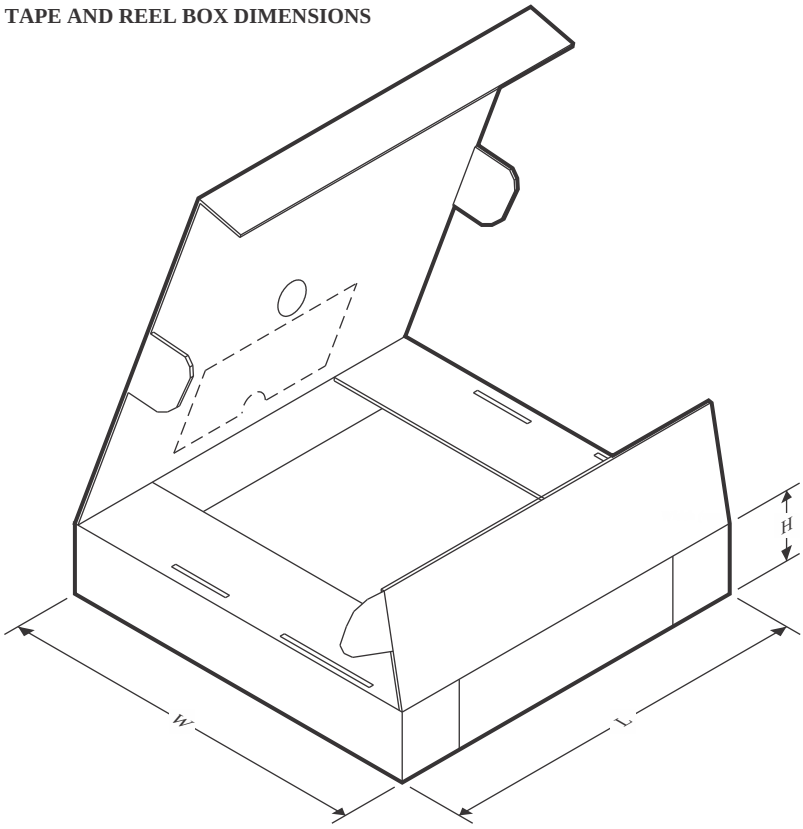
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40180RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS40180RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



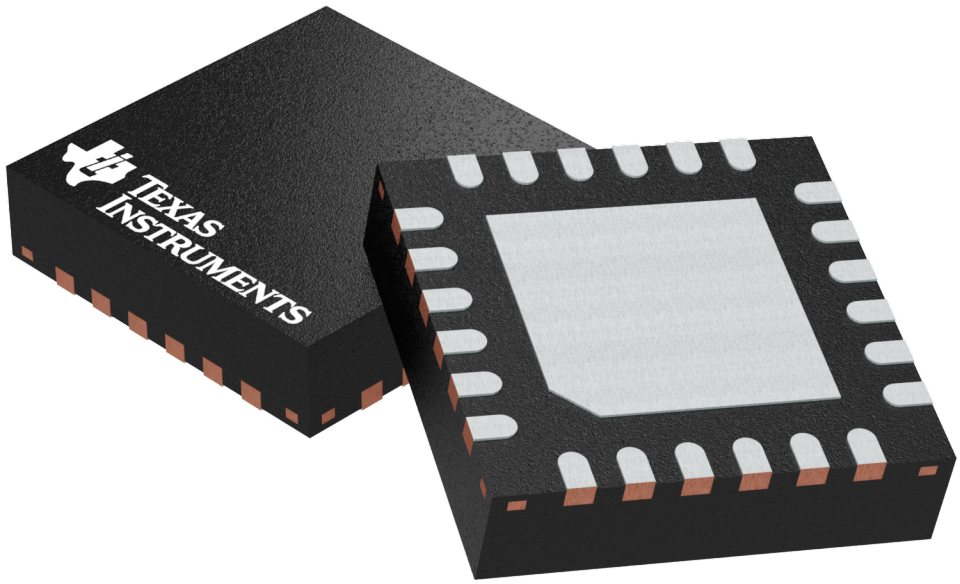
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40180RGER	VQFN	RGE	24	3000	356.0	356.0	35.0
TPS40180RGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

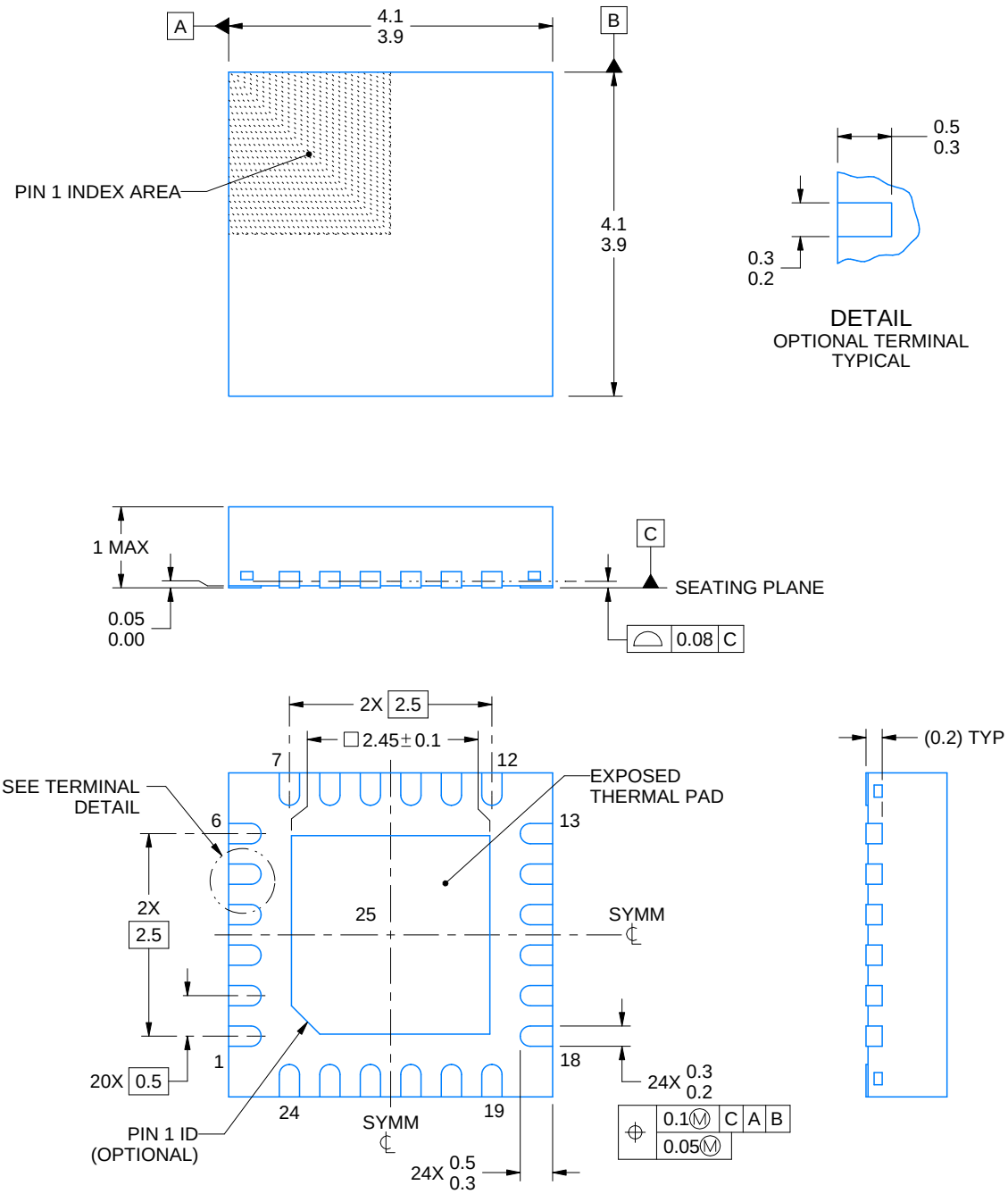
4204104/H

PACKAGE OUTLINE

RGE0024B

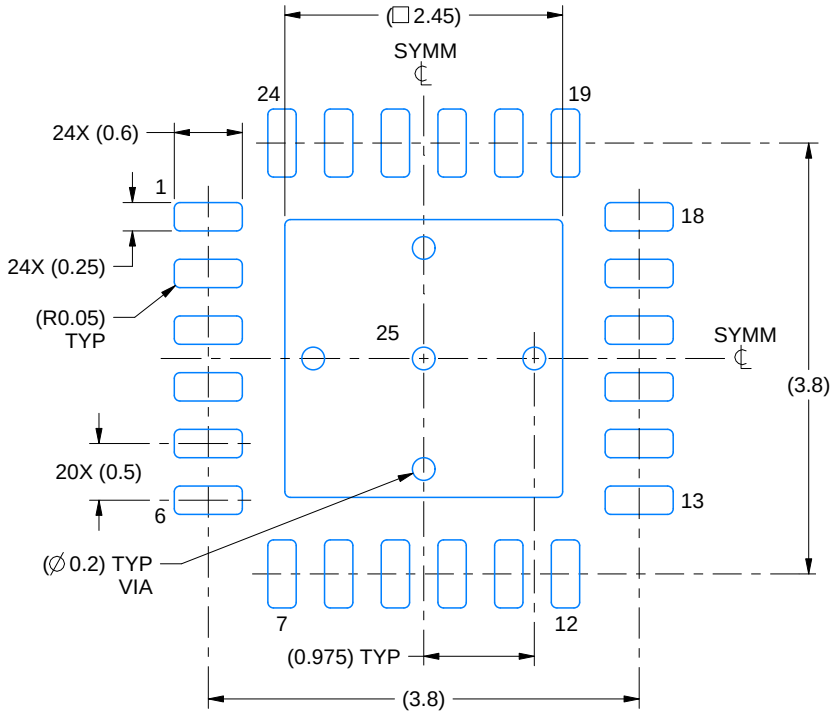
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

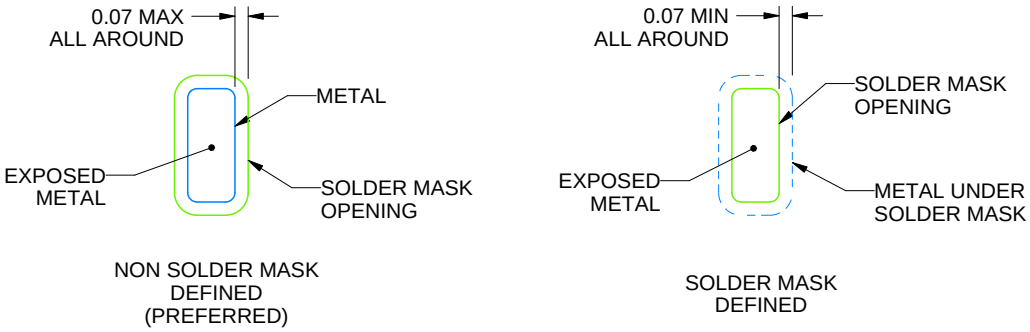


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

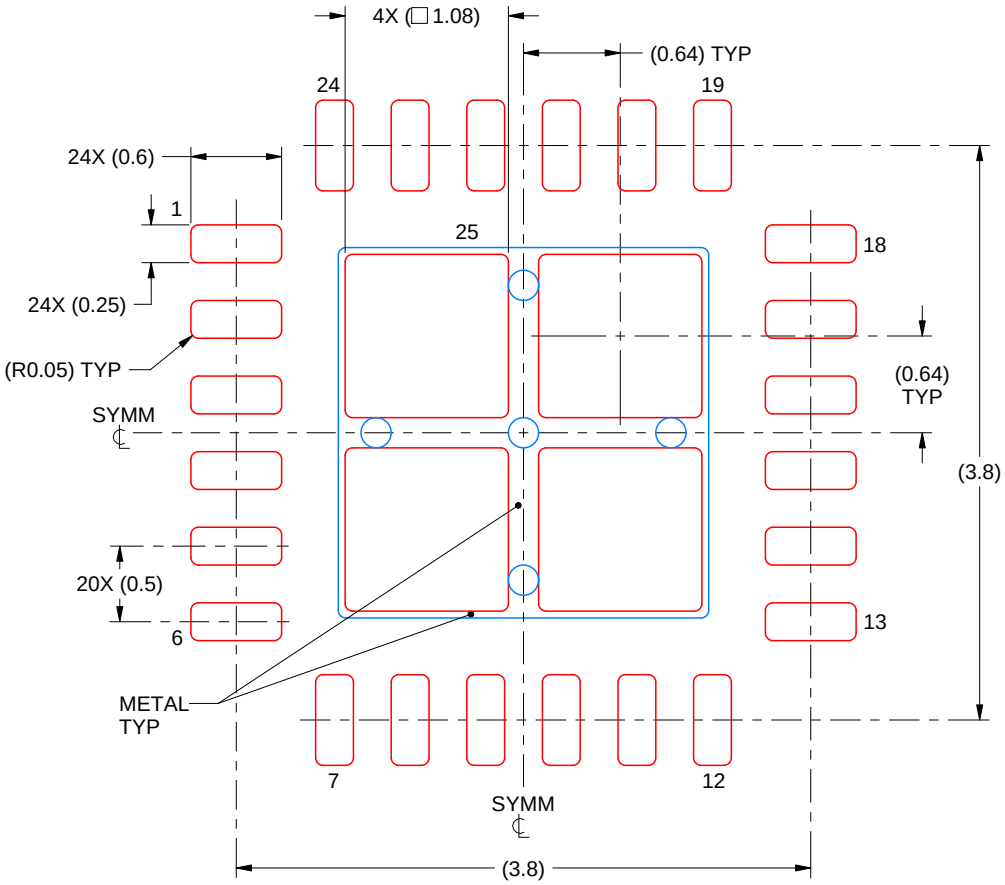


SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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