CSD17552Q3A 30 V N-Channel NexFET™ Power MOSFETs

1 Features

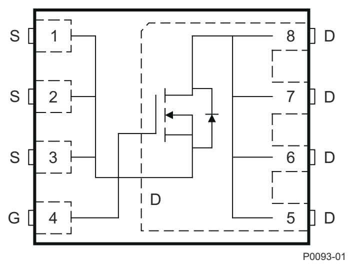
- Ultra-Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free
- RoHS Compliant
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

2 Applications

- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems
- Optimized for Control FET Applications

3 Description

This 30 V, 5.5 mΩ, 3.3 mm × 3.3 mm SON NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Top View

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5 V)	9.0		nC
Q_{gd}	Gate Charge Gate-to-Drain	2.3		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 4.5 V	6.5	mΩ
		V_{GS} = 10 V	5.5	mΩ
$V_{GS(th)}$	Threshold Voltage	1.5		V

Ordering Information(1)

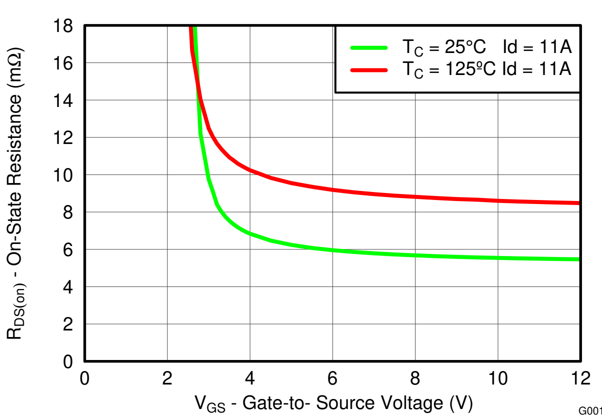
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD17552Q3A	2500	13-Inch Reel	SON 3.3 mm × 3.3 mm Plastic Package	Tape and Reel
CSD17552Q3AT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

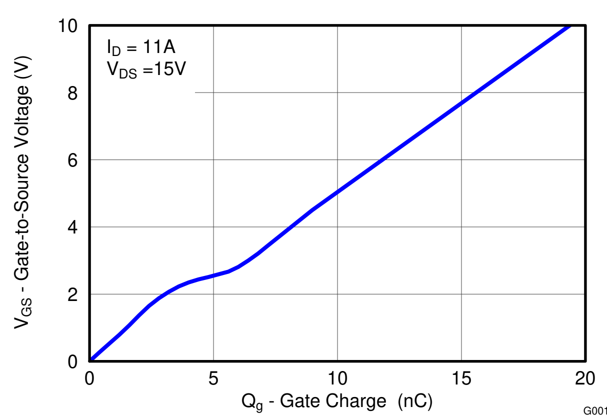
Absolute Maximum Ratings

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current, T_C = 25°C	60	A
	Continuous Drain Current, Silicon Limited	74	A
	Continuous Drain Current, T_A = 25°C(1)	15	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	84	A
P_D	Power Dissipation(1)	2.6	W
T_J, T_{stg}	Operating Junction Temperature, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 30 A, L = 0.1 mH, R_G = 25 Ω	45	mJ

(1) Typical $R_{\theta JA}$ = 48°C/W on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.
(2) Pulse duration ≤300 μs, duty cycle ≤2%



$R_{DS(on)}$ vs V_{GS}



Gate Charge

Table of Contents

4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

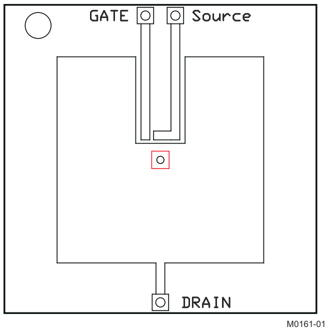
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 24 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.1	1.5	1.9	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = 4.5 V, I_D = 11 A		6.5	8.1	mΩ
		V_{GS} = 10 V, I_D = 11 A		5.5	6.0	mΩ
g_{fs}	Transconductance	V_{DS} = 15 V, I_D = 11 A		106		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz		1580	2050	pF
C_{oss}	Output capacitance			385	500	pF
C_{rss}	Reverse transfer capacitance			28	36	pF
R_G	Series gate resistance			.9	1.8	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15 V, I_D = 11 A		9	12	nC
Q_{gd}	Gate charge gate to drain			2.3		nC
Q_{gs}	Gate charge gate to source			3.6		nC
$Q_{g(th)}$	Gate charge at V_{th}			1.8		nC
Q_{oss}	Output charge	V_{DS} = 15 V, V_{GS} = 0 V		11		nC
$t_{d(on)}$	Turn on delay time	V_{DS} = 15 V, V_{GS} = 4.5 V, I_{DS} = 11 A, R_G = 2 Ω		7.2		ns
t_r	Rise time			7.4		ns
$t_{d(off)}$	Turn off delay time			11.0		ns
t_f	Fall time			3.4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 11 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DS}= 13.5 V, I_F = 11 A, di/dt = 300 A/μs		17		nC
t_{rr}	Reverse recovery time			15		ns

4.2 Thermal Information

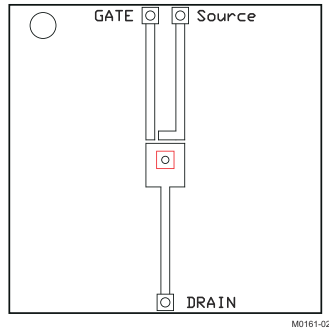
(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{θJC}$	Junction-to-case thermal resistance(1)			2.3	°C/W
$R_{θJA}$	Junction-to-ambient thermal resistance(1) (2)			60	°C/W

(1) $R_{θJC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches × 1.5 inches (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{θJC}$ is specified by design, whereas $R_{θJA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 60°C/W when mounted on 1 inch^2 (6.45 cm^2) of 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA}$ = 146°C/W when mounted on a minimum pad area of 2 oz. (0.071 mm thick) Cu.

4.3 Typical MOSFET Characteristics

(T_A = 25°C unless otherwise stated)

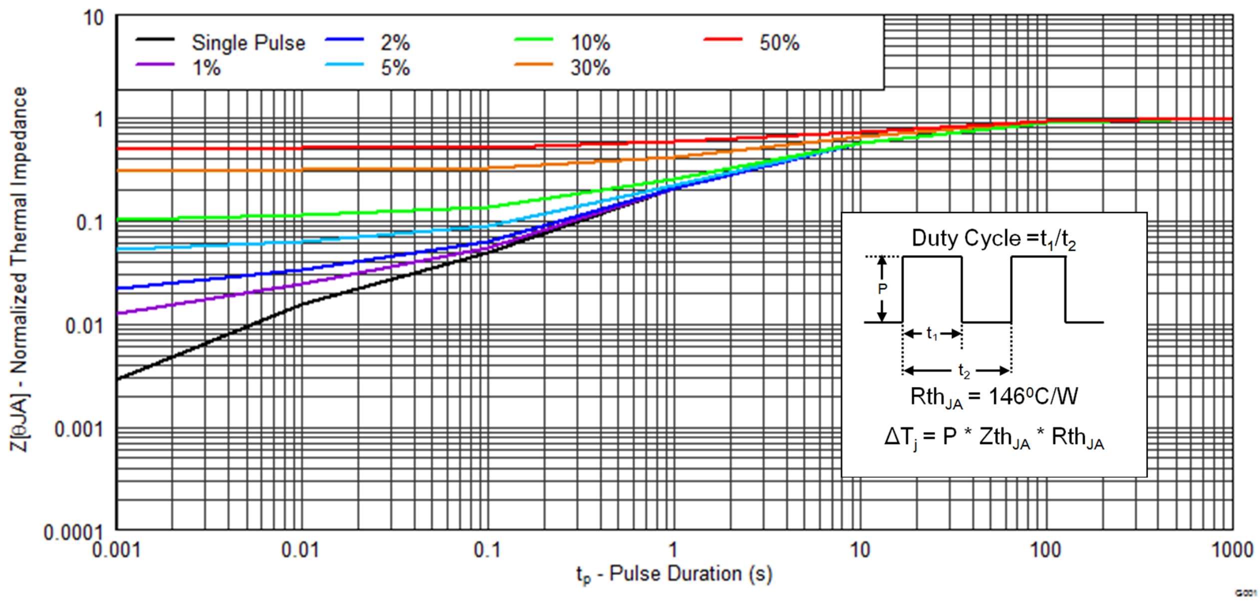


Figure 4-1. Transient Thermal Impedance

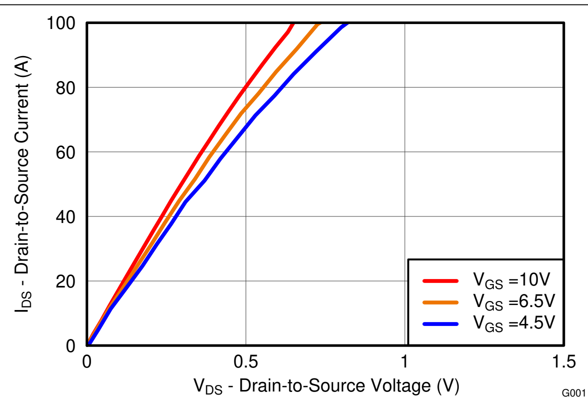


Figure 4-2. Saturation Characteristics

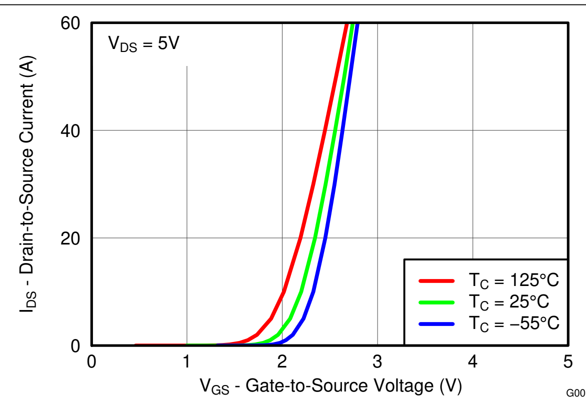


Figure 4-3. Transfer Characteristics

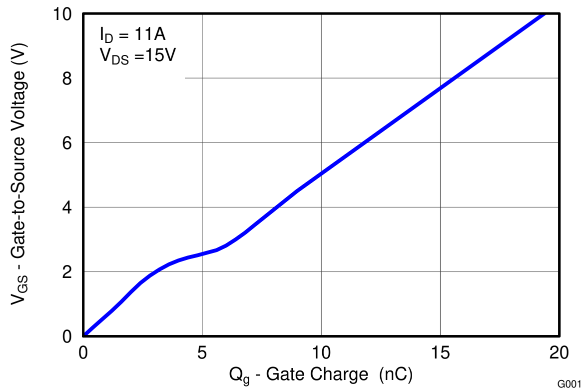


Figure 4-4. Gate Charge

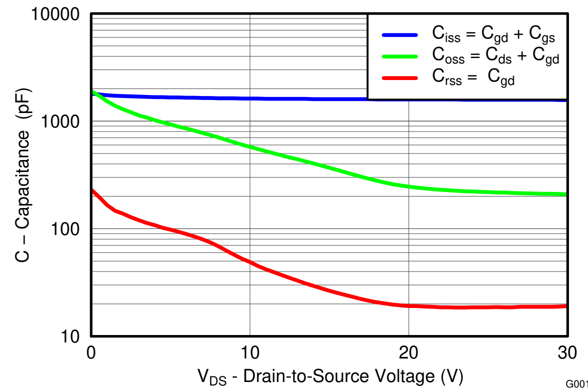


Figure 4-5. Capacitance

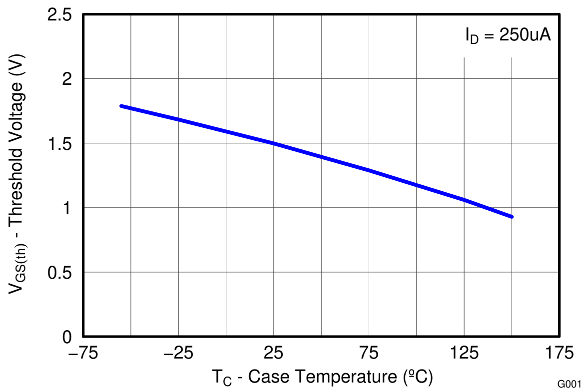


Figure 4-6. Threshold Voltage vs Temperature

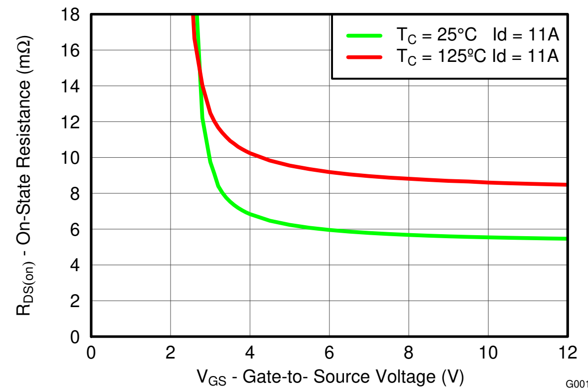


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

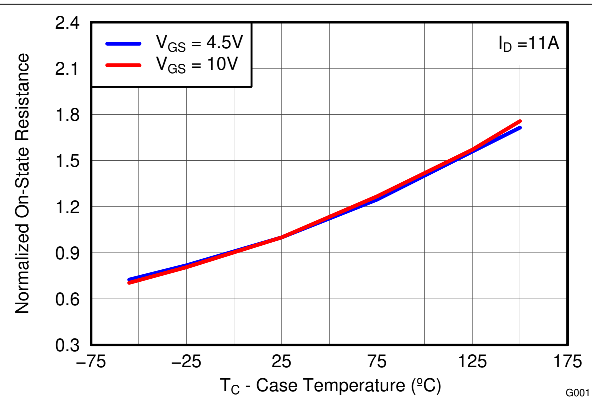


Figure 4-8. Normalized On-State Resistance vs Temperature

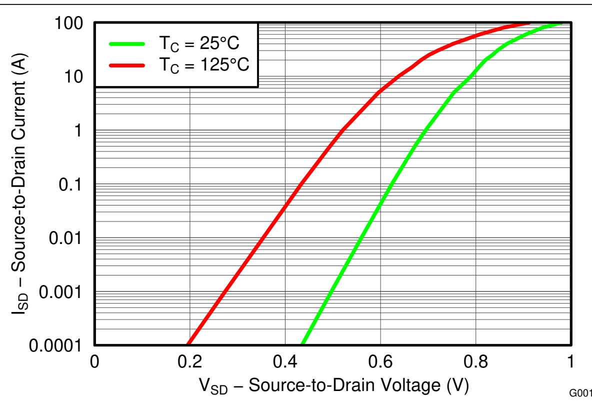


Figure 4-9. Typical Diode Forward Voltage

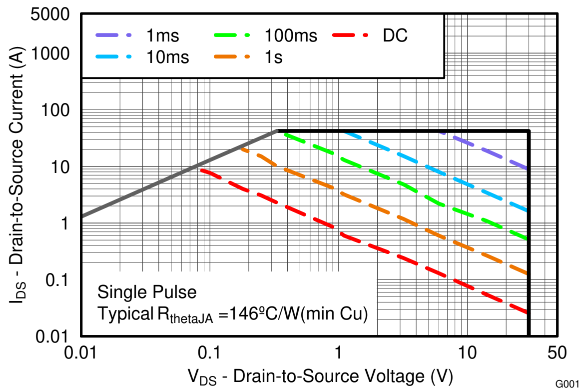


Figure 4-10. Maximum Safe Operating Area

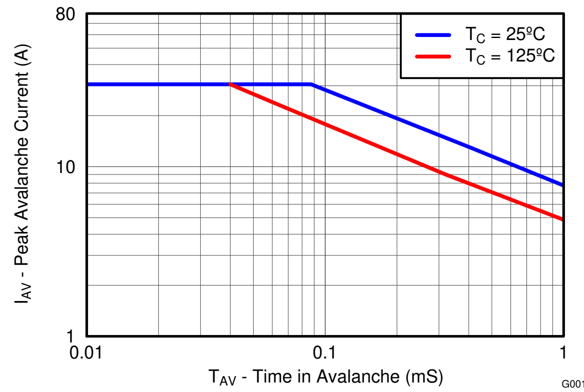


Figure 4-11. Single Pulse Unclamped Inductive Switching

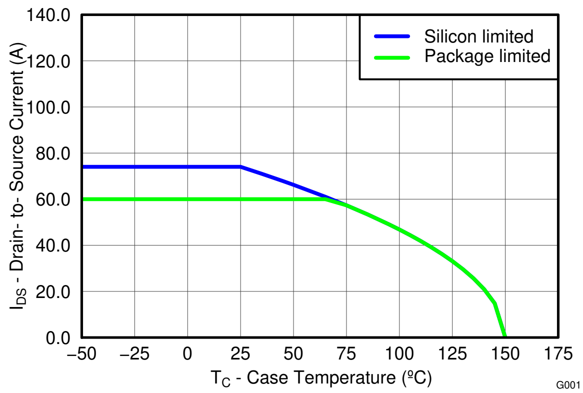


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

5.2 Trademarks

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5.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.4 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (January 2016) to Revision C (November 2023)	Page
• Updated formatting for tables, figures, and cross-references throughout the document	1

Changes from Revision A (June 2014) to Revision B (January 2016)	Page
• Enhanced *Section 3* text	1

Changes from Revision * (September 2012) to Revision A (June 2014)	Page
• Changed "Pb-Free terminal plating" feature to state "Pb Free"	1

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17552Q3A	ACTIVE	VSONP	DNH	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	17552	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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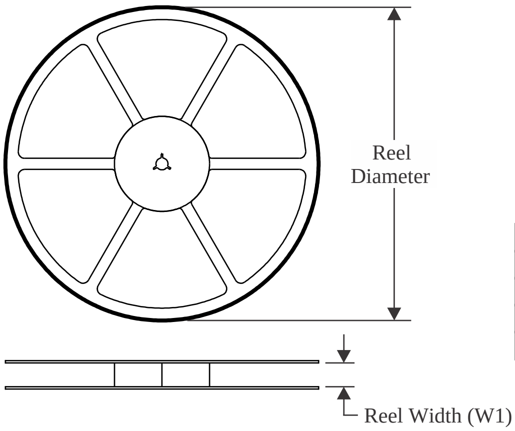
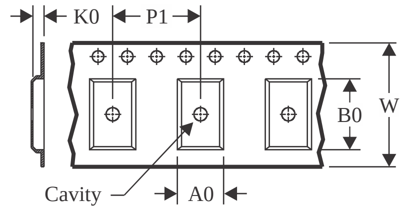
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

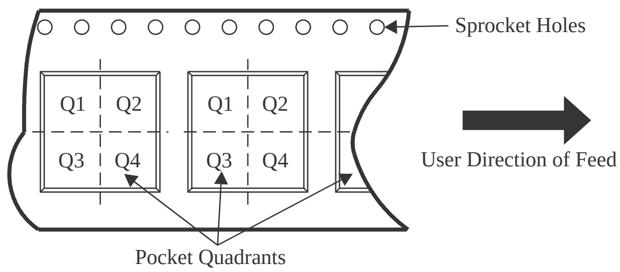


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

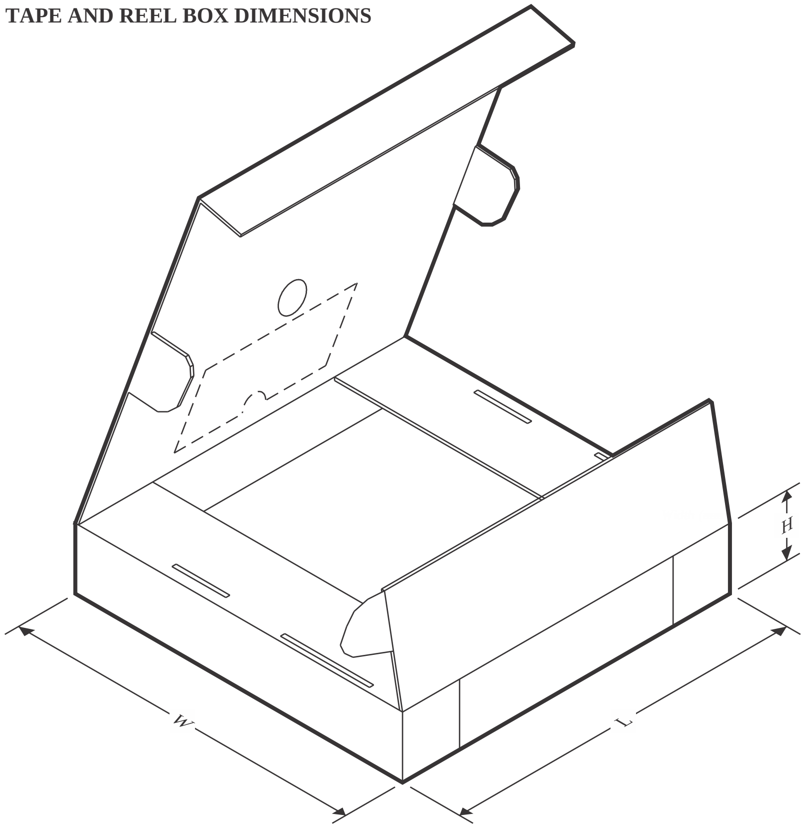
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

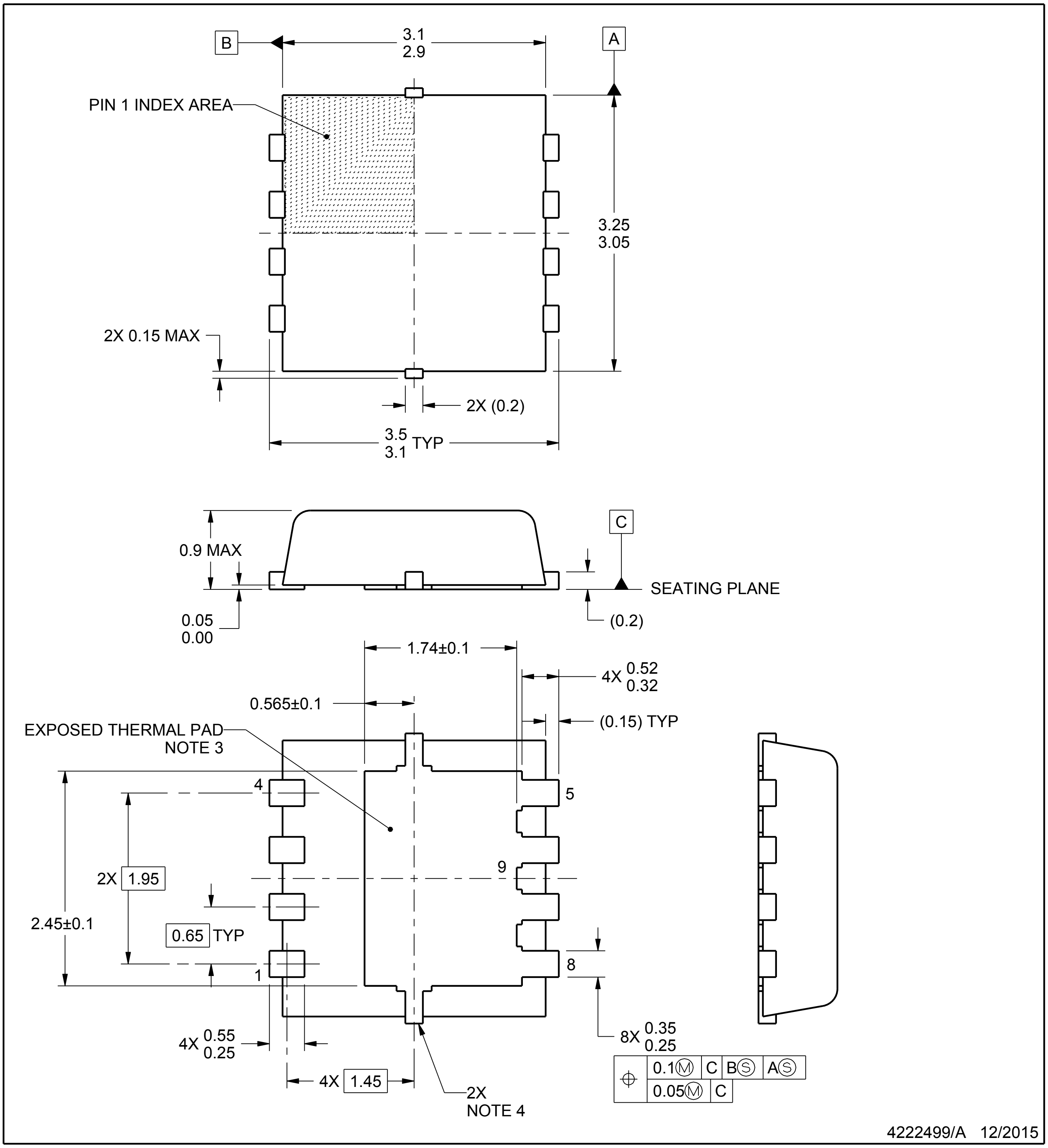
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17552Q3A	VSONP	DNH	8	2500	330.0	12.4	3.6	3.6	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



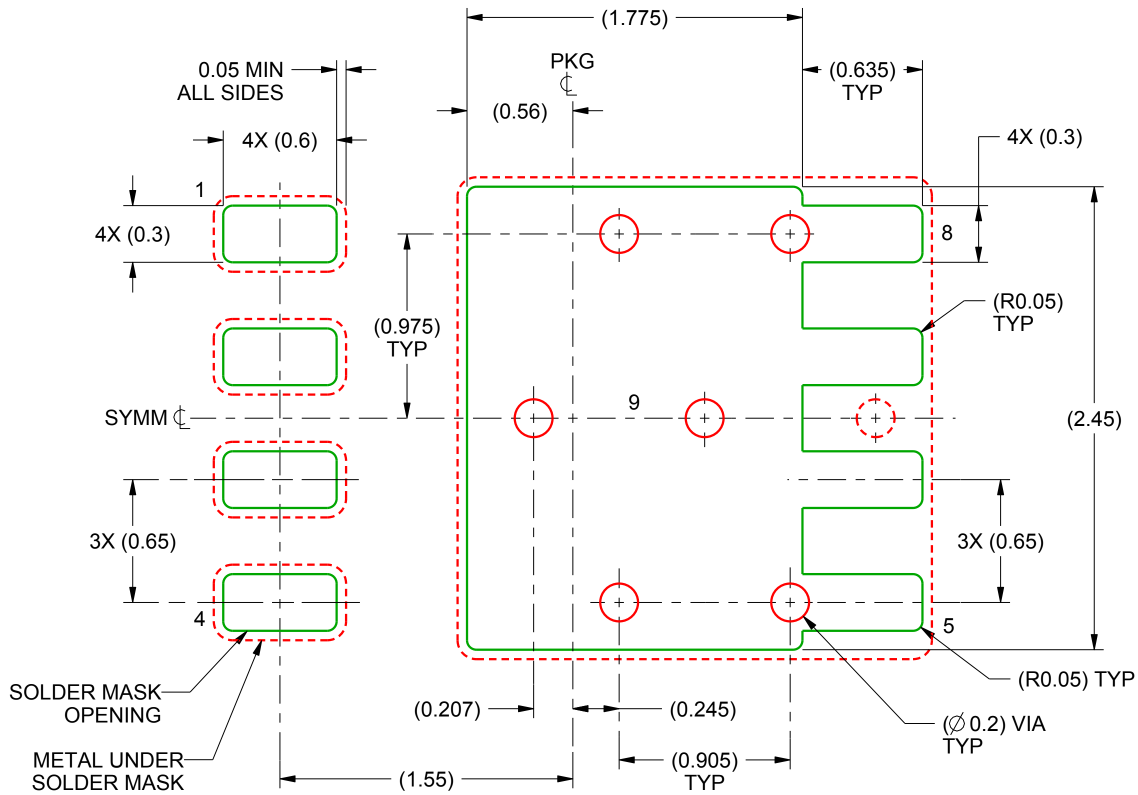
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17552Q3A	VSONP	DNH	8	2500	340.0	340.0	38.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. All dimensions do not include mold flash or protrusions.

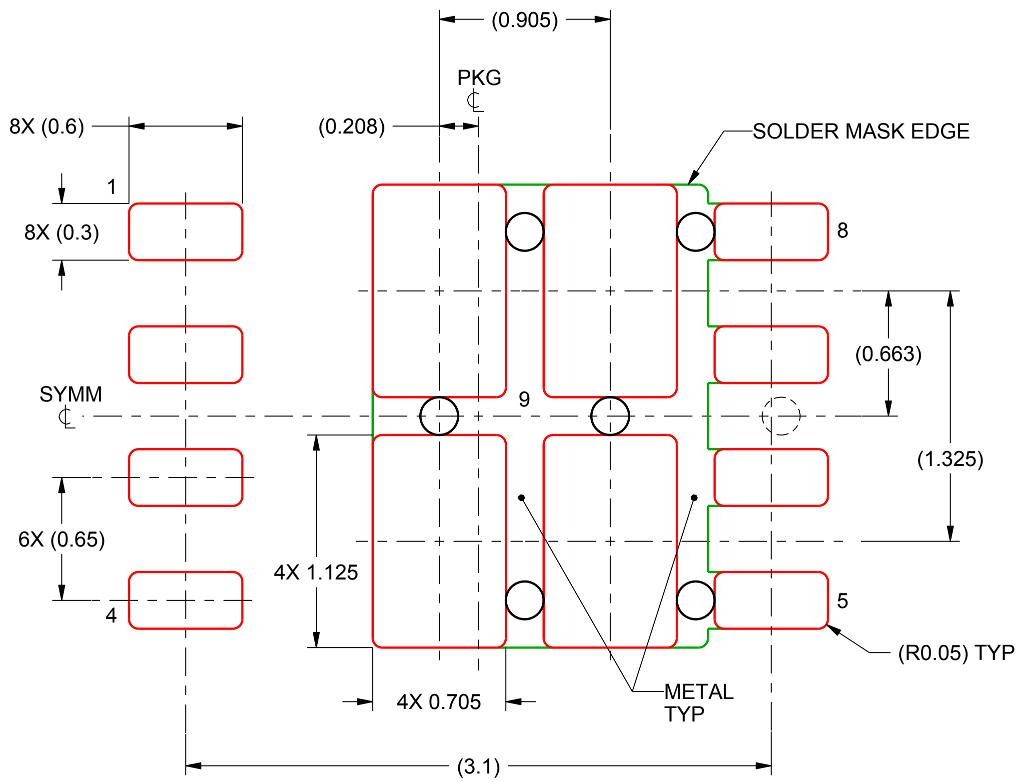


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE: 25X

4222499/A 12/2015

NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 25X

4222499/A 12/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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