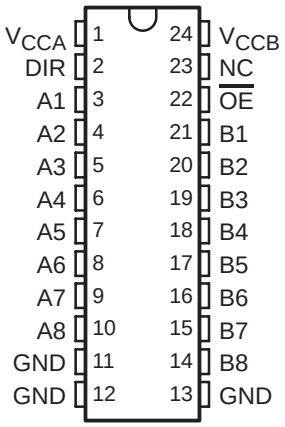
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Bidirectional Voltage Translator**
- **2.3 V to 3.6 V on A Port and 3 V to 5.5 V on B Port**
- **Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

DB, DW, OR PW PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

This 8-bit (octal) noninverting bus transceiver contains two separate supply rails. The B port is designed to track V_{CCB}, which accepts voltages from 3 V to 5.5 V, and the A port is designed to track V_{CCA}, which operates at 2.3 V to 3.6 V. This allows for translation from a 3.3-V to a 5-V system environment and vice versa, from a 2.5-V to a 3.3-V system environment and vice versa.

The SN74LVCC3245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are isolated. The control circuitry (DIR, $\overline{OE}$) is powered by V_{CCA}.

ORDERING INFORMATION

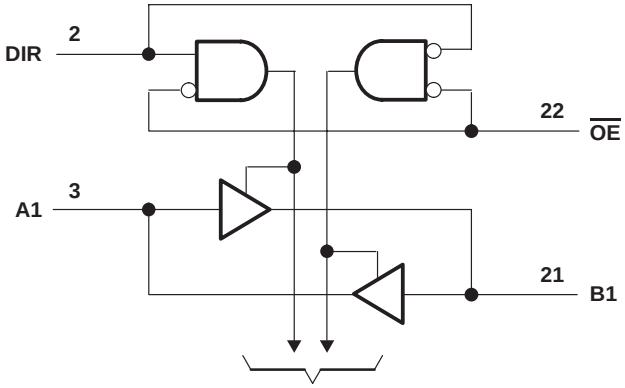
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC − DW	Reel of 2000	CLVCC3245AIDWREP	LVCC3245A
	SSOP − DB	Reel of 2000	CLVCC3245AIDBREP	LH245AEP
	TSSOP − PW	Reel of 2000	CLVCC3245AIPWREP	LH245AEP

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each transceiver)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB} . . . . . −0.5 V to 6 V
Input voltage range, V_I: All A ports (see Note 1) . . . . . −0.5 V to V_{CCA} + 0.5 V
All B ports (see Note 2) . . . . . −0.5 V to V_{CCB} + 0.5 V
Except I/O ports (see Note 1) . . . . . −0.5 V to V_{CCA} + 0.5 V
Output voltage range, V_O (see Note 2): All A ports . . . . . −0.5 V to V_{CCA} + 0.5 V
All B ports . . . . . −0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through V_{CCA}, V_{CCB}, or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 63°C/W
DW package . . . . . 46°C/W
PW package . . . . . 88°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 4.6 V maximum.
2. This value is limited to 6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
V_{CCA}	Supply voltage			2.3	3.3	3.6	V
V_{CCB}	Supply voltage			3	5	5.5	V
V_{IHA}	High-level input voltage	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V_{IHB}	High-level input voltage	2.3 V	3 V	2			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	3.85			
V_{ILA}	Low-level input voltage	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
V_{ILB}	Low-level input voltage	2.3 V	3 V			0.8	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			1.65	
V_{IH}	High-level input voltage (control pins) (Referenced to V_{CCA})	2.3 V	3 V	1.7			V
		2.7 V	3 V	2			
		3 V	3.6 V	2			
		3.6 V	5.5 V	2			
V_{IL}	Low-level input voltage (control pins) (Referenced to V_{CCA})	2.3 V	3 V			0.7	V
		2.7 V	3 V			0.8	
		3 V	3.6 V			0.8	
		3.6 V	5.5 V			0.8	
V_{IA}	Input voltage			0		V_{CCA}	V
V_{IB}	Input voltage			0		V_{CCB}	V
V_{OA}	Output voltage			0		V_{CCA}	V
V_{OB}	Output voltage			0		V_{CCB}	V

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions (see Note 4) (continued)

		V_{CCA}	V_{CCB}	MIN	NOM	MAX	UNIT
I_{OHA}	High-level output current	2.3 V	3 V			−8	mA
		2.7 V	3 V			−12	
		3.3 V	3 V			−24	
I_{OHB}	High-level output current	2.3 V	3.3 V			−12	mA
		2.7 V	3.3 V			−12	
		3.3 V	3 V			−24	
I_{OLA}	Low-level output current	2.3 V	3 V			8	mA
		2.7 V	3 V			12	
		3.3 V	3 V			24	
I_{OLB}	Low-level output current	2.3 V	3.3 V			12	mA
		2.7 V	3.3 V			12	
		3.3 V	3 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate					10	ns/V
T_A	Operating free-air temperature			−40		85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = −100 μA	3 V	3 V	2.9	3		V
		I_{OH} = −8 mA	2.3 V	3 V	2			
		I_{OH} = −12 mA	2.7 V	3 V	2.2	2.5		
			3 V	3 V	2.4	2.8		
		I_{OH} = −24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	2	2.3		
V_{OHB}		I_{OH} = −100 μA	3 V	3 V	2.9	3		V
		I_{OH} = −12 mA	2.3 V	3 V	2.4			
			2.7 V	3 V	2.4	2.8		
		I_{OH} = −24 mA	3 V	3 V	2.2	2.6		
			2.7 V	4.5 V	3.2	4.2		
V_{OLA}		I_{OL} = 100 μA	3 V	3 V			0.1	V
		I_{OL} = 8 mA	2.3 V	3 V			0.6	
		I_{OL} = 12 mA	2.7 V	3 V		0.1	0.5	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
			2.7 V	4.5 V		0.2	0.5	
V_{OLB}		I_{OL} = 100 μA	3 V	3 V			0.1	V
		I_{OL} = 12 mA	2.3 V	3 V			0.4	
		I_{OL} = 24 mA	3 V	3 V		0.2	0.5	
				4.5 V		0.2	0.5	
I_I	Control inputs	V_I = V_{CCA} or GND	3.6 V	3.6 V		±0.1	±1	μA
				5.5 V		±0.1	±1	
I_{OZ}†	A or B ports	V_O = $V_{CCA/B}$ or GND, V_I = V_{IL} or V_{IH}	3.6 V	3.6 V		±0.5	±5	μA
I_{CCA}	B to A	A port = V_{CCA} or GND, I_O = 0	3.6 V	Open		5	50	μA
		B port = V_{CCB} or GND, I_O = 0	3.6 V	3.6 V		5	50	
				5.5 V		5	50	
I_{CCB}	A to B	A port = V_{CCA} or GND, I_O = 0	3.6 V	3.6 V		5	50	μA
				5.5 V		8	80	
ΔI_{CCA}‡	A port	V_I = V_{CCA} − 0.6 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND and DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	mA
	$\overline{OE}$	V_I = V_{CCA} − 0.6 V, Other inputs at V_{CCA} or GND, DIR at V_{CCA}	3.6 V	3.6 V		0.35	0.5	
	DIR	V_I = V_{CCA} − 0.6 V, Other inputs at V_{CCA} or GND, $\overline{OE}$ at GND	3.6 V	3.6 V		0.35	0.5	
ΔI_{CCB}‡	B port	V_I = V_{CCB} − 2.1 V, Other inputs at V_{CCB} or GND, $\overline{OE}$ at GND and DIR at GND	3.6 V	5.5 V		1	1.5	mA
C_i	Control inputs	V_I = V_{CCA} or GND	Open	Open		4		pF
C_{io}	A or B ports	V_O = $V_{CCA/B}$ or GND	3.3 V	5 V		18.5		pF

† For I/O ports, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input that is at one of the specified voltage levels, rather than 0 V or the associated V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 2.5 V ± 0.2 V, V_{CCB} = 3.3 V ± 0.3 V		V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 5 V ± 0.5 V		V_{CCA} = 2.7 V TO 3.6 V, V_{CCB} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	9.4	1	6	1	7.1	ns
t_{PLH}			1	9.1	1	5.3	1	7.2	
t_{PHL}	B	A	1	11.2	1	5.8	1	6.4	ns
t_{PLH}			1	9.9	1	7	1	7.6	
t_{PZL}	$\overline{OE}$	A	1	14.5	1	9.2	1	9.7	ns
t_{PZH}			1	12.9	1	9.5	1	9.5	
t_{PZL}	$\overline{OE}$	B	1	13	1	8.1	1	9.2	ns
t_{PZH}			1	12.8	1	8.4	1	9.9	
t_{PLZ}	$\overline{OE}$	A	1	7.1	1	7	1	6.6	ns
t_{PHZ}			1	6.9	1	7.8	1	6.9	
t_{PLZ}	$\overline{OE}$	B	1	8.8	1	7.3	1	7.5	ns
t_{PHZ}			1	8.9	1	7	1	7.9	

operating characteristics, V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50, f = 10 MHz	38	pF
		Outputs disabled		4.5	

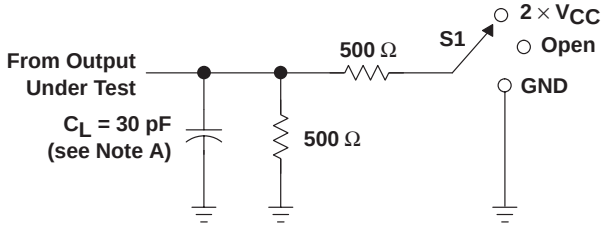
power-up considerations†

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. To guard against such power-up problems, take these precautions:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

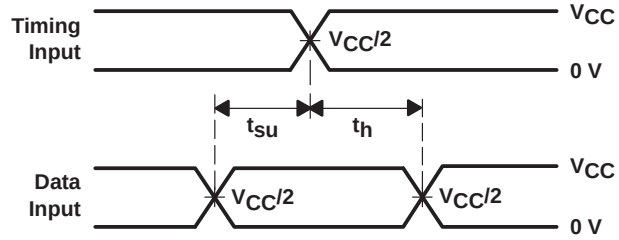
† Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

PARAMETER MEASUREMENT INFORMATION FOR A PORT
V_{CCA} = 2.5 V ± 0.2 V AND V_{CCB} = 3.3 V ± 0.3 V

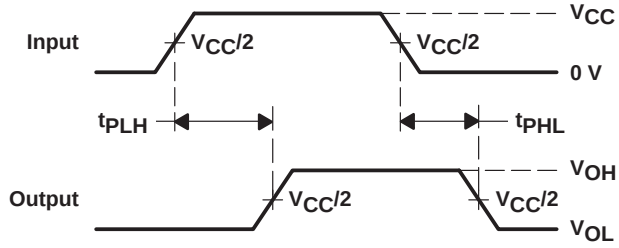


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

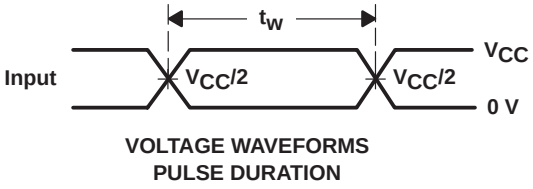
LOAD CIRCUIT



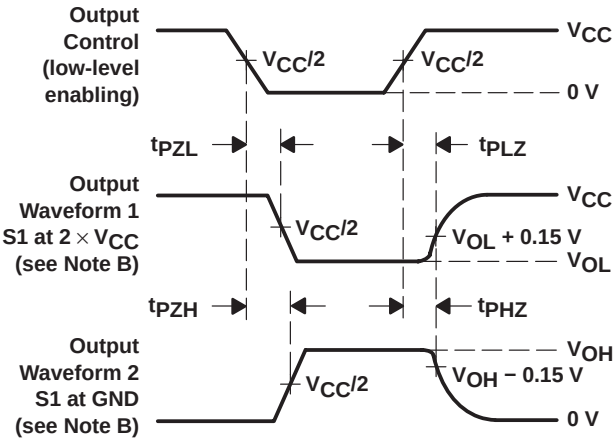
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

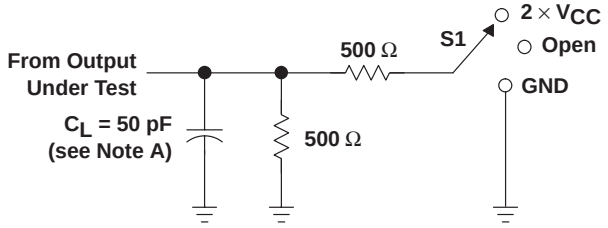


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

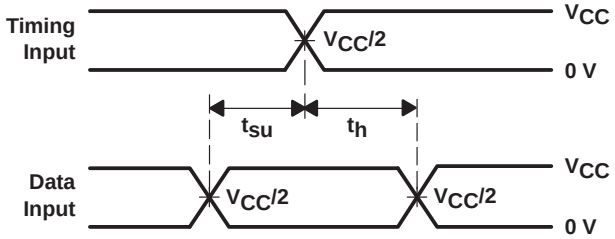
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR B PORT
V_{CCA} = 2.5 V ± 0.2 V AND V_{CCB} = 3.3 V ± 0.3 V

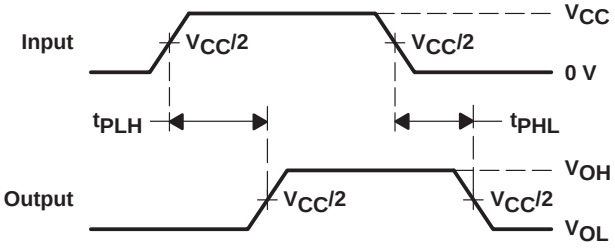


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

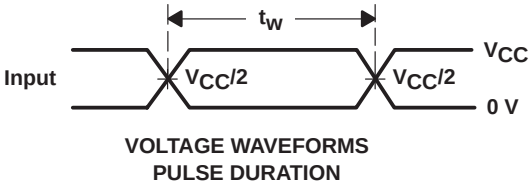
LOAD CIRCUIT



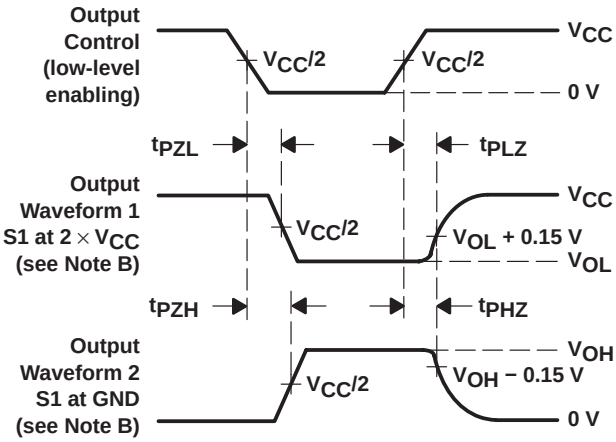
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION

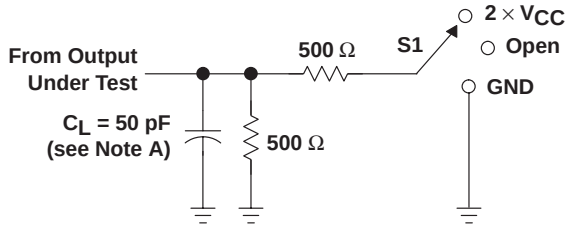


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

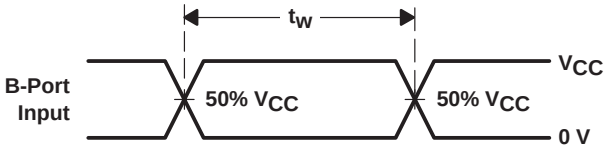
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR B PORT
V_{CCA} = 3.6 V AND V_{CCB} = 5.5 V

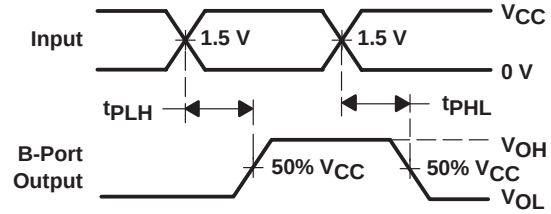


LOAD CIRCUIT

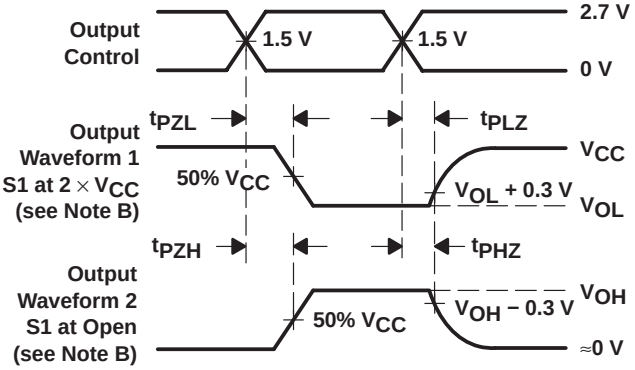
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

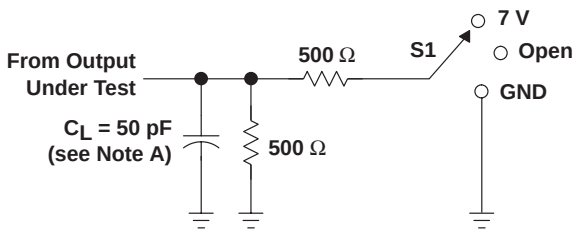


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

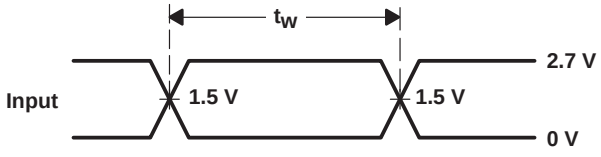
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION FOR A AND B PORT
V_{CCA} AND V_{CCB} = 3.6 V

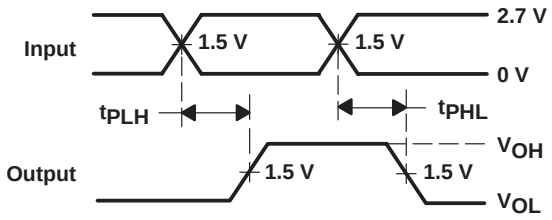


LOAD CIRCUIT

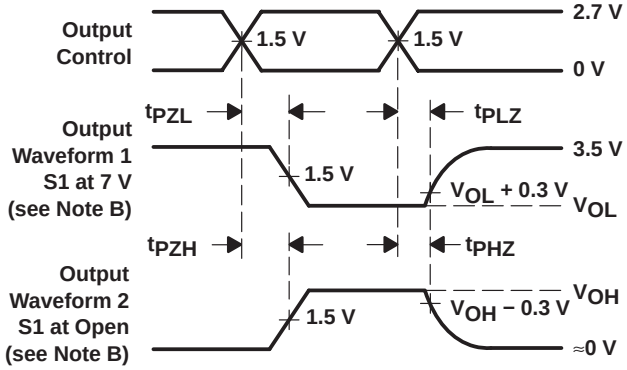
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLVCC3245AIDBREP	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245AEP	Samples
CLVCC3245AIDWREP	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples
CLVCC3245AIPWREP	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245AEP	Samples
V62/05602-01XE	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245AEP	Samples
V62/05602-01YE	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH245AEP	Samples
V62/05602-01ZE	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCC3245A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVCC3245A-EP :

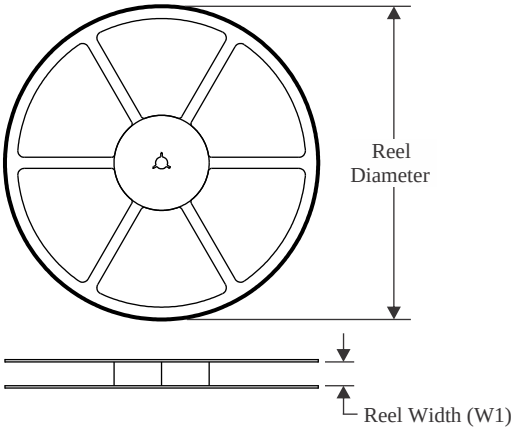
- Catalog: SN74LVCC3245A

NOTE: Qualified Version Definitions:

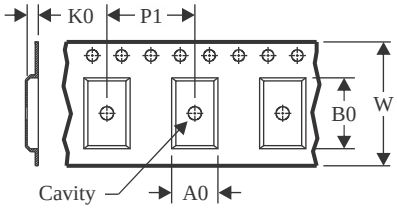
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

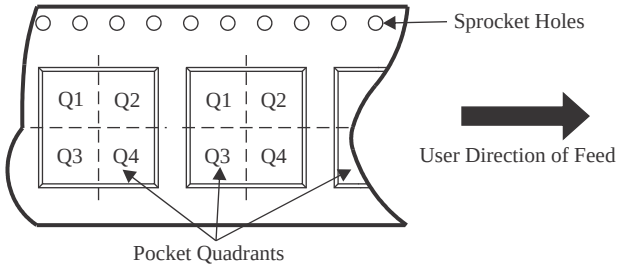


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

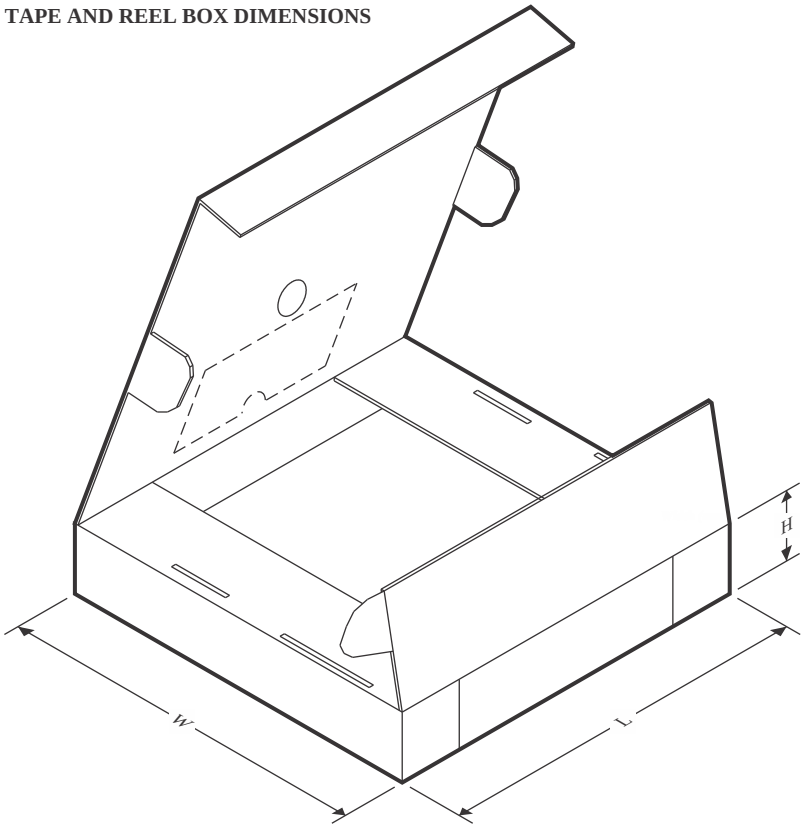
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLVCC3245AIDBREP	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
CLVCC3245AIDWREP	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CLVCC3245AIPWREP	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



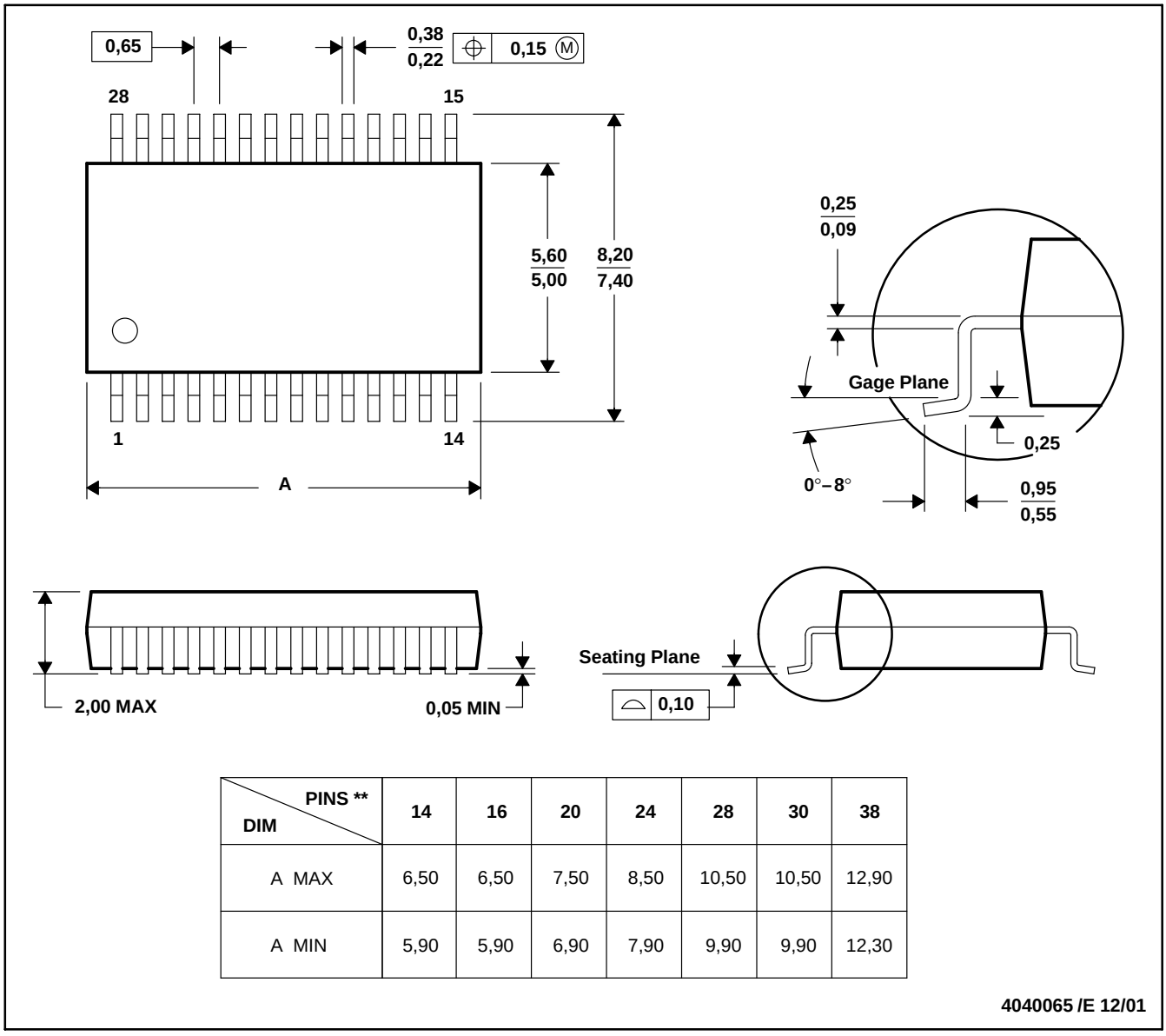
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLVCC3245AIDBREP	SSOP	DB	24	2000	356.0	356.0	35.0
CLVCC3245AIDWREP	SOIC	DW	24	2000	350.0	350.0	43.0
CLVCC3245AIPWREP	TSSOP	PW	24	2000	356.0	356.0	35.0

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN

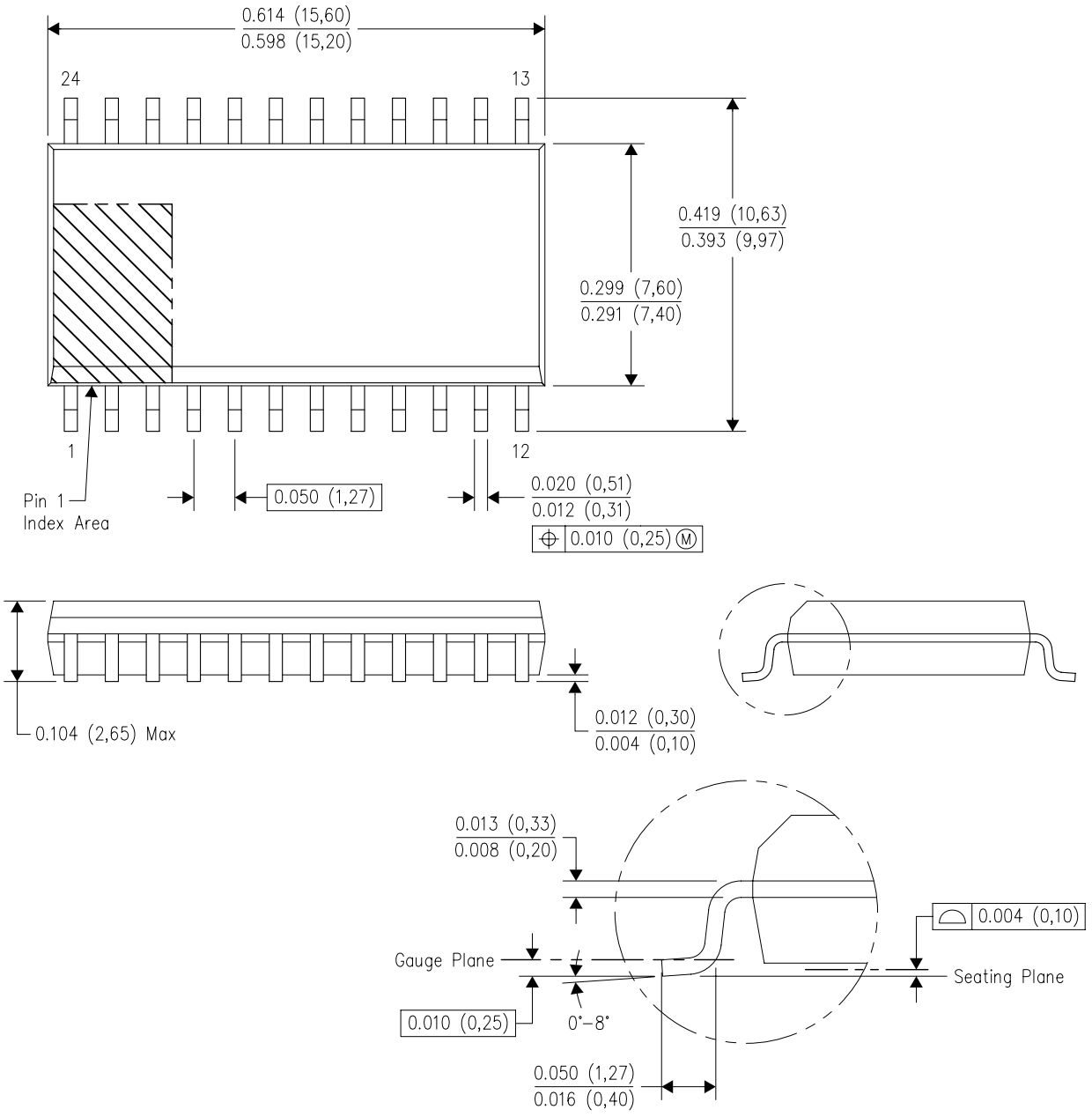


DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



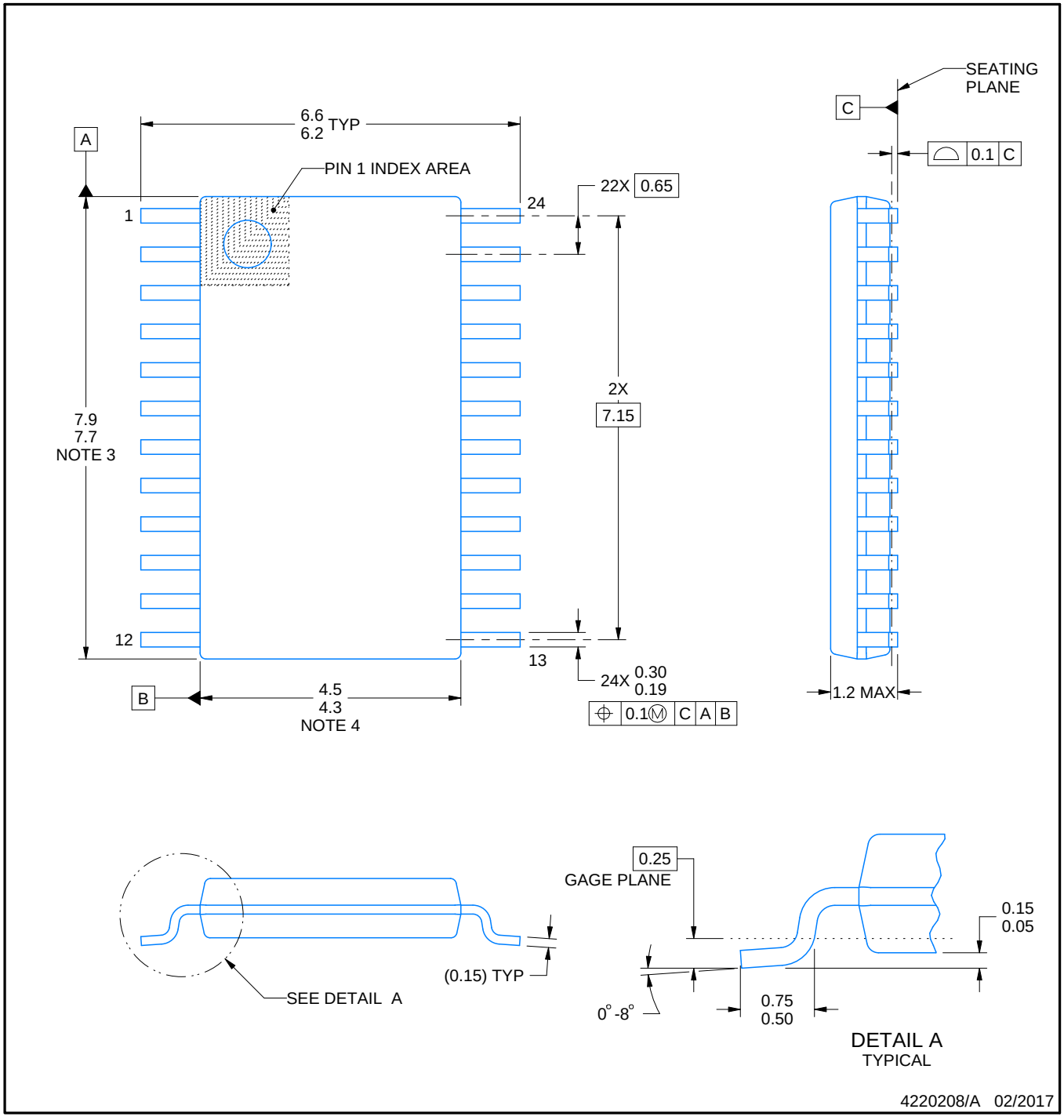
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

PACKAGE OUTLINE

PW0024A

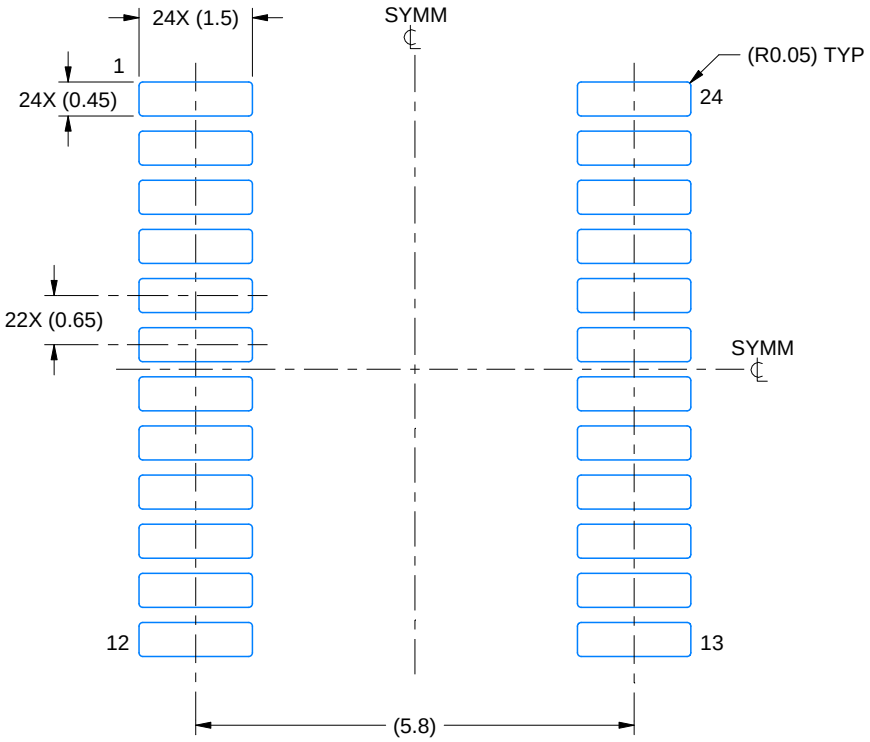
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

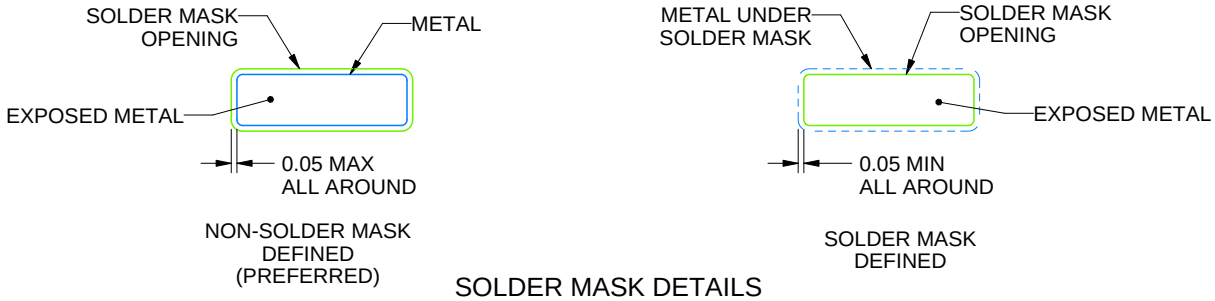


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

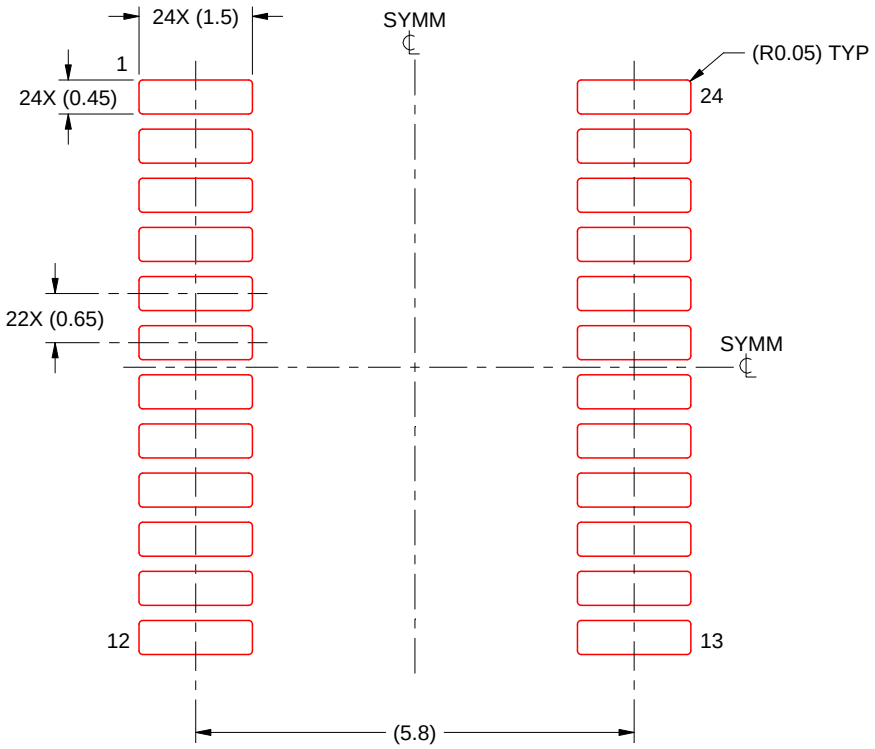


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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