TXB0102 2-Bit Bidirectional Voltage-Level Translator With Auto Direction Sensing and ±15-kV ESD Protection

1 Features

- Available in the Texas Instruments NanoFree™ Packages
- 1.2 V to 3.6 V on A Port and 1.65 V to 5.5 V On B Port ($V_{CCA} \leq V_{CCB}$)
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All Outputs Are in the High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- Low Power Consumption, 4-µA Max I_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port
    - 2500-V Human-Body Model (A114-B)
    - 200-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)
  - B Port
    - 15-kV Human-Body Model (A114-B)
    - 200-V Machine Model (A115-A)
    - 1500-V Charged-Device Model (C101)

2 Applications

- Handsets
- Smartphones
- Tablets
- Desktop PCs

3 Description

The TXB0102 device is a 2-bit noninverting translator that uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes. V_{CCA} must not exceed V_{CCB}.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

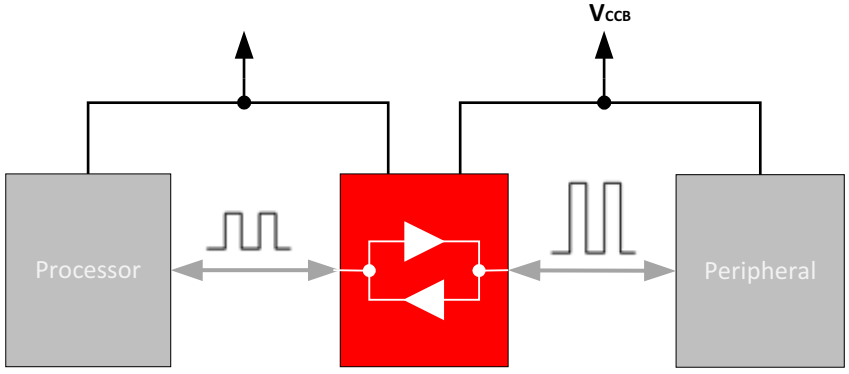
OE must be tied to GND through a pulldown resistor to assure the high-impedance state during power up or power down; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

NanoFree™ technology is a major breakthrough in IC packaging concepts, using the die as the package.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TXB0102DCU	VSSOP (8)	2.30 mm × 2.00 mm
TXB0102YZP	DSBGA (8)	0.90 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Typical Operating Circuit

Table of Contents

4 Pin Configuration and Functions

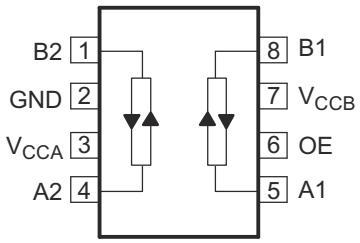


Figure 4-1. DCT Or DCU Package 8-Pin VSSOP Top View

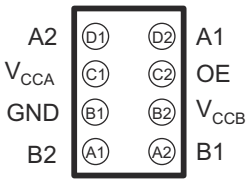


Figure 4-2. YZP Package 8-Pin DSBGA Bottom View

A. Pullup resistors are not recommended on TXB0102 I/O pins.
B. If pullup resistors are needed for open drain communication, please refer to the TXS0102 or contact TI.
C. If pullup or pulldown resistors are needed, the resistor value must be over 50 kΩ. See *Effects of External Pullup and Pulldown Resistors on TXS and TXB Devices* .
D. 50 kΩ is a safe recommended value, if the customer can accept higher Vol or lower V_{CCOUT}, smaller pullup or pulldown resistor is allowed, the draft estimation is $V_{OL} = V_{CCOUT} \times 4.5k/(4.5k + Rpu)$ and $V_{OH} = V_{CCOUT} \times Rdw/(4.5k + Rdw)$.
E. For detailed information, See *A Guide to Voltage Translation With TXB-Type Translators*.

Table 4-1. Pin Functions: YZP

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
A1	B2	I/O	Input/output B2. Referenced to V_{CCB}.
A2	B1	I/O	Input/output B1. Referenced to V_{CCB}.
B1	GND	S	Ground
B2	V_{CCB}	S	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V
C1	V_{CCA}	S	A-port supply voltage. 1.1 V ≤ V_{CCA} ≤ 3.6 V, V_{CCA} ≤ V_{CCB}
C2	OE	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}
D1	A2	I/O	Input/output A2. Referenced to V_{CCA}
D2	A1	I/O	Input/output A1. Referenced to V_{CCA}

(1) I = input, O = output, I/O = input and output, S = power supply

Table 4-2. Pin Functions: DCT or DCU

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
B2	1	I/O	Input/output B2. Referenced to V_{CCB}
GND	2	S	Ground
V_{CCA}	3	S	A-port supply voltage. 1.1 V ≤ V_{CCA} ≤ 3.6 V, V_{CCA} ≤ V_{CCB}
A2	4	I/O	Input/output A2. Referenced to V_{CCA}
A1	5	I/O	Input/output A1. Referenced to V_{CCA}
OE	6	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}
V_{CCB}	7	S	B-port supply voltage. 1.65 V ≤ V_{CCB} ≤ 5.5 V
B1	8	I/O	Input/output B1. Referenced to V_{CCB}

(1) I = input, O = output, I/O = input and output, S = power supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		–0.5	4.6	V
V_{CCB}			–0.5	6.5	
V_I	Input voltage(2)	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

5.2 ESD Ratings

			PORTS	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	A Port	±2500	V
			B Port	±1500	
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	A Port	±1500	V
			B Port	±1500	
		Machine model (MM), per A115-A	A Port	±200	V
			B Port	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

See(1) (2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}					1.65	5.5	
V_{IH}	High-level input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCI} × 0.65(3)	V_{CCI}	V
		OE input	1.2 V to 3.6 V	1.65 V to 5.5 V	V_{CCA} × 0.65	5.5	
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	V_{CCI} × 0.35(3)	V
		OE input	1.2 V to 3.6 V	1.65 V to 5.5 V	0	V_{CCA} × 0.35	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A port	1.2 V to 3.6 V	1.65 V to 5.5 V	0	3.6	V
		B port			0	5.5	
Δt/Δv	Input transition rise or fall rate	A port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
		B port inputs	1.2 V to 3.6 V	1.65 V to 1.95 V		40	
				4.5 V to 5.5 V		30	
T_A	Operating free-air temperature				–40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, that is, both at V_{CCI} or both at GND.
(2) V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.
(3) V_{CCI} is the supply voltage associated with the input port.

5.4 Thermal Information

THERMAL METRIC(1)		TXB0102			UNIT
		DCT (VSSOP)	DCU (VSSOP)	YZP (VSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	168.7	199.1	105.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	111.7	72.4	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.1	77.8	10.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.0	6.2	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.5	77.4	10.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics: T_A = 25°C

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER(1) (2)		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}		I_{OH} = –20 µA	1.2 V			1.1		V
			1.4 V to 3.6 V					
V_{OLA}		I_{OL} = 20 µA	1.2 V			0.3		V
			1.4 V to 3.6 V					
V_{OHB}		I_{OH} = –20 µA		1.65 V to 5.5 V				V
V_{OLB}		I_{OL} = 20 µA		1.65 V to 5.5 V				V
I_I	OE	V_I = V_{CCI} or GND	1.2 V to 3.6 V	1.65 V to 5.5 V			±1	µA
I_{off}	A port	V_I or V_O = 0 to 3.6 V	0 V	0 V to 5.5 V			±1	µA
	B port	V_I or V_O = 0 to 5.5 V	0 V to 3.6 V	0 V			±1	
I_{OZ}	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V			±1	µA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		0.06		µA
			1.4 V to 3.6 V	1.65 V to 5.5 V				
			3.6 V	0 V				
			0 V	5.5 V				
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.4		µA
			1.4 V to 3.6 V	1.65 V to 5.5 V				
			3.6 V	0 V				
			0 V	5.5 V				
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V		3.5		µA
			1.4 V to 3.6 V	1.65 V to 5.5 V				
I_{CCZA}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		0.05		µA
			1.4 V to 3.6 V	1.65 V to 5.5 V				
I_{CCZB}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V		3.3		µA
			1.4 V to 3.6 V	1.65 V to 5.5 V				
C_i	OE		1.2 V to 3.6 V	1.65 V to 5.5 V		2.5		pF
C_{io}	A port		1.2 V to 3.6 V	1.65 V to 5.5 V		5		pF
	B port					11		

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

5.6 Electrical Characteristics: T_A = –40°C to +85°C

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER(1) (2)		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{OHA}		I_{OH} = –20 µA	1.2 V				V
			1.4 V to 3.6 V		V_{CCA} – 0.4		
V_{OLA}		I_{OL} = 20 µA	1.2 V				V
			1.4 V to 3.6 V			0.4	
V_{OHB}		I_{OH} = –20 µA		1.65 V to 5.5 V	V_{CCB} – 0.4		V
V_{OLB}		I_{OL} = 20 µA		1.65 V to 5.5 V		0.4	V
I_I	OE	V_I = V_{CCI} or GND	1.2 V to 3.6 V	1.65 V to 5.5 V		±2	µA
I_{off}	A port	V_I or V_O = 0 to 3.6 V	0 V	0 V to 5.5 V		±2	µA
	B port	V_I or V_O = 0 to 5.5 V	0 V to 3.6 V	0 V		±2	
I_{OZ}	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V		±2	µA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V			µA
			1.4 V to 3.6 V	1.65 V to 5.5 V		3	
			3.6 V	0 V		2	
			0 V	5.5 V		–2	
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V			µA
			1.4 V to 3.6 V	1.65 V to 5.5 V		5	
			3.6 V	0 V		–2	
			0 V	5.5 V		2	
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V	1.65 V to 5.5 V			µA
			1.4 V to 3.6 V	1.65 V to 5.5 V		8	
I_{CCZA}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V			µA
			1.4 V to 3.6 V	1.65 V to 5.5 V		3	
I_{CCZB}		V_I = V_{CCI} or GND, I_O = 0, OE = GND	1.2 V	1.65 V to 5.5 V			µA
			1.4 V to 3.6 V	1.65 V to 5.5 V		5	
C_i	OE		1.2 V to 3.6 V	1.65 V to 5.5 V		3	pF
C_{io}	A port		1.2 V to 3.6 V	1.65 V to 5.5 V		6	pF
	B port					14	

(1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.

5.7 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pdA}	A port input, B port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = V_{CCA} (outputs enabled)	V_{CCA} = 1.2 V, V_{CCB} = 5 V	7.8	pF
			V_{CCA} = 1.2 V, V_{CCB} = 1.8 V	8	
			V_{CCA} = 1.5 V, V_{CCB} = 1.8 V	8	
			V_{CCA} = 1.8 V, V_{CCB} = 1.8 V	7	
			V_{CCA} = 2.5 V, V_{CCB} = 2.5 V	7	
			V_{CCA} = 2.5 V, V_{CCB} = 5 V	8	
			V_{CCA} = 3.3 V, V_{CCB} = 3.3 V to 5 V	8	
	B port input, A port output		V_{CCA} = 1.2 V, V_{CCB} = 5 V	12	
			V_{CCA} = 1.2 V, V_{CCB} = 1.8 V	11	
			V_{CCA} = 1.5 V, V_{CCB} = 1.8 V	11	
			V_{CCA} = 1.8 V, V_{CCB} = 1.8 V	11	
			V_{CCA} = 2.5 V, V_{CCB} = 2.5 V	11	
			V_{CCA} = 2.5 V, V_{CCB} = 5 V	11	
			V_{CCA} = 3.3 V, V_{CCB} = 3.3 V to 5 V	11	
C_{pdB}	A port input, B port output		V_{CCA} = 1.2 V, V_{CCB} = 5 V	38.1	
			V_{CCA} = 1.2 V, V_{CCB} = 1.8 V	29	
			V_{CCA} = 1.5 V, V_{CCB} = 1.8 V	29	
			V_{CCA} = 1.8 V, V_{CCB} = 1.8 V	29	
			V_{CCA} = 2.5 V, V_{CCB} = 2.5 V	29	
			V_{CCA} = 2.5 V, V_{CCB} = 5 V	30	
			V_{CCA} = 3.3 V, V_{CCB} = 3.3 V to 5 V	30	
	B port input, A port output		V_{CCA} = 1.2 V, V_{CCB} = 5 V	25.4	
			V_{CCA} = 1.2 V, V_{CCB} = 1.8 V	19	
			V_{CCA} = 1.5 V, V_{CCB} = 1.8 V	18	
			V_{CCA} = 1.8 V, V_{CCB} = 1.8 V	18	
			V_{CCA} = 2.5 V, V_{CCB} = 2.5 V	18	
			V_{CCA} = 2.5 V, V_{CCB} = 5 V	21	
			V_{CCA} = 3.3 V, V_{CCB} = 3.3 V to 5 V	21	

5.7 Operating Characteristics (continued)

T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pdA}	A port input, B port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = GND (outputs disabled)	V_{CCA} = 1.2 V, V_{CCB} = 5 V	0.01	pF
			V_{CCA} = 1.2 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 1.5 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 1.8 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 2.5 V, V_{CCB} = 2.5 V	0.01	
			V_{CCA} = 2.5 V, V_{CCB} = 5 V	0.01	
			V_{CCA} = 3.3 V, V_{CCB} = 3.3 V to 5 V	0.01	
	B port input, A port output		V_{CCA} = 1.2 V, V_{CCB} = 5 V	0.01	
			V_{CCA} = 1.2 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 1.5 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 1.8 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 2.5 V, V_{CCB} = 2.5 V	0.01	
			V_{CCA} = 2.5 V, V_{CCB} = 5 V	0.01	
			V_{CCA} = 3.3 V, V_{CCB} = 3.3 V to 5 V	0.01	
C_{pdB}	A port input, B port output		V_{CCA} = 1.2 V, V_{CCB} = 5 V	0.01	
			V_{CCA} = 1.2 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 1.5 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 1.8 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 2.5 V, V_{CCB} = 2.5 V	0.01	
			V_{CCA} = 2.5 V, V_{CCB} = 5 V	0.01	
			V_{CCA} = 3.3 V, V_{CCB} = 3.3 V to 5 V	0.02	
	B port input, A port output		V_{CCA} = 1.2 V, V_{CCB} = 5 V	0.01	
			V_{CCA} = 1.2 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 1.5 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 1.8 V, V_{CCB} = 1.8 V	0.01	
			V_{CCA} = 2.5 V, V_{CCB} = 2.5 V	0.01	
			V_{CCA} = 2.5 V, V_{CCB} = 5 V	0.02	
			V_{CCA} = 3.3 V, V_{CCB} = 3.3 V to 5 V	0.03	

5.8 V_{CCA} = 1.2 V Timing Requirements

T_A = 25°C, V_{CCA} = 1.2 V

			TEST CONDITIONS	NOM	UNIT
Data rate			V_{CCB} = 1.8 V	20	Mbps
			V_{CCB} = 2.5 V	20	
			V_{CCB} = 3.3 V	20	
			V_{CCB} = 5 V	20	
t_w	Pulse duration	Data inputs	V_{CCB} = 1.8 V	50	ns
			V_{CCB} = 2.5 V	50	
			V_{CCB} = 3.3 V	50	
			V_{CCB} = 5 V	50	

5.9 V_{CCA} = 1.5 V ± 0.1 V Timing Requirements

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

			TEST CONDITIONS	MIN	MAX	UNIT
Data rate			V_{CCB} = 1.8 V ± 0.15 V		40	Mbps
			V_{CCB} = 2.5 V ± 0.2 V		40	
			V_{CCB} = 3.3 V ± 0.3 V		40	
			V_{CCB} = 5 V ± 0.5 V		40	
t_w	Pulse duration	Data inputs	V_{CCB} = 1.8 V ± 0.15 V	25		ns
			V_{CCB} = 2.5 V ± 0.2 V	25		
			V_{CCB} = 3.3 V ± 0.3 V	25		
			V_{CCB} = 5 V ± 0.5 V	25		

5.10 V_{CCA} = 1.8 V ± 0.15 V Timing Requirements

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

			TEST CONDITIONS	MIN	MAX	UNIT
Data rate			V_{CCB} = 1.8 V ± 0.15 V		60	Mbps
			V_{CCB} = 2.5 V ± 0.2 V		60	
			V_{CCB} = 3.3 V ± 0.3 V		60	
			V_{CCB} = 5 V ± 0.5 V		60	
t_w	Pulse duration	Data inputs	V_{CCB} = 1.8 V ± 0.15 V	17		ns
			V_{CCB} = 2.5 V ± 0.2 V	17		
			V_{CCB} = 3.3 V ± 0.3 V	17		
			V_{CCB} = 5 V ± 0.5 V	17		

5.11 V_{CCA} = 2.5 V ± 0.2 V Timing Requirements

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

			TEST CONDITIONS	MIN	MAX	UNIT
Data rate			V_{CCB} = 2.5 V ± 0.2 V		100	Mbps
			V_{CCB} = 3.3 V ± 0.3 V		100	
			V_{CCB} = 5 V ± 0.5 V		100	
t_w	Pulse duration	Data inputs	V_{CCB} = 2.5 V ± 0.2 V	10		ns
			V_{CCB} = 3.3 V ± 0.3 V	10		
			V_{CCB} = 5 V ± 0.5 V	10		

5.12 V_{CCA} = 3.3 V ± 0.3 V Timing Requirements

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

			TEST CONDITIONS	MIN	MAX	UNIT
Data rate			V_{CCB} = 3.3 V ± 0.3 V		100	Mbps
			V_{CCB} = 5 V ± 0.5 V		100	
t_w	Pulse duration	Data inputs	V_{CCB} = 3.3 V ± 0.3 V	10		ns
			V_{CCB} = 5 V ± 0.5 V	10		

5.13 V_{CCA} = 1.2 V Switching Characteristics

T_A = 25°C, V_{CCA} = 1.2 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TYP	UNIT
t_{pd}	A	B	V_{CCB} = 1.8 V	6.9	ns
			V_{CCB} = 2.5 V	5.7	
			V_{CCB} = 3.3 V	5.3	
			V_{CCB} = 5 V	5.5	
	B	A	V_{CCB} = 1.8 V	7.4	
			V_{CCB} = 2.5 V	6.4	
			V_{CCB} = 3.3 V	6	
			V_{CCB} = 5 V	5.8	
t_{en}	OE	A	V_{CCB} = 1.8 V	1	µs
			V_{CCB} = 2.5 V	1	
			V_{CCB} = 3.3 V	1	
			V_{CCB} = 5 V	1	
		B	V_{CCB} = 1.8 V	1	
			V_{CCB} = 2.5 V	1	
			V_{CCB} = 3.3 V	1	
			V_{CCB} = 5 V	1	
t_{dis}	OE	A	V_{CCB} = 1.8 V	18	ns
			V_{CCB} = 2.5 V	15	
			V_{CCB} = 3.3 V	14	
			V_{CCB} = 5 V	14	
		B	V_{CCB} = 1.8 V	20	
			V_{CCB} = 2.5 V	17	
			V_{CCB} = 3.3 V	16	
			V_{CCB} = 5 V	16	
t_{rA}	A port rise time		V_{CCB} = 1.8 V	4.2	ns
			V_{CCB} = 2.5 V	4.2	
			V_{CCB} = 3.3 V	4.2	
			V_{CCB} = 5 V	4.2	
t_{fA}	A port fall times		V_{CCB} = 1.8 V	4.2	ns
			V_{CCB} = 2.5 V	4.2	
			V_{CCB} = 3.3 V	4.2	
			V_{CCB} = 5 V	4.2	

5.13 V_{CCA} = 1.2 V Switching Characteristics (continued)

T_A = 25°C, V_{CCA} = 1.2 V

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TYP	UNIT
t_{rB}	B port rise times		V_{CCB} = 1.8 V	2.1	ns
			V_{CCB} = 2.5 V	1.5	
			V_{CCB} = 3.3 V	1.2	
			V_{CCB} = 5 V	1.1	
t_{fB}	B port fall times		V_{CCB} = 1.8 V	2.1	ns
			V_{CCB} = 2.5 V	1.5	
			V_{CCB} = 3.3 V	1.2	
			V_{CCB} = 5 V	1.1	
$t_{sk(o)}$	Channel-to-channel		V_{CCB} = 1.8 V	0.5	ns
			V_{CCB} = 2.5 V	0.5	
			V_{CCB} = 3.3 V	0.5	
			V_{CCB} = 5 V	1.4	
Max data rate			V_{CCB} = 1.8 V	20	Mbps
			V_{CCB} = 2.5 V	20	
			V_{CCB} = 3.3 V	20	
			V_{CCB} = 5 V	20	

5.14 V_{CCA} = 1.5 V ± 0.1 V Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	A	B	V_{CCB} = 1.8 V ± 0.15 V	1.4	12.9	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.2	10.1	
			V_{CCB} = 3.3 V ± 0.3 V	1.1	10	
			V_{CCB} = 5 V ± 0.5 V	0.8	9.9	
	B	A	V_{CCB} = 1.8 V ± 0.15 V	0.9	14.2	
			V_{CCB} = 2.5 V ± 0.2 V	0.7	12	
			V_{CCB} = 3.3 V ± 0.3 V	0.4	11.7	
			V_{CCB} = 5 V ± 0.5 V	0.3	13.7	
t_{en}	OE	A	V_{CCB} = 1.8 V ± 0.15 V		1	µs
			V_{CCB} = 2.5 V ± 0.2 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
			V_{CCB} = 5 V ± 0.5 V		1	
		B	V_{CCB} = 1.8 V ± 0.15 V		1	
			V_{CCB} = 2.5 V ± 0.2 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
			V_{CCB} = 5 V ± 0.5 V		1	
t_{dis}	OE	A	V_{CCB} = 1.8 V ± 0.15 V	5.9	31	ns
			V_{CCB} = 2.5 V ± 0.2 V	5.7	25.9	
			V_{CCB} = 3.3 V ± 0.3 V	5.6	23	
			V_{CCB} = 5 V ± 0.5 V	5.7	22.4	
		B	V_{CCB} = 1.8 V ± 0.15 V	5.4	30.3	
			V_{CCB} = 2.5 V ± 0.2 V	4.9	22.8	
			V_{CCB} = 3.3 V ± 0.3 V	4.8	20	
			V_{CCB} = 5 V ± 0.5 V	4.9	19.5	
t_{rA}	A port rise times		V_{CCB} = 1.8 V ± 0.15 V	1.4	5.1	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.4	5.1	
			V_{CCB} = 3.3 V ± 0.3 V	1.4	5.1	
			V_{CCB} = 5 V ± 0.5 V	1.4	5.1	
t_{fA}	A port fall times		V_{CCB} = 1.8 V ± 0.15 V	1.4	5.1	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.4	5.1	
			V_{CCB} = 3.3 V ± 0.3 V	1.4	5.1	
			V_{CCB} = 5 V ± 0.5 V	1.4	5.1	
t_{rB}	B port rise times		V_{CCB} = 1.8 V ± 0.15 V	0.9	4.5	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.6	3.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	2.8	
			V_{CCB} = 5 V ± 0.5 V	0.4	2.7	
t_{fB}	B port fall times		V_{CCB} = 1.8 V ± 0.15 V	0.9	4.5	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.6	3.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	2.8	
			V_{CCB} = 5 V ± 0.5 V	0.4	2.7	

5.14 V_{CCA} = 1.5 V ± 0.1 V Switching Characteristics (continued)

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
$t_{sk(o)}$	Channel-to-channel		V_{CCB} = 1.8 V ± 0.15 V		0.5	ns
			V_{CCB} = 2.5 V ± 0.2 V		0.5	
			V_{CCB} = 3.3 V ± 0.3 V		0.5	
			V_{CCB} = 5 V ± 0.5 V		0.5	
Max data rate			V_{CCB} = 1.8 V ± 0.15 V	40		Mbps
			V_{CCB} = 2.5 V ± 0.2 V	40		
			V_{CCB} = 3.3 V ± 0.3 V	40		
			V_{CCB} = 5 V ± 0.5 V	40		

5.15 V_{CCA} = 1.8 V ± 0.15 V Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	A	B	V_{CCB} = 1.8 V ± 0.15 V	1.6	11	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.4	7.7	
			V_{CCB} = 3.3 V ± 0.3 V	1.3	6.8	
			V_{CCB} = 5 V ± 0.5 V	1.2	6.5	
	B	A	V_{CCB} = 1.8 V ± 0.15 V	1.5	12	
			V_{CCB} = 2.5 V ± 0.2 V	1.3	8.4	
			V_{CCB} = 3.3 V ± 0.3 V	1	7.6	
			V_{CCB} = 5 V ± 0.5 V	0.9	7.1	
t_{en}	OE	A	V_{CCB} = 1.8 V ± 0.15 V		1	µs
			V_{CCB} = 2.5 V ± 0.2 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
			V_{CCB} = 5 V ± 0.5 V		1	
		B	V_{CCB} = 1.8 V ± 0.15 V		1	
			V_{CCB} = 2.5 V ± 0.2 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
			V_{CCB} = 5 V ± 0.5 V		1	
t_{dis}	OE	A	V_{CCB} = 1.8 V ± 0.15 V	5.9	31	ns
			V_{CCB} = 2.5 V ± 0.2 V	5.1	21.3	
			V_{CCB} = 3.3 V ± 0.3 V	5	19.3	
			V_{CCB} = 5 V ± 0.5 V	5	17.4	
		B	V_{CCB} = 1.8 V ± 0.15 V	5.4	30.3	
			V_{CCB} = 2.5 V ± 0.2 V	4.4	20.8	
			V_{CCB} = 3.3 V ± 0.3 V	4.2	17.9	
			V_{CCB} = 5 V ± 0.5 V	4.3	16.3	
t_{rA}	A port rise times		V_{CCB} = 1.8 V ± 0.15 V	1	4.2	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.1	4.1	
			V_{CCB} = 3.3 V ± 0.3 V	1.1	4.1	
			V_{CCB} = 5 V ± 0.5 V	1.1	4.1	
t_{fA}	A port fall times		V_{CCB} = 1.8 V ± 0.15 V	1	4.2	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.1	4.1	
			V_{CCB} = 3.3 V ± 0.3 V	1.1	4.1	
			V_{CCB} = 5 V ± 0.5 V	1.1	4.1	
t_{rB}	B port rise times		V_{CCB} = 1.8 V ± 0.15 V	0.9	4.5	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.6	3.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	2.8	
			V_{CCB} = 5 V ± 0.5 V	0.4	2.7	
t_{fB}	B port fall times		V_{CCB} = 1.8 V ± 0.15 V	0.9	4.5	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.6	3.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5	2.8	
			V_{CCB} = 5 V ± 0.5 V	0.4	2.7	

5.15 V_{CCA} = 1.8 V ± 0.15 V Switching Characteristics (continued)

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
$t_{sk(o)}$	Channel-to-channel		V_{CCB} = 1.8 V ± 0.15 V		0.5	ns
			V_{CCB} = 2.5 V ± 0.2 V		0.5	
			V_{CCB} = 3.3 V ± 0.3 V		0.5	
			V_{CCB} = 5 V ± 0.5 V		0.5	
Max data rate			V_{CCB} = 1.8 V ± 0.15 V	60		Mbps
			V_{CCB} = 2.5 V ± 0.2 V	60		
			V_{CCB} = 3.3 V ± 0.3 V	60		
			V_{CCB} = 5 V ± 0.5 V	60		

5.16 V_{CCA} = 2.5 V ± 0.2 V Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted)

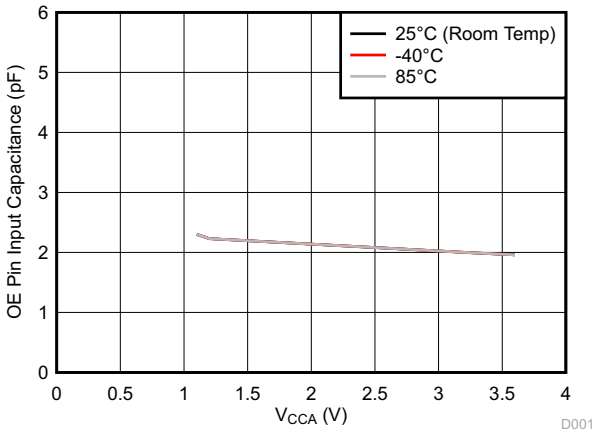
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	A	B	V_{CCB} = 2.5 V ± 0.2 V	1.1	6.3	ns
			V_{CCB} = 3.3 V ± 0.3 V	1	5.2	
			V_{CCB} = 5 V ± 0.5 V	0.9	4.7	
	B	A	V_{CCB} = 2.5 V ± 0.2 V	1.2	6.6	
			V_{CCB} = 3.3 V ± 0.3 V	1.1	5.1	
			V_{CCB} = 5 V ± 0.5 V	0.9	4.4	
t_{en}	OE	A	V_{CCB} = 2.5 V ± 0.2 V		1	µs
			V_{CCB} = 3.3 V ± 0.3 V		1	
			V_{CCB} = 5 V ± 0.5 V		1	
		B	V_{CCB} = 2.5 V ± 0.2 V		1	
			V_{CCB} = 3.3 V ± 0.3 V		1	
			V_{CCB} = 5 V ± 0.5 V		1	
t_{dis}	OE	A	V_{CCB} = 2.5 V ± 0.2 V	5.1	21.3	ns
			V_{CCB} = 3.3 V ± 0.3 V	4.6	15.2	
			V_{CCB} = 5 V ± 0.5 V	4.6	13.2	
		B	V_{CCB} = 2.5 V ± 0.2 V	4.4	20.8	
			V_{CCB} = 3.3 V ± 0.3 V	3.8	16	
			V_{CCB} = 5 V ± 0.5 V	3.9	13.9	
t_{rA}	A port rise times		V_{CCB} = 2.5 V ± 0.2 V	0.8	3	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.8	3	
			V_{CCB} = 5 V ± 0.5 V	0.8	3	
t_{fA}	A port fall times		V_{CCB} = 2.5 V ± 0.2 V	0.8	3	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.8	3	
			V_{CCB} = 5 V ± 0.5 V	0.8	3	
t_{rB}	B port rise times		V_{CCB} = 2.5 V ± 0.2 V	0.7	3	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.5	2.8	
			V_{CCB} = 5 V ± 0.5 V	0.4	2.7	
t_{fB}	B port fall times		V_{CCB} = 2.5 V ± 0.2 V	0.7	3	ns
			V_{CCB} = 3.3 V ± 0.3 V	0.5	2.8	
			V_{CCB} = 5 V ± 0.5 V	0.4	2.7	
$t_{sk(o)}$	Channel-to-channel		V_{CCB} = 2.5 V ± 0.2 V		0.5	ns
			V_{CCB} = 3.3 V ± 0.3 V		0.5	
			V_{CCB} = 5 V ± 0.5 V		0.5	
Max data rate			V_{CCB} = 2.5 V ± 0.2 V	100		Mbps
			V_{CCB} = 3.3 V ± 0.3 V	100		
			V_{CCB} = 5 V ± 0.5 V	100		

5.17 V_{CCA} = 3.3 V ± 0.3 V Switching Characteristics

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted)

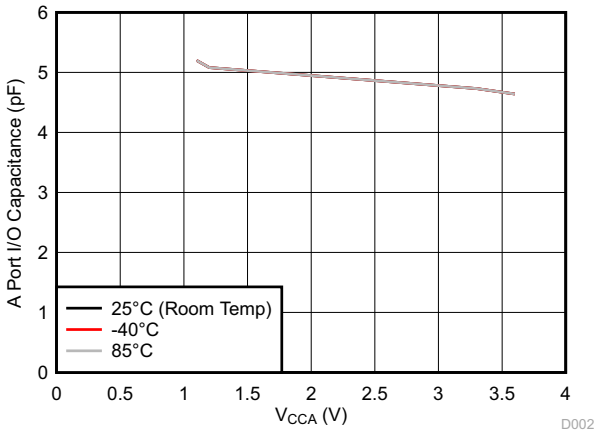
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{pd}	A	B	V_{CCB} = 3.3 V ± 0.3 V	0.9	4.7	ns
			V_{CCB} = 5 V ± 0.5 V	0.8	4	
	B	A	V_{CCB} = 3.3 V ± 0.3 V	1	4.9	
			V_{CCB} = 5 V ± 0.5 V	0.9	4.5	
t_{en}	OE	A	V_{CCB} = 3.3 V ± 0.3 V		1	µs
			V_{CCB} = 5 V ± 0.5 V		1	
		B	V_{CCB} = 3.3 V ± 0.3 V		1	
			V_{CCB} = 5 V ± 0.5 V		1	
t_{dis}	OE	A	V_{CCB} = 3.3 V ± 0.3 V	4.6	15.2	ns
			V_{CCB} = 5 V ± 0.5 V	4.3	12.1	
		B	V_{CCB} = 3.3 V ± 0.3 V	3.8	16	
			V_{CCB} = 5 V ± 0.5 V	3.4	13.2	
t_{rA}	A port rise times		V_{CCB} = 3.3 V ± 0.3 V	0.7	2.5	ns
			V_{CCB} = 5 V ± 0.5 V	0.7	2.5	
t_{fA}	A port fall times		V_{CCB} = 3.3 V ± 0.3 V	0.7	2.5	ns
			V_{CCB} = 5 V ± 0.5 V			
t_{rB}	B port rise times		V_{CCB} = 3.3 V ± 0.3 V	0.5	2.3	ns
			V_{CCB} = 5 V ± 0.5 V	0.4	2.7	
t_{fB}	B port fall times		V_{CCB} = 3.3 V ± 0.3 V	0.5	2.3	ns
			V_{CCB} = 5 V ± 0.5 V	0.4	2.7	
$t_{sk(o)}$	Channel-to-channel		V_{CCB} = 3.3 V ± 0.3 V		0.5	ns
			V_{CCB} = 5 V ± 0.5 V		0.5	
Max data rate			V_{CCB} = 3.3 V ± 0.3 V	100		Mbps
			V_{CCB} = 5 V ± 0.5 V	100		

5.18 Typical Characteristics



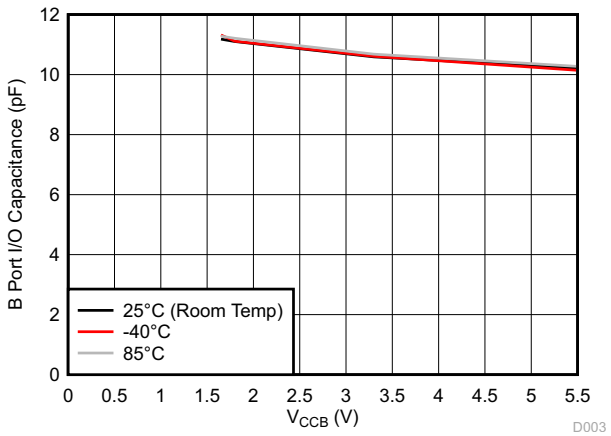
V_{CCB} = 3.3 V

Figure 5-1. Input Capacitance for OE pin (C_I) vs Power Supply (V_{CCA})



V_{CCB} = 3.3 V

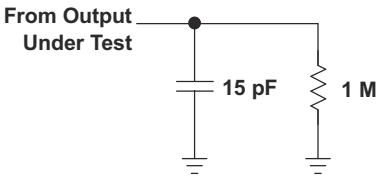
Figure 5-2. Capacitance for A Port I/O Pins (C_{IO}) vs Power Supply (V_{CCA})



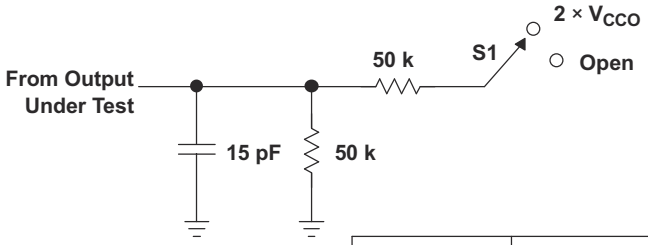
V_{CCA} = 1.8 V

Figure 5-3. Capacitance for B Port I/O Pins (C_{IO}) vs Power Supply (V_{CCB})

6 Parameter Measurement Information

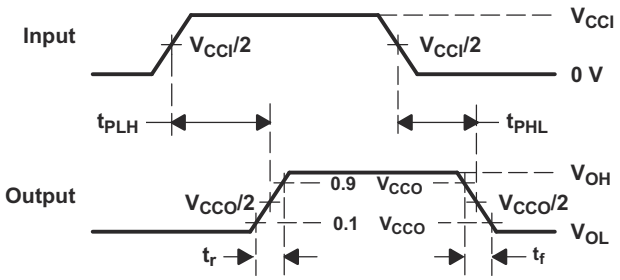


LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

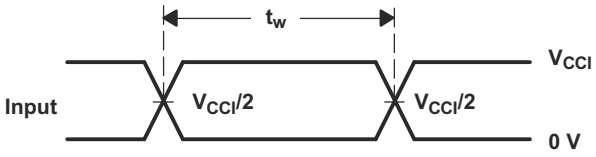


LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ} t_{PHZ}/t_{PZH}	2 × V_{CCO} Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION

A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 W, dv/dt ≥ 1 V/ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. V_{CCI} is the V_{CC} associated with the input port.
F. V_{CCO} is the V_{CC} associated with the output port.
G. All parameters and waveforms are not applicable to all devices.

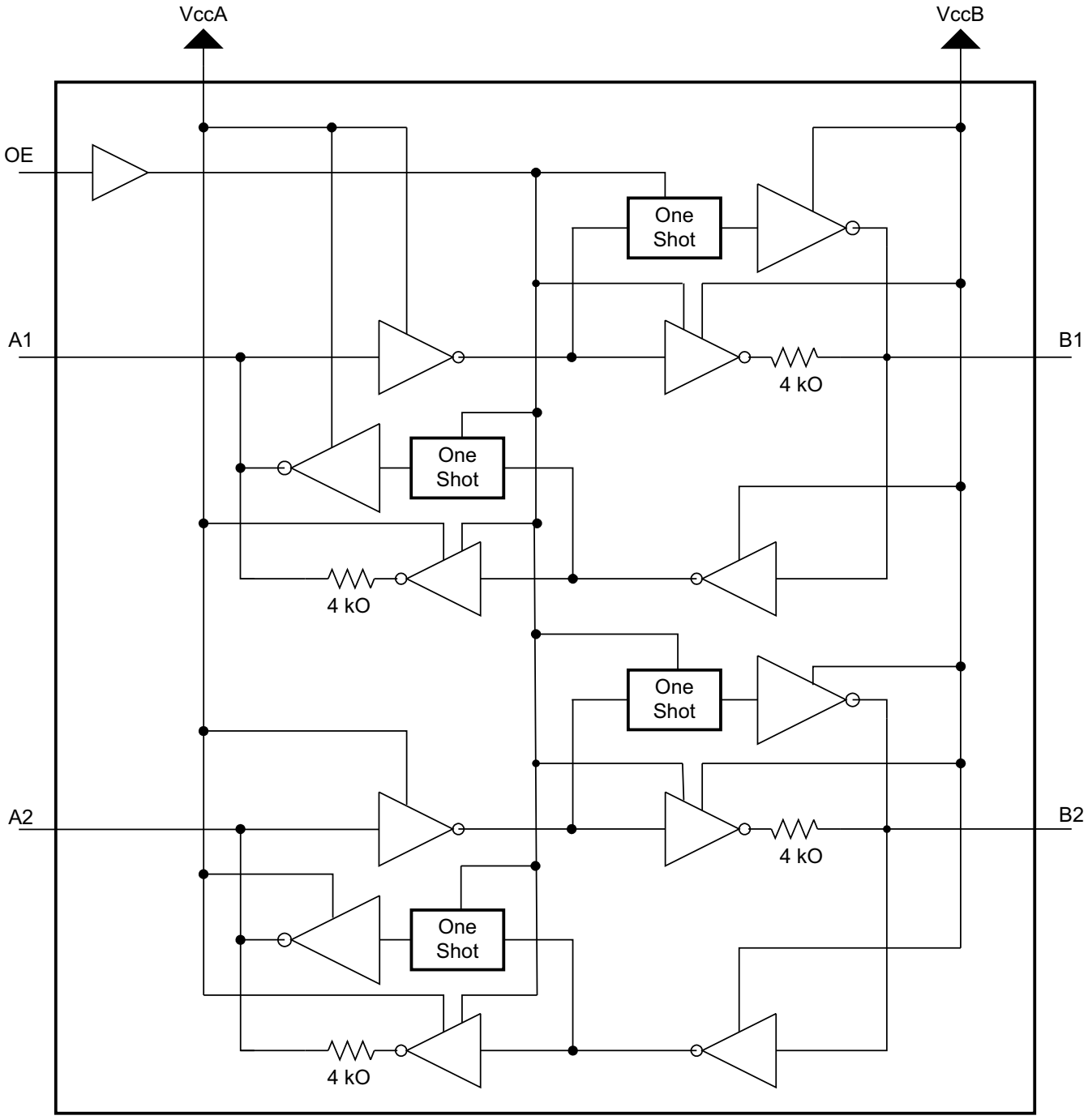
Figure 6-1. Load Circuits And Voltage Waveforms

7 Detailed Description

7.1 Overview

The TXB0102 device is a 4-bit directionless voltage-level translator specifically designed for translating logic voltage levels. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge rate accelerators (one shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. For open drain signal translation, see TI TXS010X products.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Architecture

The TXB0102 architecture (see Figure 7-1) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the TXB0102 can maintain a high or low, but are designed to be weak, so that the drivers can be overdriven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70 Ω at VCCO = 1.2 V to 1.8 V, 50 Ω at VCCO = 1.8 V to 3.3 V and 40 Ω at VCCO = 3.3 V to 5 V.

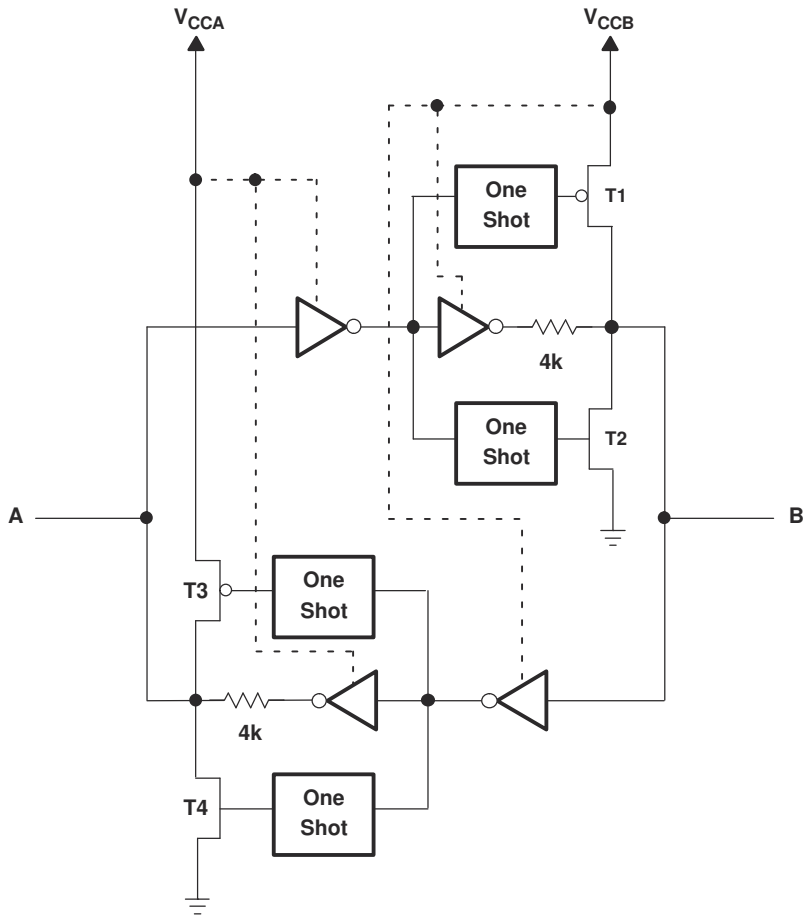
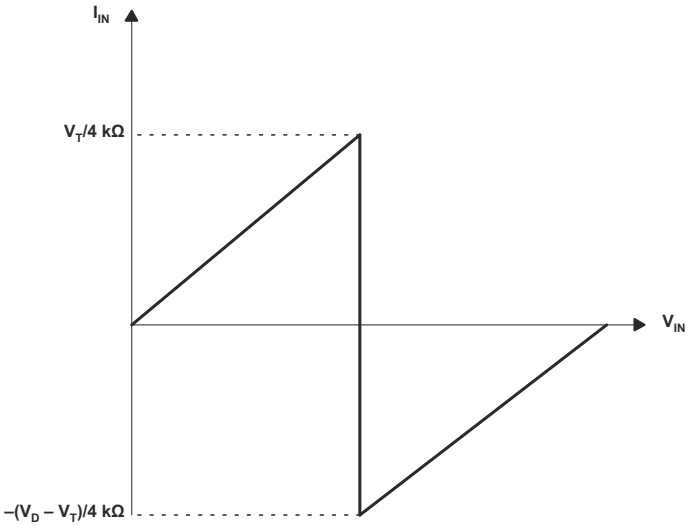


Figure 7-1. Architecture of TXB0102 I/O Cell

7.3.2 Input Driver Requirements

Figure 7-2 shows the typical I_{IN} versus V_{IN} characteristics of the TXB0102. For proper operation, the device driving the data I/Os of the TXB0102 must have drive strength of at least ±2 mA.



A. V_T is the input threshold voltage of the TXB0102 (typically $V_{CCI}/2$.
B. V_D is the supply voltage of the external driver.

Figure 7-2. Typical I_{IN} vs V_{IN} Curve

7.3.3 Output Load Considerations

TI recommends careful printed-circuit board (PCB) layout practices with short PCB trace lengths to avoid excessive capacitive loading and to assure that proper O.S. triggering takes place. PCB signal trace-lengths must be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by assuring that any reflection sees a low impedance at the driver. The O.S. circuits have been designed to stay on for approximately 10 ns. The maximum capacitance of the lumped load that is driven also depends directly on the one-shot duration. With heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The O.S. duration has been set to best optimize trade-offs between dynamic ICC, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance that the TXB0102 output sees, so TI recommends that this lumped-load capacitance be considered to avoid O.S. retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

7.3.4 Enable and Disable

The TXB0102 has an output-enable (OE) input that is used to disable the device by setting OE = low, which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

7.3.5 Pullup or Pulldown Resistors on I/O Lines

The TXB0102 is designed to drive capacitive loads of up to 70 pF. The output drivers of the TXB0102 have low DC drive strength. If pullup or pulldown resistors are connected externally to the data I/Os, their values must be kept higher than 50 kΩ to assure that they do not contend with the output drivers of the TXB0102.

For the same reason, the TXB0102 device must not be used in applications such as I2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS01xx series of level translators.

7.4 Device Functional Modes

The TXB0102 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high impedance state. Setting the OE input high enables the device.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXB0102 is used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open drain signal translation, please refer to TI TXS010X products. Any external pulldown or pullup resistors are recommended larger than 50 kΩ.

8.2 Typical Application

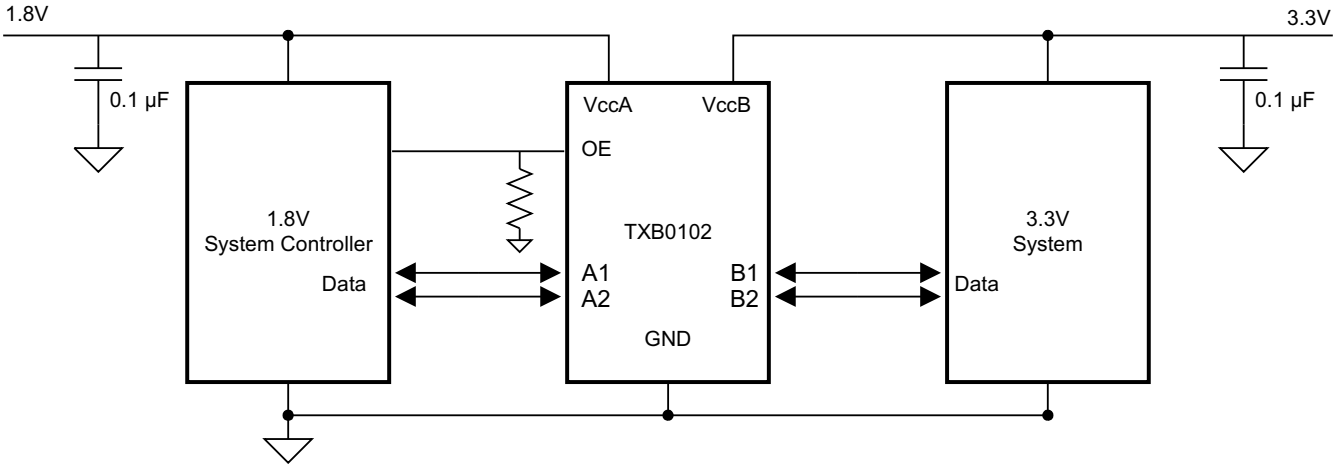


Figure 8-1. Typical Operating Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 and make sure that $V_{CCA} \leq V_{CCB}$.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0102 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXB0102 device is driving to determine the output voltage range.
  - TI does not recommend to have the external pullup or pulldown resistors. If mandatory, TI recommends that the value should be larger than 50 kΩ.

- An external pulldown or pullup resistor decreases the output V_{OH} and V_{OL}. Use Equation 1 and Equation 2 to draft estimate the V_{OH} and V_{OL} as a result of an external pulldown and pullup resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4.5\ k\Omega) \quad (1)$$

$$V_{OL} = V_{CCx} \times 4.5\ k\Omega / (R_{PU} + 4.5\ k\Omega) \quad (2)$$

where

  - V_{CCx} is the output port supply voltage on either V_{CCA} or V_{CCB}
  - R_{PD} is the value of the external pulldown resistor
  - R_{PU} is the value of the external pullup resistor
  - 4.5 kΩ is the counting the variation of the serial resistor 4 kΩ in the I/O line.

8.2.3 Application Curve

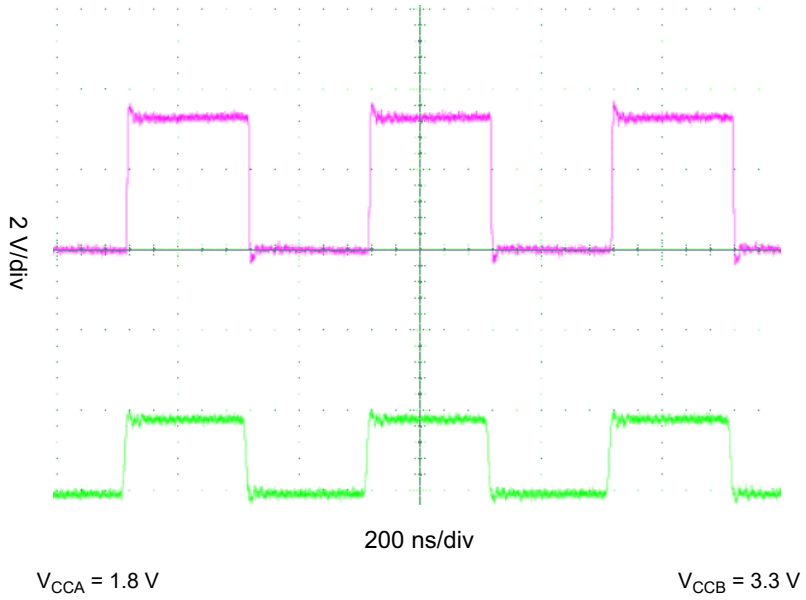


Figure 8-2. Level-Translation of a 2.5-MHz Signal

8.3 Power Supply Recommendations

During operation, assure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first. The TXB0102 device has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V). The (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To assure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver.

8.4 Layout

8.4.1 Layout Guidelines

Follow common PCB layout guidelines to assure reliability of the device.

Bypass capacitors must be used on power suppliesand placed as close as possible to the V_{CCA}, V_{CCB} pin, and GND pin.

Short trace lengths must be used to avoid excessive loading.

PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the oneshot duration, approximately 10 ns, assuring that any reflection encounters low impedance at the source driver.

8.4.2 Layout Example

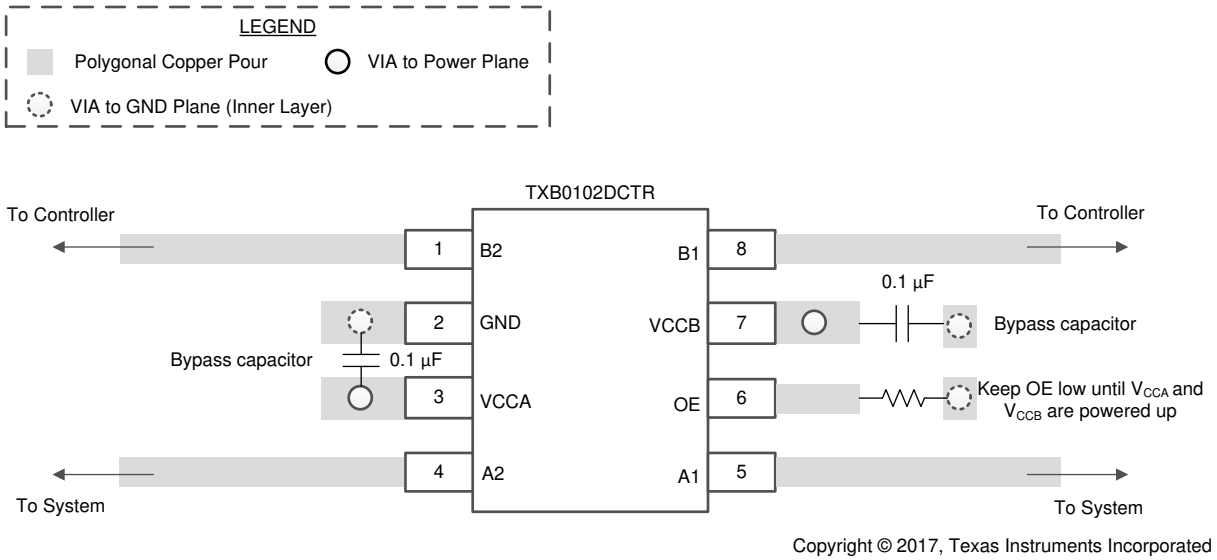


Figure 8-3. TXB0102 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *A Guide to Voltage Translation With TXB-Type Translators* Application Report
- Texas Instruments, *Effects of pullup and pulldown resistors on TXS and TXB devices* Application Report
- Texas Instruments, *Introduction to Logic* Application Report
- Texas Instruments, *A Guide to Voltage Translation With TXS-Type Translators* Application Report
- Texas Instruments, *A Guide to Voltage Translation With TXB-Type Translators* Application Report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

NanoFree™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2017) to Revision E (October 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.	1

Changes from Revision C (December 2014) to Revision D (September 2017)	Page
• Added Junction temperature, T_J in *Absolute Maximum Ratings*	4

Changes from Revision B (March 2012) to Revision C (December 2014)	Page
• Added *Pin Configuration and Functions* section, *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision A (January 2011) to Revision B (March 2012)	Page
• Added notes to pin out graphics	3

Changes from Revision * (May 2007) to Revision A ()	Page
• Added ball labels to the YZP Package	3

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0102DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(FD, NFDQ, NFDR) NZ	Samples
TXB0102DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFDR	Samples
TXB0102DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(FD, NFDQ, NFDR) NZ	Samples
TXB0102DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NFDR	Samples
TXB0102YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(2E, 2E2, 2EN)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

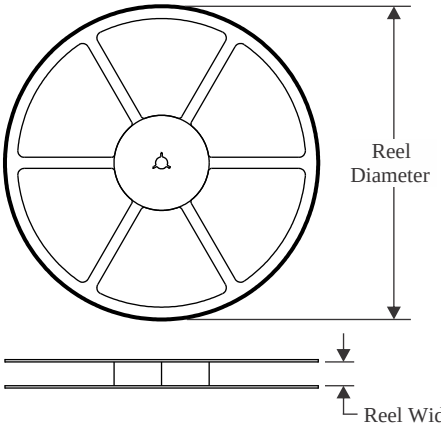
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

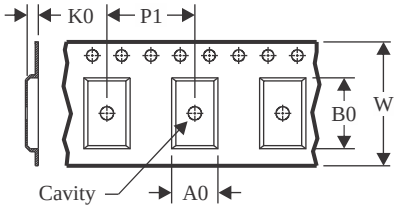
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

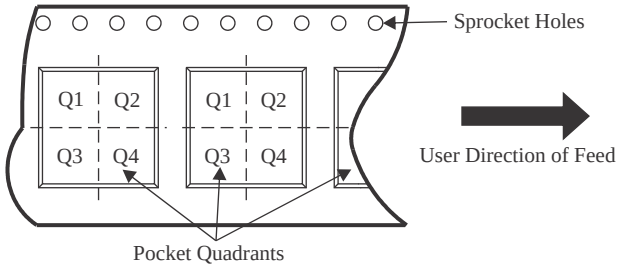


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

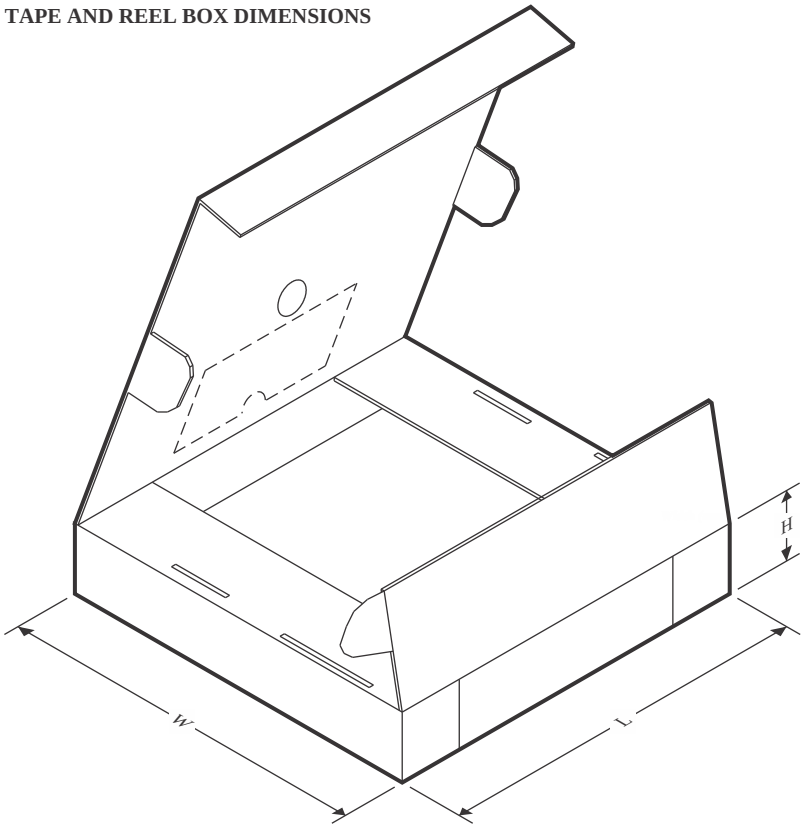
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0102DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXB0102DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TXB0102YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1
TXB0102YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

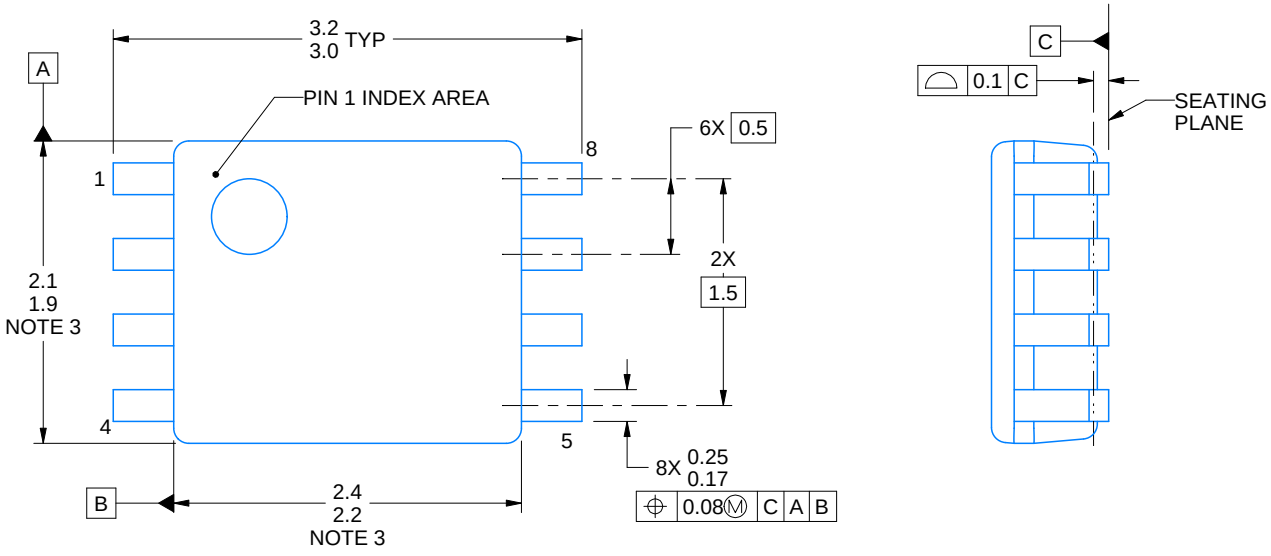
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0102DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TXB0102DCURG4	VSSOP	DCU	8	3000	183.0	183.0	20.0
TXB0102YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0
TXB0102YZPR	DSBGA	YZP	8	3000	182.0	182.0	20.0

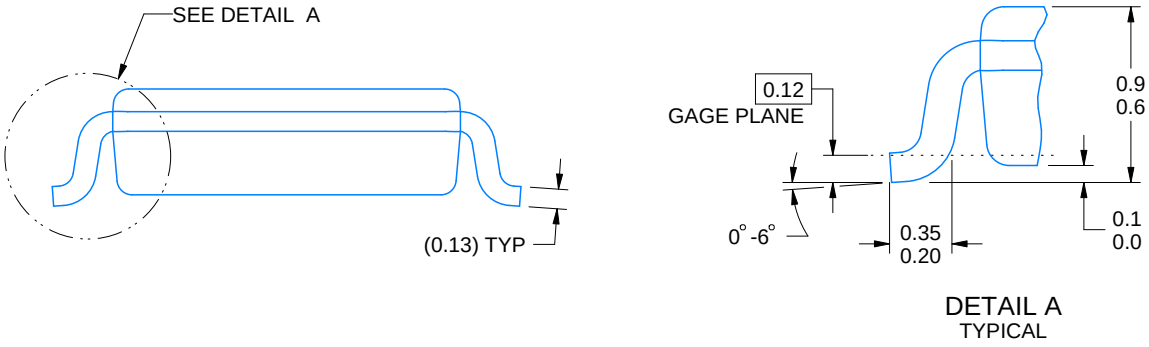
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

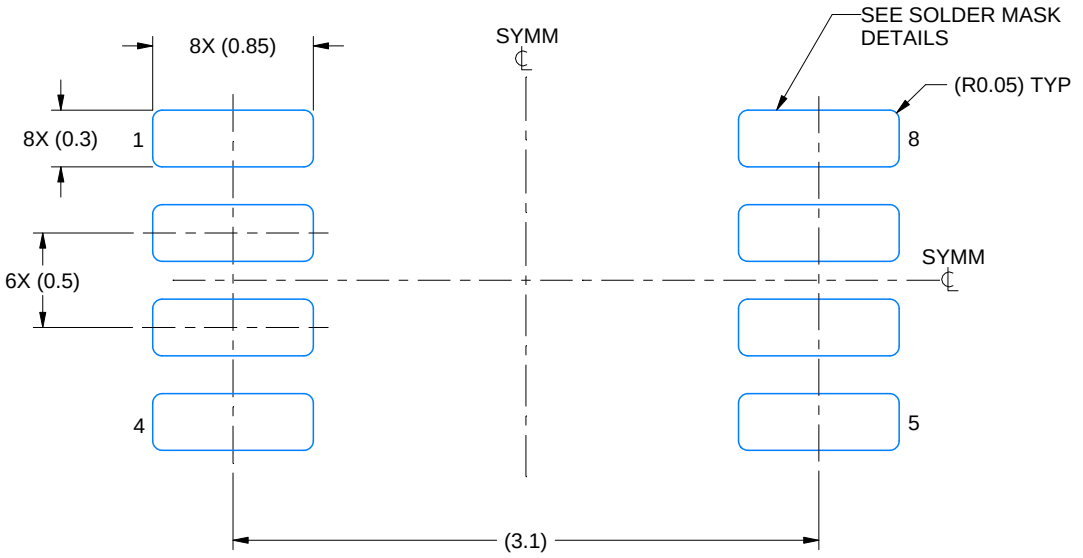




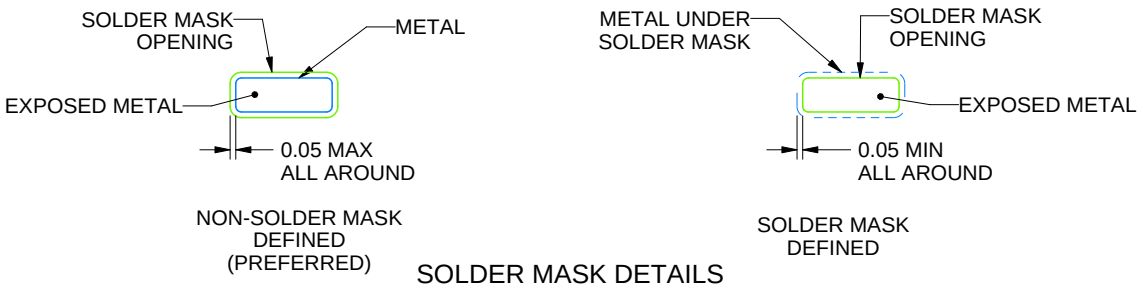
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

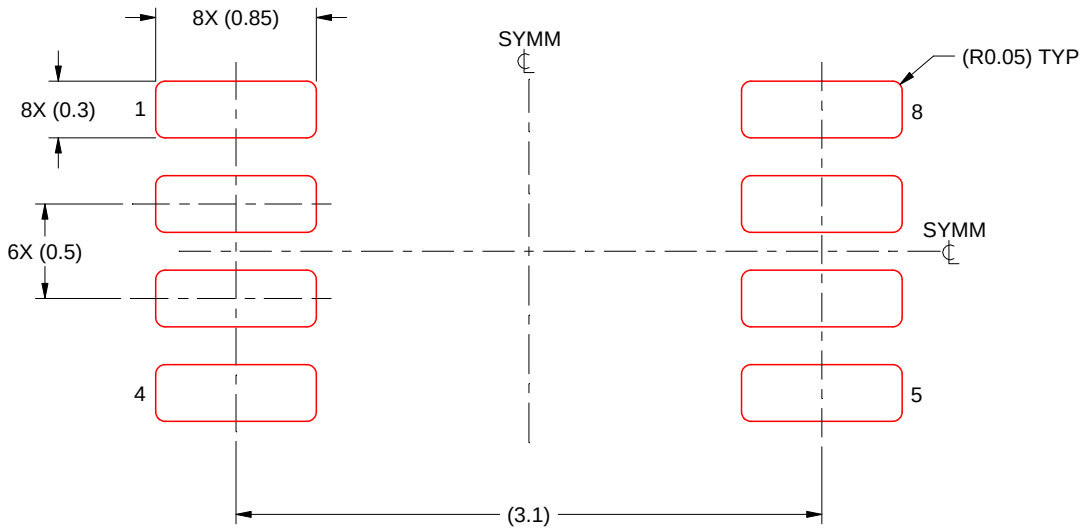


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

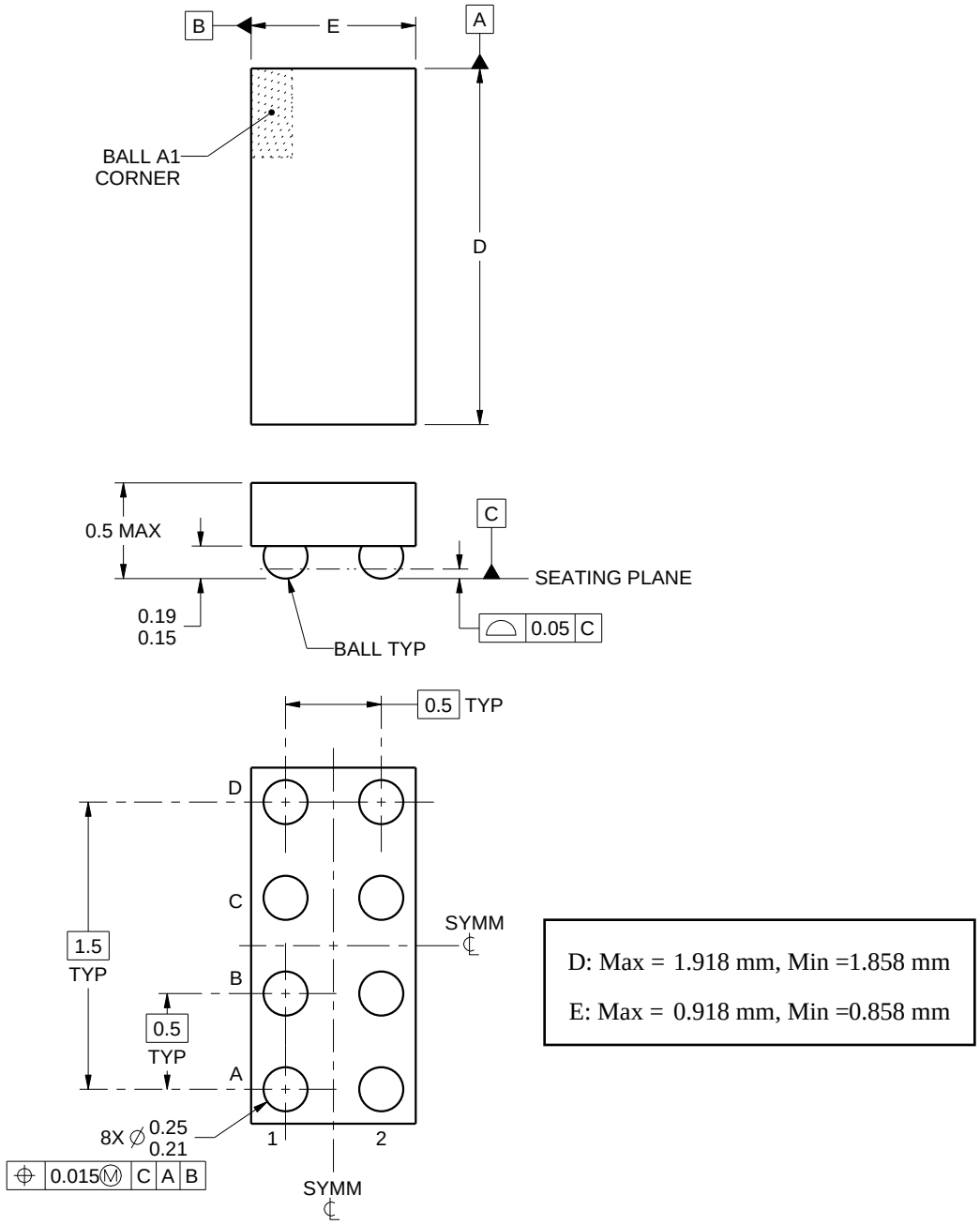
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

YZP0008

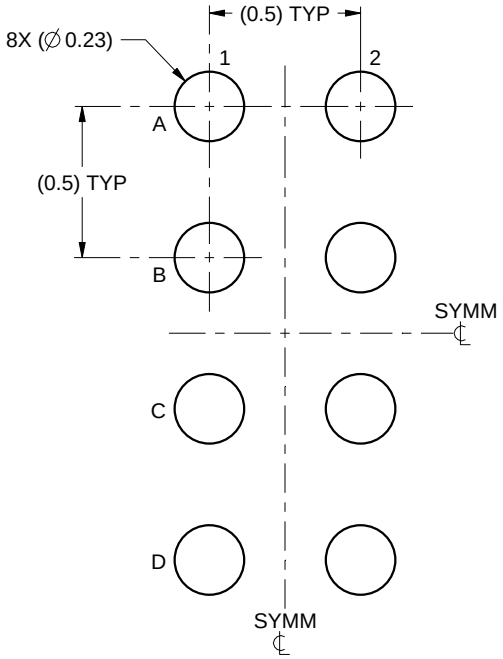
DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

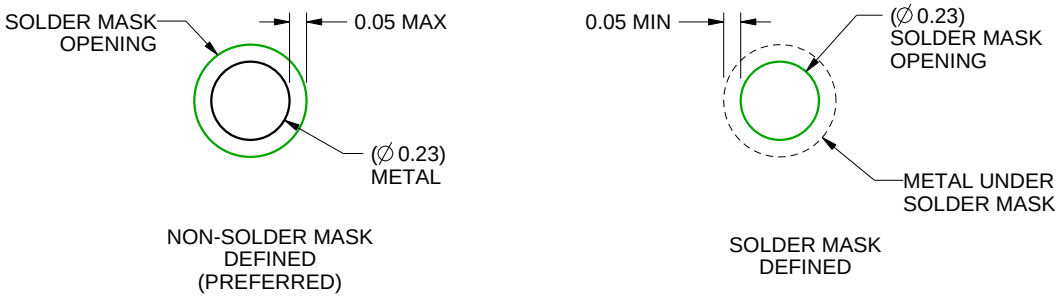


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

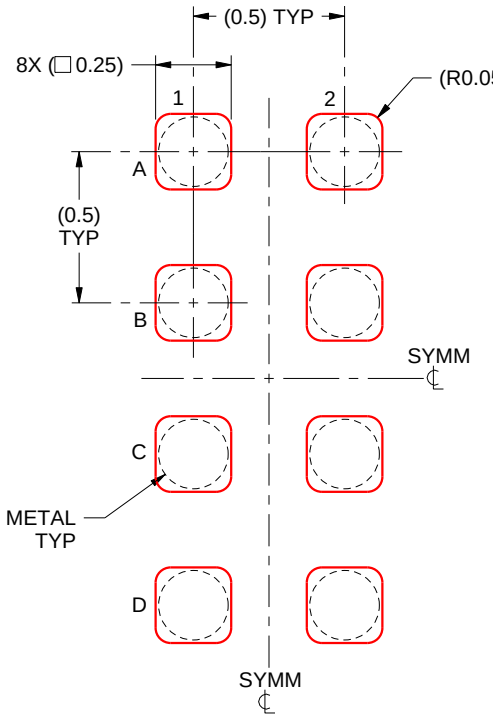


SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265