

## CURRENT MODE PWM CONTROLLER (KNOWN GOOD DIE)

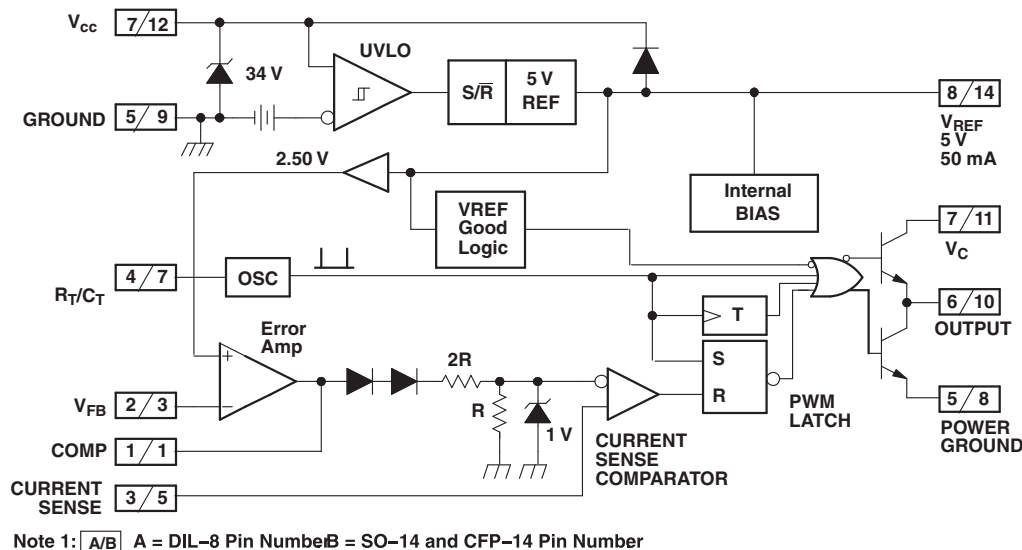
### FEATURES

- **–55°C to 125°C Known Good Die**
- **Controlled Baseline**
- **Optimized For Off-line and DC-to-DC Converters**
- **Low Start-Up Current (<1 mA)**
- **Automatic Feed Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load Response Characteristics**
- **Under-Voltage Lockout With Hysteresis**
- **Double Pulse Suppression**
- **High Current Totem Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500-kHz Operation**
- **Low  $R_O$  Error Amp**

### DESCRIPTION

The UC1843 family of control devices provides the necessary features to implement off-line or dc-to-dc fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-Channel MOSFETs, is low in the off state. The under-voltage lockout threshold is 8.4 V and maximum duty cycle range is around 100%.

### BLOCK DIAGRAM



### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	KGD	UC1843KGD1	NA

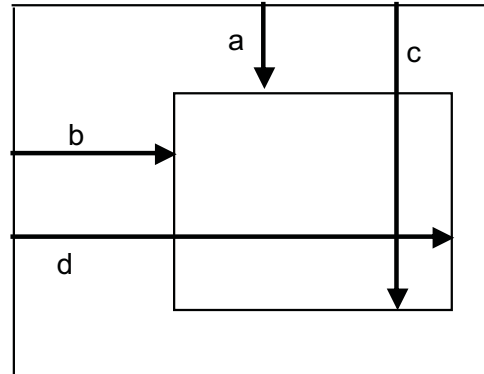
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



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**BARE DIE INFORMATION**

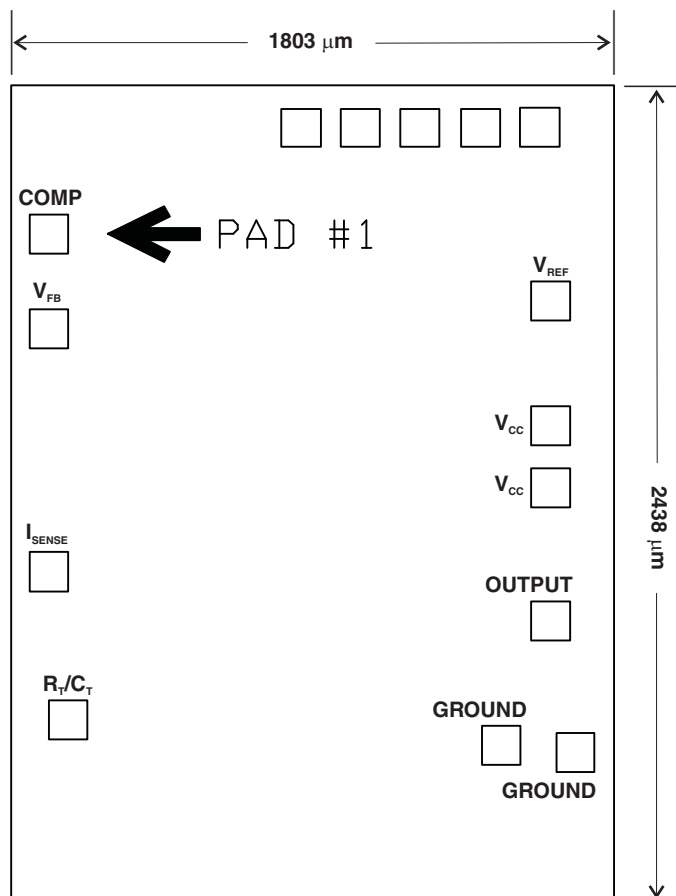
DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	GND	Al-Si-Cu (0.5%)



Origin

**BOND PAD COORDINATES (in Mils)**

DESCRIPTION	PAD NUMBER	a	b	c	d
COMP	1	78.70	63.40	82.90	67.60
V <sub>FB</sub>	2	70.60	63.40	74.80	67.60
I <sub>SENSE</sub>	3	39.40	63.40	43.60	67.60
R <sub>T</sub> /C <sub>T</sub>	4	18.60	61.20	22.60	65.60
GROUND	5	17.80	11.70	22.00	15.90
GROUND	6	17.40	3.90	21.80	8.10
OUTPUT	7	32.60	6.40	36.80	10.60
V <sub>CC</sub>	8	47.50	6.40	51.70	10.60
V <sub>CC</sub>	9	54.60	6.40	58.80	10.60
V <sub>REF</sub>	10	68.70	6.40	72.90	10.60
NC	TESTPAD	87.10	6.30	90.80	10.30
NC	TESTPAD	87.10	12.60	90.80	16.60
NC	TESTPAD	87.10	18.00	90.80	22.00
NC	TESTPAD	87.10	24.30	90.80	28.30
NC	TESTPAD	87.10	30.60	90.80	34.60



**ABSOLUTE MAXIMUM RATINGS**

		<b>UNIT</b>
Supply voltage	Low impedance source	30 V
	$I_{CC} < 30 \text{ mA}$	Self Limiting
Output current		$\pm 1 \text{ A}$
Output energy (capacitive load)		5 $\mu\text{J}$
Analog inputs (Pins 2, 3)		-0.3 V to 6.3 V
Error amp output sink current		10 mA
Storage temperature range		-65°C to 150°C
Junction temperature range		-55°C to 150°C

## ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for  $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ;  $V_{CC} = 15\text{ V}^{(1)}$ ;  $R_T = 10\text{ kW}$ ;  $C_T = 3.3\text{ nF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>REFERENCE SECTION</b>					
Output Voltage	$T_J = 25^{\circ}\text{C}$ , $I_O = 1\text{ mA}$	4.95	5.00	5.05	V
Line Regulation	$12 \leq V_{IN} \leq 25\text{ V}$		6	20	mV
Load Regulation	$1 \leq I_O \leq 20\text{ mA}$		6	25	
Temperature Stability	See <sup>(2)(3)</sup>		0.2	0.4	mV/ $^{\circ}\text{C}$
Total Output Variation	Line, load, tempature <sup>(2)</sup>	4.9		5.1	V
Output Noise Voltage	$10\text{ Hz} \leq f \leq 10\text{ kHz}$ , $T_J = 25^{\circ}\text{C}$ <sup>(2)</sup>		50		$\mu\text{V}$
Long Term Stability	$T_A = 125^{\circ}\text{C}$ , 1000 Hrs <sup>(2)</sup>		5	25	mV
Output Short Circuit		-30	-100	-180	mA
<b>OSCILLATOR SECTION</b>					
Initial Accuracy	$T_J = 25^{\circ}\text{C}$ <sup>(4)</sup>	47	52	57	kHz
Voltage Stability	$12 \leq V_{CC} \leq 25\text{ V}$		0.2%	1%	
Temperature Stability	$T_{MIN} \leq T_A \leq T_{MAX}$ <sup>(2)</sup>		5%		
Amplitude	$V_{PIN\ 4}$ peak-to-peak <sup>(2)</sup>		1.7		V
<b>ERROR AMP SECTION</b>					
Input Voltage	$V_{PIN\ 1} = 2.5\text{ V}$	2.45	2.50	2.55	V
Input Bias Current			-0.3	-1	$\mu\text{A}$
$A_{VOL}$	$2 \leq V_O \leq 4\text{ V}$	65	90		dB
Unity Gain Bandwidth	$T_J = 25^{\circ}\text{C}$ <sup>(2)</sup>	0.7	1		MHz
PSRR	$12 \leq V_{CC} \leq 25\text{ V}$	60	70		dB
Output Sink Current	$V_{PIN\ 2} = 2.7\text{ V}$ , $V_{PIN\ 1} = 1.1\text{ V}$	2	6		mA
Output Source Current	$V_{PIN\ 2} = 2.3\text{ V}$ , $V_{PIN\ 1} = 5\text{ V}$	-0.5	-0.8		
$V_{OUT\ High}$	$V_{PIN\ 2} = 2.3\text{ V}$ , $R_L = 15\text{ k}\Omega$ to ground	5	6		V
$V_{OUT\ Low}$	$V_{PIN\ 2} = 2.7\text{ V}$ , $R_L = 15\text{ k}\Omega$ to Pin 8		0.7	1.1	
<b>CURRENT SENSE SECTION</b>					
Gain	See <sup>(5)(6)</sup>	2.85	3	3.15	V/V
Maximum Input Signal	$V_{PIN\ 1} = 5\text{ V}$ <sup>(5)</sup>	0.9	1	1.1	V
PSRR	$12 \leq V_{CC} \leq 25\text{ V}$ <sup>(2)(5)</sup>		70		dB
Input Bias Current			-2	-10	$\mu\text{A}$
Delay to Output	$V_{PIN\ 3} = 0\text{ V}$ to $2\text{ V}$ <sup>(2)</sup>		150	300	ns
<b>OUTPUT SECTION</b>					
Output Low Level	$I_{SINK} = 20\text{ mA}$		0.1	0.4	V
	$I_{SINK} = 200\text{ mA}$		1.5	2.2	
Output High Level	$I_{SOURCE} = 20\text{ mA}$	13	13.5		
	$I_{SOURCE} = 200\text{ mA}$	12	13.5		
Rise Time	$T_J = 25^{\circ}\text{C}$ , $C_L = 1\text{ nF}$ <sup>(2)</sup>		50	150	ns
Fall Time	$T_J = 25^{\circ}\text{C}$ , $C_L = 1\text{ nF}$ <sup>(2)</sup>		50	150	

(1) Adjust  $V_{CC}$  above the start threshold before setting at 15 V.

(2) These parameters, although specified, are not 100% tested in production.

(3) Temperature stability, sometimes referred to as average temperature coefficient, is described by the equation:

$$\text{Temp Stability} = \frac{V_{REF(\text{max})} - V_{REF(\text{min})}}{T_J(\text{max}) - T_J(\text{min})}$$

$V_{REF(\text{max})}$  and  $V_{REF(\text{min})}$  are the maximum and minimum reference voltages measured over the appropriate temperature range. Note that the extremes in voltage do not necessarily occur at the extremes in temperature.

(4) Output frequency equals oscillator frequency.

(5) Parameter measured at trip point of latch with  $V_{PIN\ 2} = 0$ .

$$A = \frac{\Delta V_{PIN\ 1}}{\Delta V_{PIN\ 3}}, \quad 0 \leq V_{PIN\ 3} \leq 0.8\text{ V}$$

(6) Gain defined as:

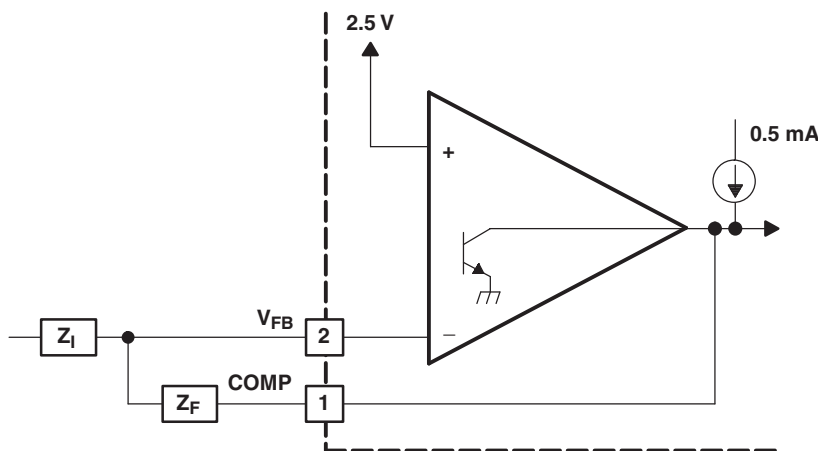
### ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated, these specifications apply for  $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ;  $V_{CC} = 15\text{ V}$ ;  $R_T = 10\text{ kW}$ ;  $C_T = 3.3\text{ nF}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>UNDER-VOLTAGE LOCKOUT SECTION</b>					
Start Threshold		7.8	8.4	9.0	V
Min. Operating Voltage After Turn On		7.0	7.6	8.2	
<b>PWM SECTION</b>					
Maximum Duty Cycle		95%	97%	100%	
Minimum Duty Cycle				0%	
<b>TOTAL STANDBY CURRENT</b>					
Start-Up Current			0.5	1	mA
Operating Supply Current	$V_{PIN\ 2} = V_{PIN\ 3} = 0\text{ V}$		11	17	
$V_{CC}$ Zener Voltager	$I_{CC} = 25\text{ mA}$	30	34		V

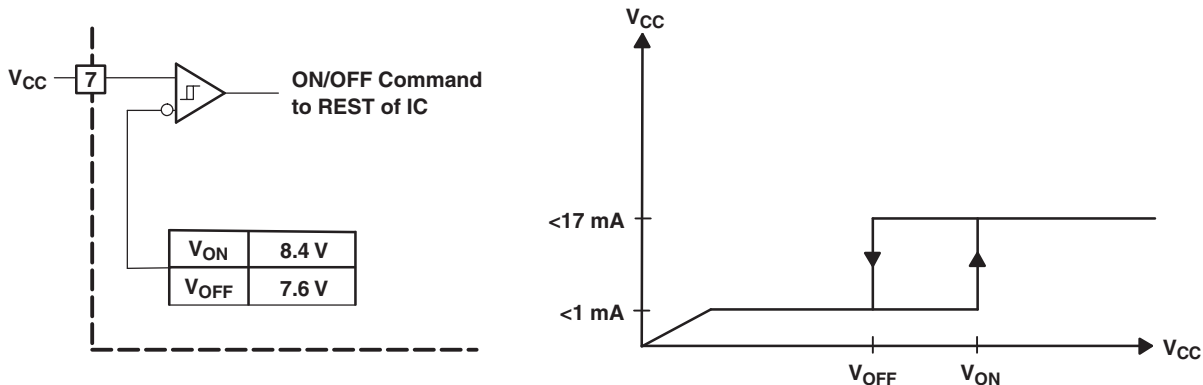
### ERROR AMP CONFIGURATION

Error amp can source or sink up to 0.5 mA.



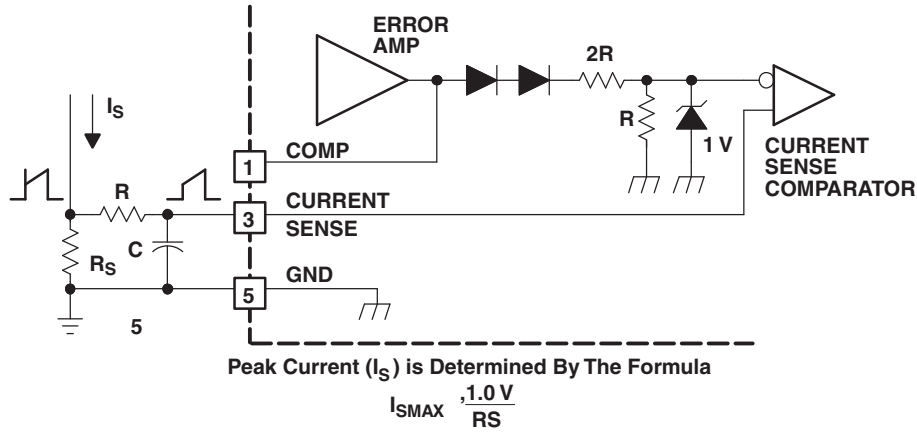
### UNDER-VOLTAGE LOCKOUT

During under-voltage lock-out, the output drive is biased to sink minor amounts of current. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with extraneous leakage currents.

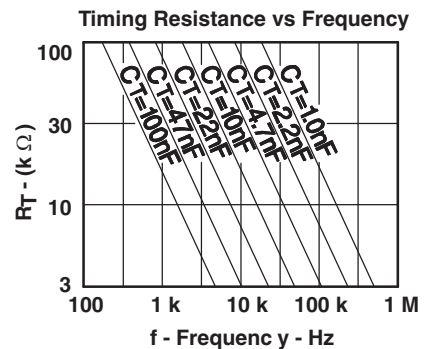
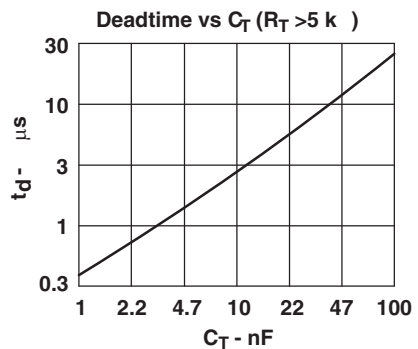
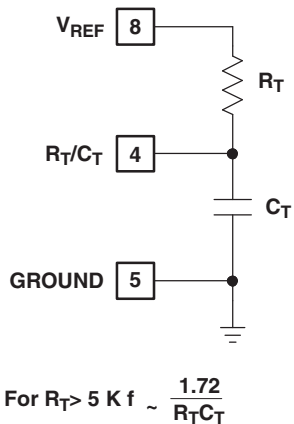


### CURRENT SENSE CIRCUIT

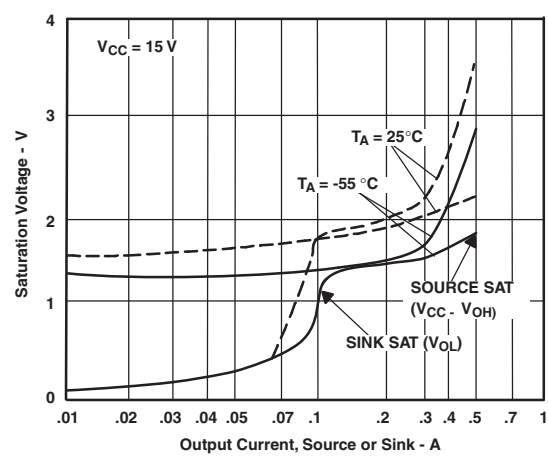
A small RC filter may be required to suppress switch transients.



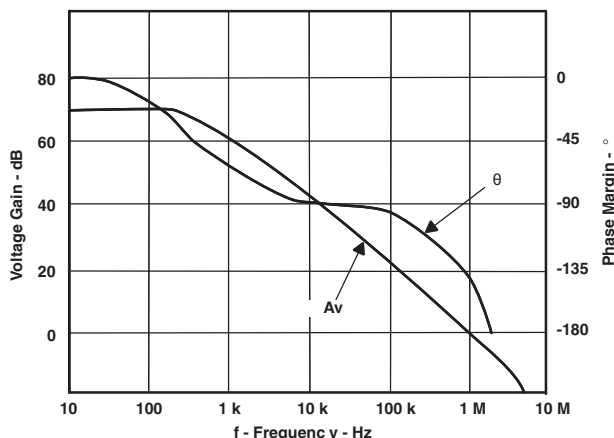
### OSCILLATOR SECTION



### OUTPUT SATURATION CHARACTERISTICS

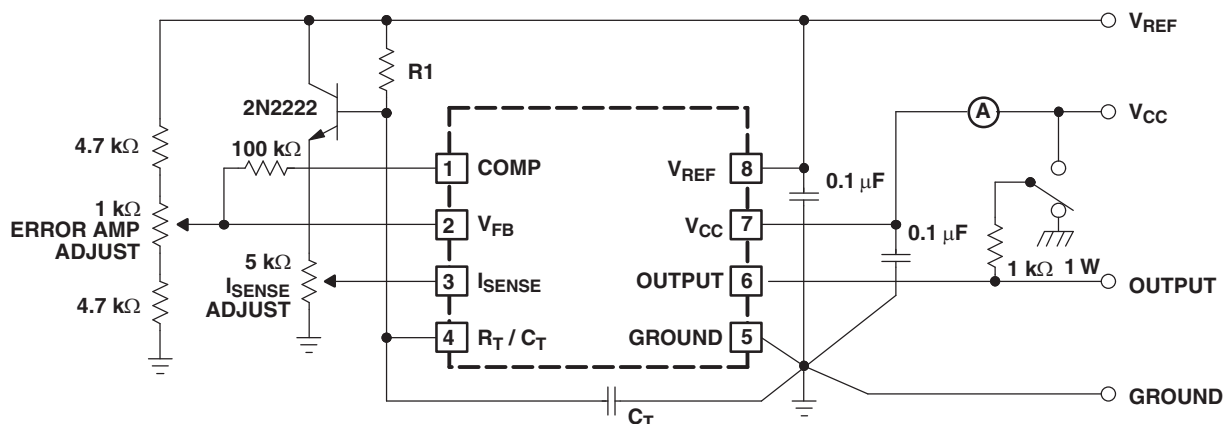


## ERROR AMPLIFIER OPEN-LOOP FREQUENCY RESPONSE



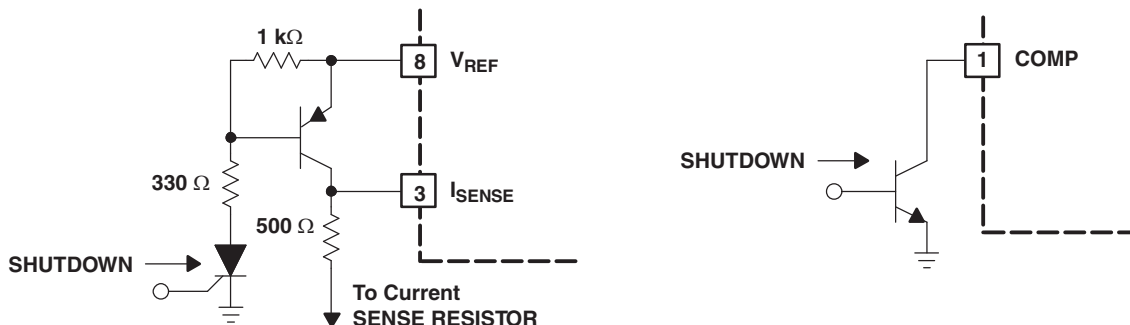
## OPEN-LOOP LABORATORY FIXTURE

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

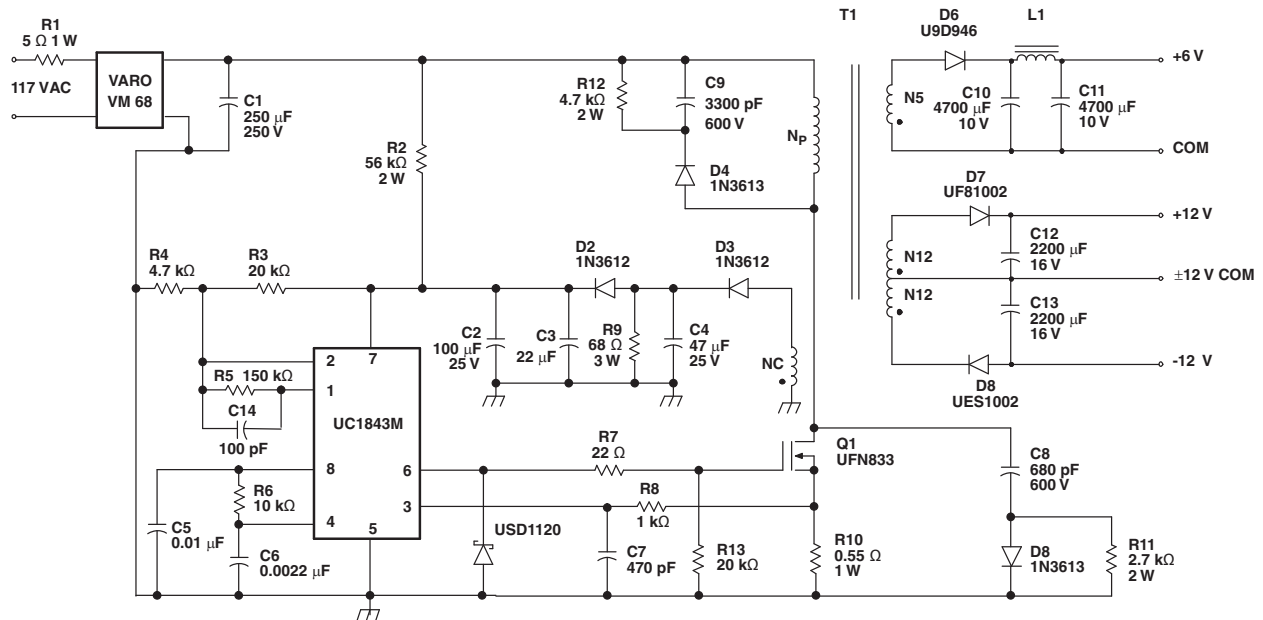


## SHUTDOWN TECHNIQUES

Shutdown of the UC1843 can be accomplished by two methods; either raise pin 3 above 1 V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pin 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SCR which will be reset by cycling  $V_{CC}$  below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.



## OFFLINE FLYBACK REGULATOR

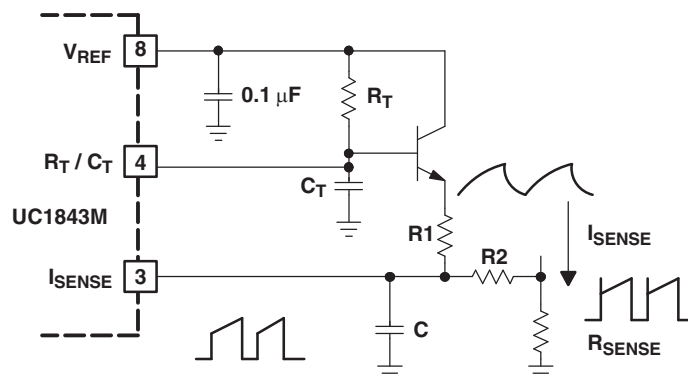


### Power Supply Specifications

1. Input Voltages
  - a. 5VAC to 130VA (50 Hz/60 Hz)
2. Line Isolation: 3750 V
3. Switchng Frequency: 40 kHz
4. Efficiency at Full Load 70%
5. Output Voltage:
  - a. +5 V,  $\pm 5\%$ ; 1A to 4A load  
Ripple voltage: 50 mV P-P Max
  - b. +12 V,  $\pm 3\%$ ; 0.1A to 0.3A load  
Ripple voltage: 100 mV P-P Max
  - c. -12 V,  $\pm 3\%$ ; 0.1A to 0.3A load  
Ripple voltage: 100 mV P-P Max

### SLOPE COMPENSATION

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%.





**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC1843MKGD1	LIFEBUY	XCEPT	KGD	0	100	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF UC1843-HIREL :**

- Space : [UC1843-SP](#)

NOTE: Qualified Version Definitions:

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

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