

## PRECISION MICROPOWER SHUNT VOLTAGE REFERENCE

 Check for Samples: [TL4050-Q1](#)

### FEATURES

- Qualified for Automotive Applications
- Fixed Output Voltages of 2.048 V, 2.5 V, 4.096 V, 5 V
- Tight Output Tolerances and Low Temperature Coefficient
  - Max 0.1%, 50 ppm/°C – A Grade
  - Max 0.2%, 50 ppm/°C – B Grade
  - Max 0.5%, 50 ppm/°C – C Grade
- Low Output Noise: 41  $\mu\text{V}_{\text{RMS}}$  Typ
- Wide Operating Current Range: 60  $\mu\text{A}$  Typ to 15 mA
- Stable With All Capacitive Loads; No Output

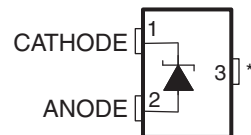
### Capacitor Required

- Available in Extended Temperature Range: –40°C to 125°C

### APPLICATIONS

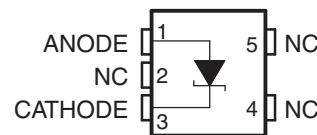
- Data-Acquisition Systems
- Power Supplies and Power-Supply Monitors
- Instrumentation and Test Equipment
- Process Controls
- Precision Audio
- Automotive Electronics
- Energy Management
- Battery-Powered Equipment

DBZ (SOT-23-3) PACKAGE  
(TOP VIEW)



\*Pin 3 is attached to Substrate and must be connected to ANODE or left open.

DCK (SC-70) PACKAGE  
(TOP VIEW)



NC – No internal connection

### DESCRIPTION

The TL4050-Q1 family of shunt voltage references are versatile easy-to-use references suitable for a wide array of applications. The two-terminal fixed-output device requires no external capacitors for operation and is stable with all capacitive loads. Additionally, the reference offers low dynamic impedance, low noise, and low temperature coefficient to ensure a stable output voltage over a wide range of operating currents and temperatures.

The TL4050-Q1 is available in three initial tolerances, ranging from 0.1% (maximum) for the A grade to 0.5% (maximum) for the C grade. Thus, a great deal of flexibility is available to designers in choosing the best cost-to-performance ratio for their applications. Packaged in the space-saving SOT-23-3 and SC-70 packages and requiring a minimum current of 45  $\mu\text{A}$  (typical), the TL4050-Q1 also is ideal for portable applications.

The TL4050x-Q1 characterization is for operation over an ambient temperature range of –40°C to 125°C.

### PACKAGE AND ORDERING INFORMATION

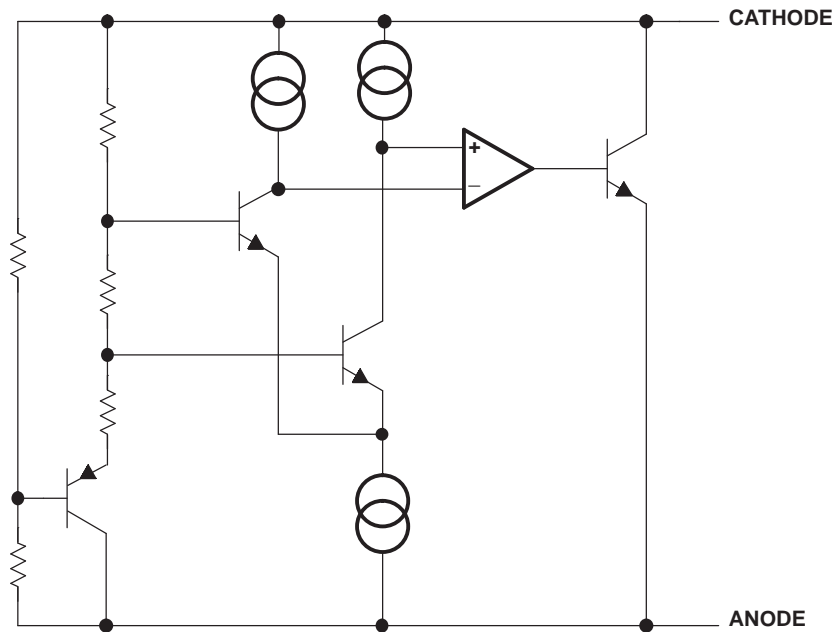
For the most-current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).



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**FUNCTIONAL BLOCK DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$I_Z$	Continuous cathode current	-10	20	mA
$T_J$	Operating virtual junction temperature		150	°C
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>	TL4050-Q1		UNIT
	DBZ	DCK	
	3 PINS	5 PINS	
$\theta_{JA}$ Junction-to-ambient thermal resistance <sup>(2)</sup>	331.1	289.9	°C/W
$\theta_{JcTop}$ Junction-to-case (top) thermal resistance <sup>(3)</sup>	107.5	56.4	°C/W
$\theta_{JB}$ Junction-to-board thermal resistance <sup>(4)</sup>	63.4	93	°C/W
$\psi_{JT}$ Junction-to-top characterization parameter <sup>(5)</sup>	4.9	0.7	°C/W
$\psi_{JB}$ Junction-to-board characterization parameter <sup>(6)</sup>	61.7	91.4	°C/W
$\theta_{JcBot}$ Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT	
$I_Z$	Cathode current	(1)	15	mA	
$T_A$	Free-air temperature	I temperature	-40	85	°C
		Q temperature	-40	125	

- (1) See parametric tables

### TL4050x20-Q1 ELECTRICAL CHARACTERISTICS

at extended temperature range, full range  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$	TL4050A20-Q1			TL4050B20-Q1			TL4050C20-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_Z$	Reverse breakdown voltage $I_Z = 100 \mu\text{A}$	$25^{\circ}\text{C}$	2.048			2.048			2.048			V
$\Delta V_Z$	Reverse breakdown voltage tolerance $I_Z = 100 \mu\text{A}$	$25^{\circ}\text{C}$	-2.048	2.048		-4.096	4.096		-10.24	10.24		mV
		Full range	-12.288	12.288		-14.7456	14.7456		-17.2032	17.2032		
$I_{Z,\text{min}}$	Minimum cathode current	$25^{\circ}\text{C}$	41		60		41		60		$\mu\text{A}$	
		Full range			65				65			
$\alpha_{VZ}$	Average temperature coefficient of reverse breakdown voltage $I_Z = 10 \text{ mA}$	$25^{\circ}\text{C}$	$\pm 20$			$\pm 20$			$\pm 20$			ppm/ $^{\circ}\text{C}$
		$25^{\circ}\text{C}$	$\pm 15$			$\pm 15$			$\pm 15$			
		$25^{\circ}\text{C}$	$\pm 15$			$\pm 15$			$\pm 15$			
		Full range	$\pm 50$			$\pm 50$			$\pm 50$			
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change $I_{Z,\text{min}} < I_Z < 1 \text{ mA}$	$25^{\circ}\text{C}$	0.3	0.8		0.3	0.8		0.3	0.8		mV
		Full range			1.2				1.2			
	$1 \text{ mA} < I_Z < 15 \text{ mA}$	$25^{\circ}\text{C}$	2.3		6		2.3		6			
		Full range			8				8			
$Z_Z$	Reverse dynamic impedance $I_Z = 1 \text{ mA}$ , $f = 120 \text{ Hz}$ , $I_{AC} = 0.1 I_Z$	$25^{\circ}\text{C}$	0.3			0.3			0.3			$\Omega$
$e_N$	Wideband noise $I_Z = 100 \mu\text{A}$ , $10 \text{ Hz} \leq f \leq 10 \text{ kHz}$	$25^{\circ}\text{C}$	34			34			34			$\mu\text{V}_{\text{RMS}}$
	Long-term stability of reverse breakdown voltage $t = 1000 \text{ h}$ , $T_A = 25^{\circ}\text{C} \pm 0.1^{\circ}\text{C}$ , $I_Z = 100 \mu\text{A}$		120			120			120			ppm
$V_{\text{HYST}}$	Thermal hysteresis <sup>(1)</sup> $\Delta T_A = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$		0.7			0.7			0.7			mV

(1) Thermal hysteresis is defined as  $V_{Z,25^{\circ}\text{C}}$  (after cycling to  $-40^{\circ}\text{C}$ ) –  $V_{Z,25^{\circ}\text{C}}$  (after cycling to  $125^{\circ}\text{C}$ ).

**TL4050x25-Q1 ELECTRICAL CHARACTERISTICS**

 at extended temperature range, full range  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$	TL4050B25-Q1			UNIT
			MIN	TYP	MAX	
$V_Z$	Reverse breakdown voltage	$I_Z = 100\ \mu\text{A}$		2.5		V
$\Delta V_Z$	Reverse breakdown voltage tolerance	$I_Z = 100\ \mu\text{A}$			5	mV
		Full range	-5		18	
$I_{Z,\text{min}}$	Minimum cathode current	$I_Z = 100\ \mu\text{A}$		41	60	$\mu\text{A}$
		Full range	-18		65	
$\alpha_{VZ}$	Average temperature coefficient of reverse breakdown voltage	$I_Z = 10\ \text{mA}$	$25^\circ\text{C}$	$\pm 20$		ppm/ $^\circ\text{C}$
		$I_Z = 1\ \text{mA}$	$25^\circ\text{C}$	$\pm 15$		
		$I_Z = 100\ \mu\text{A}$	$25^\circ\text{C}$	$\pm 15$		
		Full range			$\pm 50$	
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,\text{min}} < I_Z < 1\ \text{mA}$	$25^\circ\text{C}$	0.3	0.8	mV
			Full range			
		$1\ \text{mA} < I_Z < 15\ \text{mA}$	$25^\circ\text{C}$	2.3	6	
			Full range			
$Z_Z$	Reverse dynamic impedance	$I_Z = 1\ \text{mA}$ , $f = 120\ \text{Hz}$ , $I_{AC} = 0.1\ I_Z$	$25^\circ\text{C}$	0.3		$\Omega$
$e_N$	Wideband noise	$I_Z = 100\ \mu\text{A}$ , $10\ \text{Hz} \leq f \leq 10\ \text{kHz}$	$25^\circ\text{C}$	41		$\mu\text{V}_{\text{RMS}}$
	Long-term stability of reverse breakdown voltage	$t = 1000\ \text{h}$ , $T_A = 25^\circ\text{C} \pm 0.1^\circ\text{C}$ , $I_Z = 100\ \mu\text{A}$		120		ppm
$V_{\text{HYST}}$	Thermal hysteresis <sup>(1)</sup>	$\Delta T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		0.7		mV

 (1) Thermal hysteresis is defined as  $V_{Z,25^\circ\text{C}}$  (after cycling to  $-40^\circ\text{C}$ ) –  $V_{Z,25^\circ\text{C}}$  (after cycling to  $125^\circ\text{C}$ ).

### TL4050x41-Q1 ELECTRICAL CHARACTERISTICS

at extended temperature range, full range  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$	TL4050B41-Q1			UNIT
			MIN	TYP	MAX	
$V_Z$	Reverse breakdown voltage	$I_Z = 100\ \mu\text{A}$		4.096		V
$\Delta V_Z$	Reverse breakdown voltage tolerance	$I_Z = 100\ \mu\text{A}$	25°C	-8.2	8.2	mV
			Full range	-29	29	
$I_{Z,\text{min}}$	Minimum cathode current		25°C	52	68	$\mu\text{A}$
			Full range		78	
$\alpha_{VZ}$	Average temperature coefficient of reverse breakdown voltage	$I_Z = 10\ \text{mA}$	25°C	$\pm 30$		ppm/°C
		$I_Z = 1\ \text{mA}$	25°C	$\pm 20$		
		$I_Z = 100\ \mu\text{A}$	25°C	$\pm 20$		
			Full range		$\pm 50$	
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,\text{min}} < I_Z < 1\ \text{mA}$	25°C	0.2	0.9	mV
			Full range			
		$1\ \text{mA} < I_Z < 15\ \text{mA}$	25°C	2	7	
			Full range			
$Z_Z$	Reverse dynamic impedance	$I_Z = 1\ \text{mA}$ , $f = 120\ \text{Hz}$ , $I_{AC} = 0.1\ I_Z$	25°C	0.5		$\Omega$
$e_N$	Wideband noise	$I_Z = 100\ \mu\text{A}$ , $10\ \text{Hz} \leq f \leq 10\ \text{kHz}$	25°C	93		$\mu\text{V}_{\text{RMS}}$
	Long-term stability of reverse breakdown voltage	$t = 1000\ \text{h}$ , $T_A = 25^{\circ}\text{C} \pm 0.1^{\circ}\text{C}$ , $I_Z = 100\ \mu\text{A}$		120		ppm
$V_{\text{HYST}}$	Thermal hysteresis <sup>(1)</sup>	$\Delta T_A = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$		1.148		mV

(1) Thermal hysteresis is defined as  $V_{Z,25^{\circ}\text{C}}$  (after cycling to  $-40^{\circ}\text{C}$ ) –  $V_{Z,25^{\circ}\text{C}}$  (after cycling to  $125^{\circ}\text{C}$ ).

**TL4050x50-Q1 ELECTRICAL CHARACTERISTICS**

 at extended temperature range, full range  $T_A = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A$	TL4050A50-Q1			TL4050B50-Q1			TL4050C50-Q1			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$V_Z$	Reverse breakdown voltage	$I_Z = 100\ \mu\text{A}$	25°C			5			5			V
$\Delta V_Z$	Reverse breakdown voltage tolerance	$I_Z = 100\ \mu\text{A}$	25°C			-5			5			mV
			Full range			-30			30			
$I_{Z,\text{min}}$	Minimum cathode current		25°C			56			74			$\mu\text{A}$
			Full range			90			90			
$\alpha_{V_Z}$	Average temperature coefficient of reverse breakdown voltage	$I_Z = 10\ \text{mA}$	25°C			$\pm 30$			$\pm 30$			ppm/°C
		$I_Z = 1\ \text{mA}$	25°C			$\pm 20$			$\pm 20$			
		$I_Z = 100\ \mu\text{A}$	25°C			$\pm 20$			$\pm 20$			
			Full range			$\pm 50$			$\pm 50$			
$\frac{\Delta V_Z}{\Delta I_Z}$	Reverse breakdown voltage change with cathode current change	$I_{Z,\text{min}} < I_Z < 1\ \text{mA}$	25°C			0.2			1			mV
			Full range			1.4			1.4			
		$1\ \text{mA} < I_Z < 15\ \text{mA}$	25°C			2			8			
			Full range			12			12			
$Z_Z$	Reverse dynamic impedance	$I_Z = 1\ \text{mA}$ , $f = 120\ \text{Hz}$ , $I_{AC} = 0.1 I_Z$	25°C			0.5			0.5			$\Omega$
$e_N$	Wideband noise	$I_Z = 100\ \mu\text{A}$ , $10\ \text{Hz} \leq f \leq 10\ \text{kHz}$	25°C			93			93			$\mu\text{V}_{\text{RMS}}$
	Long-term stability of reverse breakdown voltage	$t = 1000\ \text{h}$ , $T_A = 25^{\circ}\text{C} \pm 0.1^{\circ}\text{C}$ , $I_Z = 100\ \mu\text{A}$				120			120			ppm
$V_{\text{HYST}}$	Thermal hysteresis <sup>(1)</sup>	$\Delta T_A = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$				1.4			1.4			mV

 (1) Thermal hysteresis is defined as  $V_{Z,25^{\circ}\text{C}}$  (after cycling to  $-40^{\circ}\text{C}$ ) –  $V_{Z,25^{\circ}\text{C}}$  (after cycling to  $125^{\circ}\text{C}$ ).

TYPICAL CHARACTERISTICS

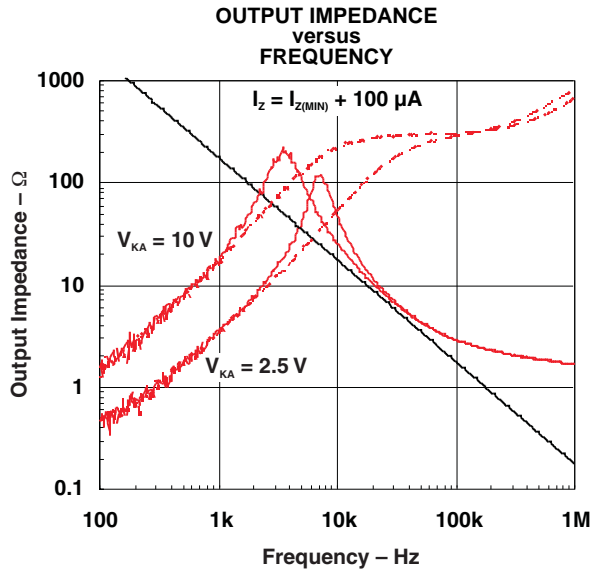


Figure 1.

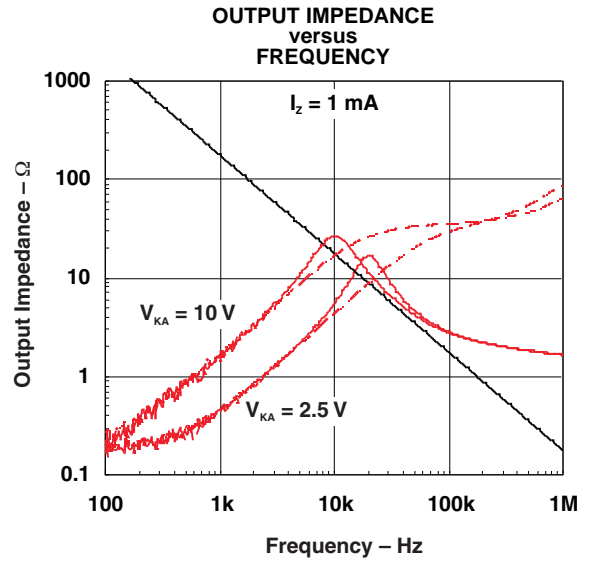


Figure 2.

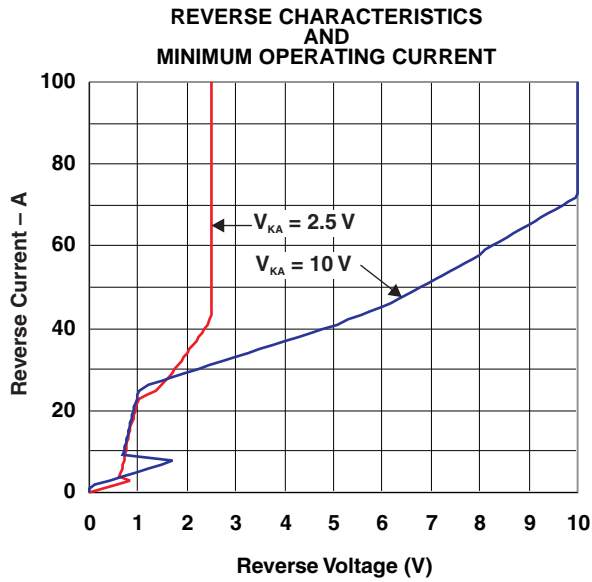


Figure 3.

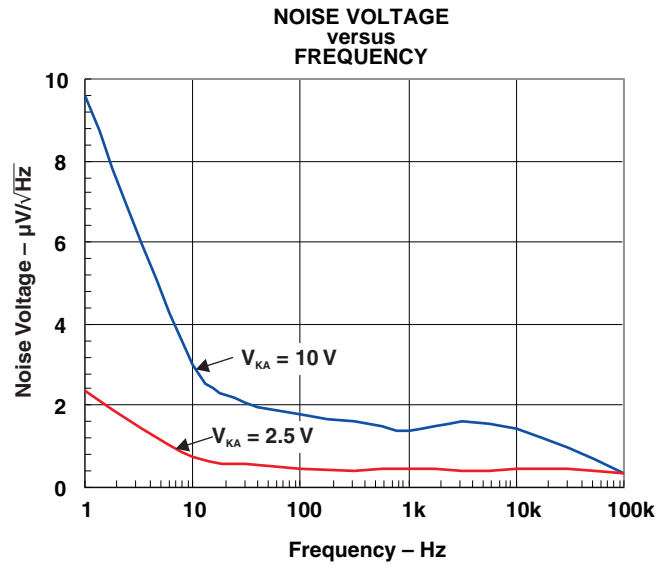


Figure 4.



**TYPICAL CHARACTERISTICS (continued)**

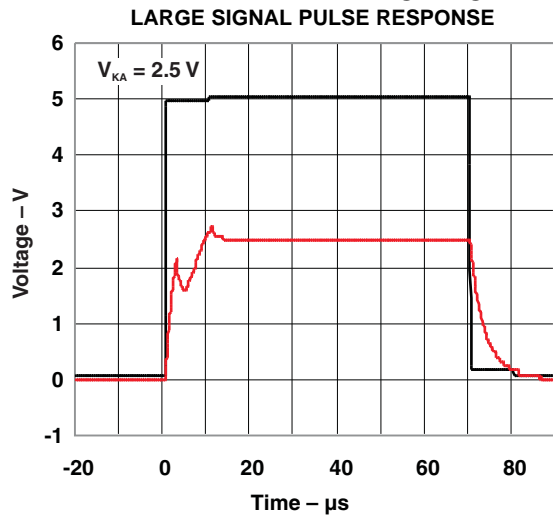


Figure 5.

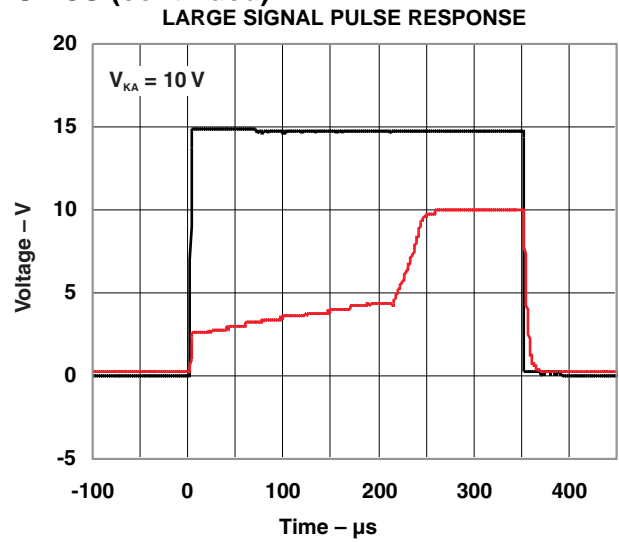
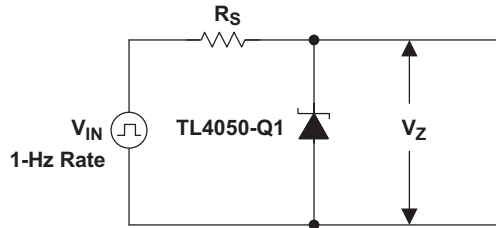


Figure 6.

**APPLICATION INFORMATION**



**Figure 7. Start-Up Test Circuit**

**Output Capacitor**

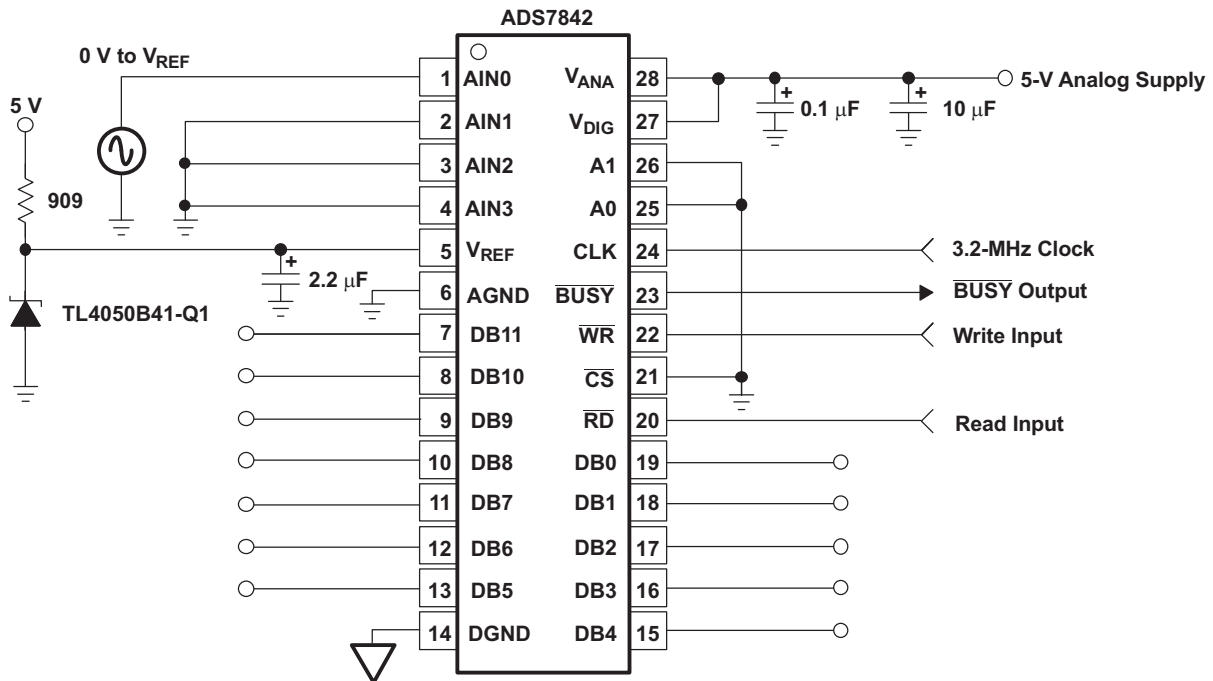
The TL4050-Q1 does not require an output capacitor across cathode and anode for stability. However, in an application using an output bypass capacitor, the TL4050-Q1 is stable with all capacitive loads.

**SOT-23-3 Pin Connections**

There is a parasitic Schottky diode connected between pins 2 and 3 of the SOT-23-3 packaged device. Thus, pin 3 of the SOT-23-3 package must be left floating or connected to pin 2.

**Use With ADCs or DACs**

The design of the TL4050x41-Q1 is as a cost-effective voltage reference, as required in 12-bit data-acquisition systems. For 12-bit systems operating from 5-V supplies, such as the ADS7842 (see Figure 8), the TL4050x41-Q1 (4.096 V) permits operation with an LSB of 1 mV.



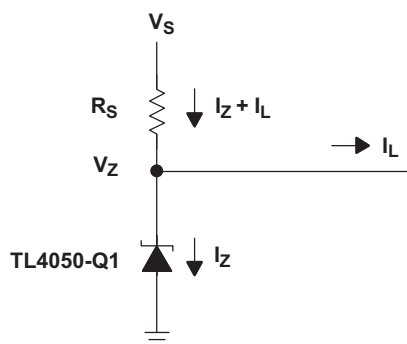
**Figure 8. Data-Acquisition Circuit With TL4050x41-Q1**

## Cathode and Load Currents

In a typical shunt-regulator configuration (see [Figure 9](#)), an external resistor,  $R_S$ , connects between the supply and the cathode of the TL4050-Q1. Proper choice of  $R_S$  is essential, as  $R_S$  sets the total current available to supply the load ( $I_L$ ) and bias the TL4050-Q1 ( $I_Z$ ). In all cases,  $I_Z$  must stay within a specified range for proper operation of the reference. Taking into consideration one extreme in the variation of the load and supply voltage (maximum  $I_L$  and minimum  $V_S$ ),  $R_S$  must be small enough to supply the minimum  $I_Z$  required for operation of the regulator, as given by data-sheet parameters. At the other extreme, maximum  $V_S$  and minimum  $I_L$ ,  $R_S$  must be large enough to limit  $I_Z$  to less than its maximum-rated value of 15 mA.

[Equation 1](#) calculates  $R_S$ :

$$R_S = \frac{(V_S - V_Z)}{(I_L + I_Z)} \quad (1)$$



**Figure 9. Shunt Regulator**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL4050A50QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLGU	<a href="#">Samples</a>
TL4050A50QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7GU	<a href="#">Samples</a>
TL4050B25QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLHU	<a href="#">Samples</a>
TL4050B25QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7HU	<a href="#">Samples</a>
TL4050B41QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMXU	<a href="#">Samples</a>
TL4050B50QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLJU	<a href="#">Samples</a>
TL4050B50QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	7JU	<a href="#">Samples</a>
TL4050C20QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMYU	<a href="#">Samples</a>
TL4050C50QDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TKZU	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL4050A50QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050A50QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL4050B25QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050B25QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL4050B41QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050B50QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050B50QDCKRQ1	SC70	DCK	5	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TL4050C20QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
TL4050C50QDBZRQ1	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL4050A50QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050A50QDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
TL4050B25QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050B25QDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
TL4050B41QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050B50QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050B50QDCKRQ1	SC70	DCK	5	3000	200.0	183.0	25.0
TL4050C20QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0
TL4050C50QDBZRQ1	SOT-23	DBZ	3	3000	200.0	183.0	25.0

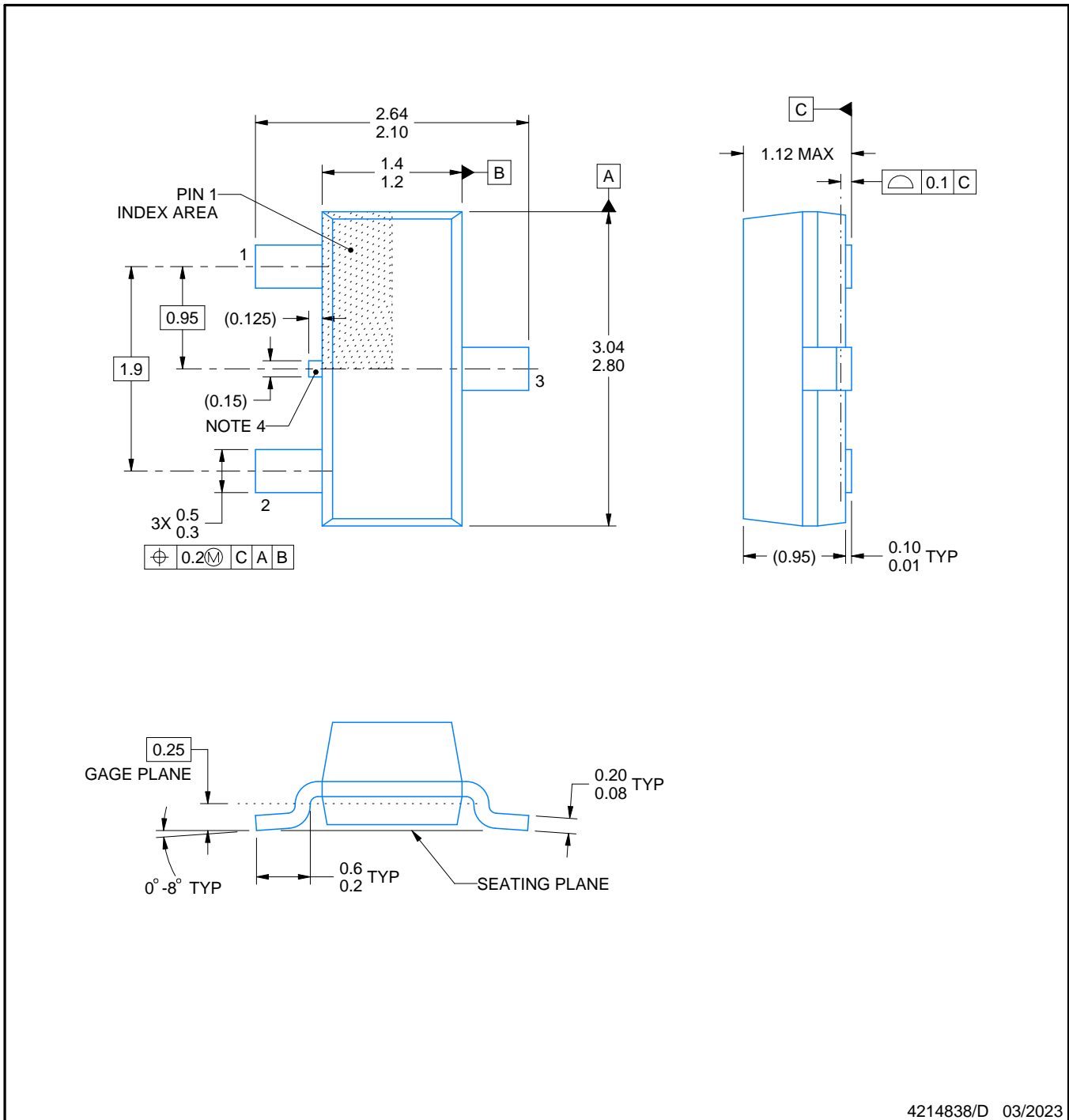
# DBZ0003A



# PACKAGE OUTLINE

## SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.

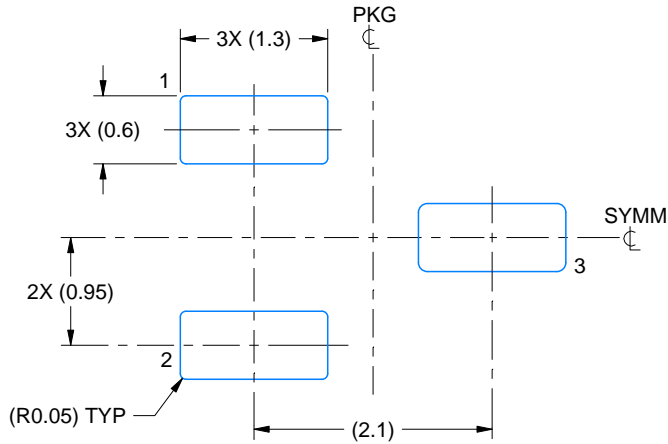


# EXAMPLE BOARD LAYOUT

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS

4214838/D 03/2023

NOTES: (continued)

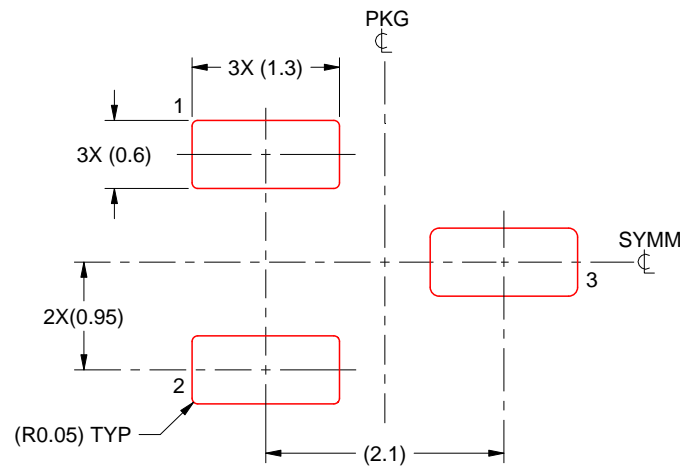
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

# DCK0005A



## PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/D 07/2023

### NOTES:

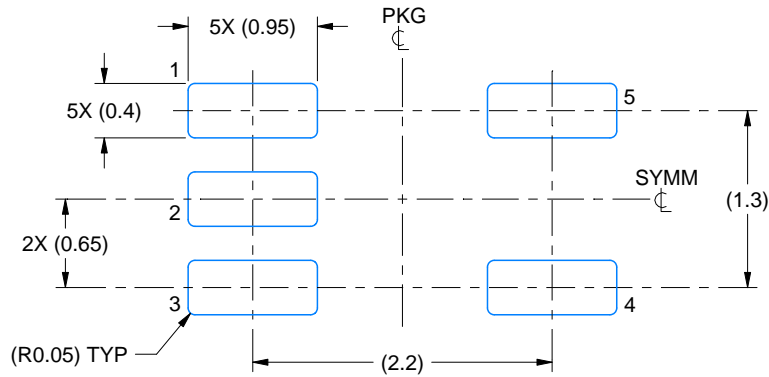
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.

# EXAMPLE BOARD LAYOUT

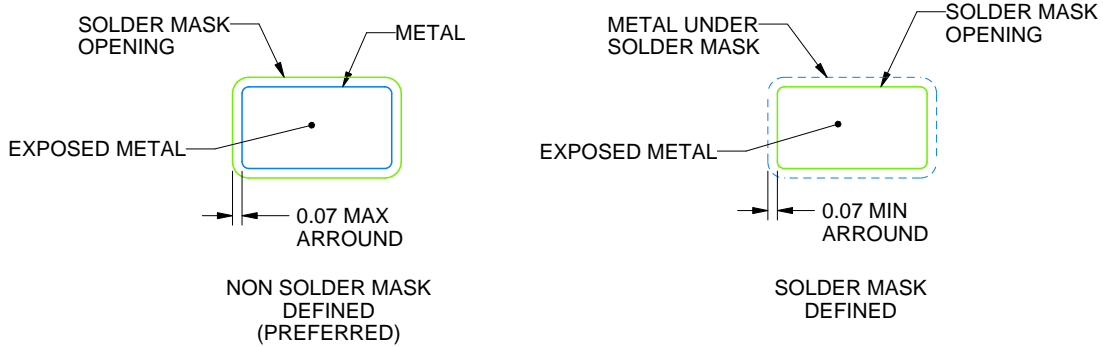
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

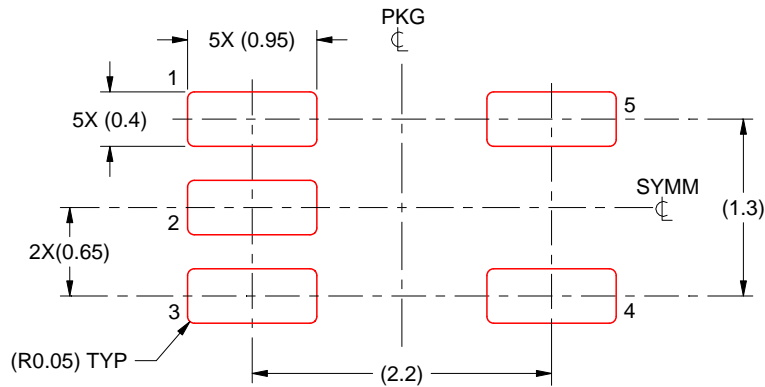
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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