TPS715-Q1 50-mA, 24-V, 3.2-µA Quiescent Current Low-Dropout Linear Regulators in SC70 Package

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
  - Device HBM ESD classification level H2
  - Device CDM ESD classification level C4B for legacy chip and C5 for new chip
- Input voltage range: 2.5 V to 24 V
- Available output voltage options:
  - Fixed: 1.8 V to 5 V
  - Adjustable: 1.2 V to 15 V
- Output current: Up to 50 mA
- Very low I_Q: 3.2 µA at 50-mA load current
- Stable with output capacitor ≥ 0.47 µF
- Overcurrent protection
- Package: 5-pin SC70 (DCK)

2 Applications

- Hybrid, electric, and powertrain systems
- Body electronics and lighting
- Infotainment and clusters
- Factory automation and control

3 Description

The TPS715-Q1 low-dropout (LDO) linear voltage regulator is a low quiescent current device that offers the benefits of a wide input voltage range and low-power operation in miniaturized packaging. Thus, the TPS715-Q1 is designed for battery-powered applications and as a power-management attachment to low-power microcontrollers.

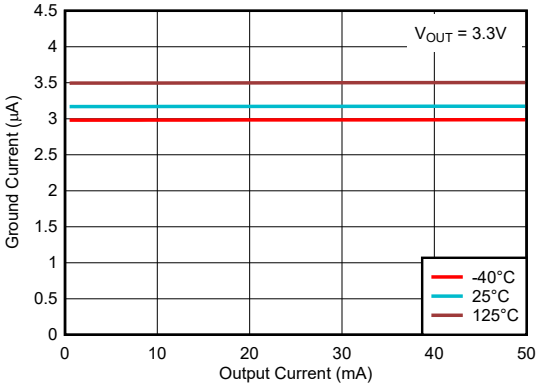
The TPS715-Q1 is available in both fixed and adjustable versions. For more flexibility or higher output voltages, the adjustable version uses feedback resistors to set the output voltage from 1.2 V to 15 V. The TPS715-Q1 LDO supports a low dropout of typically 415 mV at 50 mA of load current. The low quiescent current (3.2 µA typically) is stable over the entire range of output load current (0 mA to 50 mA). The TPS715-Q1 also features an internal soft-start to lower the inrush current. The built-in overcurrent limit helps protect the regulator in the event of a load short or fault.

The TPS715-Q1 is available in a 2.00 mm × 1.25 mm, 5-pin SC-70 (DCK) package for fixed and adjustable outputs.

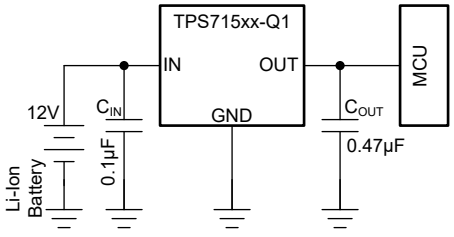
Package Information

PART NUMBER	PACKAGE(1) (2)	BODY SIZE (NOM)
TPS715-Q1	DCK (SC70, 5)	2.00 mm × 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Contact Texas Instruments for other voltage options between 1.8 V and 5.0 V.



Quiescent Current vs Load Current for the TPS715-Q1 (New Chip Only)



Typical Application Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (October 2015) to Revision I (May 2023)	Page
• Added M3 devices to document	1
• Changed document title and *Features*, *Applications*, and *Description* sections	1
• Changed *Pin Configuration and Functions* section: Added fixed and adjustable pinouts and changed *Description* column of *Pin Functions* table	3
• Changed *Typical Characteristics* section: Reordered curves and added M3-specific curves	7
• Changed *Overview* section	11
• Changed *Feature Description*: Added new subsections, deleted *Regulator Protection* and *Adjustable Output Voltage* sections, changed *Current Limit* section	11
• Changed *Device Functional Modes* section: Deleted *Disabled* row from *Device Functional Mode Comparison* table and changed *Dropout Operation* section	13
• Changed *Application Information* section	14
• Changed *Typical Application Circuit (Fixed-Voltage Version)* figure and added *TPS71501 Adjustable LDO Regulator Programming* figure	14
• Changed *Detailed Design Procedure* section: Added subsections, changed *External Capacitor Requirements* section	14
• Added M3-specific curves to *Application Curves* section	17
• Added *Device Support* and *Documentation Support* sections	20

Changes from Revision G (July 2013) to Revision H (October 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation*section, *Power Supply Recommendations*section, *Layout*section, *Device and Documentation Support*section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

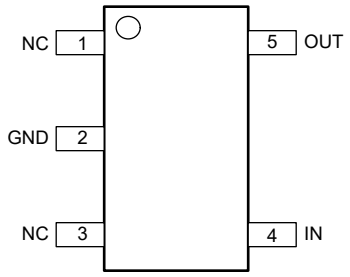


Figure 5-1. DCK Package (Fixed), 5-Pin SC70 (Top View)

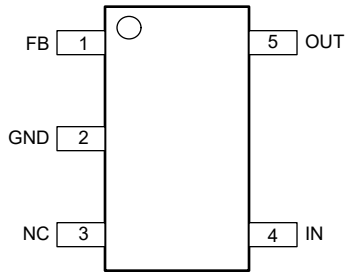


Figure 5-2. DCK Package (Adjustable), 5-Pin SC70 (Top View)

Table 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SC70			
	FIXED	ADJ.		
FB		1	Input	In the adjustable configuration, this pin sets the output voltage with the help of the feedback divider.
NC	1		NC	No connect pin. This pin is not connected internally. Connect this pin to ground for best thermal performance or leave floating.
GND	2	2	GND	Ground pin.
NC	3	3	NC	No connect pin. This pin is not connected internally. Connect this pin to ground for best thermal performance or leave floating.
IN	4	4	Input	Input supply pin. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Requirements* section for more information.
OUT	5	5	Output	Output of the regulator. See the *Recommended Operating Conditions* table and the *Input and Output Capacitor Requirements* section for more information.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Voltage	V_{IN} (for legacy chip only)	–0.3	24	V
	V_{IN} (for new chip only)	–0.3	30	
	V_{OUT} (for fixed output new chip only)	–0.3	2 × $V_{OUT(typ)}$ or V_{IN} + 0.3 or 5.5 (whichever is lower)	
Current	Peak output current	Internally limited		
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE (legacy chip)	VALUE (new chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	±3000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	±1500	
			Corner pins (1, 3, 4, and 5)	±700		

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.5		24	V
C_{IN}	Input capacitor(2)	0	0.047		µF
C_{OUT}	Output capacitor (for legacy chip only)	0.47	1		
	Output capacitor (for new chip only) (3)	1			
T_J	Operating junction temperature	-40		125	°C

(1) All voltages are with respect to GND.
(2) An input capacitor is not required for LDO stability. However, an input capacitor with an effective value of 0.047 µF is recommended to counteract the effect of source resistance and inductance, which may in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.
(3) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 0.47 µF minimum for the stability.

Thermal Information

THERMAL METRIC (1)		Legacy Chip (2) DCK (SC-70) 5 PINS	New Chip (2) DCK (SC-70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	253.8	195.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.7	88.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	84.6	40.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	11.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	83.9	40.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC package thermal metrics application report.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB config. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application report.

6.4 Electrical Characteristics

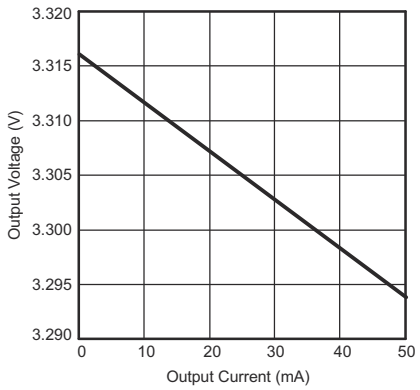
over operating junction temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 1 V, I_{OUT} = 1 mA, and C_{OUT} = 1 µF (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage (1)	I_O = 10 mA	2.5		24	V
		I_O = 50 mA	3		24	
V_{OUT}	Output voltage range (TPS71501)		1.205		15	V
	Output voltage accuracy (1) (2)	V_{OUT} + 1 V ≤ V_{IN} ≤ 24 V, 100 µA ≤ I_{OUT} ≤ 50 mA	–4		4	%
I_{GND}	Ground pin current (legacy chip)(3)	0 ≤ I_{OUT} ≤ 50 mA , T_J = –40°C to 85°C		3.2	4.2	µA
		0 mA ≤ I_{OUT} ≤ 50 mA		3.2	4.8	
		0 mA ≤ I_{OUT} ≤ 50 mA , V_{IN} = 24 V			5.8	
	Ground pin current (new chip) (3)	0 ≤ I_{OUT} ≤ 50 mA , T_J = –40°C to 85°C		3.2	4.1	
		0 mA ≤ I_{OUT} ≤ 50 mA		3.2	4.3	
		0 mA ≤ I_{OUT} ≤ 50 mA , V_{IN} = 24 V			4.5	
$\Delta V_{OUT\ (\Delta IOUT)}$	Load regulation	I_{OUT} = 100 µA to 50 mA		22		mV
$\Delta V_{OUT\ (\Delta VIN)}$	Output voltage line regulation (legacy chip) (1)	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 24 V		20	60	mV
	Output voltage line regulation (new chip) (1)	$V_{OUT(NOM)}$ + 1 V ≤ V_{IN} ≤ 24 V		20	22	
V_n	Output noise voltage (legacy chip) (4)	BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		575		µVrms
	Output noise voltage (new chip)(4)	BW = 200 Hz to 100 kHz, C_{OUT} = 10 µF, I_{OUT} = 50 mA		425		
I_{CL}	Output current limit (legacy chip)	V_{OUT} = 0 V, V_{IN} ≥ 3.5 V	125		750	mA
		V_{OUT} = 0 V, V_{IN} < 3.5 V	90		750	
	Output current limit (new chip)	V_{OUT} = 0 V, V_{IN} ≥ 3.5 V	125		350	
		V_{OUT} = 0 V, V_{IN} < 3.5 V	90		350	
PSRR	Power-supply ripple rejection	f = 100 kHz, C_{OUT} = 10 µF		60		dB
V_{DO}	Dropout voltage (legacy chip)	I_{OUT} = 50 mA, V_{IN} = $V_{OUT(nom)}$ – 0.1 V		415	750	mV
	Dropout voltage (new chip)			415	525	

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or the value shown for *Input voltage* in this table, whichever is greater.
(2) For adjustable device, output accuracy excludes the tolerance and mismatch associated with external resistors used for setting up the output voltage level.
(3) This device employs a leakage null control circuit. This circuit is active only if output current is less than pass transistor leakage current. The circuit is typically active when output load is less than 5 µA, V_{IN} is greater than 18 V, and die temperature is greater than 100°C.
(4) See *Device nomenclature* for details about new and legacy chip descriptions.

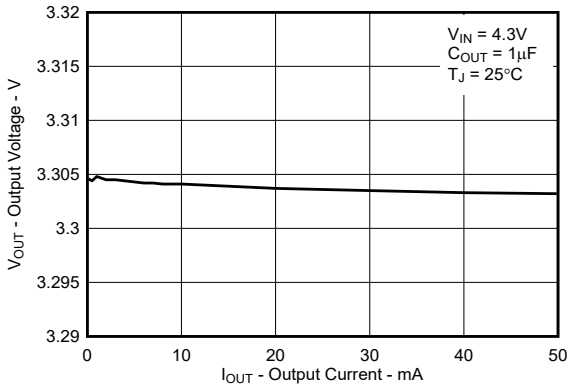
6.5 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



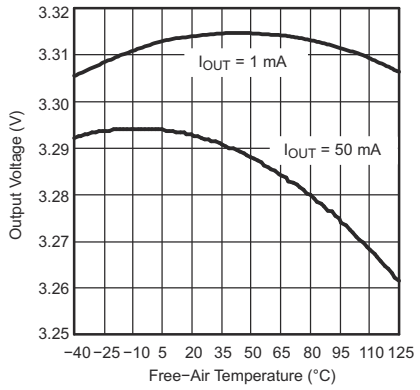
V_{IN} = 4.3 V, C_{OUT} = 1 µF, T_J = 25°C

Figure 6-1. Output Voltage vs Output Current for Legacy Chip



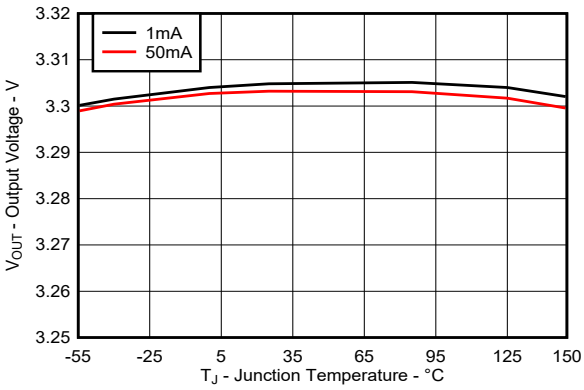
V_{IN} = 4.3 V, C_{OUT} = 1 µF, T_J = 25°C

Figure 6-2. Output Voltage vs Output Current for New Chip



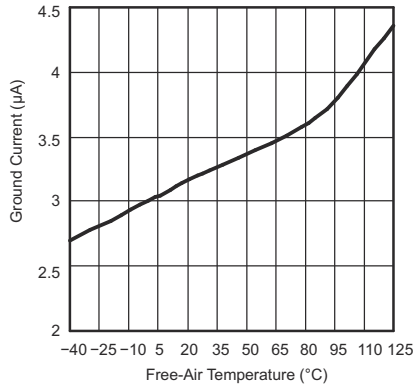
V_{IN} = 4.3 V, C_{OUT} = 1 µF

Figure 6-3. Output Voltage vs Free-Air Temperature for Legacy Chip



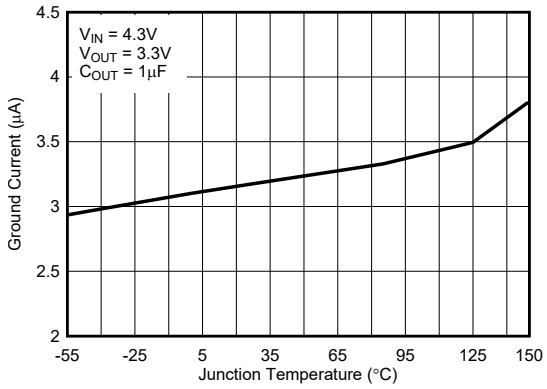
V_{IN} = 4.3 V, C_{OUT} = 1 µF

Figure 6-4. Output Voltage vs Free-Air Temperature for New Chip



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, I_{OUT} = 1 µF

Figure 6-5. Quiescent Current vs Free-Air Temperature for Legacy Chip

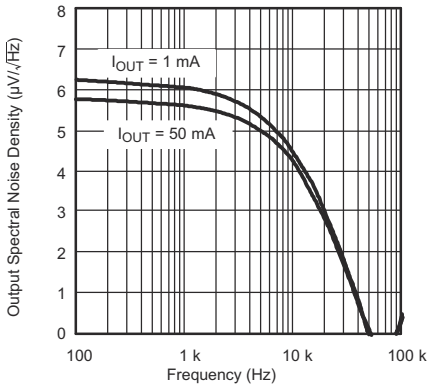


V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF

Figure 6-6. Quiescent Current vs Free-Air Temperature for New Chip

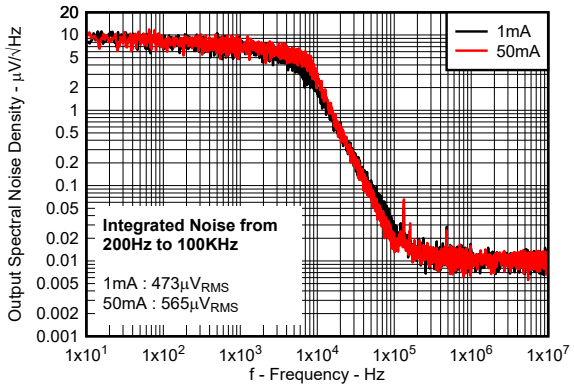
6.5 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



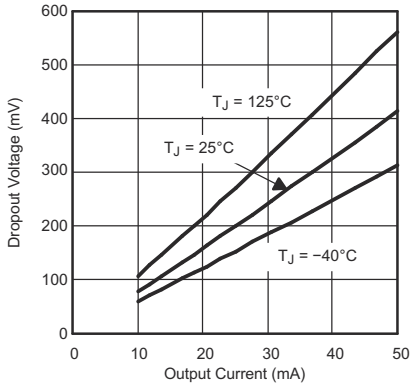
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF

Figure 6-7. Output Spectral Noise Density vs Frequency for Legacy Chip



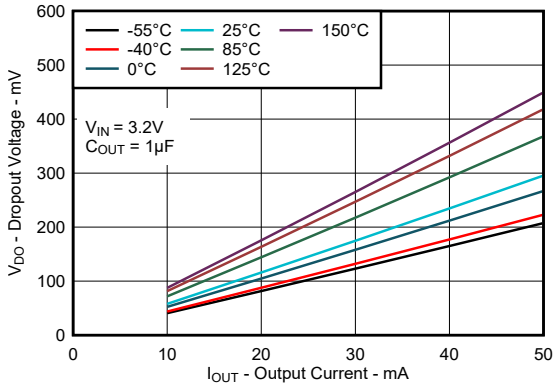
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF

Figure 6-8. Output Spectral Noise Density vs Frequency for New Chip



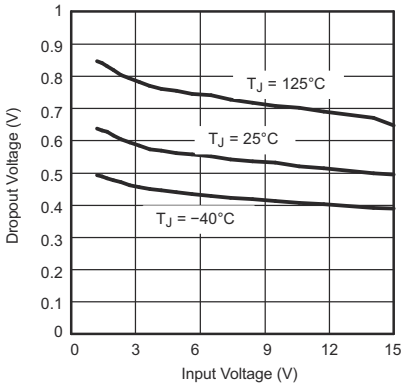
V_{IN} = 3.2 V, C_{OUT} = 1 µF

Figure 6-9. Dropout Voltage vs Output Current for Legacy Chip



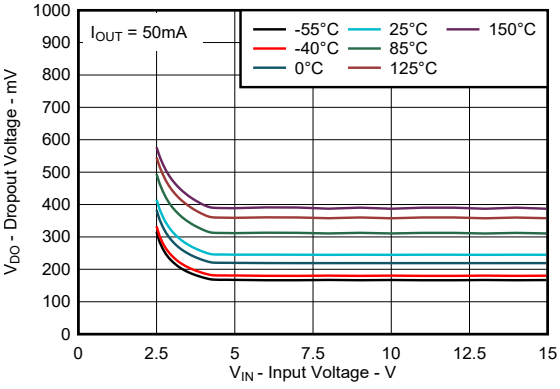
V_{IN} = 3.2 V, C_{OUT} = 1 µF

Figure 6-10. Dropout Voltage vs Output Current for New Chip



I_{OUT} = 50 mA

Figure 6-11. TPS71501 Dropout Voltage vs Input Voltage for Legacy Chip

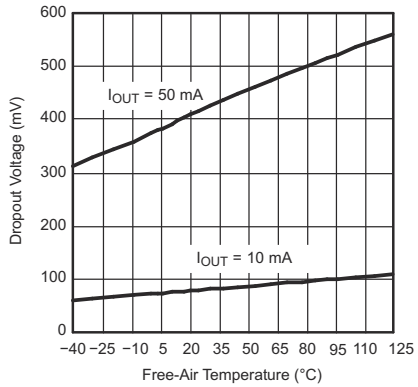


I_{OUT} = 50 mA

Figure 6-12. TPS71501 Dropout Voltage vs Input Voltage for New Chip

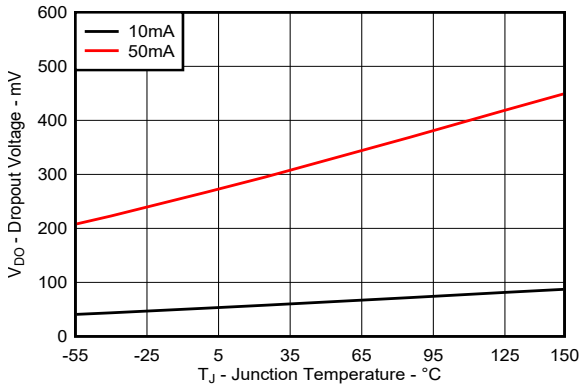
6.5 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



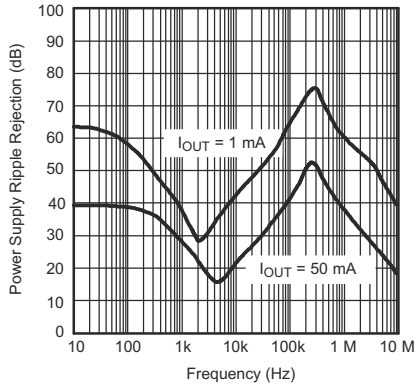
V_{IN} = 3.2 V

Figure 6-13. Dropout Voltage vs Free-Air Temperature for Legacy Chip



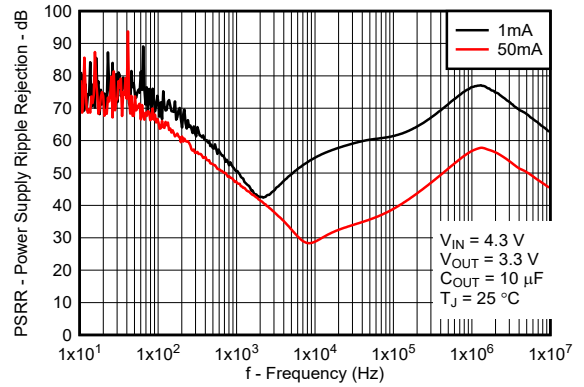
V_{IN} = 3.2 V

Figure 6-14. Dropout Voltage vs Free-Air Temperature for New Chip



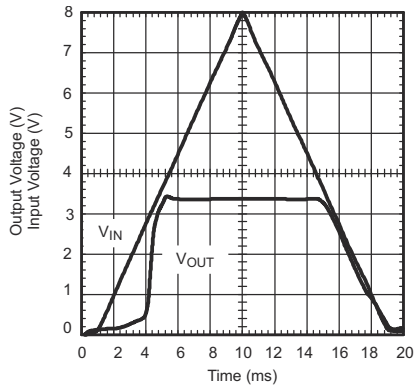
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF, T_J = 25°C

Figure 6-15. Power-Supply Ripple Rejection vs Frequency for Legacy Chip



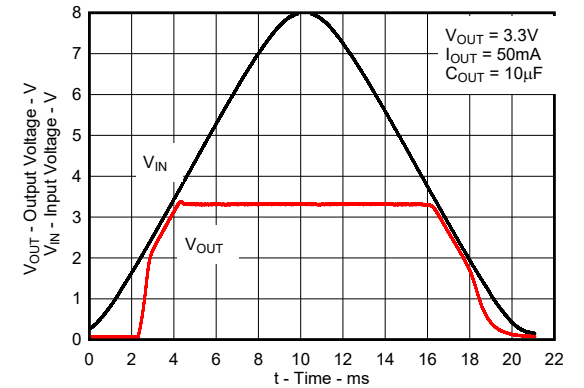
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF, T_J = 25°C

Figure 6-16. Power-Supply Ripple Rejection vs Frequency for New Chip



V_{OUT} = 3.3 V, R_L = 66 Ω, C_{OUT} = 10 µF

Figure 6-17. Power-Up and Power-Down for Legacy Chip

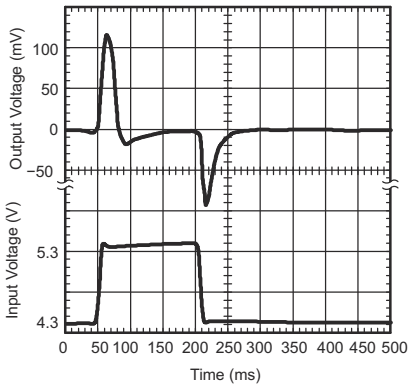


V_{OUT} = 3.3 V, R_L = 66 Ω, C_{OUT} = 10 µF

Figure 6-18. Power-Up and Power-Down for New Chip

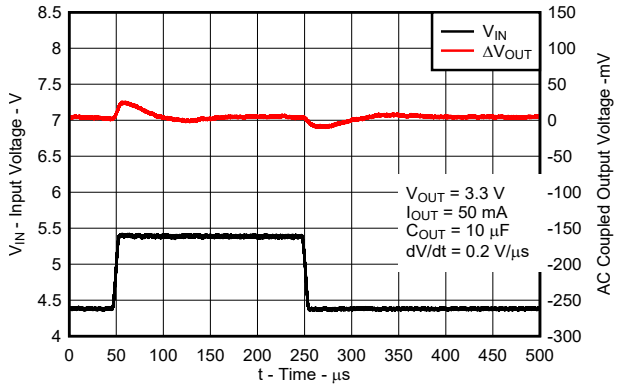
6.5 Typical Characteristics (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1mA, C_{IN} = 1 µF, and C_{OUT} = 1 µF (unless otherwise noted)



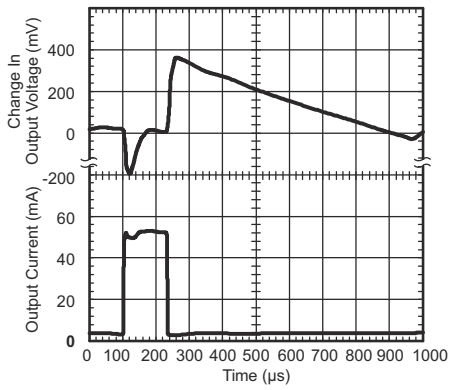
V_{OUT} = 3.3 V, I_{OUT} = 50 mA, C_{OUT} = 10 µF

Figure 6-19. Line Transient Response for Legacy Chip



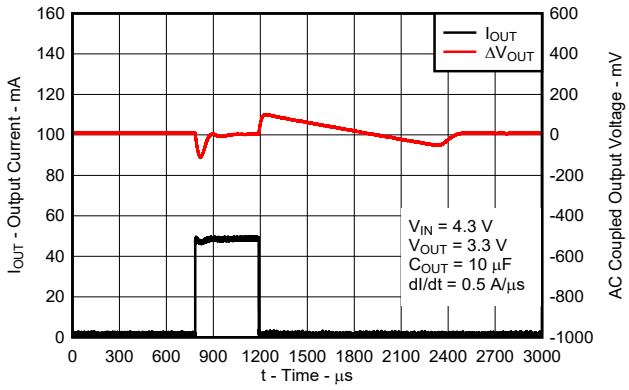
V_{OUT} = 3.3 V, I_{OUT} = 50 mA, C_{OUT} = 10 µF

Figure 6-20. Line Transient Response for New Chip



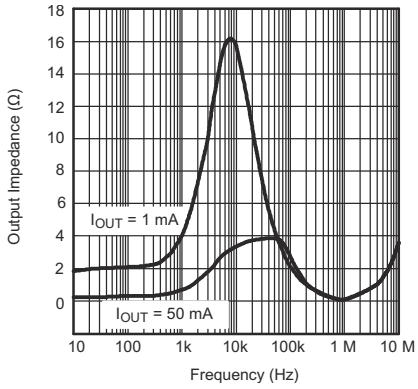
V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF

Figure 6-21. Load Transient Response for Legacy Chip



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 10 µF

Figure 6-22. Load Transient Response for New Chip



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF, T_J = 25°C

Figure 6-23. Output Impedance vs Frequency for Legacy Chip

7 Detailed Description

7.1 Overview

The TPS715-Q1 low-dropout regulator (LDO) consumes only 3.2 µA (typ) of quiescent current across the entire output current range, while offering a wide input voltage range and low-dropout voltage in small packaging. The device, which operates over an input range of 2.5 V to 24 V, is stable with any output capacitor greater than or equal to 0.47 µF. The low quiescent current across the complete load current range makes the TPS715-Q1 optimal for powering battery-operated applications. The TPS715-Q1 has internal soft-start to control inrush current into the output capacitor. This LDO also has overcurrent protection during a load-short or fault condition on the output.

7.2 Functional Block Diagrams

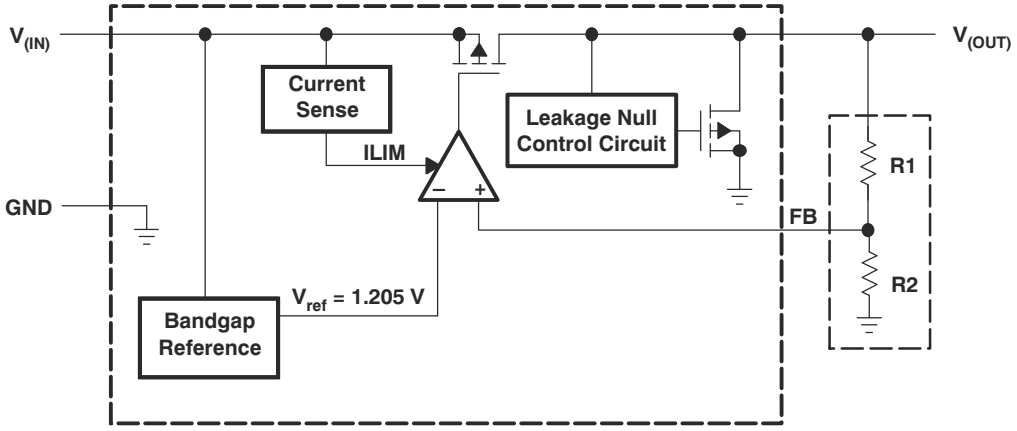


Figure 7-1. Functional Block Diagram—Adjustable Version

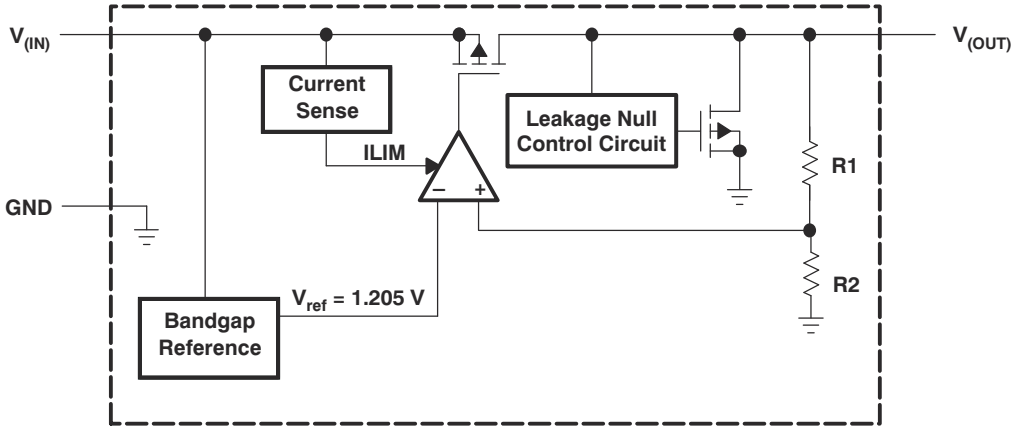


Figure 7-2. Functional Block Diagram—Fixed Version

7.3 Feature Description

7.3.1 Wide Supply Range

The TPS715-Q1 has an operational input supply range of 2.5 V to 24 V, allowing for a wide range of applications. This wide supply range is designed for applications that have either large transients or high DC voltage supplies.

7.3.2 Low Quiescent Current

The TPS715-Q1 only requires 3.2 µA (typical) of quiescent current across the complete load current range (0 mA to 50 mA) from –40°C to +125°C.

7.3.3 Dropout Voltage (V_{DO})

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} – V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. In dropout operation, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the value required to maintain output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source, on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use Equation 1 to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

7.3.4 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [($V_{IN} – V_{OUT}$) × I_{CL}]. For more information on current limits, see the *Know Your Limits* application note.

Figure 7-3 shows a diagram of the current limit.

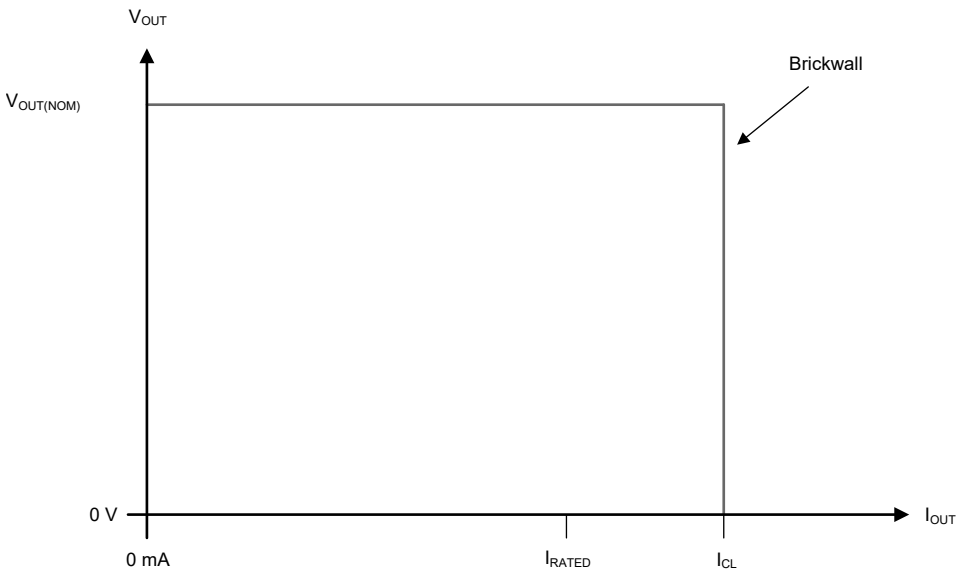


Figure 7-3. Current Limit

7.4 Device Functional Modes

Table 7-1 provides a quick comparison between the normal and dropout modes of operation.

Table 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER	
	V_{IN}	I_{OUT}
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{CL}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is greater than –40°C and less than +125°C

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start-up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS715-Q1 LDO regulator is designed for battery-powered applications and is a good supply for low-power microcontrollers (such as the MSP430) because of the device low I_Q performance across load current range. The ultra-low-supply current of the TPS715-Q1 maximizes efficiency at light loads, and the high input voltage range and flexibility of output voltage selection in the adjustable configuration and fixed output levels makes the device an optimal supply for infotainment and cluster systems and body electronics in automotive applications.

8.2 Typical Application

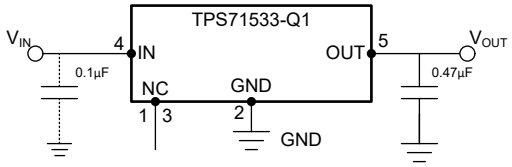
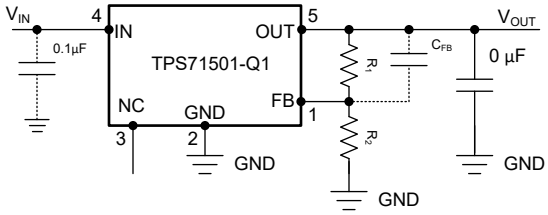


Figure 8-1. Typical Application Circuit (Fixed-Voltage Version)



Output Voltage	R1	R2
1.8V	0.499 MΩ	1MΩ
2.8V	1.33 MΩ	1MΩ
5.0V	3.16 MΩ	1MΩ

Figure 8-2. TPS71501-Q1 Adjustable LDO Regulator Programming

8.2.1 Detailed Design Procedure

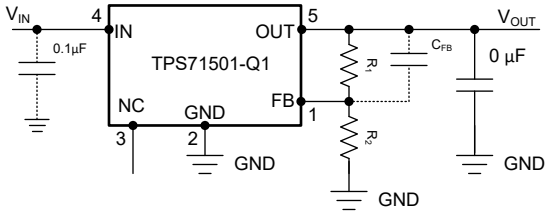
8.2.1.1 Programming the TPS71501-Q1 Adjustable LDO Regulator

The output voltage of the TPS71501-Q1 adjustable regulator is programmed using an external resistor divider as shown in Figure 8-3. The output voltage is calculated using Equation 2.

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \tag{2}$$

where:

- V_{REF} = 1.205 V typ (the internal reference voltage)



Output Voltage	R1	R2
1.8V	0.499 MΩ	1MΩ
2.8V	1.33 MΩ	1MΩ
5.0V	3.16 MΩ	1MΩ

Figure 8-3. TPS71501-Q1 Adjustable LDO Regulator Programming

Choose resistors R1 and R2 for an approximately 1.5-µA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Avoid higher resistor values because leakage current into and out of FB across R1 and R2 creates an offset voltage that artificially increases or decreases the feedback voltage and thus erroneously decreases or increases V_O. The recommended design procedure is to choose R2 equal to 1 MΩ to set the divider current at 1.5 µA and then calculate R1 using Equation 3.

$$R1 = \left(\frac{V_O}{V_{ref}} - 1 \right) \times R2 \tag{3}$$

8.2.1.2 External Capacitor Requirements

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.2.1.3 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of a large output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.2.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the PMOS pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V. These conditions are:

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated. Limit reverse current to 5% or less of the rated output current of the device in the event this current cannot be avoided.

Figure 8-4 shows one approach for protecting the device.

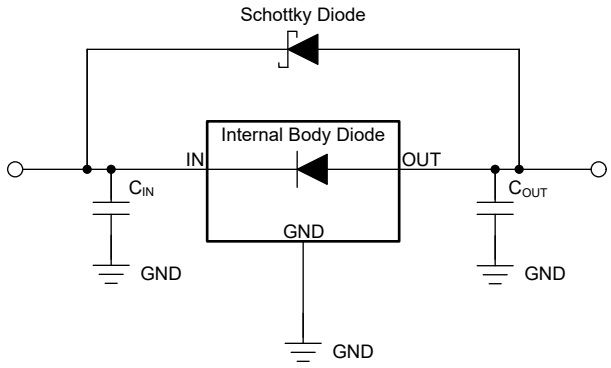


Figure 8-4. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.2.1.5 Feed-Forward Capacitor (C_{FF})

For the adjustable-voltage version device, a feed-forward capacitor (C_{FF}) can be connected from the OUT pin to the FB pin. C_{FF} improves transient, noise, and PSRR performance, but is not required for regulator stability. Recommended C_{FF} values are listed in the *Recommended Operating Conditions* table. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

C_{FF} and R_1 form a zero in the loop gain at frequency f_Z, while C_{FF}, R_1, and R_2 form a pole in the loop gain at frequency f_P. C_{FF} zero and pole frequencies can be calculated from the following equations:

$$f_Z = 1 / (2 \times \pi \times C_{FF} \times R_1) \quad (4)$$

$$f_P = 1 / (2 \times \pi \times C_{FF} \times (R_1 \parallel R_2)) \quad (5)$$

$C_{FF} \geq 10$ pF is required for stability if the feedback divider current is less than 5 µA. Equation 6 calculates the feedback divider current.

$$I_{FB\_Divider} = V_{OUT} / (R_1 + R_2) \quad (6)$$

To avoid start-up time increases from C_{FF}, limit the product $C_{FF} \times R_1 < 50$ µs.

For an output voltage of 1.205 V with the FB pin tied to the OUT pin, no C_{FF} is used.

8.2.1.6 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (7)$$

Note

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation, use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (8)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.2.1.7 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \quad (9)$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \psi_{JB} \times P_D \quad (10)$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8.2.2 Application Curves

Figure 8-5 illustrates the input voltage ramp from 0 V to just below 24 V (CH1), the 3.3-V regulated output voltage (CH3), and the 50-mA output current (CH4). The scale on CH4 is 50 mA/div.

Figure 8-6 illustrates the input voltage ramp from 0 V to 8 V, the 3.3-V regulated output voltage, and the 50-mA output current.

Figure 8-7 illustrates the load transient waveform of the TPS71533-Q1, output current is switched between 0 mA and 50 mA (CH4). Input voltage is set at 4.3 V (CH1). Output voltage DC (CH3) and output voltage AC (CH2) are also illustrated in the waveform.

Figure 8-8 illustrates the load transient waveform of the TPS71533-Q1, output current is switched between 0 mA and 50 mA with a slew rate of 0.5 A/µs. Input voltage is set at 4.3 V. Output voltage AC is illustrated in the waveform to capture the undershoot and overshoot behavior.

Figure 8-9 illustrates the line transient waveform of the TPS71533-Q1, where input voltage is switched between 5 V and 14 V with slew rate of 0.66 V/µs. Load current is set at 50 mA. Output voltage AC is illustrated in the waveform to capture the undershoot and overshoot behavior.

Figure 8-10 illustrates the fast dropout exit waveform of the TPS71533-Q1, where input voltage is switched between 2.5 V and 14 V with slew rate of 1.15 V/µs. Load current is set at 1 mA and 50 mA. Output voltage AC is illustrated in the waveform to capture the undershoot and overshoot behavior.

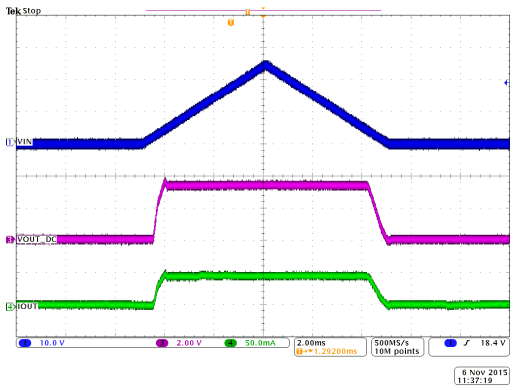


Figure 8-5. TPS71533-Q1 Power-Up and Power-Down Waveform for Legacy Chip

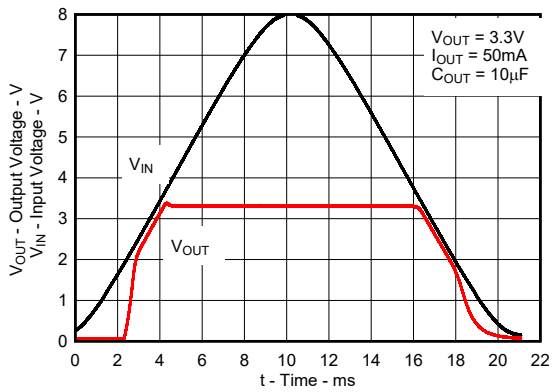


Figure 8-6. TPS71533-Q1 Power-Up and Power-Down Waveform for New Chip

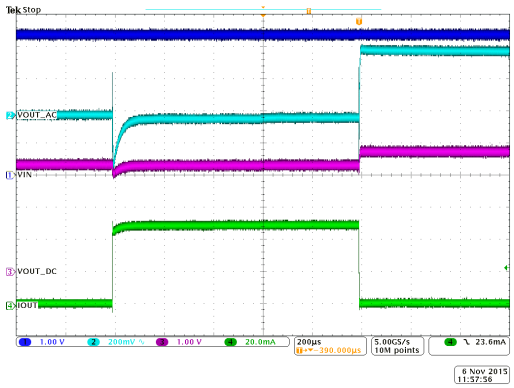


Figure 8-7. TPS71533-Q1 Load Transient Waveform for Legacy Chip

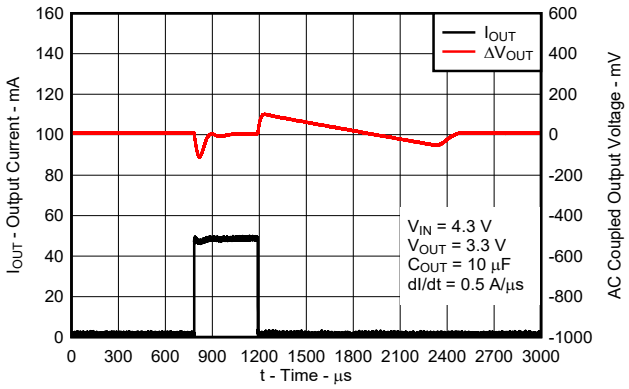


Figure 8-8. TPS71533-Q1 Load Transient Waveform for New Chip

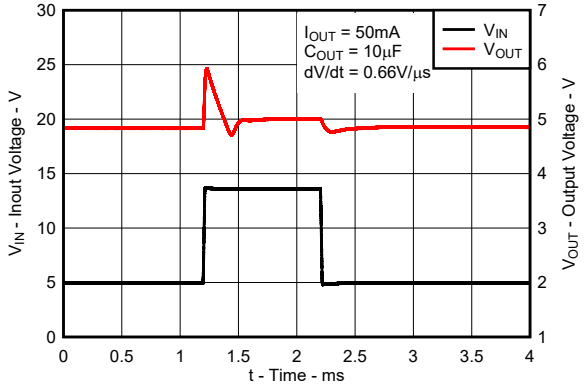


Figure 8-9. TPS71533-Q1 Fast Line Transient Waveform for New Chip

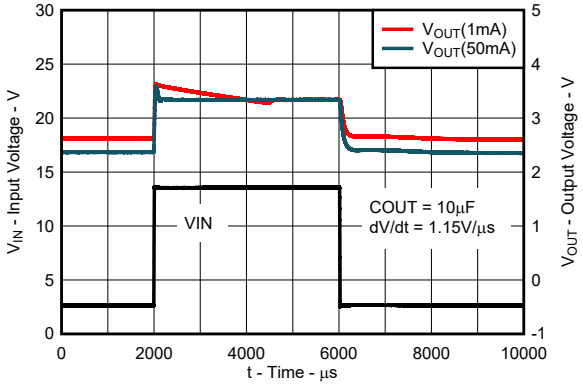


Figure 8-10. TPS71533-Q1 Dropout Exit Transient Response for New Chip

8.3 Power Supply Recommendations

The device is designed to operate from a max 24-V input voltage supply. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS715-Q1, add a microfarad (µF) level bulk capacitor and a nanofarad (nF) level ceramic bypass capacitor at the input.

8.4 Layout

8.4.1 Layout Guidelines

For the LDO power supply, layout is an important step. If layout is not carefully designed, the regulator can possibly not deliver enough output current because of the thermal limitation. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, spread the ground copper as large as possible. Figure 8-11 shows an example layout.

8.4.1.1 Power Dissipation

To provide reliable operation, worst-case junction temperature must not exceed 125°C. This restriction limits the power dissipation the regulator can handle in any given application. To make sure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 11:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \tag{11}$$

where:

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the *Thermal Information* table)
- T_A is the ambient temperature

The regulator dissipation is calculated using Equation 12:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{12}$$

8.4.2 Layout Example

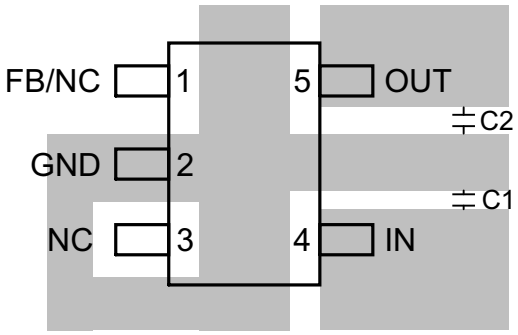


Figure 8-11. TPS715-Q1 Layout Example

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

9.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS715-Q1. The TPS71533EVM evaluation module (and related user's guide) can be requested at the TI website through the product folders or purchased directly from the TI eStore.

9.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS715-Q1 is available through the product folders under *Tools & Software*.

9.1.2 Device Nomenclature

Table 9-1. Device Nomenclature(1)

PRODUCT	V_{OUT}
TPS715**xx**Q***yyy*** **z**Q1 Legacy chip	**xx** is the nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **yyy** is the package designator. **z** is the package quantity.
TPS715**xx**Q***yyy*** **z M3** New chip	**xx** is the nominal output voltage (for example, 28 = 2.8 V, 285 = 2.85 V, 01 = Adjustable). **yyy** is the package designator. **z** is the package quantity. **M3** is a suffix designator for new chip redesigns on the latest TI process technology.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS715A 24-V High Input Voltage, Micropower, 80-mA LDO Voltage Regulator* data sheet
- Texas Instruments, *TPS71533EVM LDO Evaluation Module* user guide
- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note
- Texas Instruments, *Know Your Limits* application note

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS71501QDCKRM3Q1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANS	Samples
TPS71501QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ANS	Samples
TPS71525QDCKRM3Q1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANU	Samples
TPS71525QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ANU	Samples
TPS71530QDCKRM3Q1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANV	Samples
TPS71530QDCKRQ1	LIFEBUY	SC70	DCK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ANV	
TPS71533QDCKRM3Q1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANW	Samples
TPS71533QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ANW	Samples
TPS71550QDCKRM3Q1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANX	Samples
TPS71550QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	ANX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS715-Q1 :

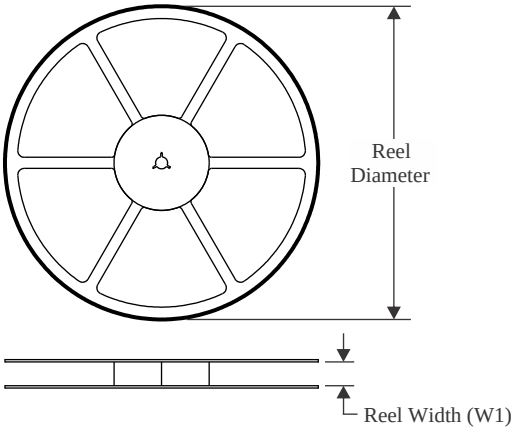
- Catalog : TPS715

NOTE: Qualified Version Definitions:

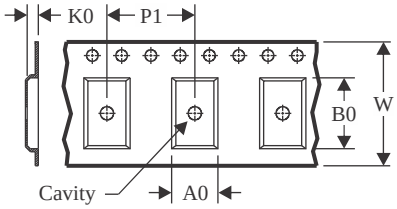
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

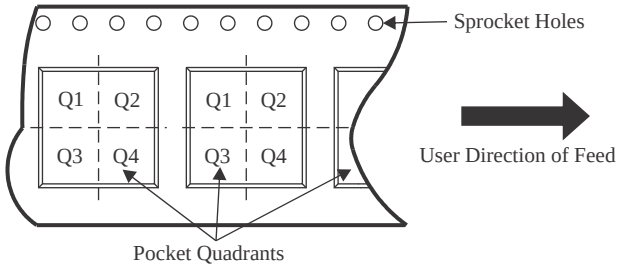


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

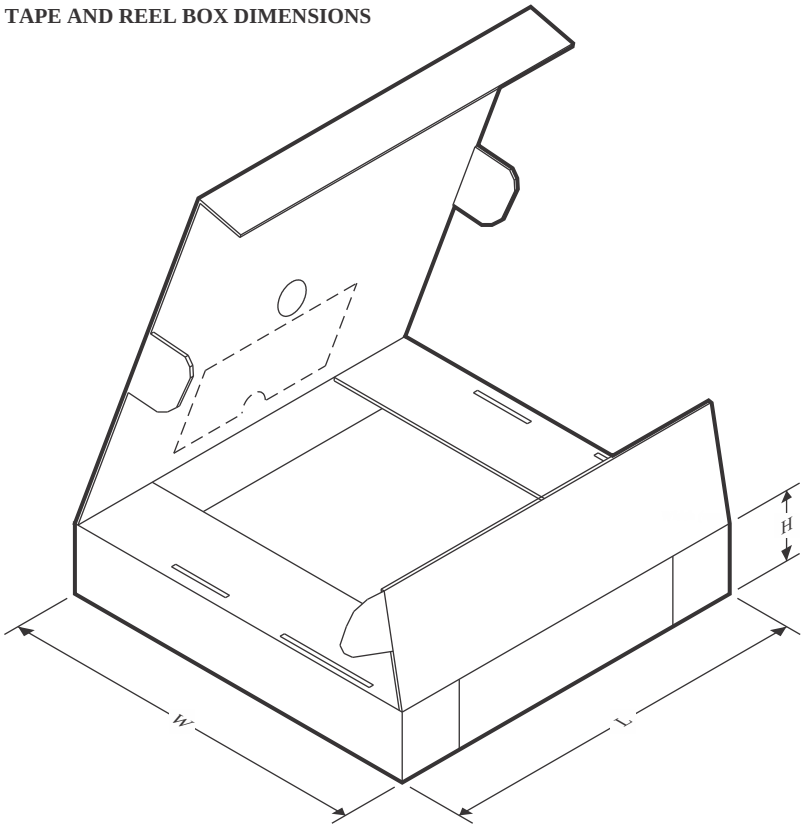
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS71501QDCKRM3Q1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71501QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71525QDCKRM3Q1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71525QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71530QDCKRM3Q1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71533QDCKRM3Q1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71533QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPS71550QDCKRM3Q1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

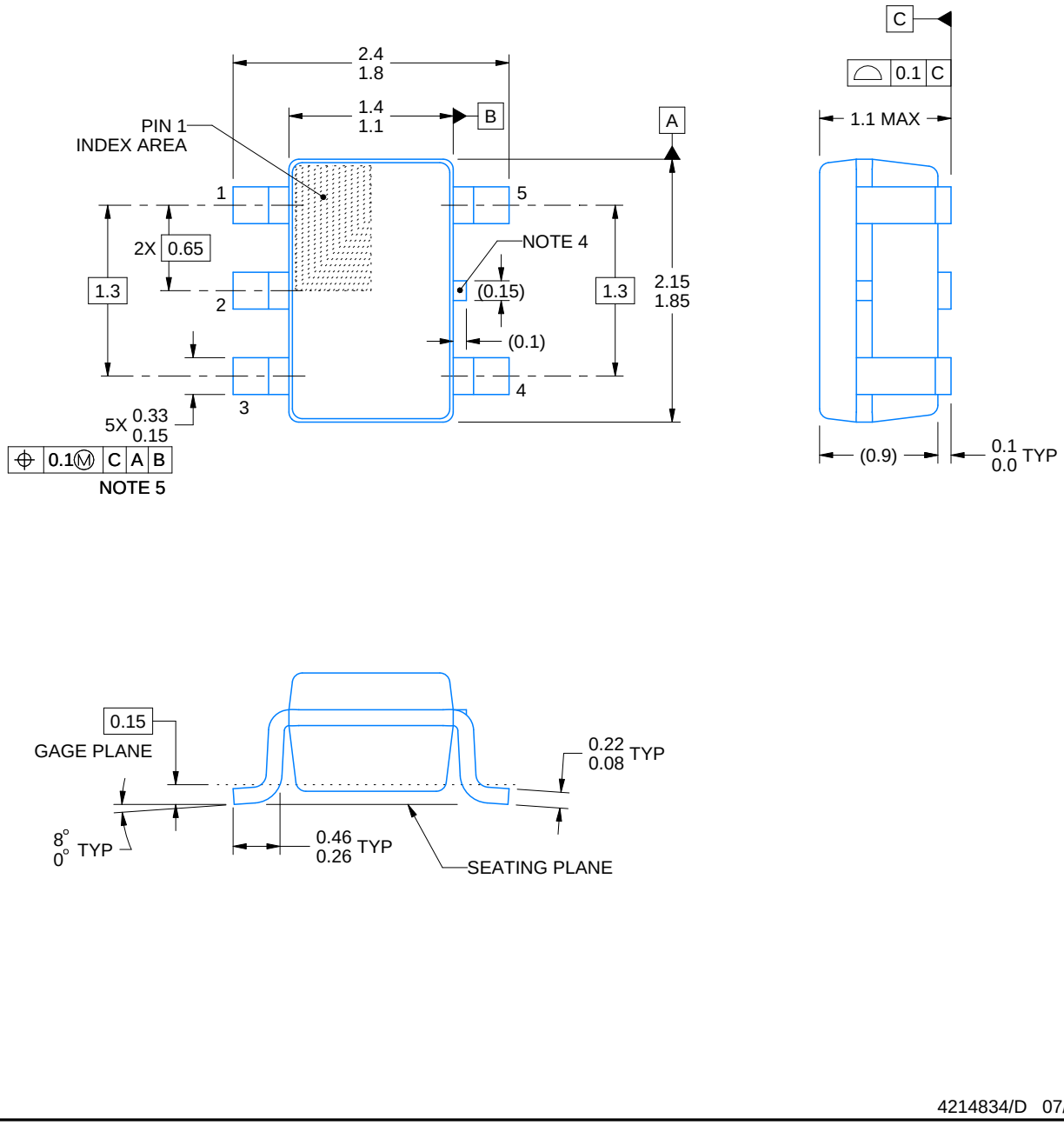
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS71501QDCKRM3Q1	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71501QDCKRQ1	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71525QDCKRM3Q1	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71525QDCKRQ1	SC70	DCK	5	3000	340.0	340.0	38.0
TPS71530QDCKRM3Q1	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71533QDCKRM3Q1	SC70	DCK	5	3000	180.0	180.0	18.0
TPS71533QDCKRQ1	SC70	DCK	5	3000	340.0	340.0	38.0
TPS71550QDCKRM3Q1	SC70	DCK	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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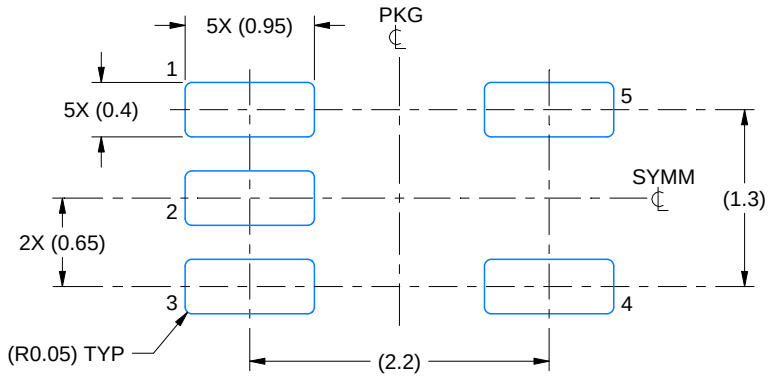
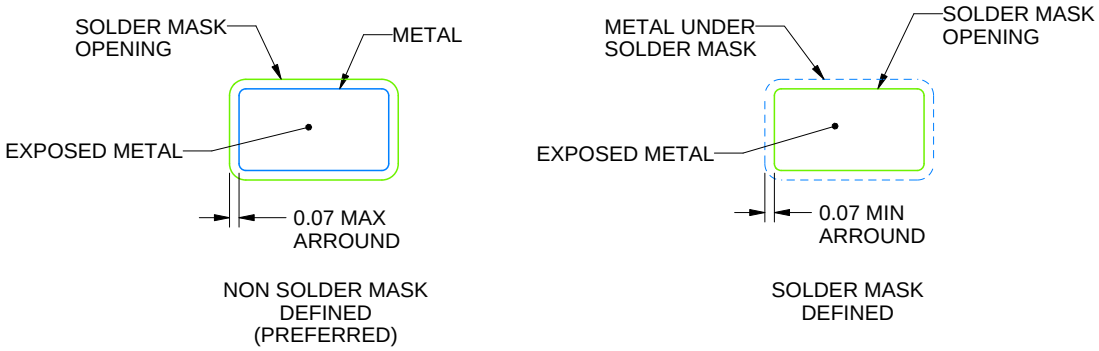
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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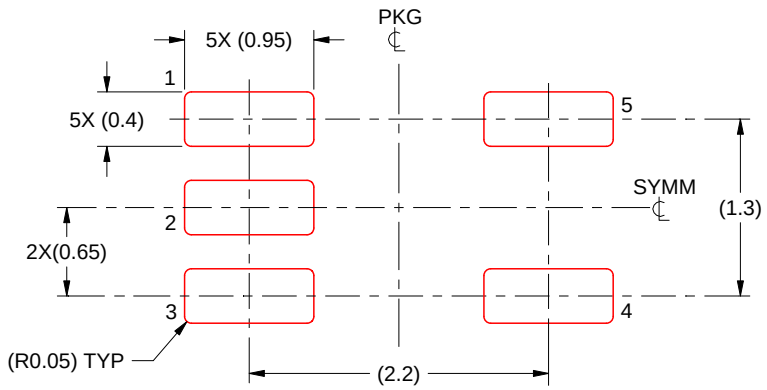
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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