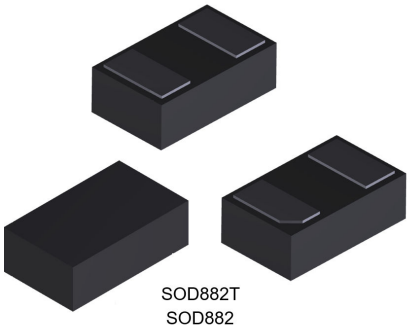
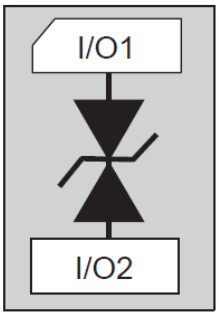
ESDALC5-1BT2, ESDALC5-1BM2

Datasheet

Single-line low capacitance Transil, transient surge voltage suppressor (TVS) for ESD protection



SOD882T
SOD882



Product status link
ESDALC5-1BT2, ESDALC5-1BM2

Features

- Single-line bidirectional protection
- Breakdown voltage = 5.8 V min.
- Low capacitance = 26 pF at 0 V
- Lead-free packages
- ECOPACK2 compliant component
- Benefits
  - Low capacitance for optimized data integrity
  - Low leakage current < 60 nA
  - Low PCB space consumption: 0.6 mm²
  - High reliability offered by monolithic integration
- Complies with IEC 61000-4-2 (exceeds level 4)
  - ±30 kV (air discharge)
  - ±30 kV (contact discharge)
- Complies MIL STD 883G - Method 3015-7: class 3
  - Human body model

Application

Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems
- Cellular phone handsets and accessories
- Video equipment

Description

The ESDALC5-1BM2 (SOD882) and ESDALC5-1BT2 (SOD882T) are bidirectional single-line TVS diodes designed to protect data lines or other I/O ports against ESD transients.

These devices are ideal for applications where both reduced line capacitance and board space saving are required.

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2: contact discharge	30	kV
		IEC 61000-4-2: air discharge	30	
P_{PP}	Peak pulse power dissipation (8/20 µs), T_j initial = Tamb		150	W
I_{PP}	Peak Pulse current (8/20 µs)		9	A
T_{stg}	Storage temperature range		-65 to +150	°C
T_j	Junction temperature		-55 to +150	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

Figure 1. Electrical characteristics (definitions)

Symbol — Parameter
V_{BR} = Breakdown voltage
V_{RM} = Stand-of voltage
V_{CL} = Clamping voltage
I_{RM} = Leakage current at V_{RM}
I_{PP} = Peak pulse current
R_d = Dynamic impedance
C_{LINE} = Input capacitance per line

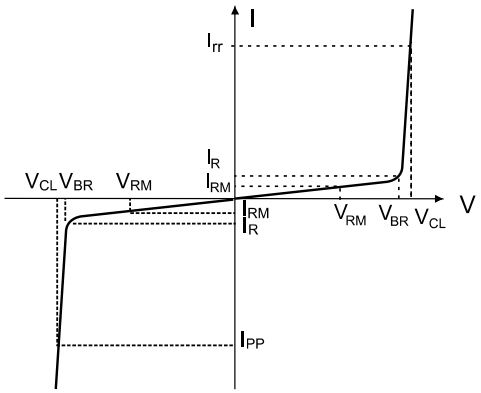


Table 2. Electrical characteristics (values) (T_{amb} = 25° C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	From I/O1 to I/O2, I_R = 1 mA	11	13	17	V
	From I/O2 to I/O1, IR = 1 mA	5.8	8	11	
I_{RM}	V_R = 5 V			60	nA
R_d	Dynamic resistance, pulse width 100 ns From I/O1 to I/O2 From I/O2 to I/O1		0.25 0.23		Ω
V_{CL}	8 kV contact discharge after 30 ns IEC 61000 4-2: From I/O1 to I/O2 From I/O2 to I/O1		16 11		V
C_{LINE}	F = 1 MHz, VR = 0 V		26	30	pF

1.1 Characteristics (curves)

Figure 2. Peak pulse power versus initial junction temperature (maximum values)

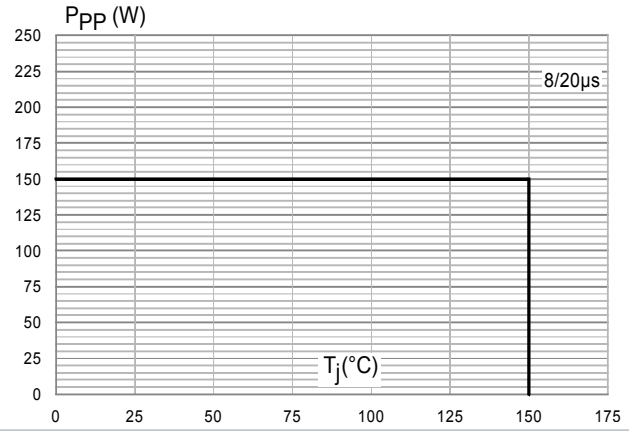


Figure 3. Leakage current versus junction temperature (typical values)

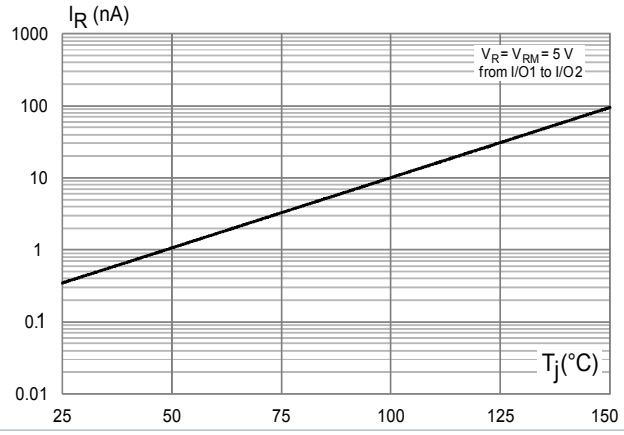


Figure 4. Leakage current versus junction temperature (typical values)

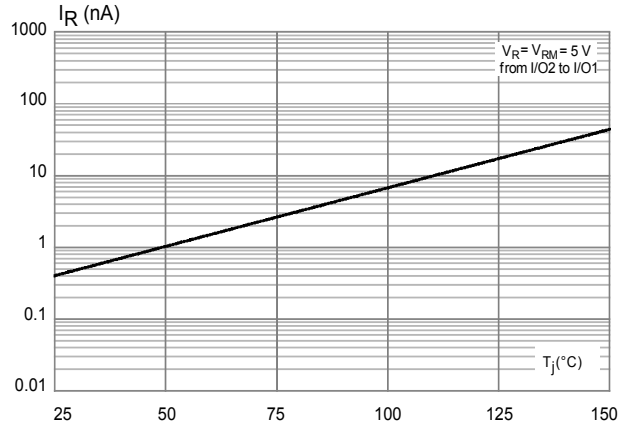


Figure 5. Peak pulse power versus exponential pulse duration (direct)

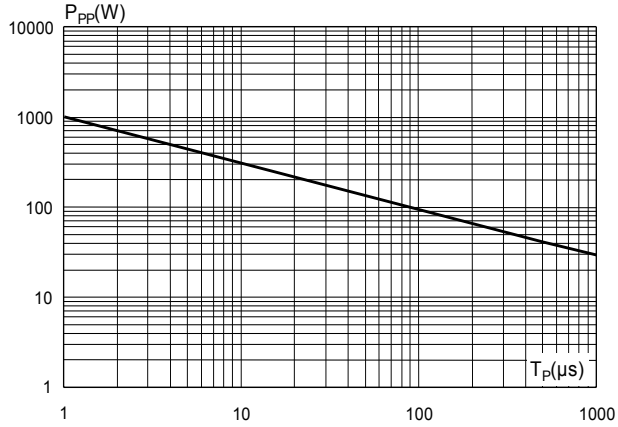


Figure 6. Clamping voltage versus peak pulse current (typical values)

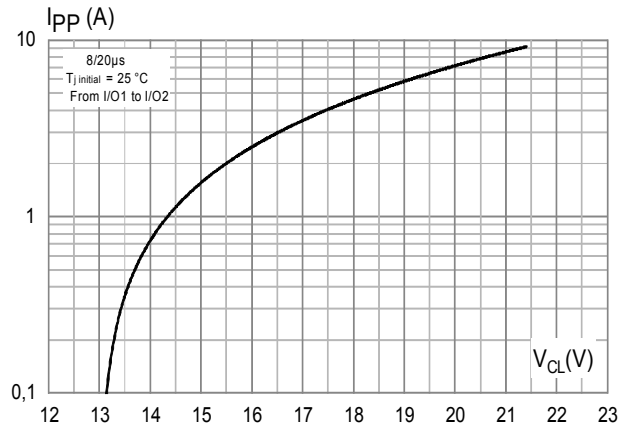


Figure 7. Clamping voltage versus peak pulse current (typical values)

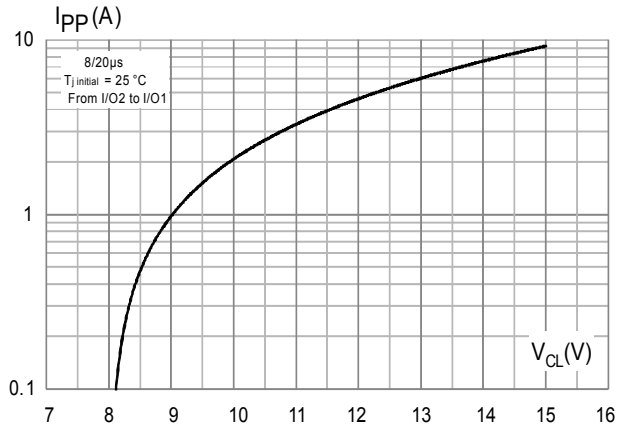


Figure 8. Junction capacitance versus reverse applied voltage (typical values from I/O1 to I/O2)

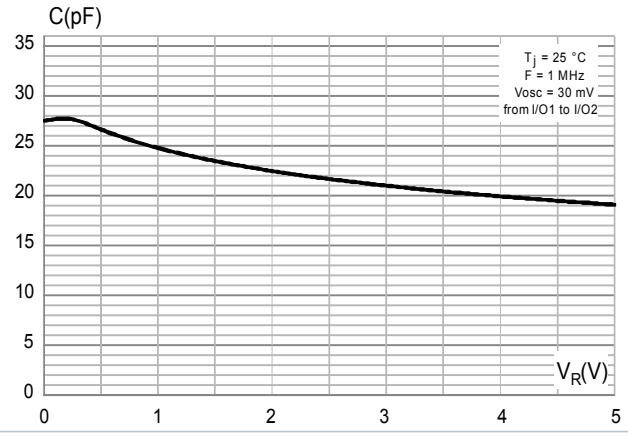


Figure 9. Junction capacitance versus reverse applied voltage (typical values from I/O2 to I/O1)

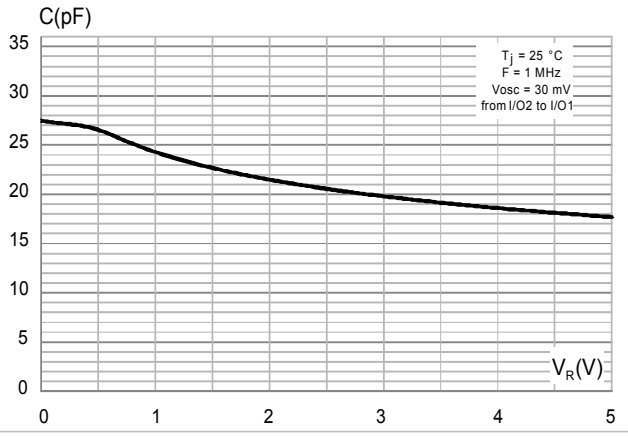


Figure 10. ESD response to IEC 61000-4-2 (+8 kV air discharge)

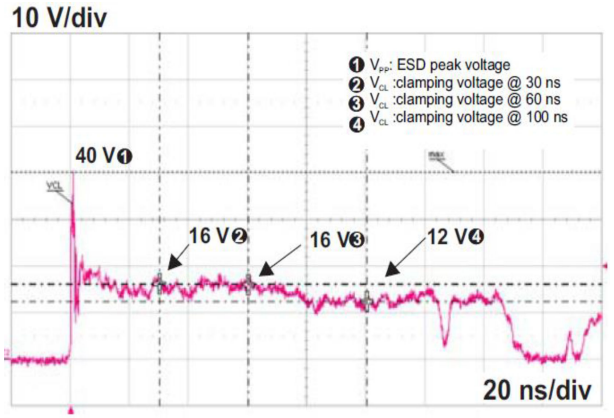


Figure 11. ESD response to IEC 61000-4-2 (-8 kV air discharge)

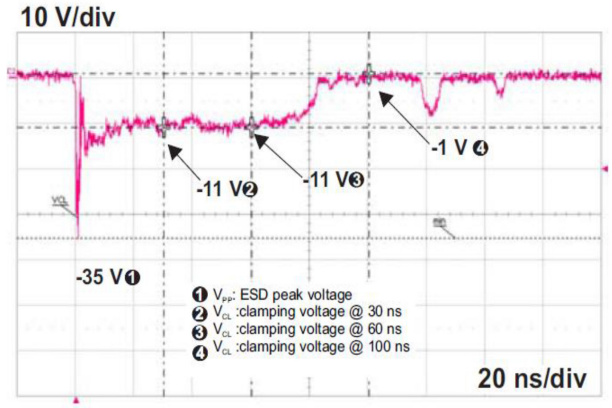


Figure 12. S21 attenuation measurement result

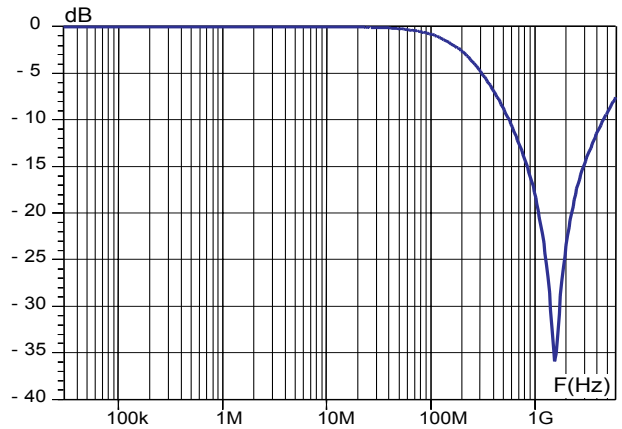
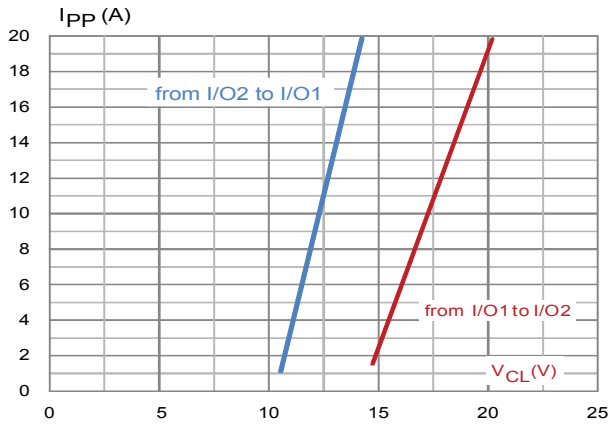


Figure 13. TLP measurements



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 SOD882 package information

Figure 14. SOD882 package outline

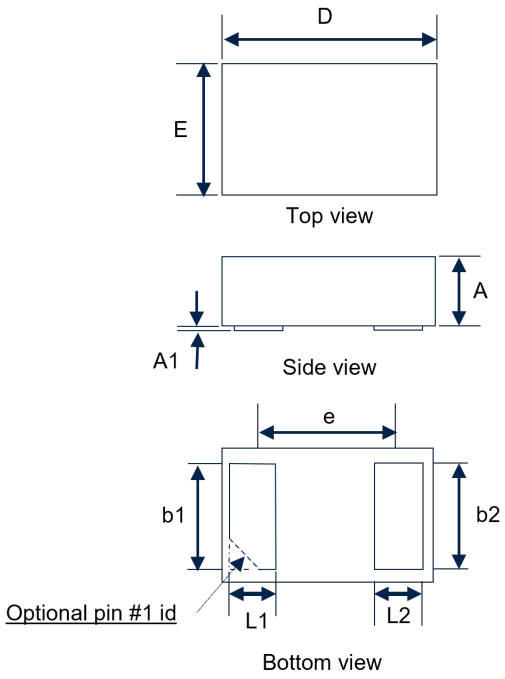


Table 3. SOD882 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.40	0.47	0.50	0.016	0.019	0.020
A1	0.00		0.05	0.000		0.002
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.45	0.50	0.55	0.018	0.020	0.022
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.55	0.60	0.65	0.022	0.024	0.026
e	0.60	0.65	0.70	0.024	0.026	0.028
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

Figure 15. Recommended footprint

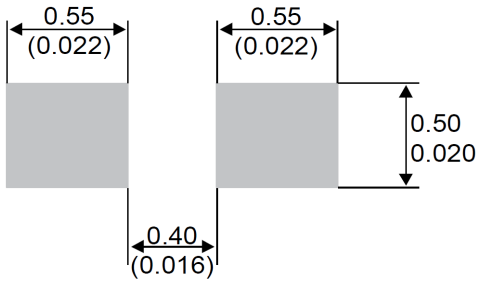
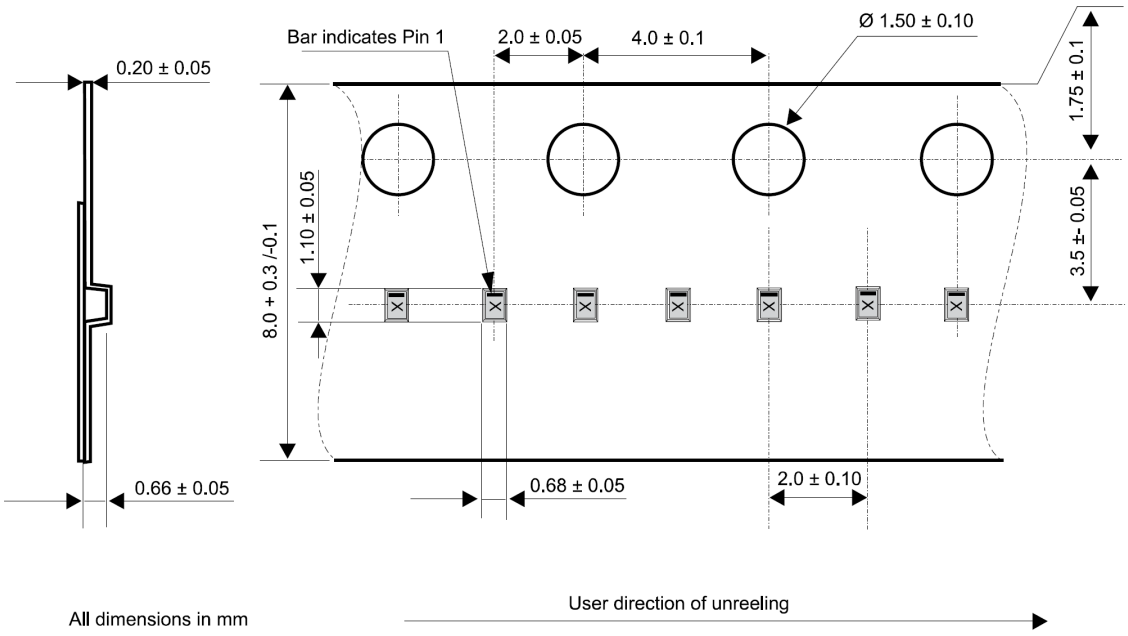


Figure 16. Marking layout

Note: Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 17. Tape outline



2.2 SOD882T package information

Figure 18. **SOD882T package outline**

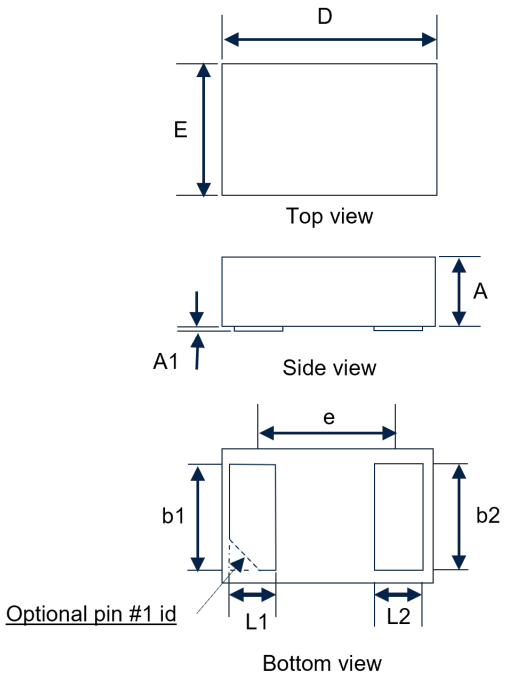


Table 4. **SOD882T package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.30		0.40	0.012		0.016
A1	0.00		0.05	0.000		0.002
b1	0.45	0.50	0.55	0.018	0.020	0.022
b2	0.45	0.50	0.55	0.018	0.020	0.022
D	0.95	1.00	1.05	0.037	0.039	0.041
E	0.55	0.60	0.65	0.022	0.024	0.026
e	0.60	0.65	0.70	0.024	0.026	0.028
L1	0.20	0.25	0.30	0.008	0.010	0.012
L2	0.20	0.25	0.30	0.008	0.010	0.012

Figure 19. Recommended footprint

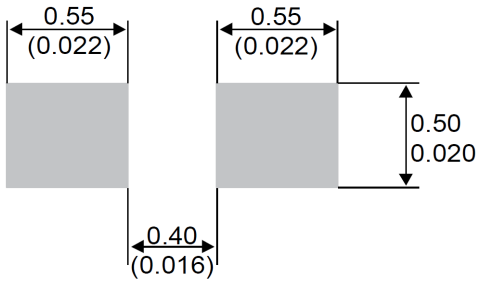
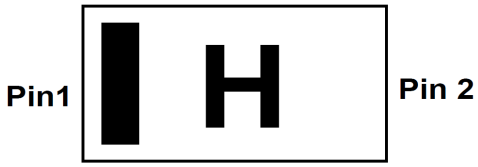
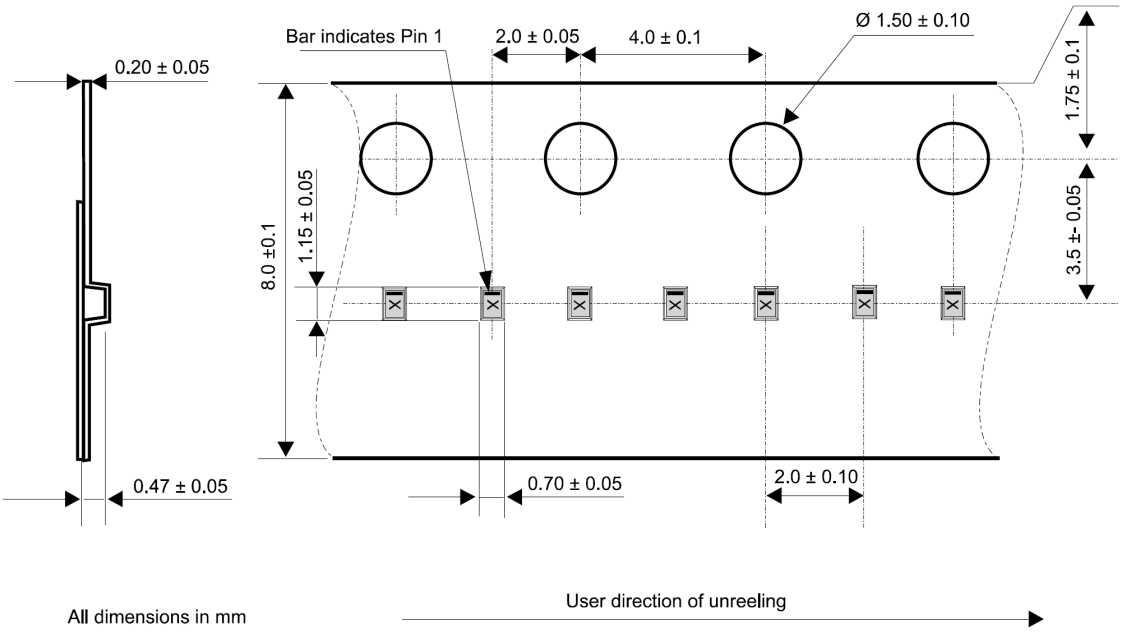


Figure 20. Marking layout



Note: Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 21. Tape outline

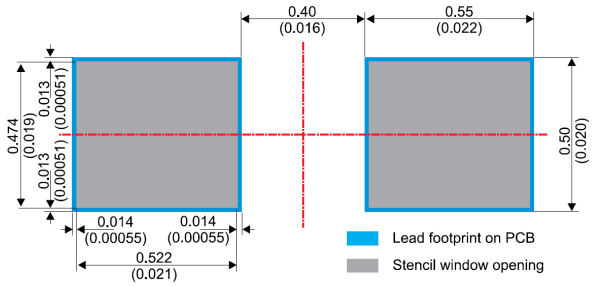


3 Recommendations on PCB assembly

3.1 Stencil opening design

Stencil opening thickness: 100 µm

Figure 22. Recommended stencil window position in mm (inches)



3.2 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-38 µm.

3.3 Placement

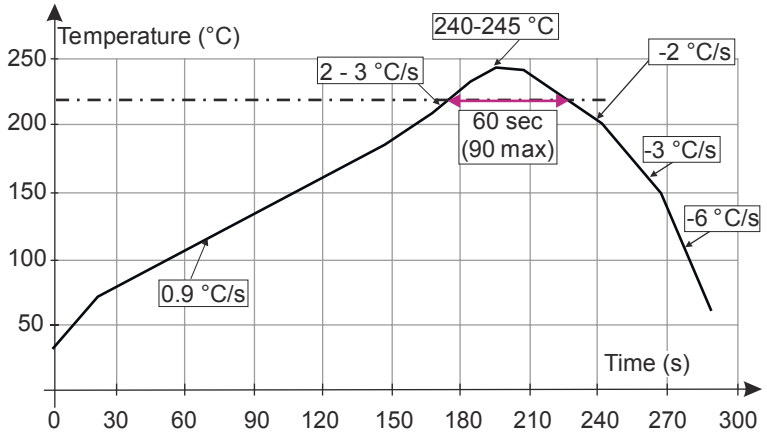
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering.
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is paste printing, pick and place and reflow soldering by using optimized tools.

3.5 Reflow profile

Figure 23. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 24. **Ordering information scheme**

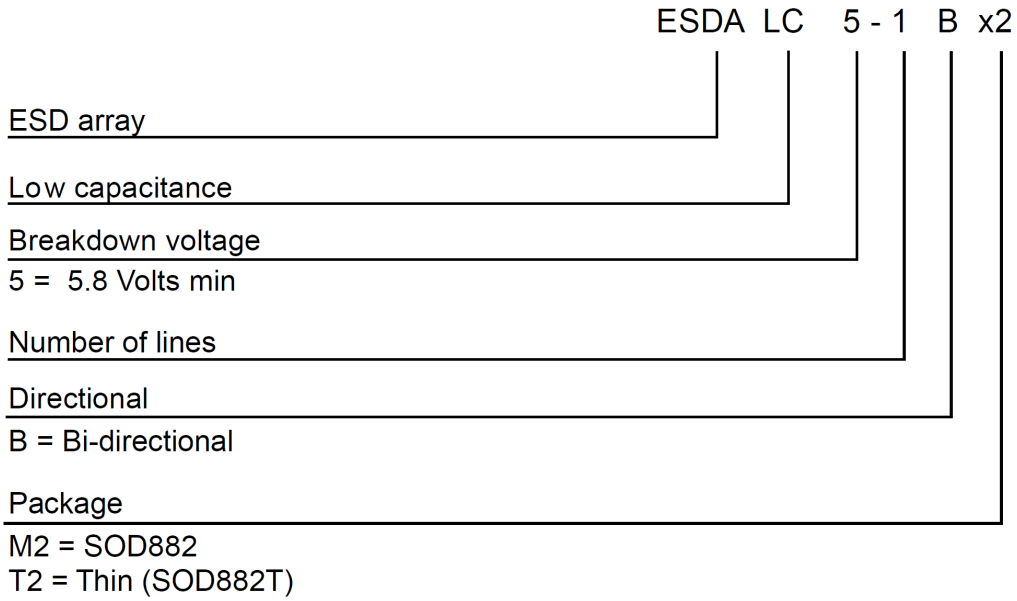


Table 5. **Ordering information**

Order code	Marking[1]	Package	Weight	Base qty.	Delivery mode
ESDALC5-1BM2	G	SOD882	0.93 mg	12000	Tape and reel
ESDALC5-1BT2	H	SOD882T	0.82 mg	12000	Tape and reel

1. *The marking can be rotated by multiples of 90° to differentiate assembly location*

Revision history

Table 6. **Document revision history**

Date	Version	Changes
02-Feb-2010	1	Initial release.
06-Jun-2012	2	Updated Figure 11, Figure 12, Figure 15, Figure 19, Table 3, and Table 4. Updated note in page 7, 8 and 13. Updated IRM in Table 2.
05-Mar-2013	3	Clamping voltage at 30 ns added in Table 2.
09-Jan-2014	4	Updated Table 1, Table 2, Table 5, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 16, Figure 17, Figure 20, Figure 21 and Figure 24. Added Figure 14.
02-Apr-2014	5	Updated Figure 4 and Figure 5.
28-Nov-2016	6	Updated cover image, Table 2: "Electrical characteristics (Tamb = 25 °C)" and Figure 2: "Electrical characteristics (definitions)".
04-Jul-2023	7	Updated Section Cover image, Section 2.1 SOD882 package information, and Section 2.2 SOD882T package information. Minor text changes.