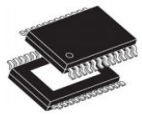
VNI4140K, VNI4140K-32

Datasheet

Quad high-side smart power solid-state relay



PowerSSO-24

Product status
VNI4140K
VNI4140K-32

Product label


Features

- Operating output current: 0.6 A (VNI4140K) or 1.0 A (VNI4140K-32) per channel
- Per channel short-circuit protection
- Per channel overtemperature protection
- Thermal case protection
- Not simultaneous channel reactivation at Thermal case reset
- All type of loads (resistive, capacitive, inductive load) are driven
- Loss of GND protection
- Undervoltage shutdown with hysteresis
- Overvoltage protection (V_{CC} clamping)
- Very low supply current
- Per channel open drain thermal fault pins
- 5 V and 3.3 V compatible I/Os
- Fast demagnetization of inductive loads
- Designed to meet IEC61131-2, IEC61000-4-4, and IEC61000-4-5
- ESD according to IEC 61000-4-2 up to ±25 kV

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines

Description

The VNI414K (for loads up to 0.6 A) and VNI4140K-32 (for loads up to 1.0 A) are monolithic 4-channel drivers featuring very low $R_{DS(on)}$ and per-channel diagnostic. The ICs, realized in STMicroelectronics™ VIPower™ technology, are intended to drive any kind of load with one side connected to ground.

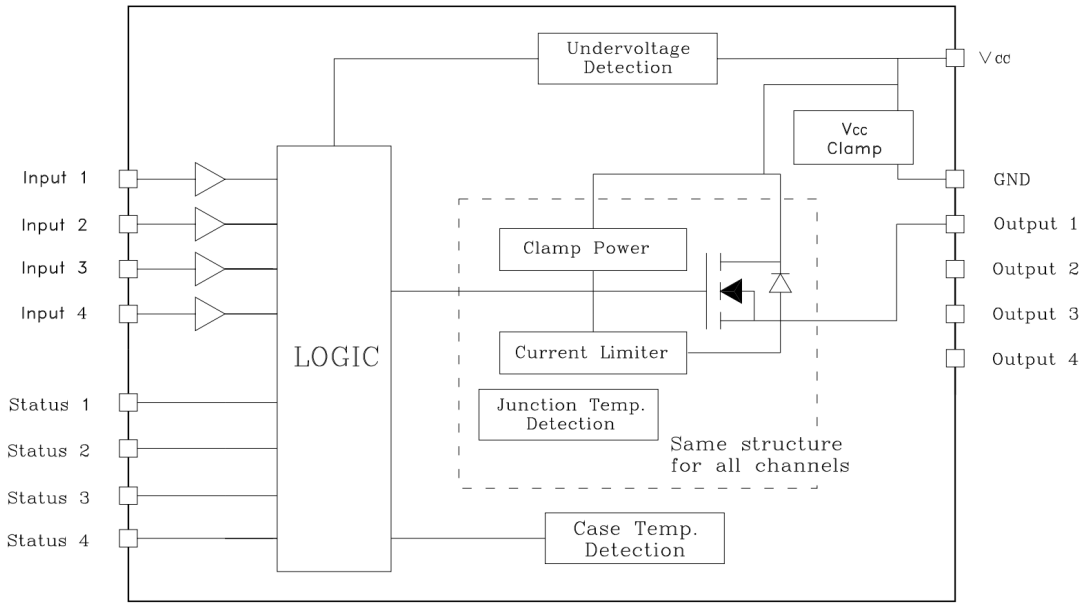
Active channel current limitation combined with thermal shutdown, independent for each channel, and automatic restart, protect the device against overload.

A channel in an overload condition overheats and turns OFF and back ON automatically in order to maintain its junction temperature between T_{TSD} and T_R. If this condition makes case temperature reach T_{CSD}, the overloaded channel is turned OFF and restarts only when case temperature has decreased down to T_{CR}. In case of more than one channel in overload, restart of the overloaded channels is not simultaneous, in order to avoid high peak current from the supply. Non-overloaded (non-overheated) channels continue operating normally.

The four open drain $STATUS_X$ output pins indicate per-channel overtemperature conditions.

1 Block diagram

Figure 1. **Block diagram**



2 Pin connection

Figure 2. **Pin connection (top view)**

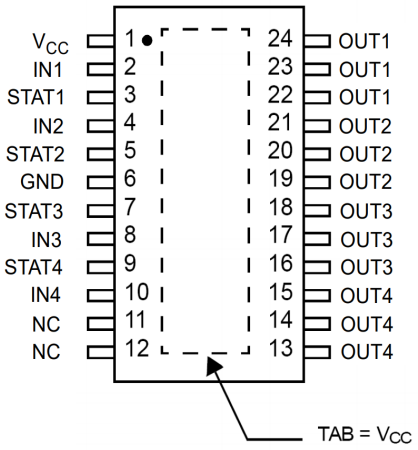


Table 1. **Pin description**

Pin	Name	Type	Description
1, TAB	VCC	Supply	IC supply voltage.
2	IN1	Logic input	Channel 1 input, 3.3 V CMOS/TTL compatible.
3	STAT1	Output/Open Drain	Channel 1 overtemperature status (active low).
4	IN2	Logic input	Channel 2 input, 3.3 V CMOS/TTL compatible.
5	STAT2	Output/Open Drain	Channel 2 overtemperature status (active low).
6	GND	Ground	Device ground connection.
7	STAT3	Output/Open Drain	Channel 3 overtemperature status (active low).
8	IN3	Logic input	Channel 3 input, 3.3 V CMOS/TTL compatible.
9	STAT4	Output/Open Drain	Channel 4 overtemperature status (active low).
10	IN4	Logic input	Channel 4 input, 3.3 V CMOS/TTL compatible.
11, 12	NC	-	Not connected.
13, 14, 15	OUT4	Output	Channel 4 power stage output, internally protected.
16, 17, 18	OUT3	Output	Channel 3 power stage output, internally protected.
19, 20, 21	OUT2	Output	Channel 2 power stage output, internally protected.
22, 23, 24	OUT1	Output	Channel 1 power stage output, internally protected.

3 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	-0.3 to 41	V
I_{GND}	DC ground reverse current	-250	mA
I_{OUT}	DC output current	Internally limited (1)	A
I_R	DC reverse output current (per channel)	-5	A
I_{IN}	Input pin current (per channel)	+/-10	mA
V_{IN}	Input pin voltage	$+V_{CC}$	V
V_{STAT}	Status pin voltage	$+V_{CC}$	V
I_{STAT}	Status pin current (per pin)	+/-10	mA
V_{ESD}	Electrostatic discharge (R = 1.5k Ω; C = 100 pF)	2000	V
E_{AS}	Single channel/single pulse avalanche energy @T_{amb} = 125 °C, I_{OUT} = 0.5 A	5	J
P_{TOT}	Power dissipation at T_C = 25 °C	Internally limited (1)	W
T_J	Junction operating temperature	Internally limited (1)	°C
T_{STG}	Storage temperature	-55 to 150	°C

1. *Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous and repetitive operation of protection functions may reduce the IC lifetime.*

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case (1)	2	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	See Figure 12	°C/W

1. *per channel*

4 Recommended operating conditions

Table 4. Input switching limits

Symbol	Parameter	Value	Unit
$f_{VIN(MAX)}$	Maximum input switching frequency	10	kHz

5 Electrical characteristics

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified

5.1 Power section

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		10.5		36	V
$R_{DS(on)}$	ON-state resistance	I_{OUT} = 0.5 A @T_J = 25 °C			0.08	Ω
		I_{OUT} = 0.5 A			0.14	
I_S	V_{CC} supply current	All channels in OFF-state		0.25		mA
		All channels in ON-state, $V_{IN1..4}$ = 5 V		2.4	4	mA
V_{CC} clamp	Clamp on V_{CC}	I_S = 20 mA	41	45	52	V
$V_{OUT(OFF)}$	OFF-state output voltage	V_{IN} = 0 V, I_{OUT} = 0 A			1	V
$I_{OUT(OFF)}$	OFF-state output current	V_{IN} = V_{OUT} = 0 V	0		5	µA
I_{LGND}	VNI4140K output current at GND disconnection	V_{CC} = V_{IN} = V_{STAT} = V_{GND} = 24 V; V_{OUT} = 0 V			1.0	mA
	VNI4140K-32 output current at GND disconnection				0.5	mA
f_{CP}	Charge pump frequency	Channel in ON-state (1)		1.45		MHz

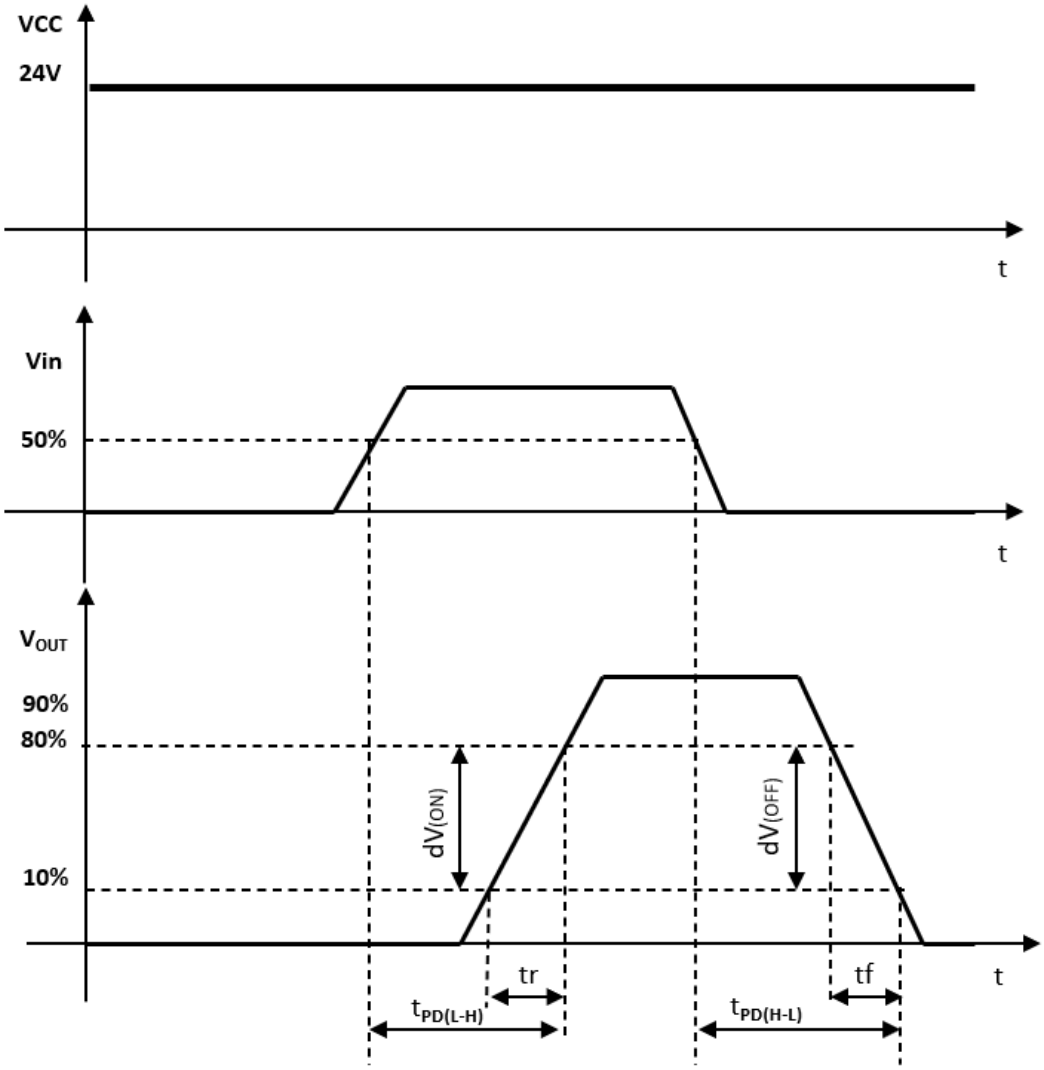
1. *To cover EN55022 class A and class B normative.*

5.2 Switching

Table 6. Switching

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{PD(L-H)}$	Turn-on delay time	V_{CC} = 24 V, R_L = 48 Ω, input rise time < 0.1 µs, see Figure 3	-	16	35	µs
t_r	Rise time		-	8	25	µs
$t_{PD(H-L)}$	Turn-off delay time		-	21	36	µs
t_f	Fall time		-	4	12	µs
$dV_{(ON)}/dt_r$	Turn-on voltage slope		-	2	-	V/µs
$dV_{(OFF)}/dt_f$	Turn-off voltage slope		-	4	-	V/µs

Figure 3. **Timing in normal operation**



5.3 Logic inputs

Table 7. **Logic inputs**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				0.8	V
V_{IH}	Input high level voltage		2.20			V
$V_{I(HYST)}$	Input hysteresis voltage			0.15		V
I_{IN}	Input current	V_{IN} = 15 V			10	µA
		V_{IN} = 36 V			210	

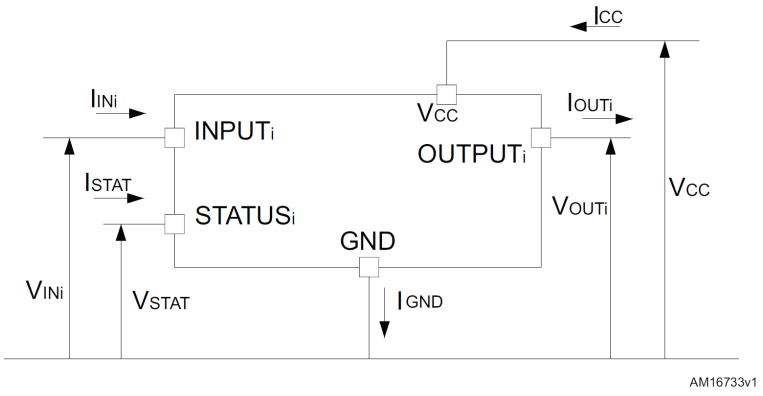
5.4 Protection and diagnostic

Table 8. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{STAT}	Status voltage output low	I_{STAT} = 1.6 mA			0.6	V
V_{USD}	Undervoltage protection		7		10.5	V
V_{USDHYS}	Undervoltage hysteresis		0.4	0.5		V
I_{PEAK}	VNI4140K maximum DC output current	Dynamic load		1.3		A
	VNI4140K-32 maximum DC output current			1.6		
I_{LIM}	VNI4140K, DC short-circuit current	V_{CC} = 24 V, R_{LOAD} ≤ 10 mΩ	0.7	1.0	1.7	A
	VNI4140K-32, DC short-circuit current		1.1	1.5	2.6	
I_{LSTAT}	Status leakage current	V_{CC} = V_{STAT} = 36 V		30		µA
T_{TSD}	Junction shutdown temperature		150	170	190	°C
T_R	Junction reset temperature		135			°C
T_{HYST}	Junction thermal hysteresis		7	15		°C
T_{CSD}	Case shutdown temperature		125	130	135	°C
T_{CR}	Case reset temperature		110			°C
T_{CHYST}	Case thermal hysteresis		7	15		°C
V_{DEMAG}	Output voltage at turn-OFF	I_{OUT} = 0.5 A; L_{LOAD} ≥ 1 mH	V_{CC} - 41	V_{CC} - 45	V_{CC} - 52	V

5.5 Current and voltage conventions

Figure 4. Current and voltage conventions



6 Truth table

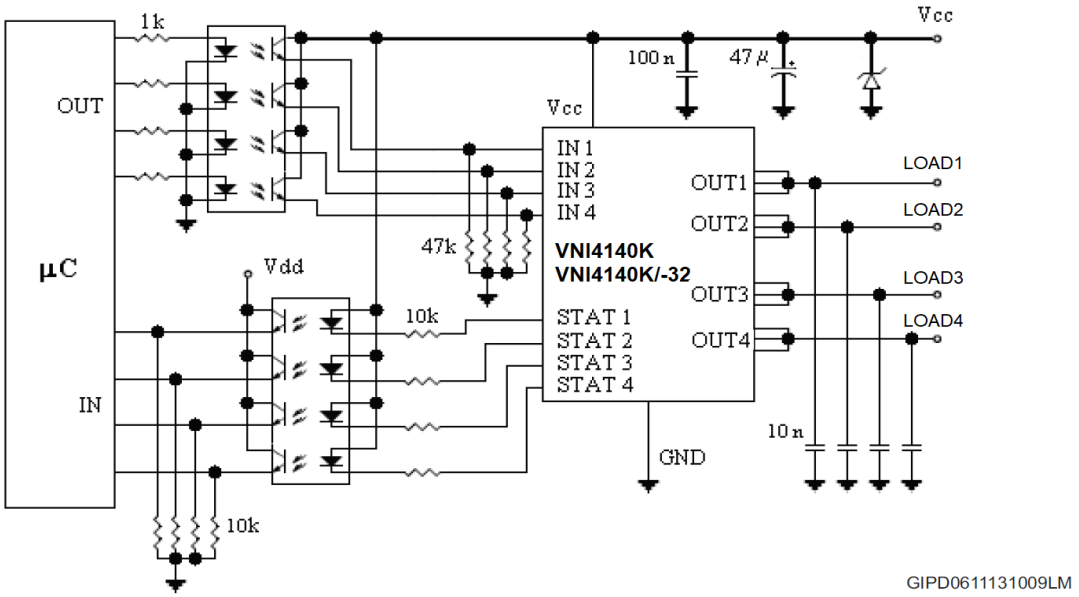
Table 9. Truth table

Condition	$Input_n$	$Output_n$	$Status_n$
Normal operation	L	L	H
	H	H	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	X
	H	L	X
Output overload (current limitation before overtemperature)	L	L	H
	H	X	H

Note: X = don't care

7 Typical application circuit

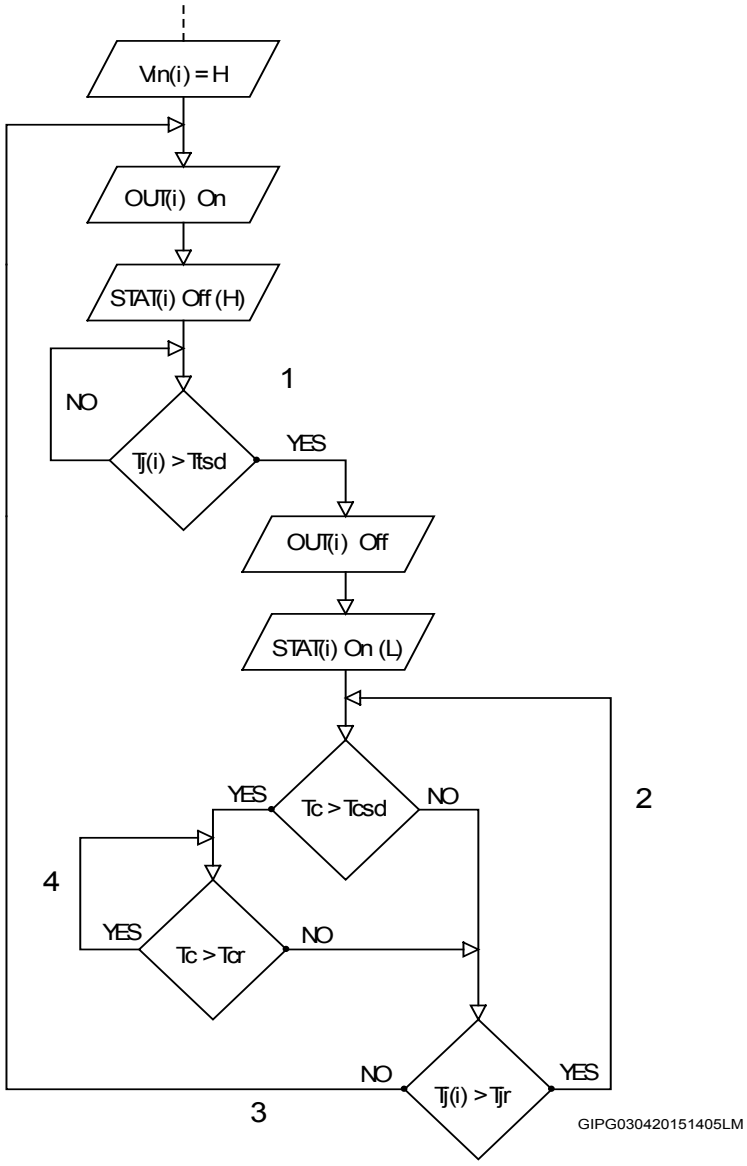
Figure 5. **Typical application circuit**



8 Thermal management

The power dissipation in the IC is the main factor that sets the safe operating condition of the device in the application. Therefore, it must be considered very carefully. Furthermore, the available space on the PCB should be chosen considering the power dissipation. Heat sinking can be achieved using copper on the PCB with proper area and thickness. Two different protections have been implemented to guarantee safety of the device if it overheats due to an overloaded condition or high environment temperature. The following flowchart explains in detail this protection functionality.

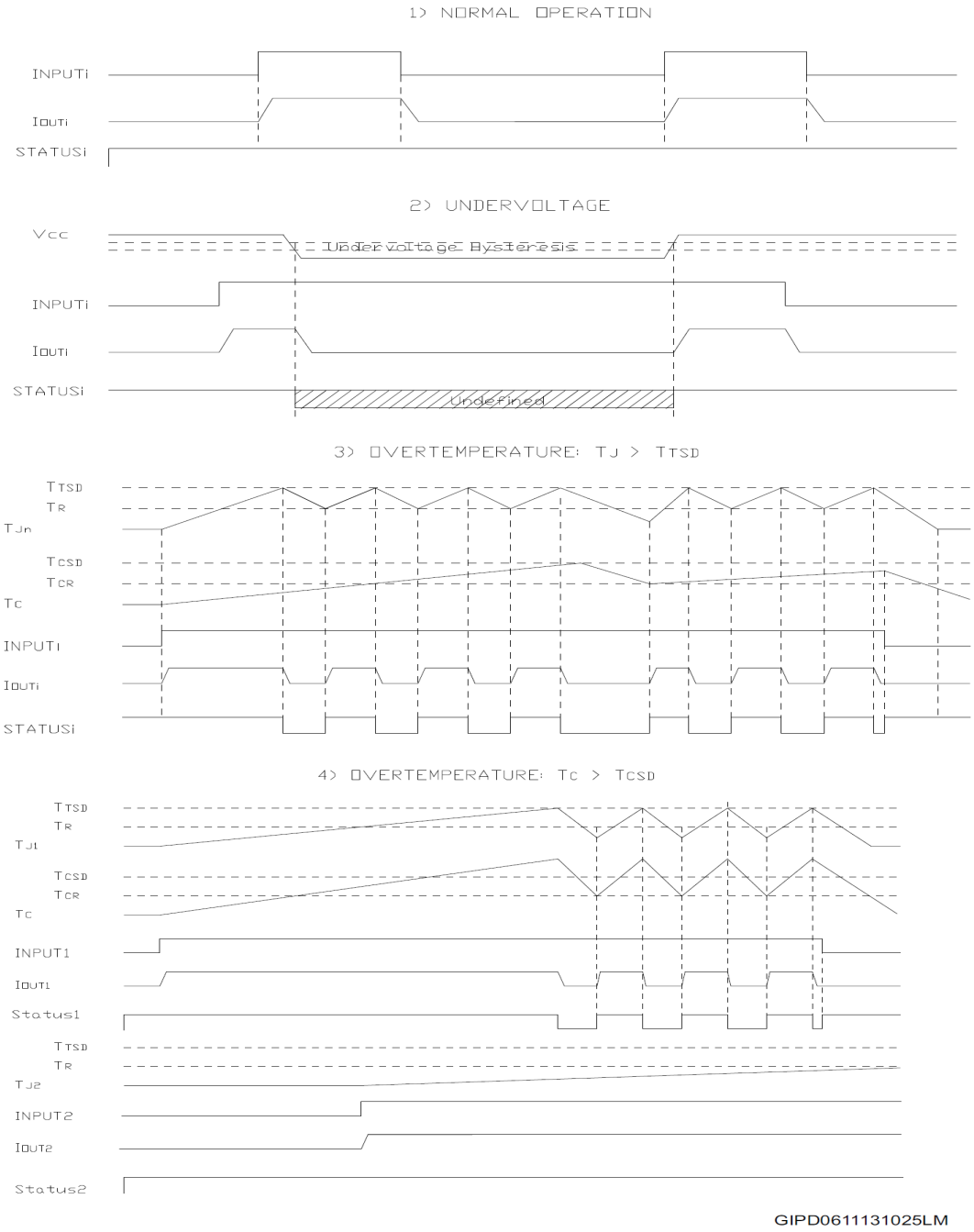
Figure 6. Thermal behavior



Note: *1 Thermal shutdown*
2 Junction hysteresis
3 Restore to idle condition
4 Case hysteresis

9 Switching waveforms

Figure 7. Switching waveforms



10 Pin function description

Figure 8. **Input circuit**

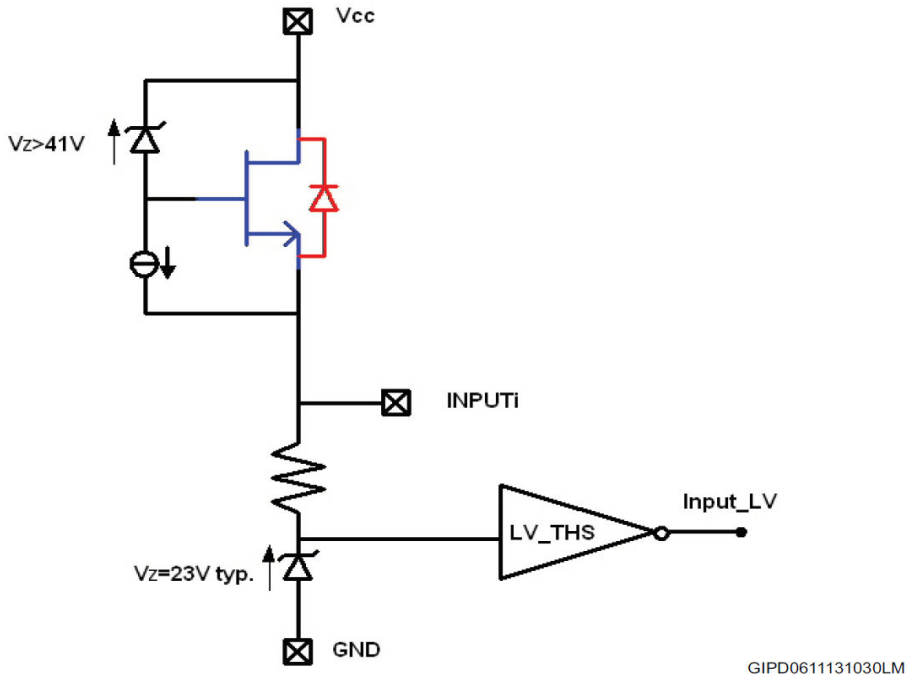


Figure 9. **Status circuit**

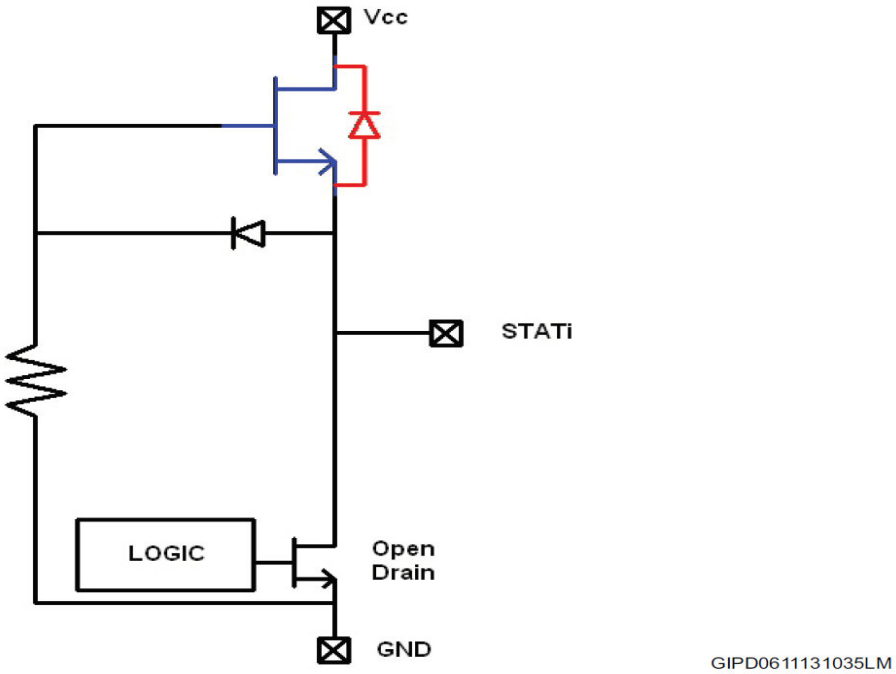
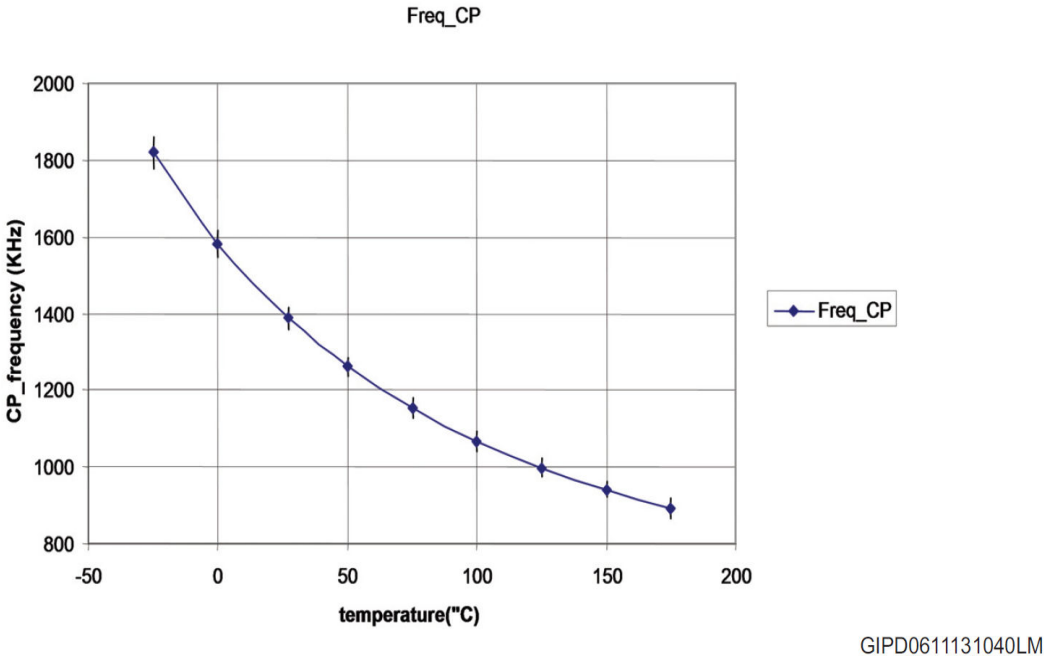


Figure 10. **Charge pump switching frequency (typical) vs. temperature**

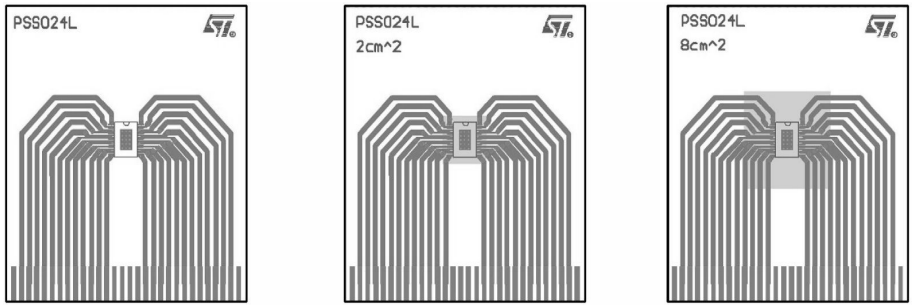


GIPD0611131040LM

11 Package and PCB thermal data

11.1 Thermal data

Figure 11. **PCB for thermal tests**



Layout condition of R_{TH} and Z_{TH} measurements (PCB: double layer, thermal vias, FR4 area = 77 mm x 86 mm, PCB thickness = 1.6 mm, Cu thickness = 70 mm (front and back side), copper areas: from minimum pad layout to 8 cm^2).

Figure 12. **$R_{TH(JA)}$ vs. PCB copper area in open box free air condition (one channel ON)**

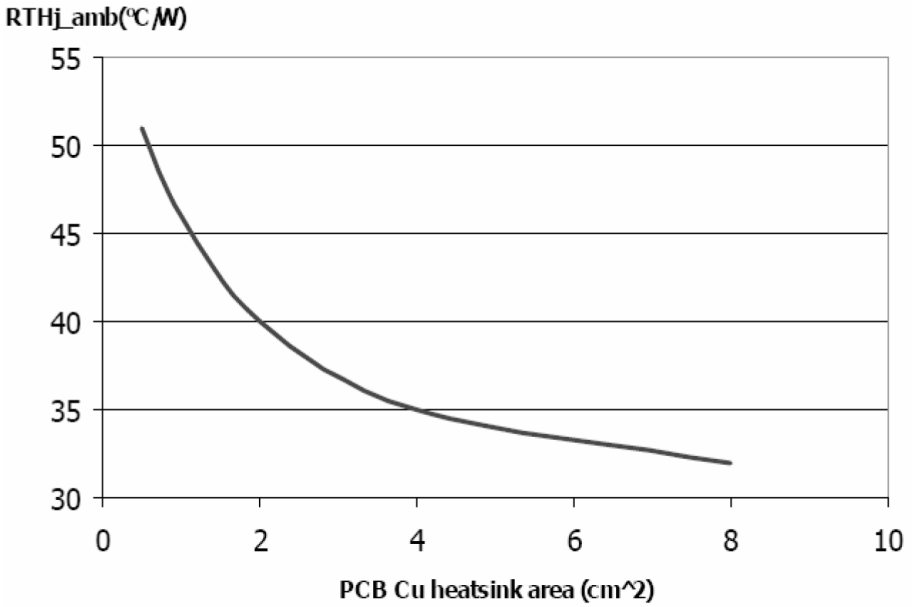
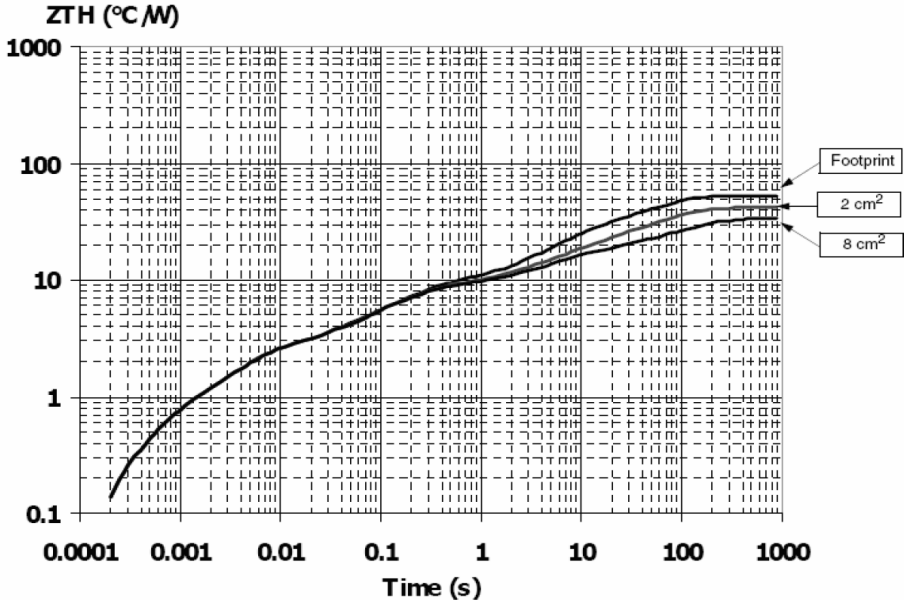


Figure 13. **Thermal impedance junction-ambient single pulse (one channel ON)**



12 Reverse polarity protection

Reverse polarity protection can be implemented on-board using two different solutions:

1. Placing a resistor (R_{GND}) between IC GND pin and load GND
2. Placing a diode between IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

$R_{GND} \geq V_{CC} / I_{GND}$

where I_{GND} is the DC reverse ground pin current and can be found in Maximum ratings of this datasheet.

Power dissipated by R_{GND} (when $V_{CC} < 0$: during reverse polarity situations) is:

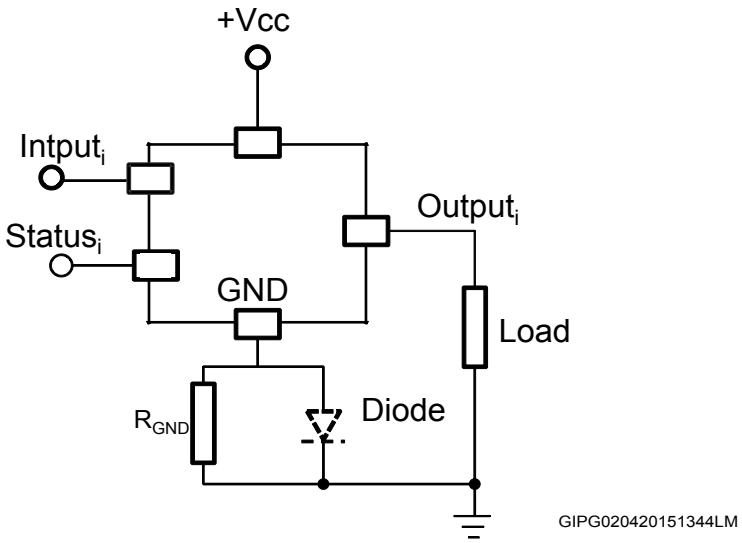
$P_D = (V_{CC})^2/R_{GND}$

If option 2 is selected, the diode has to be chosen by taking into account VRRM >$|V_{CC}|$ and its power dissipation capability:

$P_D \geq I_S * V_F$

Note: In normal conditions (no reverse polarity), due to the diode, there is a voltage drop between GND of the device and GND of the system.

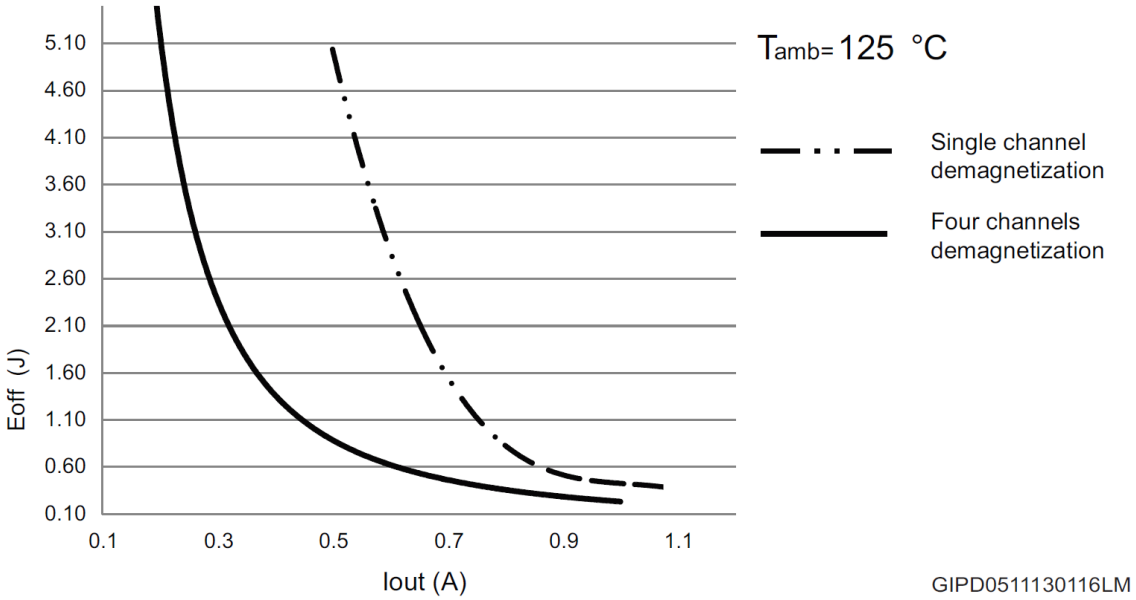
Figure 14. Reverse polarity protection



This schematic can be used with any type of load.

13 Demagnetization energy

Figure 15. **Maximum demagnetization energy vs. load current, typical values**



14 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

14.1 Package mechanical data

Figure 16. PowerSSO-24 package dimensions [mm]

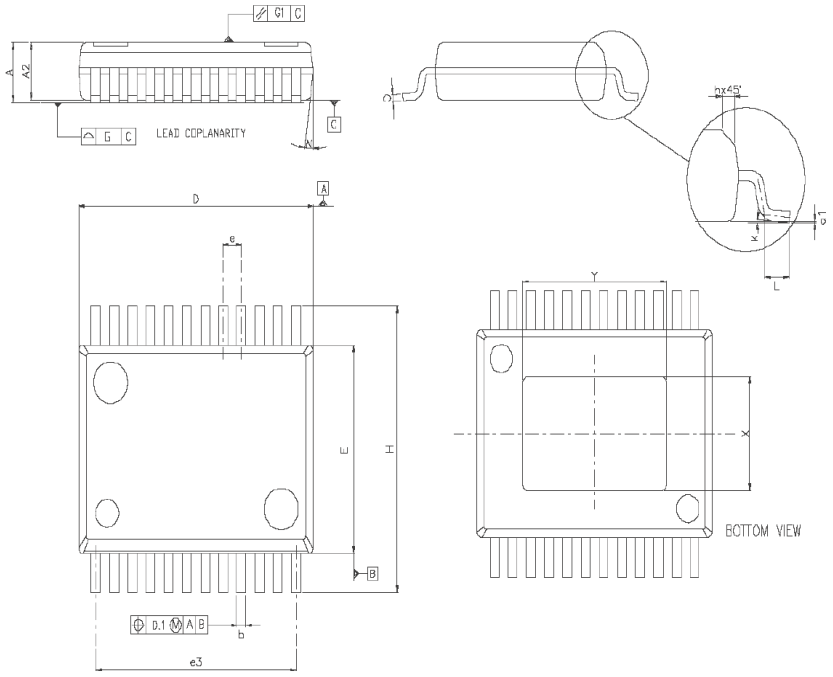
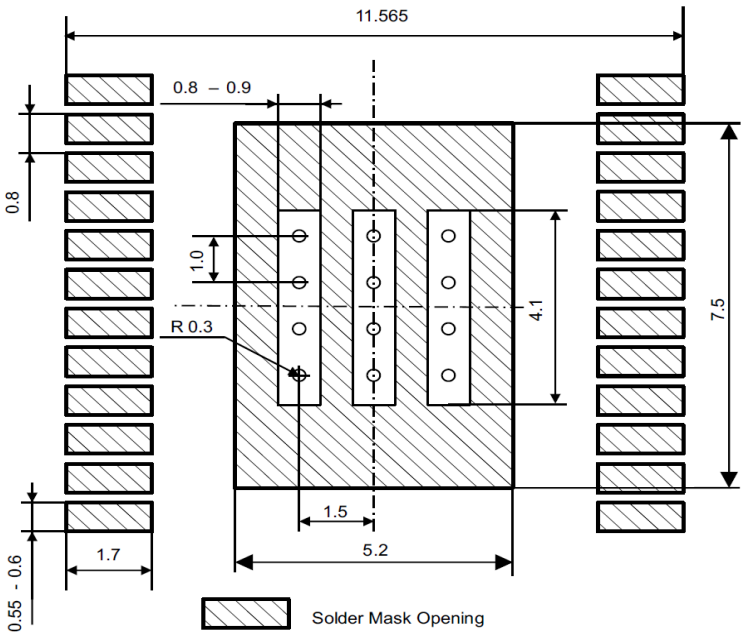


Table 10. PowerSSO24, mechanical data

Dim.	[mm]		
	Min.	Typ.	Max.
A	2.15		2.47
A2	2.15		2.40
a1	0		0.075
b	0.33		0.51
c	0.23		0.32
D	10.10		10.50
E	7.4		7.6
e		0.8	
e3		8.8	
G			0.1
G1			0.06
H	10.1		10.5
h			0.4
L	0.55		0.85

Dim.	[mm]		
	Min.	Typ.	Max.
N			10deg
X	4.1		4.7
Y	6.5		7.1

Figure 17. **PowerSSO24 suggested footprint [mm]**



STMicroelectronics is not responsible for any PCB related issues. The footprint shown in the above figure is a suggestion which might not be in line with the customer PCB supplier design rules.

14.2 PowerSSO24, packing information

Figure 18. **PowerSSO-24 tube shipment (no suffix)**

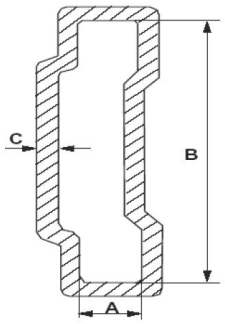


Table 11. **PowerSSO24, tube shipment information**

Description	Value
Base quantity	49
Bulk quantity	1225
Tube lenght (± 0.5)	532

Description	Value
A	3.5
B	13.8
C (± 0.1)	0.6

Note: All dimensions are in mm.

Figure 19. PowerSSO24, reel shipment

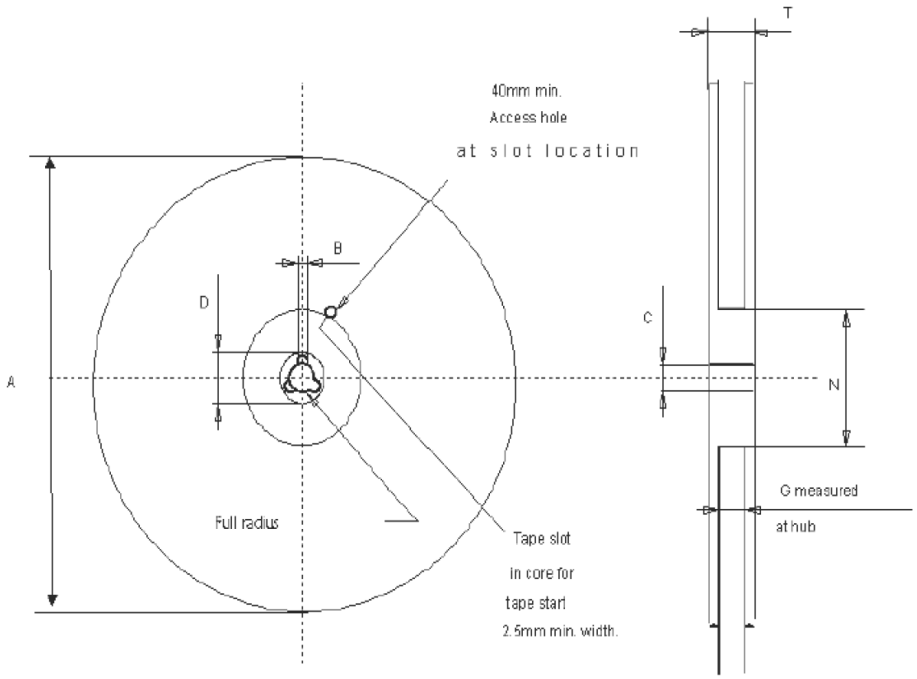


Table 12. PowerSSO24, reel information

Description	Value
Base quantity	1000
Bulk quantity	1000
A (max.)	330
B (min.)	1.5
C (± 0.2)	13
F	20.2
G (2 ± 0)	24.4
N (min.)	100
T (max.)	30.4

Note: All dimensions are in mm.

Figure 20. **PowerSSO24, tape drawings**

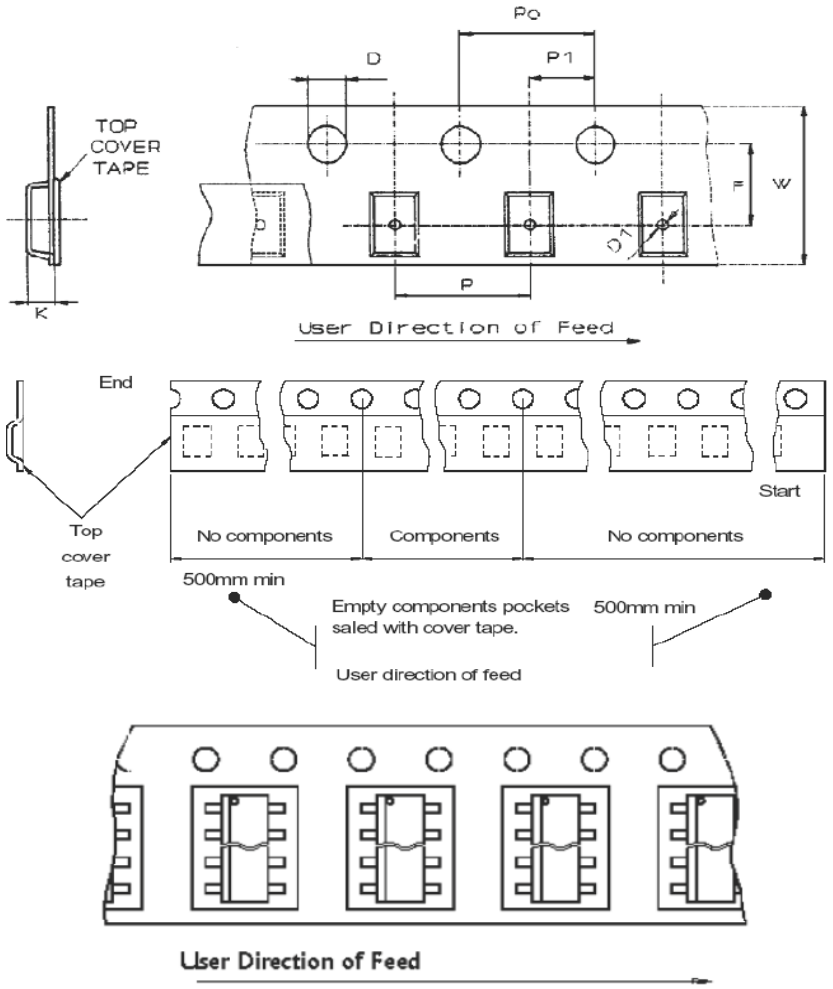


Table 13. **PowerSSO24, tape dimension**

Description	Symbol	Value
Tape width	W	24
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	12
Hole diameter	D (± 0.05)	1.55
Hole diameter	D1 (min.)	1.5
Hole position	F (± 0.1)	11.5
Compartment depth	K (max.)	2.85
Hole spacing	P1 (± 0.1)	2

Note: All dimensions are in mm.

Note: According to the Electronic Industries Association (EIA) standard 481 rev. A, Feb 1986.

15 Ordering information

Table 14. **Order codes**

Order code	Package	Package marking	Packaging
VNI4140K	PowerSSO-24	VNI4140K	Tube
VNI4140KTR			Tape and reel
VNI4140K-32		VNI4140K-32	Tube
VNI4140KTR-32			Tape and reel

Revision history

Table 15. **Document revision history**

Date	Version	Changes
05-Oct-2021	1	Initial release.
22-Nov-2023	2	Changed $R_{DS(on)}$ test conditions for VNI4140K-32 in Table 5; some minor changes.

Contents

List of tables

List of figures