AN3455

1000BASE-T Transmitter Distortion

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INTRODUCTION

This application note provides detailed information about the 1000BASE-T distortion behavior of Microchip PHYs. For more information about IEEE standards, see IEEE 802.3-2008, clause 40.6 PMA electrical specifications. For more information about the Tektronix® TDSET3 Ethernet test compliance software manual, see http://www.tek.com/manual/tdset3-ethernet-test-compliance-software-printed-help-document.

The 1000BASE-T transmitter distortion test checks the accuracy of all 17 analog signal levels transmitted over the CAT5 media and ensures those levels are sufficiently accurate in the middle of the unit interval (UI) (that is, the middle of the eye). That check guarantees a receiver that is correctly locked in the middle of the UI can recover the analog level corresponding to a specific symbol sent from its link partner's transmitter.

When distortion versus phase offset is not plotted, the peak transmitter distortion figure reported does not tell the location of the peak within the UI. Most likely, that distortion is located on the signal edges and is irrelevant for the system's performance. Moreover, the reported distortion figure does not provide any information about the distortion around the middle of the eye, which is critical to message bit error rate.

For more than a decade, all Gigabit PHYs in the Ethernet industry have been successfully designed and tested with the 1000BASE-T distortion test using the best-phase approach evaluated at the eye midpoint. Before IEEE 802.3-2008 introduced a 60% UI minimum for peak distortion compliance, all available interoperability and Ethernet compliance software within the industry, such as Tektronix TDSET3 Ethernet compliance software, tested in accordance with the best-phase approach.

For Microchip VSC PHYs, the 1000BASE-T transmitter, operating in enhanced mode, will greatly exceed the IEEE 802.3-2008 distortion specification. However, the enhanced mode of operation sacrifices power efficiency in order to decrease slew-rate-induced distortion with no benefit to system performance. Therefore, the enhanced mode of operation is not recommended.

1000BASE-T TRANSMITTER TEST MODES

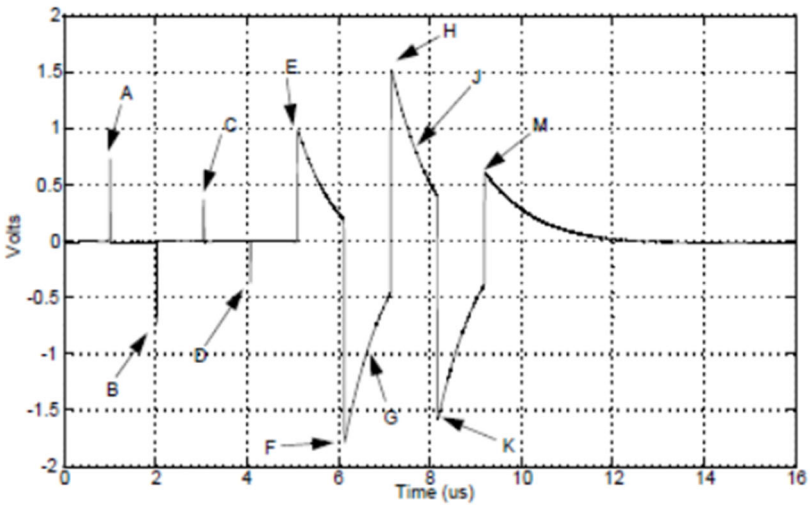
Two 1000BASE-T test modes help explain the transmitter distortion constraints:

- Transmitter Test Mode 1
- Transmitter Test Mode 4

Transmitter Test Mode 1

Figure 1 shows the waveform tested in Transmitter Test Mode 1, as it is described in Figure 40-19 of IEEE 802.3-2008.

FIGURE 1: TRANSMITTER TEST MODE 1

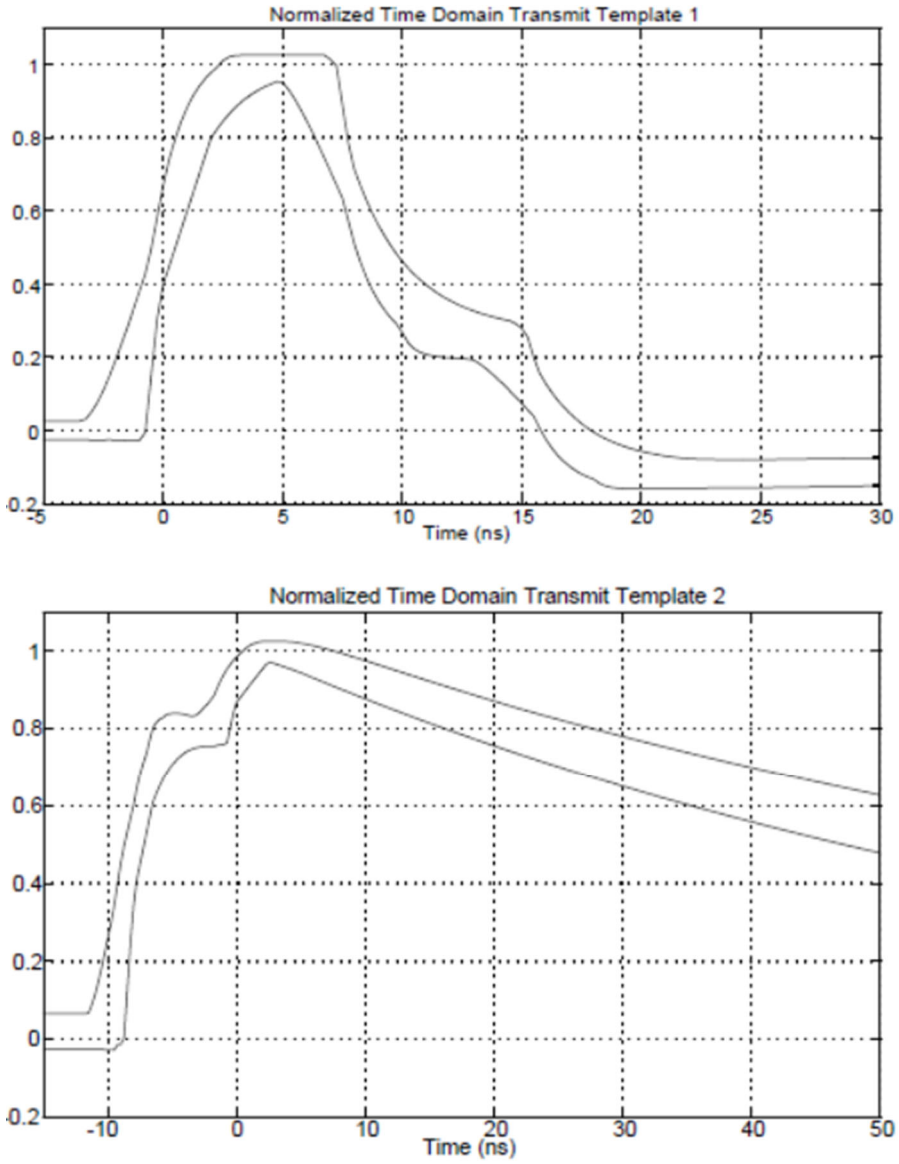


This test mode checks for the following:

- Absolute accuracy of the amplitude of the signal for the positive and negative pulses (40.6.1.2.1)
- Symmetry of the positive and negative pulses (40.6.1.2.1)
- Shape of all the pulses (40.6.1.2.3)

The shape of the pulses is checked by using very tight templates from IEEE 802.3-2008 Figure 40-26, as seen in Figure 2.

FIGURE 2: NORMALIZED TRANSMIT TEMPLATES



Note 1: The horizontal opening of the templates around the 0.4 vertical value is about 1.25 ns, which means that the edge rates of the signal are set with accuracy much better than 1 ns.

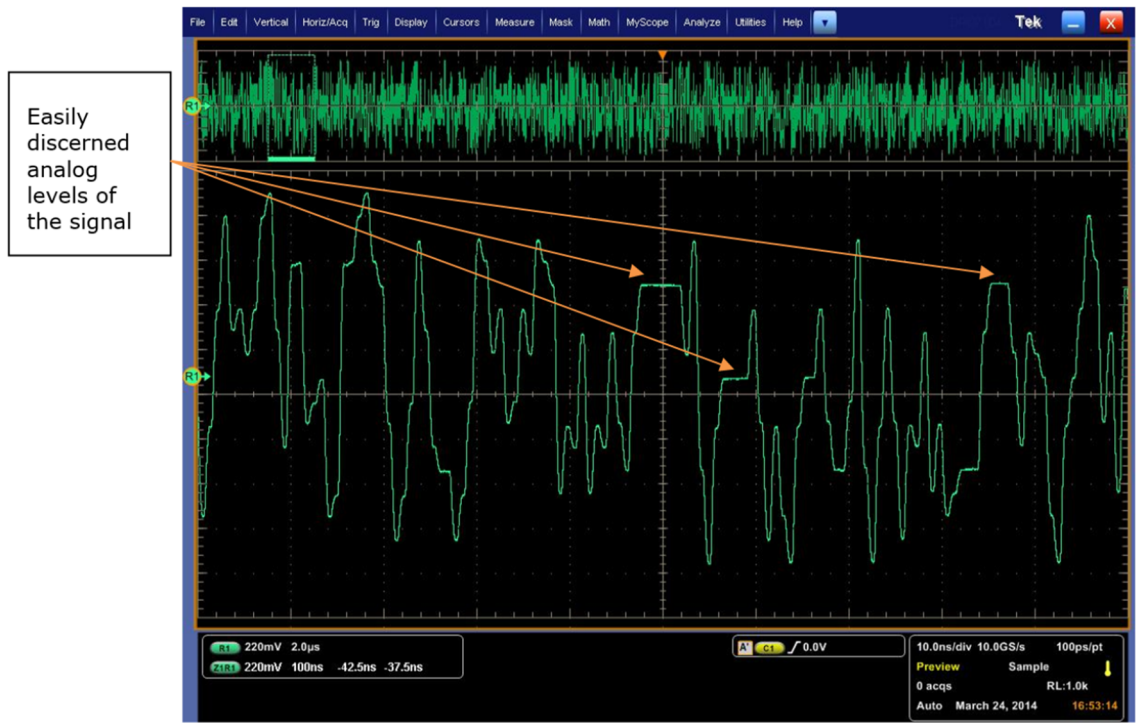
2: According to IEEE 802.3-2008 Figure 40-19, the signal is checked against 11 different templates, identified as templates A to M. Conformance with these templates guarantees that the spectral content of the signal induced by the rise and fall times of the signal will not create EMI issues.

Microchip PHYs pass the amplitude and matching tests with good margin and excellent conformance for the template tests.

Transmitter Test Mode 4

This test is described in IEEE 802.3-2008, subsection 40.6.1.24. A representative waveform associated with this test, which is acquired from a Microchip PHY, is shown in Figure 3.

FIGURE 3: TRANSMITTER TEST MODE 4 WAVEFORM



The top part of the oscilloscope trace shows the entire 2047-symbol waveform required by the standard, and the bottom part zooms in on a portion of the signal bracketed in the top part. The distortion test is defined in subsection 40.6.1.24 by a MATLAB routine that is not reproduced here, but can be found at http://ieee802.org/3/publication/ab/distortion.m.txt. For the purpose of this application note, it should be noted that the MATLAB code:

- describes an ideal signal that is 2047 symbols long with 17 levels that are generated after PAM-5 encoding and shaping through the transmit shaping filter, as seen in the zoomed part of illustration.
- determines a best-fit waveform by post-processing the acquired signal.
- computes the distortion as deviation of the acquired signal from the best-fit waveform.

The distortion is computed for all 2047 symbols. For each symbol, distortion is computed at a different time instance or arbitrary phase during a unit interval (same as a transmit clock period). For each phase, the maximum error constitutes the distortion. According to IEEE 802.3-2008, “A PHY is considered to pass this test if the peak distortion is below 10 mV for at least 60% of the UI within the eye opening.”

TRANSMITTER DISTORTION EXPLAINED

As explained in Transmitter Test Mode 1, the absolute amplitude accuracy and the shape of the signal are fully checked using the Test Mode 1 signal. Because the 1000BASE-T transmission is PAM-based, a test that checks for the accuracy of all amplitude levels used in the PAM encoding should exist. That is what the 1000BASE-T distortion test does.

The 1000BASE-T transmitter distortion test checks the accuracy of all 17 analog levels and ensures those levels are sufficiently accurate in the middle of the UI. That check guarantees a receiver that is correctly locked in the middle of the UI can recover the analog level corresponding to a specific symbol sent from its link partner's transmitter.

Prior to the IEEE 802.3-2008 revision of the transmitter distortion specification, oscilloscope Ethernet compliance software (such as Tektronix's TDSET3) measured and reported as its 1000BASE-T distortion result the level error associated with a single phase, namely the best locking phase in the middle of the UI.

Since the introduction of the 802.3-2008 amendment, oscilloscope vendors have been updating Ethernet compliance software to check distortion across the entire UI for 40 phases (for example, TDSET3 version 3.2.5 used for this report). It should be stressed that for more than a decade, all Gigabit PHYs in the Ethernet industry have been designed and tested with the 1000BASE-T distortion test using the original best-phase approach. Thus, the original best-phase approach was acceptable for 1000BASE-T PHY adoption in the marketplace, as demonstrated by over a decade of 1000BASE-T proliferation prior to the IEEE 802.3-2008 amendment.

MEASURING 1000BASE-T DISTORTION USING ETHERNET COMPLIANCE SOFTWARE

The following sections describe the results from measuring the 1000BASE-T distortion using Ethernet compliance software.

Result #1: 100% of UI Passed

Figure 4 shows the distortion results for a Microchip PHY, as reported by the TDSET3 version 3.2.5 build 5. The report shows that for all 40 phases, the distortion is below 10 mV. The peak distortion is reported as 7.792 mV.

FIGURE 4: ETHERNET COMPLIANCE REPORT FOR 100% OF THE UI PASSING

However, the report does not tell the location of the distortion within the UI. Most likely, that distortion is located on the signal edges and is irrelevant for the system's performance.

Result #2: Less Than 100% of UI Passed

Figure 5 shows another Ethernet compliance report for a Microchip PHY that passes the transmitter distortion test over less than 100% of the UI.

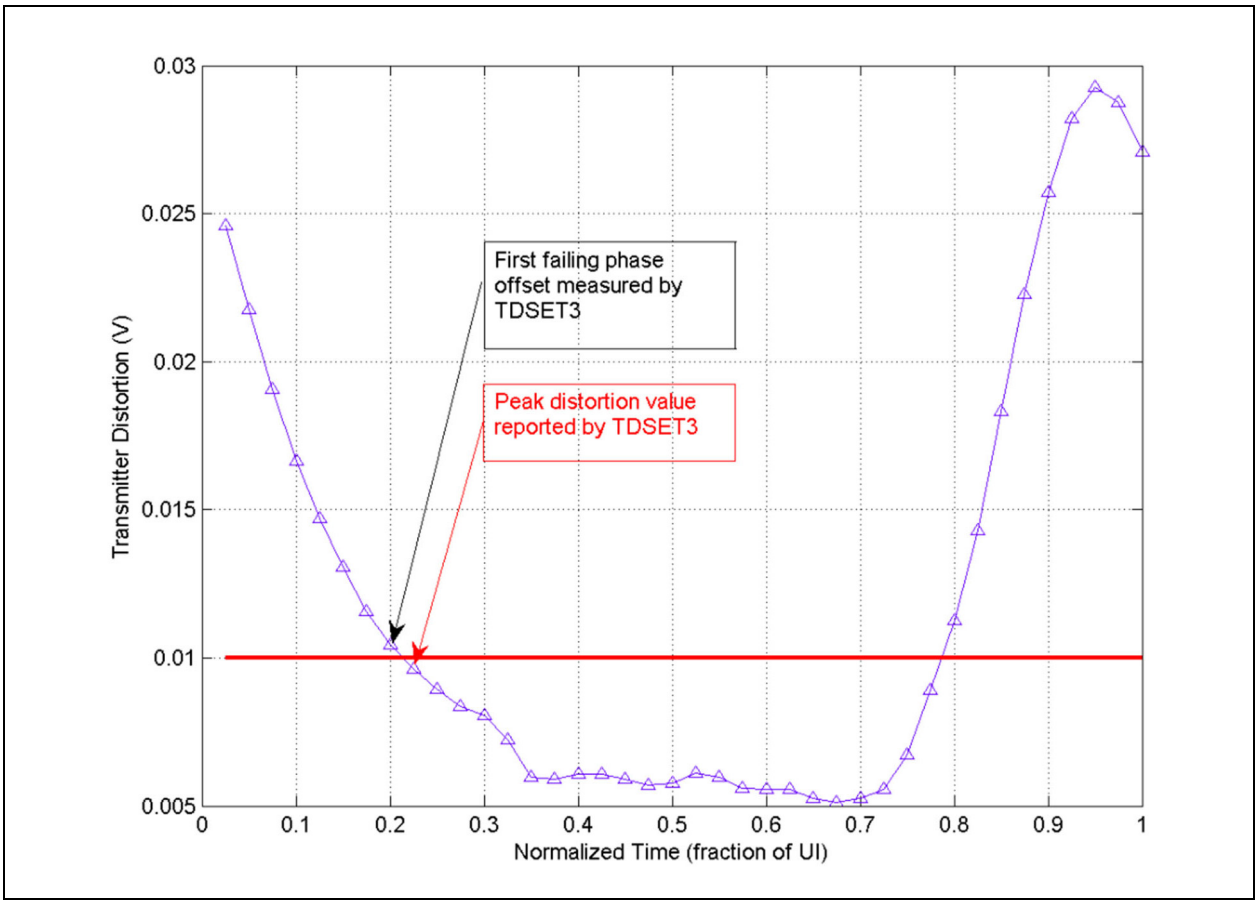
FIGURE 5: ETHERNET COMPLIANCE REPORT FOR LESS THAN 100% OF THE UI PASSING

The previous report states the PHY passes for 85% of the tested phases and that the peak distortion is 9.982 mV. The 85% value (34 out of 40) is correct.

A distortion figure of 9.982 mV versus a 10 mV maximum value suggests a very marginal pass. Strictly speaking, the 9.982 mV figure is also correct but is irrelevant.

To provide better meaning to the distortion result, a plot of measured distortion versus phase within a UI should be reported. Such a plot for a Microchip PHY that is generated using internal software is shown in Figure 6.

FIGURE 6: TRANSMITTER DISTORTION VERSUS UI-NORMALIZED PHASE

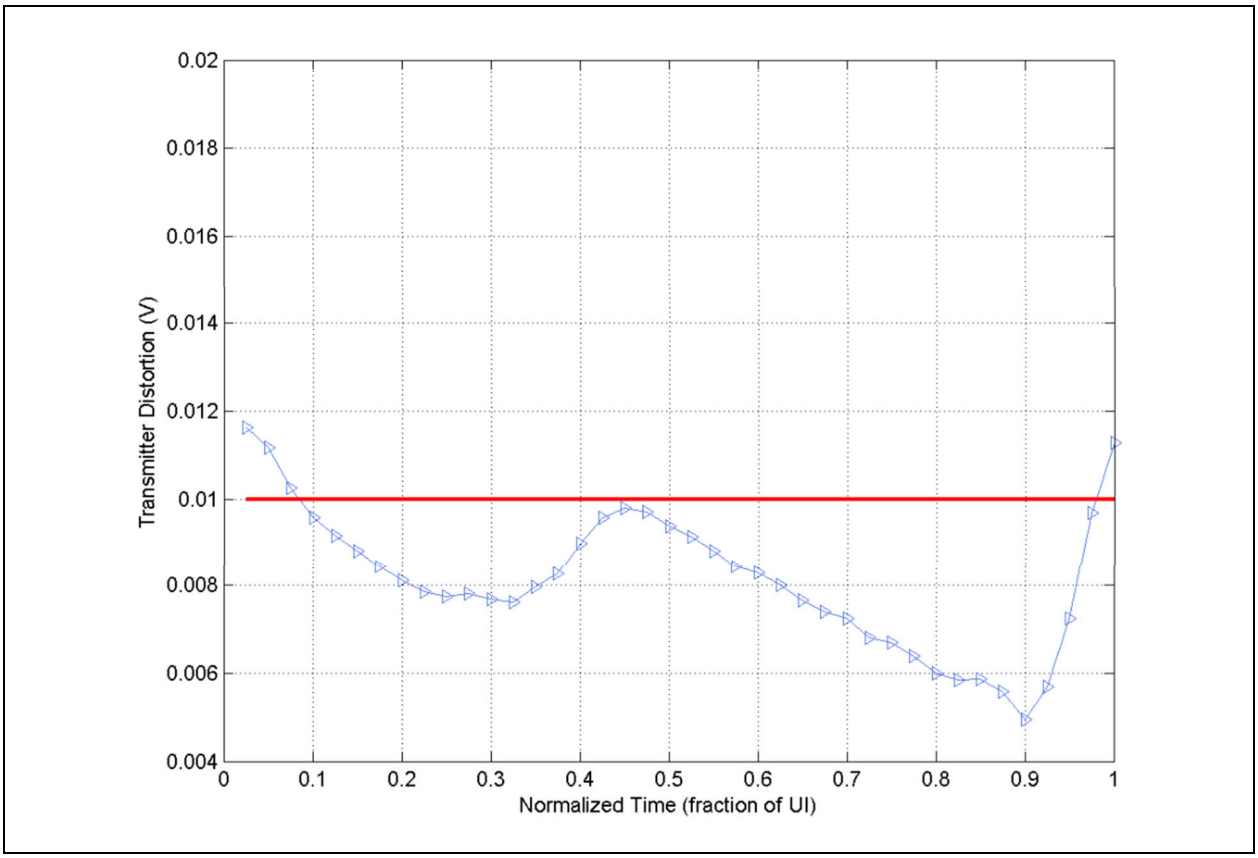


The red arrow indicates the peak distortion value reported by the oscilloscope. It is the last passing value before the first failing value as the black arrow indicates. It can be seen that if the number of phase offsets were increased to several hundreds, the reported figure of distortion would always be 9.999 mV.

Moreover, the reported distortion illustration does not provide any information about the distortion around the middle of the eye, which is a very good value of 5.8 mV in this case. As previously discussed, old versions of Ethernet compliance oscilloscope software (for example, TDSET3 version 3.2.1) would have reported the best-phase distortion value instead of 9.982 mV. In accordance with the transmitter distortion requirement prior to IEEE 802.3-2008, the best-phase value (5.8 mV) would be a well-understood figure of merit for evaluating a digital communications system, to the extent that it provides useful information about the vertical opening of the eye.

Figure 7 shows another distortion plot acquired at Microchip labs from a 1000BASE-T PHY. In this situation, TDSET3 reports a passing 36 phases out of 40 (that is, 90% of the UI). However, this case is technically a marginal distortion result, as can be seen from careful study of measured distortion versus phase instead of the peak value. The distortion in the eye's middle is 9.8 mV and does not improve to less than 8 mV for a ±15% UI range around the middle of the eye.

FIGURE 7: TRANSMITTER DISTORTION PASSING OVER 90% OF THE UI

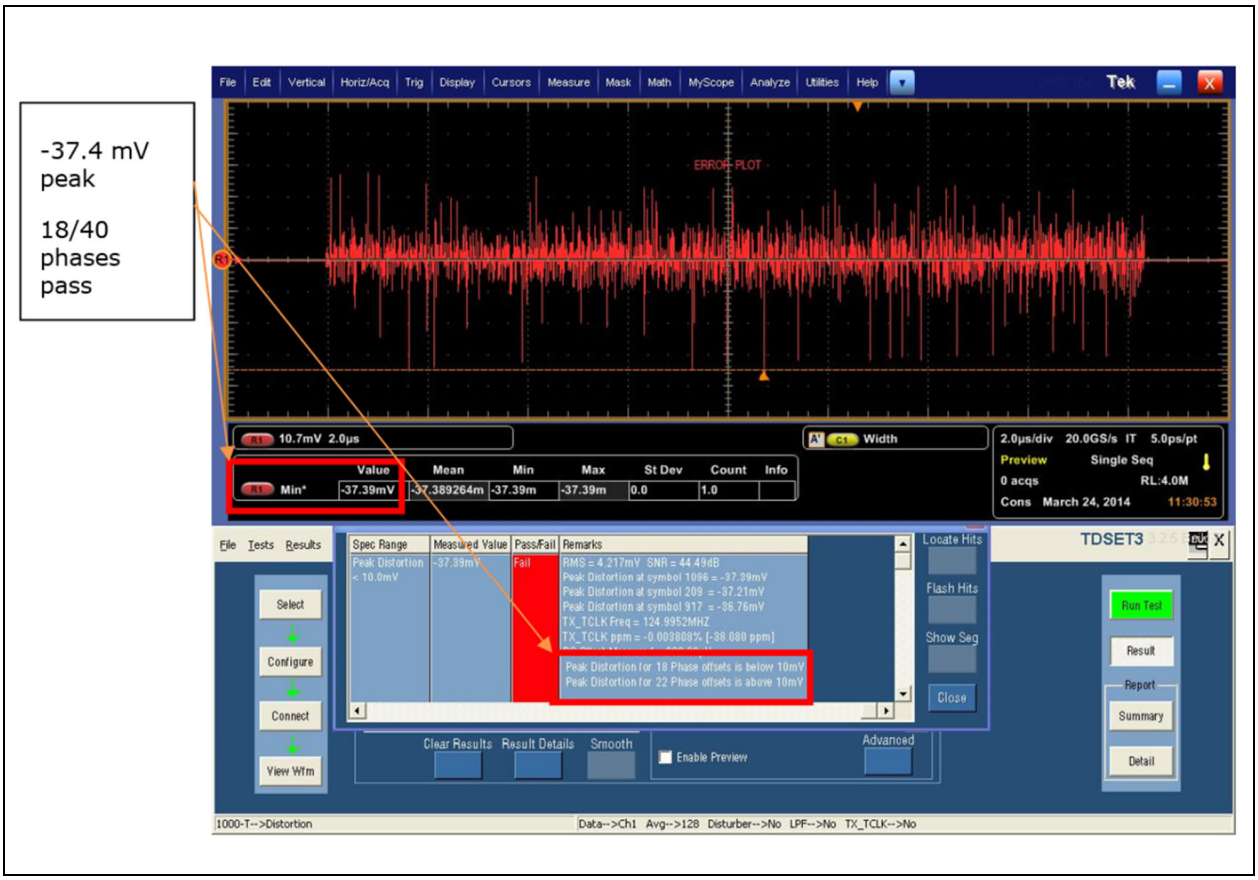


The two previous examples show that reporting a peak distortion figure rather than an actual measured distortion versus phase offset plot is irrelevant when evaluating transmitter distortion. Moreover, that data does not provide critical information about distortion in the middle of the eye, where it would have direct impact on receiver performance.

Result #3: Distortion Tests Failed

Figure 8 shows a typical Ethernet compliance report for a PHY failing the distortion test.

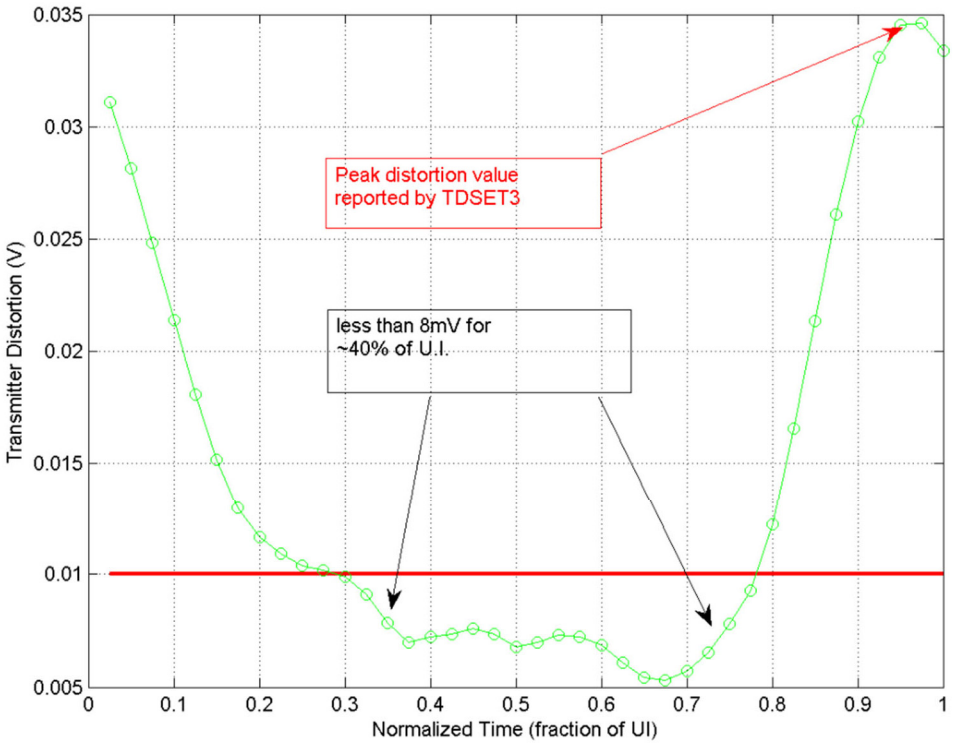
FIGURE 8: ETHERNET COMPLIANCE REPORT FOR A FAILING UI (LESS THAN 60% OF UI)



The report shows the PHY passes for 18 phases, along with a distortion figure of 37.4 mV. Such a distortion peak value is huge and, if it actually corresponds to a symbol sampling point, would be of real concern. In fact, no practical communications system would work in the presence of such a huge received symbol distortion.

Figure 9 shows the actual distortion behavior behind the result. In this case, the peak distortion figure as the oscilloscope reports is the highest value within the UI, indicated by the red arrow.

FIGURE 9: TRANSMITTER DISTORTION FAILING MORE THAN 60% OF UI



The actual distortion around the eye's midpoint is 7.5 mV and remains less than 8 mV for almost 40% of the UI. The peak distortion of 37 mV appears at the symbol edge, which is far from the eye opening, and is thus irrelevant. The distortion at the symbol edge has no impact on system functionality.

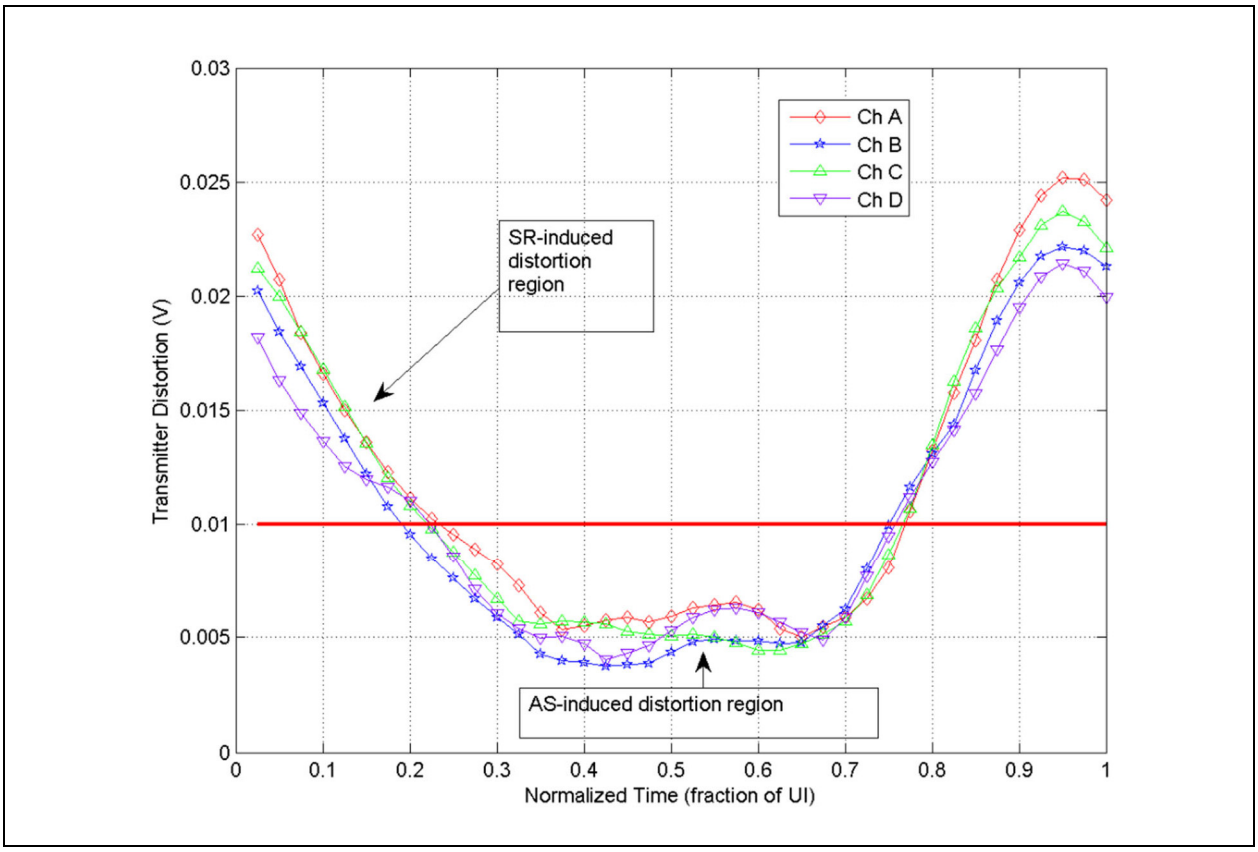
1000BASE-T TRANSMITTER DISTORTION BEHAVIOR

The following sections describe the 1000BASE-T distortion behavior for Microchip 1000BASE-T transmitters.

1000BASE-T Distortion in Normal Operation Mode

In the Normal Operation mode, a Microchip 1000BASE-T transmitter may marginally fail the distortion test in its most recent measurement method. Figure 10 shows a typical plot for a complete PHY port (channels A, B, C, and D). The average distortion in the middle of the eye is approximately 5 mV, and the distortion is flat for 15% of the UI range around the midpoint of the eye.

FIGURE 10: TYPICAL DISTORTION FOR MICROCHIP PHY IN NORMAL OPERATION MODE



There are two very distinct distortion mechanisms observable in the UI:

- Slew rate-induced (SR) distortion
- Amplitude settling-induced (AS) distortion

SR distortion appears during signal transients (at rise and fall times). In today's industry-standard circuit solution, SR distortion directly depends on the transmitter bias current. The only way to reduce SR distortion is to increase the transmitter bias current. However, SR distortion performance is not integral to signal recovery.

On the other hand, AS distortion is observed in the middle of the eye (where the amplitude level is settled). The AS distortion is important for signal recovery. The AS distortion also depends on the bias current, but can be satisfactorily improved (with a Microchip-proprietary circuit solution) in the middle of the eye with a significantly lower bias level than the industry-standard.

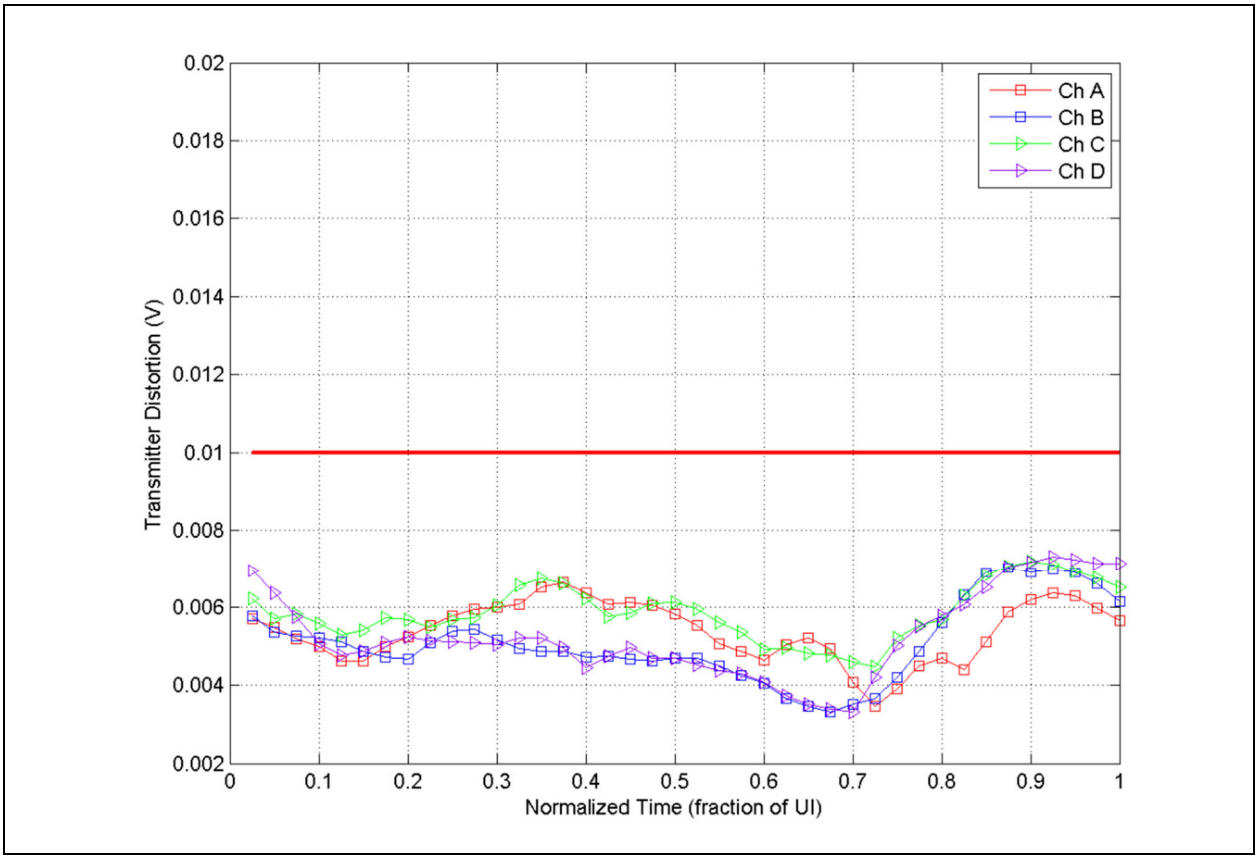
However, achieving an efficient bias level with a satisfactory amount of AS distortion also increases SR distortion. Thus, the additional SR distortion does not affect overall system performance. That is a deliberate power versus percent UI distortion trade-off, which offers a solid distortion figure for Microchip PHYs along with the lowest 1000BASE-T transmitter power consumption figure in the industry.

Extensive system-level, validation, and characterization tests have been conducted using a bias level corresponding to Normal Operation mode. Furthermore, extensive system-level tests have been conducted using the bias corresponding to Normal Operation mode. All tests proved that Microchip PHYs meet all IEEE 802.3-2008 requirements with ample margin.

1000BASE-T Distortion in Enhanced Operation Mode

Microchip's VSC PHYs have the ability to operate its 1000BASE-T transmitter in a mode that is fully compliant with IEEE 802.3-2008. The distortion plot for the same PHY measured in the previous illustration is shown operating in Enhanced Operation mode in Figure 11.

FIGURE 11: TYPICAL DISTORTION FOR MICROCHIP VSC PHY IN ENHANCED OPERATION MODE

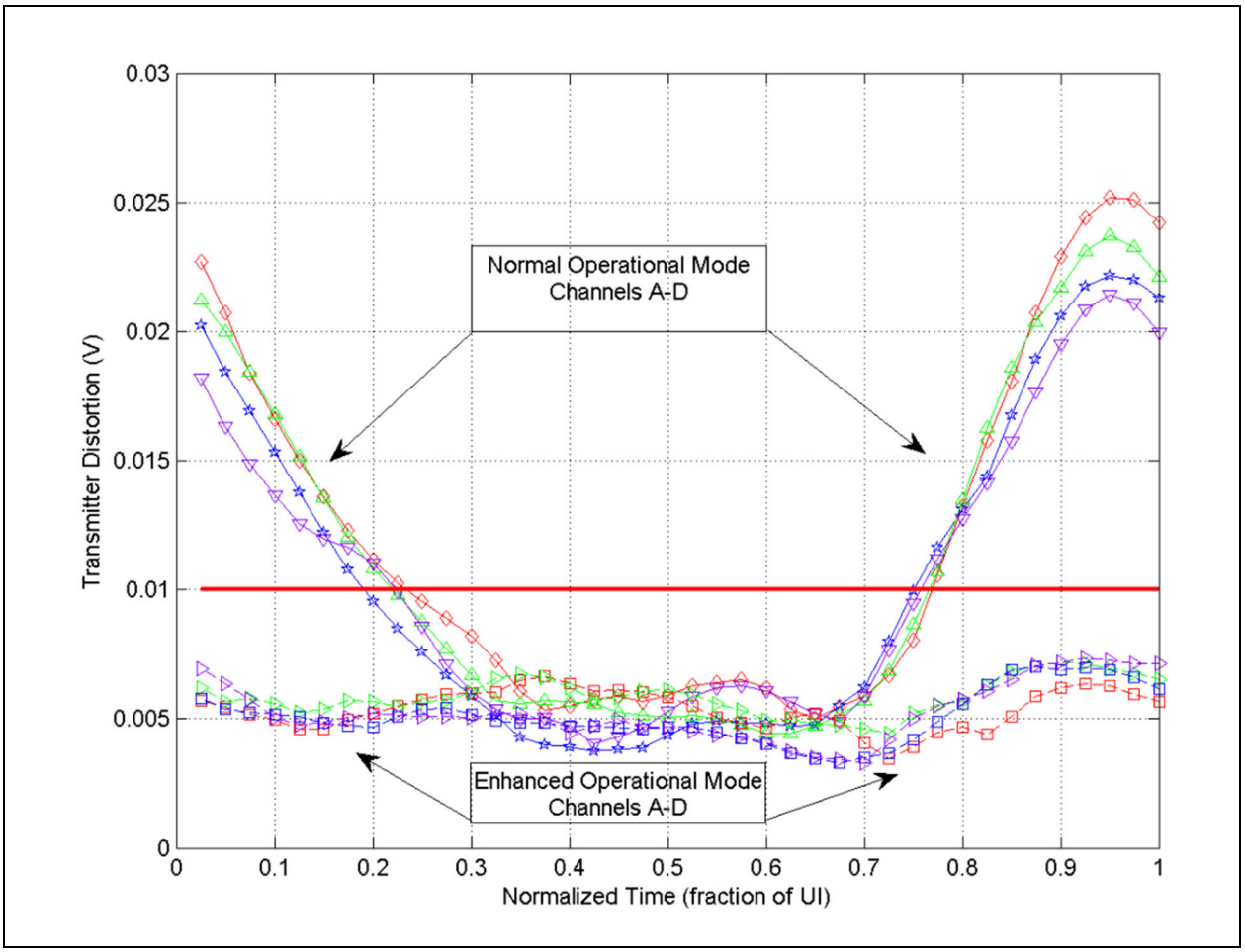


The distortion performance greatly surpasses the IEEE 802.3-2008 requirement, as it passes the 10 mV threshold requirement for 100% of the UI versus the 60% UI required. Overall, the distortion is below 7.5 mV for every phase offset and is approximately 5 mV in the middle of the eye.

DISTORTION BEHAVIOR IN NORMAL VERSUS ENHANCED OPERATION MODE

To analyze the costs and benefits of the two modes of operation, the distortion plots for both modes are overlaid, as seen in Figure 12.

FIGURE 12: COMPARISON OF TYPICAL DISTORTION FOR MICROCHIP VSC PHY: NORMAL VERSUS ENHANCED OPERATION MODES



The distortion in the eye's middle is practically the same for both modes of operation. In other words, additional power burned to reduce SR-induced distortion does not improve system performance. The enhancement of distortion figure flatness far from the eye's midpoint is insignificant whenever the system is phase-locked near the middle of the eye (that is, during normal transceiver operation). The Enhanced Operation mode has no value other than achieving standards-compliance for the distortion test.

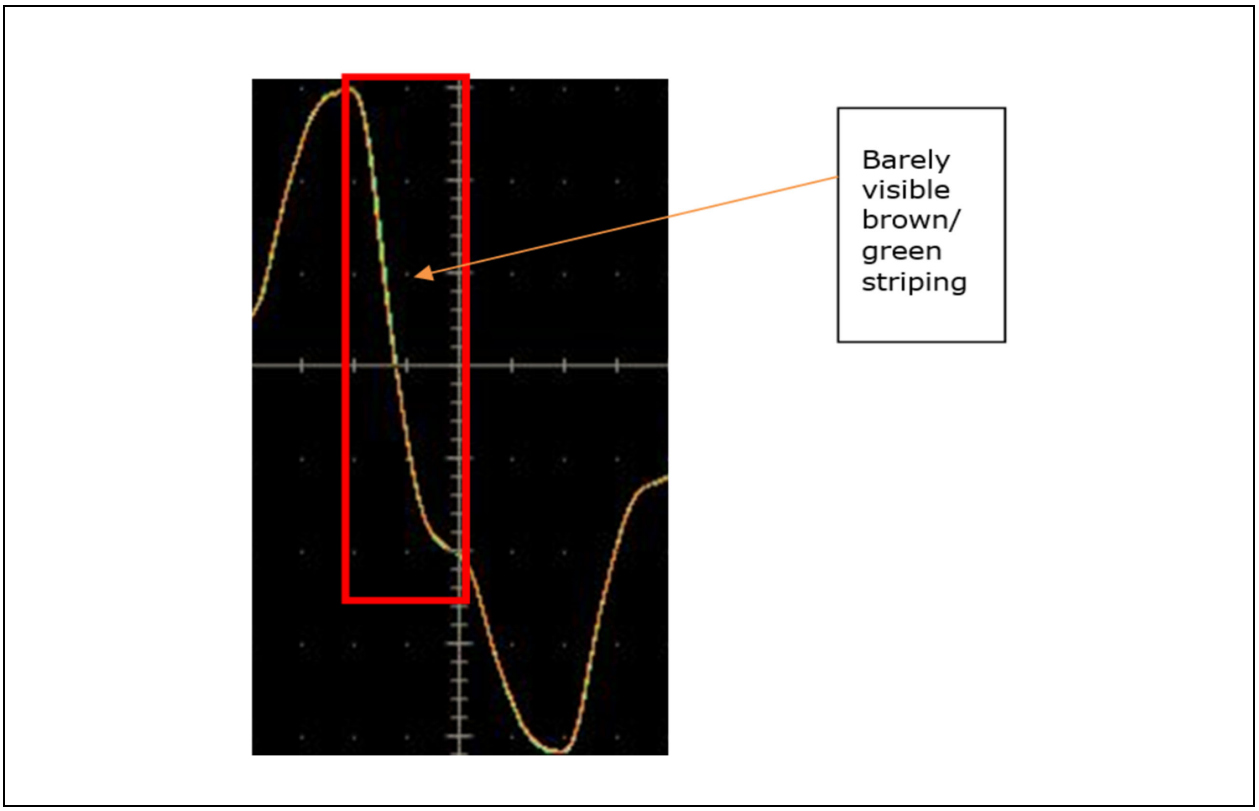
Figure 13 illustrates a waveform comparison of the two modes of operation.

FIGURE 13: COMPARISON OF TEST MODE 4 WAVEFORM: NORMAL VERSUS ENHANCED OPERATION MODE

The zoomed portion of the oscilloscope screenshot shows no practical difference in the Test Mode 4 waveform between the two operational modes. In fact, the slight difference corresponding to the SR-induced distortion region is hardly noticeable as vertical “stripe artifacts,” where the green and brown reference waveforms are overlaid, as seen in Figure 12.

Figure 14 shows the Test Mode 4 waveform zoomed in.

FIGURE 14: ZOOMED-IN COMPARISON OF TEST MODE 4 WAVEFORM



CONCLUSION

The 1000BASE-T distortion test was presented in the context of other relevant tests for the IEEE 802.3-2008 standard. The main goal of the distortion test is to check the accuracy of the 17 analog levels used in the 1000BASE-T transmitted signal. The distortion test does not aim to evaluate overall signal shape, which is primarily checked by the template tests in Test Mode 1.

The 1000BASE-T distortion test results obtained from the TDSET3 software (version 3.2.5) have been analyzed and interpreted using a Microchip-generated plot of distortion versus UI phase. The limited usefulness of the peak distortion figure at an arbitrary phase in the UI has been emphasized.

The impact of the Enhanced Operation mode on the 1000BASE-T distortion behavior has been presented in detail and has been contrasted with the Normal Operation mode. The Microchip 1000BASE-T transmitter, operating in Normal Operation mode, may marginally fail IEEE 802.3-2008 distortion specification. However, that has no direct impact on system-level performance or interoperability. Its sole impact is to the IEEE conformance test result.

The Microchip VSC PHY 1000BASE-T transmitter, operating in the Enhanced Operation mode, greatly exceeds IEEE 802.3-2008 distortion specification. However, the Enhanced Operation mode is less power-efficient, and the corresponding distortion improvement has no significance in the overall system performance. Therefore, the Enhanced Operation mode is not recommended.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003455B (09-24-20)	Changed the name of the author to Frederic Deboes.	
DS00003455A (04-16-20)	Initial release	

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