ATA8510/15

ATA8510/15 Industrial Data Sheet

Introduction

The ATA8510/15 is a highly integrated, low-power, Ultra-High Frequency (UHF) Amplitude Shift Keying (ASK)/ Frequency Shift Keying (FSK) Radio Frequency (RF) transceiver with an integrated AVR microcontroller. The ATA8510/15 is divided into three sections:

- RF front-end
- Digital baseband
- Low-power 8-bit AVR microcontroller

The product is designed for the Industrial Scientific and Medical (ISM) frequency bands ranging from 310-318 MHz, 418-477 MHz and 836-956 MHz. The external part count is kept to a minimum due to the very high level of integration in this device. By combining outstanding RF performance with highly sophisticated baseband signal processing, robust wireless communication can be easily achieved. The receive path uses a low-IF architecture with an integrated double quadrature receiver and digitized IF processing. This results in high image rejection and excellent blocking performance. The transmit path uses a closed loop fractional-N modulator with Gauss shaping and pre-emphasis functionality for high data rates. In addition, highly flexible and configurable baseband signal processing allows the transceiver to operate in several scanning, wake-up and automatic self-polling scenarios. For example, during polling, the IC can scan for specific message content (IDs) and save valid telegram data in the FIFO buffer for later retrieval. The device integrates two receive paths that enable a parallel search for two telegrams with different modulations, data rates, wake-up conditions and more.

The ATA8510/15 implements a flexible service configuration concept and supports up to 15 channels. The channels are grouped into five service configurations with three channels each. Three service configurations are located in the EEPROM. Two service configurations are located in the Static Random Access Memory (SRAM) to allow On-the-Fly (OTF) modifications during IDLEMode via Serial Programming Interface (SPI) commands or application software. The application software is located in the Flash for the ATA8510. Highly configurable and autonomous scanning capability enables flexible polling scenarios with up to 15 channels. The configuration of the transceiver is stored in a 1024-byte EEPROM. The SPI interface enables external control and device reconfiguration.

Table 1. Program Memory Comparison of the ATA8510/15 Devices

Device	Firmware ROM	User Flash	User ROM
ATA8510	24 Kbytes	20 Kbytes	—
ATA8515	24 Kbytes	—	—

In the ATA8510, use the internal microcontroller with the 20-Kbyte user Flash to add custom extensions to the firmware. The ATA8515 embeds only the firmware ROM without the user memory.

The debugWIRE and the In-System Programming (ISP) interface are available for programming purposes.

Compatibility to the ATA8210/15 and the ATA8710

The ATA8510/15 is pin-to-pin compatible with the ATA8210/15 receivers and the ATA8710 transmitter. The RX performance of the receivers and TX performance of the transmitter matches with the transceivers.

Features

- AVR microcontroller core with 1-Kbyte SRAM and 24-Kbyte RF library in firmware (ROM)
- ATA8510 – 20-Kbyte of user Flash
- ATA8515 – No user memory – RF library in firmware only
- Supported frequency ranges
  - Low-band – 310-318 MHz, 418-477 MHz
  - High-band – 836-956 MHz
  - 315.00 MHz/433.92 MHz/868.30 MHz and 915.00 MHz with one 24.305 MHz crystal
- Low current consumption
  - 9.8 mA for RXMode (Low-Band), 1.2 mA for 21 ms cycle three-channel polling
  - 9.4 mA/13.8 mA for TXMode (Low-Band, P_{OUT} = 6 dBm/10 dBm)
- Typical OFFMode current of 5 nA (maximum 600 nA at Vs = 3.6V and T = 85°C)
- Programmable output power -12 dBm to +14.5 dBm (0.4 dB step)
- Supports the 0 dBm class of ARIB STD-T96
- ASK shaping to reduce the spectral bandwidth of modulated PA output signal
- Input 1 dB compression point
  - -48 dBm (full sensitivity level)
  - -20 dBm (active antenna damping)
- Programmable channel frequency with fractional-N PLL
  - 93 Hz resolution for Low-Band
  - 185 Hz resolution for High-Band
- FSK deviation ±0.375 kHz to ±93 kHz
- FSK sensitivity (Manchester coded) at 433.92 MHz
  - -108.5 dBm at 20 Kbit/s, Δf = ±20 kHz and BW_{IF} = 165 kHz
  - -111 dBm at 10 Kbit/s, Δf = ±10 kHz and BW_{IF} = 165 kHz
  - -114 dBm at 5 Kbit/s, Δf = ±5 kHz and BW_{IF} = 165 kHz
  - -122.5 dBm at 0.75 Kbit/s, Δf = ±0.75 kHz and BW_{IF} = 25 kHz
- ASK sensitivity (Manchester coded) at 433.92 MHz
  - -110.5 dBm at 20 Kbit/s BW_{IF} = 80 kHz
  - -125 dBm at 0.5 Kbit/s BW_{IF} = 25 kHz
- Programmable RX-IF bandwidth 25 kHz to 366 kHz (approximately 10% steps)
- Blocking (BW_{IF} = 165 kHz): 64 dBc at frequency offset = 1 MHz and 48 dBc at 225 kHz
- High image rejection: 55 dB at 315 MHz/433.92 MHz and 47 dB at 868.3 MHz/915 MHz without calibration
- Supported data rate in buffered mode 0.5 Kbit/s to 80 Kbit/s (120 Kbit/s NRZ)
- Supports pattern-based wake-up and start of frame identification
- Flexible service configuration concept with on-the-fly (OTF) modification (in IDLEMode) of SRAM service parameters (data rate, …)
  - Each service consists of
    - One service-specific configuration part
    - Three channel-specific configuration parts
  - Three service configurations are located in EEPROM
  - Two service configurations are located in SRAM and can be modified via SPI or embedded application software
- Digital RSSI with very high relative accuracy of ±1 dB thanks to digitized IF processing
- Programmable clock output derived from crystal frequency
- 1024-byte EEPROM data memory for transceiver configuration
- SPI interface for RX/TX data access and transceiver configuration
- 500-Kbit SPI data rate for short periods on the SPI bus and host controller
- On demand services (SPI or API) without polling or telegram reception

- Integrated temperature sensor
- Self-check and calibration with temperature measurement
- Configurable EVENT signal indicates the status of the IC to an external microcontroller
- Automatic antenna tuning at TX center frequency for loop antenna
- Automatic low-power channel polling
- Flexible polling configuration concerning timing, order and participating channels
- Fast RX/TX reaction time
- Power-up (typical 1.5 ms OFFMode -> TXMode, OFFMode -> RXMode)
- RXMode <-> TXMode switching (typical 500 µs)
- Supports mixed ASK/FSK telegrams
- Non-byte aligned data reception and transmission
- Software customization
- Antenna diversity with external switch via GPIO control
- Antenna diversity with internal SPDT switch
- Supply voltage ranges from 1.9-3.6V and 2.4-5.5V
- Temperature range -40°C to +85°C
- ESD protection at all pins (±4 kV HBM, ±200V MM, ±750V FCDM)
- Small 5 x 5 mm QFN32 package/pitch 0.5 mm
- Suitable for applications governed by EN 300 220 and FCC part 15, title 47

Table of Contents

1. Quick References

1.1 Reference Documentation

For more details, refer to the following document:

- *ATA8510/15 Industrial User's Guide* (DS50003142)

1.2 Acronyms and Abbreviations

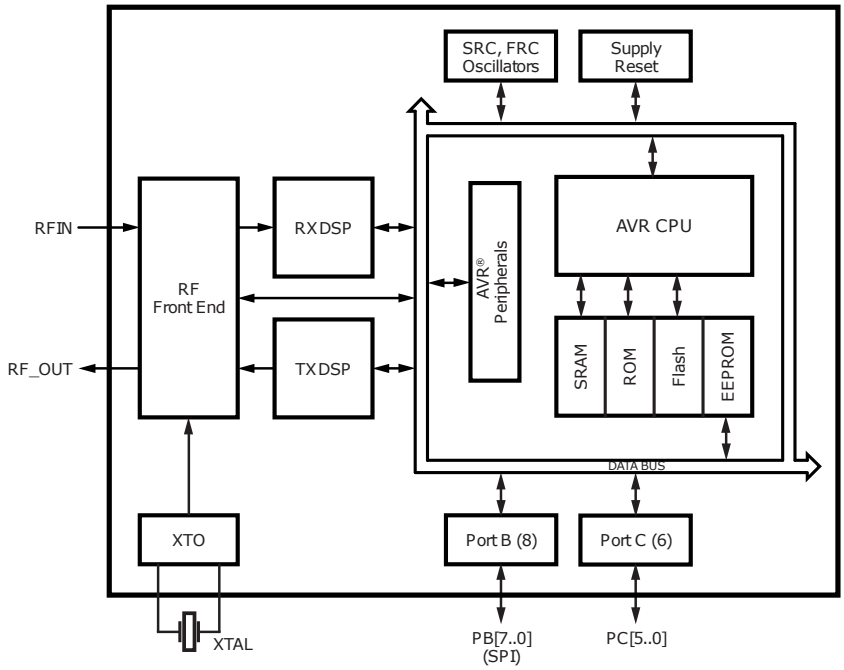
Table 1-1. Acronyms and Abbreviations

Acronyms and Abbreviations	Description
ADC	Analog-to-Digital Converter
ASK	Amplitude Shift Keying
DSP	Digital Signal Processing
EEPROM	Electrical Erasable Programmable Read-Only Memory
FRC	Fast Resistor Capacitor
FSK	Frequency Shift Keying
IF	Intermediate Frequency
ISM	Industrial Scientific and Medical
ISP	In-System Programming
LNA	Low-Noise Amplifier
NRZ	Non-return-to-zero
OOK	On-Off Keying
OTF	On-the-Fly
PA	Power Amplifier
PLL	Phase Locked Loop
RF	Radio Frequency
SPI	Serial Programming Interface
SRAM	Static Random Access Memory
UHF	Ultra-High Frequency
VCO	Voltage Controlled Oscillator
XTO	Crystal Oscillator

2. General Product Description

2.1 System Overview

Figure 2-1. Circuit Overview



The preceding figure shows an overview of the main functional blocks of the ATA8510/15. External control of the ATA8510/15 is performed through the SPI pins SCK, MOSI, MISO and NSS on port B. The configuration of the ATA8510/15 is stored in the EEPROM and a large portion of the functionality is defined by the firmware located in the ROM and processed by the AVR. An SPI command can trigger the AVR to configure the hardware according to settings that are stored in the EEPROM and start up a given system mode (e.g., RXMode, TXMode or PollingMode). Internal events such as “Start of Telegram” or “FIFO empty” are signaled to an external microcontroller on pin 28 (PB6/EVENT).

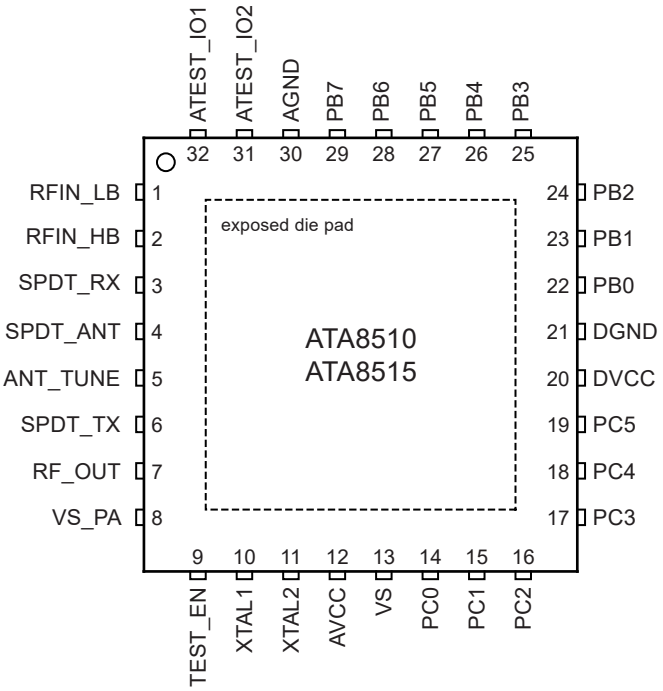
During the start-up of a service, the relevant part of the EEPROM content is copied to the SRAM. This allows faster access by the AVR during the subsequent processing steps and eliminates the need to write to the EEPROM during run-time because parameters can be modified directly in the SRAM. As a consequence, the user does not need to observe the EEPROM read/write cycle limitations.

It is important to note that all PWRON and NPWRON pins (PC1..5, PB4, PB7) are active in OFFMode. This means that even if the ATA8510/15 is in OFFMode and the DVCC voltage is switched off, the power management circuitry within the ATA8510/15 biases these pins with VS.

AVR ports can be used as button inputs, external LNA supply voltage (RX_ACTIVE), LED drivers, EVENT pin, switching control for additional SPDT switches, general purpose digital inputs, wake-up inputs, etc. Some functionality of these ports is already implemented in the firmware and can be activated by adequate EEPROM configurations. Other functionality is available only through custom software residing in the 20-Kbyte Flash program memory (ATA8510).

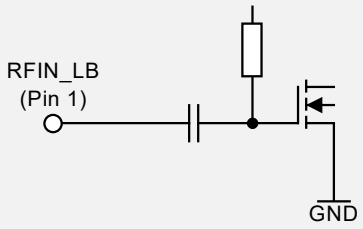
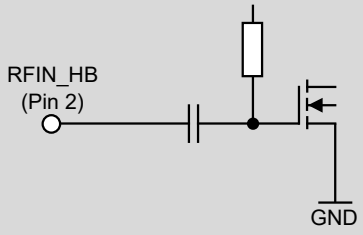
2.2 Pinning

Figure 2-2. Pin Diagram



Note: The exposed die pad is connected to the internal die.

Table 2-1. Pin Description

Pin No.	Pin Name	Type	Equivalent Circuit	Description
1	RFIN_LB	Analog		LNA input for Low-Band frequency range (< 500 MHz)
2	RFIN_HB	Analog		LNA input for High-Band frequency range (> 500 MHz)

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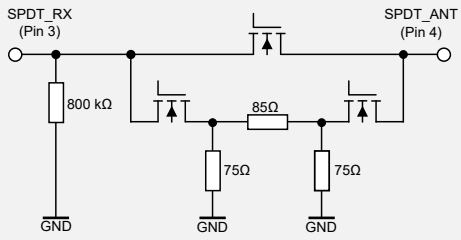
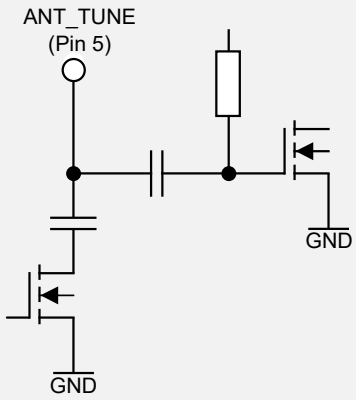
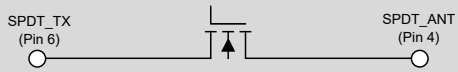
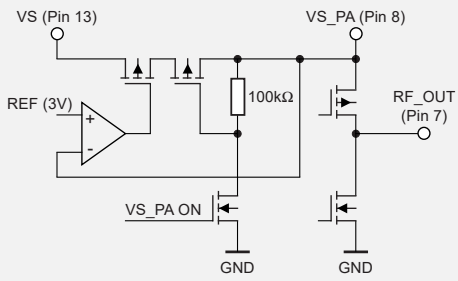
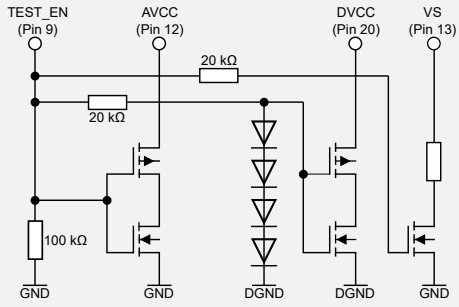
Pin No.	Pin Name	Type	Equivalent Circuit	Description
3	SPDT_RX	Analog		RX switch output (damped signal output)
4	SPDT_ANT	Analog		Antenna input (RXMode) and output (TXMode) of the SPDT switch
5	ANT_TUNE	Analog		Antenna tuning input
6	SPDT_TX	Analog	See also circuit pin 3 and 4 	TX mode input of the SPDT switch
7	RF_OUT	Analog		Power amplifier output
8	VS_PA	Analog		Power amplifier supply • 3V application: supply voltage (VS) input • 5V application: internal voltage regulator output
9	TEST_EN	—		Test enable, connected to GND in application

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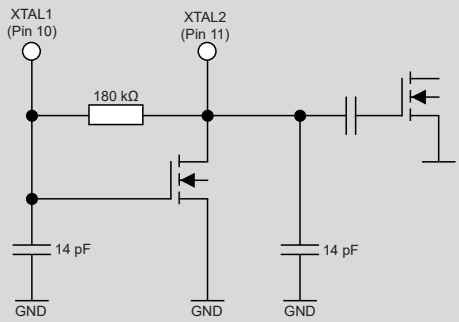
Pin No.	Pin Name	Type	Equivalent Circuit	Description	
10	XTAL1	Analog		Crystal oscillator pin 1 (input)	
11	XTAL2	Analog		Crystal oscillator pin 2 (output)	
12	AVCC	Analog	For more details, refer to 5.1. ESD Protection Circuits	RF front end supply regulator output	
13	VS	Analog	For more details, refer to 5.1. ESD Protection Circuits	Main supply voltage input	
14	PC0	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port C0 :PCINT8/NRESET/DebugWIRE
15	PC1	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port C1 :NPWRON1/PCINT9/EXT_CLK
16	PC2	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port C2 :NPWRON2/PCINT10/TRPA
17	PC3	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port C3 :NPWRON3/PCINT11/TMDO/TxD
18	PC4	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port C4 :NPWRON4/PCINT12/INT0/TMDI/RxD
19	PC5	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port C5 :NPWRON5/PCINT13/TRPB/TMDO_CLK
20	DVCC	—	For more details, refer to 5.1. ESD Protection Circuits	Digital supply voltage regulator output	
21	DGND	—	For more details, refer to 5.1. ESD Protection Circuits	Digital ground	
22	PB0	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port B0 :PCINT0/CLK_OUT
23	PB1	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port B1 :PCINT1/SCK
24	PB2	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port B2 :PCINT2/MOSI (SPI Host Out Client In)
25	PB3	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port B3 :PCINT3/MISO (SPI Host In Client Out)
26	PB4	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port B4 :PWRON/PCINT4/LED1 (strong high side driver)
27	PB5	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port B5 :PCINT5/INT1/NSS
28	PB6	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port B6 :PCINT6/EVENT (firmware controlled external microcontroller event flag)
29	PB7	Digital	For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)	Main Alternate	:AVR Port B7 :NPWRON6/ PCINT7/RX_ACTIVE (strong high side driver)/LED0 (strong low side driver)
30	AGND	—	For more details, refer to 5.1. ESD Protection Circuits	Analog ground	
31	ATEST_IO2	—	—	RF front end test I/O 2 connected to GND in application	

.....continued				
Pin No.	**Pin Name**	**Type**	**Equivalent Circuit**	**Description**
32	ATEST_IO1	—	—	RF front end test I/O 1 connected to GND in application

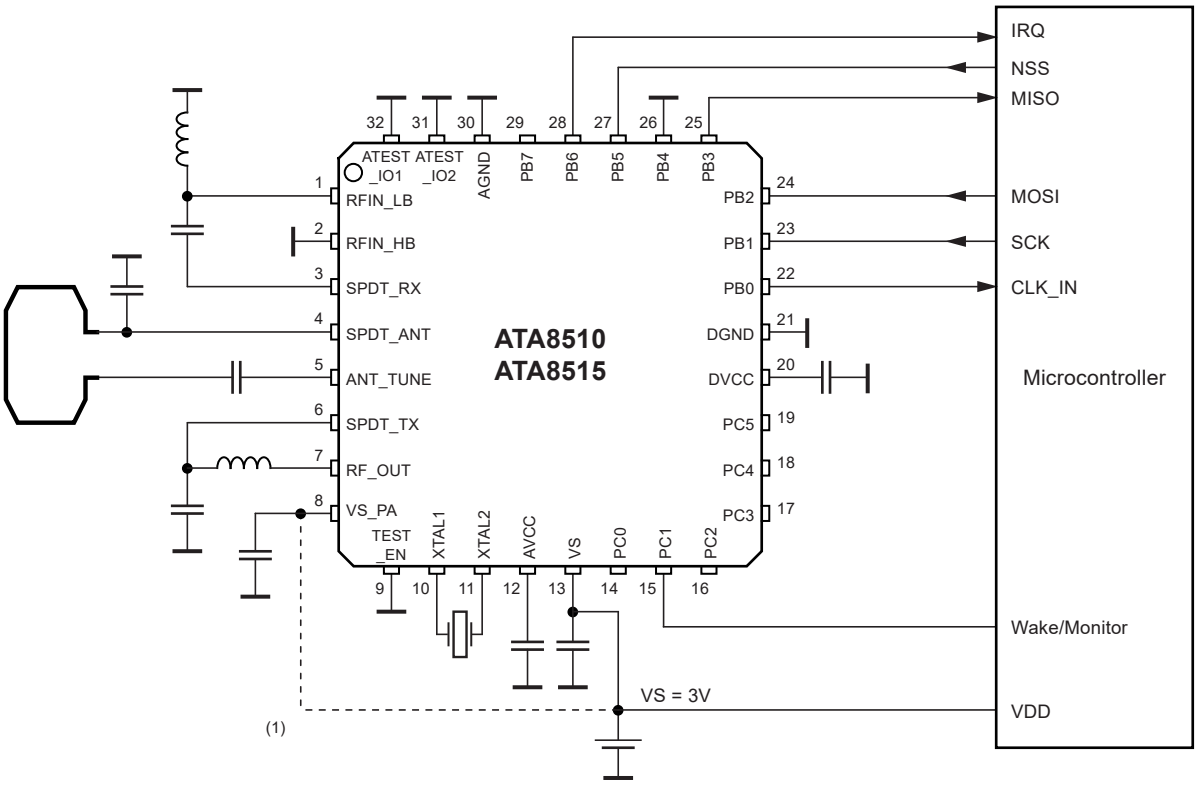
2.3 Typical Applications

The transceiver is designed to be used in the following application areas:

- Home and building automation
- Wireless sensor networks
- Weather stations
- Battery-operated remote controls
- Smoke detectors
- Wireless alarm and security systems
- Remote control systems, e.g., garage door openers
- Smart RF applications
- Telemetering systems

2.3.1 Typical 3V Application with External Microcontroller

Figure 2-3. Typical 3V Application with External Microcontroller



Note:

1. This connection depends on the setting of the bits VS5V and VS22. For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142).

The preceding figure shows a remote control application circuit with an external host microcontroller for the 315 MHz or 433.92 MHz band running from a 3V lithium cell. The ATA8510/15 stays in OFFMode until NPWRON1 (PC1) is used to wake it up. In OFFMode, the ATA8510/15 draws typically less than 5 nA (600 nA maximum at 3.6V/85°C).

In OFFMode, all the ATA8510/15 AVR ports PB0 – PB7 and PC0 – PC5 are switched to input. PC0 – PC5 and PB7 have internal pull-up resistors ensuring that the voltage at these ports is VS. PB0-PB6 are tri-state inputs and require additional consideration. PB1, PB2 and PB5 have defined voltages because they are connected to the output of the external µC. PB4 is connected to ground to avoid unwanted power-ups. PB0, PB3 and PB6 do not require external circuitry because the internal circuit avoids transverse currents in OFFMode. The external µC has to tolerate the floating inputs. Otherwise, additional pull-down resistors are required on these floating lines.

Typically, the key fob buttons are connected to the external µC, and the ATA8510/15 wake-up is done by pulling NPWRON1 (pin 15) to ground. If there are not enough ports for button inputs on the µC, it is possible to connect up to four additional buttons to the ports PC2 – PC5. In this case, the occurrence of a port event (button pressed) generates an event on pin 28. The corresponding port event is available in the event registers.

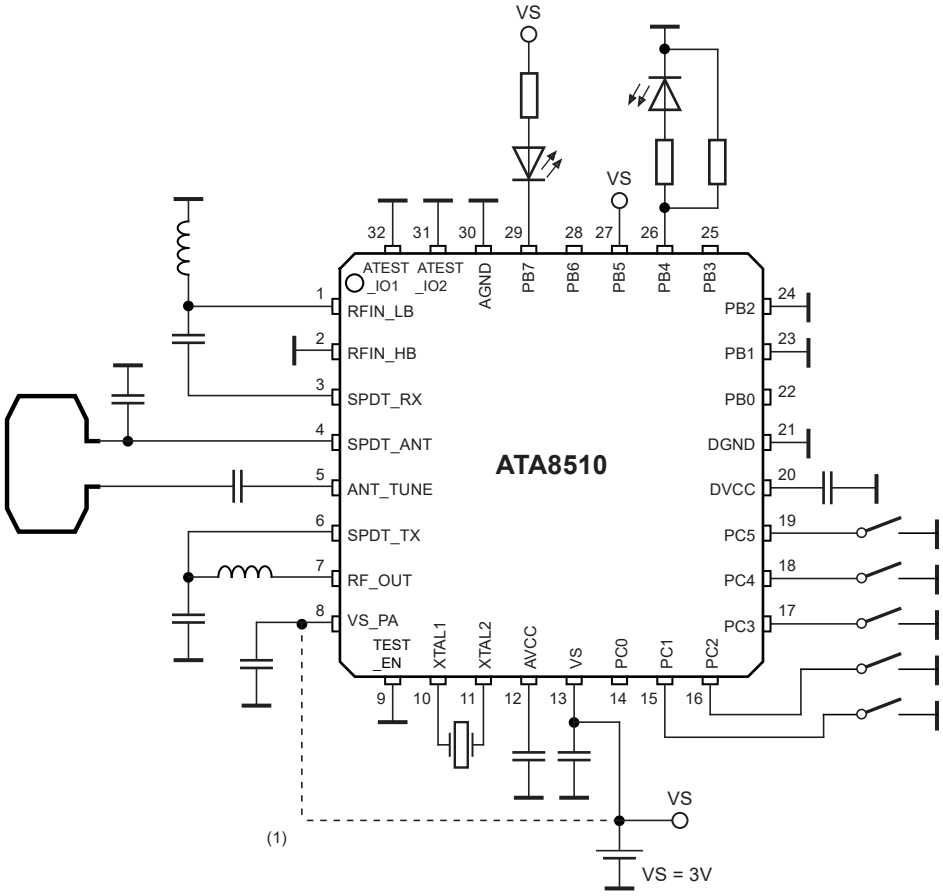
A PCB trace loop antenna is typically used in this type of application. An internal antenna tuning procedure tunes the resonant frequency of this loop antenna to the TX frequency. This is accomplished with an integrated variable capacitor on the ANT_TUNE pin. RF_OUT and RF_IN are optimally matched to the SPDT_TX and SPDT_RX pins of the integrated RX/TX switch. The SPDT_ANT pin has an impedance of 50Ω for both the RX and TX functions. The DC output voltage of the power amplifier is required at the SPDT_TX pin for proper operation. Also, the RFIN pin needs a DC path to ground, which is easily achieved with the matching shunt inductor. The impedance of the loop antenna is transformed to 50Ω with three capacitors, two of them external and one built-in at the ANT_TUNE pin.

Together with the fractional-N PLL within the ATA8510/15, an external crystal is used to fix the RX and TX frequency. Accurate load capacitors for this crystal are integrated to reduce the system part count and cost. Only four supply blocking capacitors are needed to decouple the different supply voltages AVCC, DVCC, VS and VS_PA of the ATA8510/15. The exposed die pad is the RF and analog ground of the ATA8510/15. It is connected directly to AGND via a fused lead. For applications operating in the 868.3 MHz or 915 MHz frequency bands, a High-Band RF input, RFIN_HB, is supplied and must be used instead of RFIN_LB.

The ATA8510/15 is controlled using specific SPI commands via the SPI interface and an internal EEPROM for application-specific configurations.

2.3.2 Typical Stand-Alone Application

Figure 2-4. Typical 3V Stand-Alone Application



Note:

1. This connection depends on the setting of the bits VS5V and VS22. For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142).

The preceding figure shows a stand-alone remote control application circuit for 315 MHz or 433.92 MHz running from a 3V lithium cell. The ATA8510 stays in OFFMode until one of the NPWRON ports PC1 – PC5 is pulled to ground level, waking up the circuit. The NPWRON ports PC1 – PC5 have internal 50 kΩ pull-up resistors. If not in use, the user can leave them open.

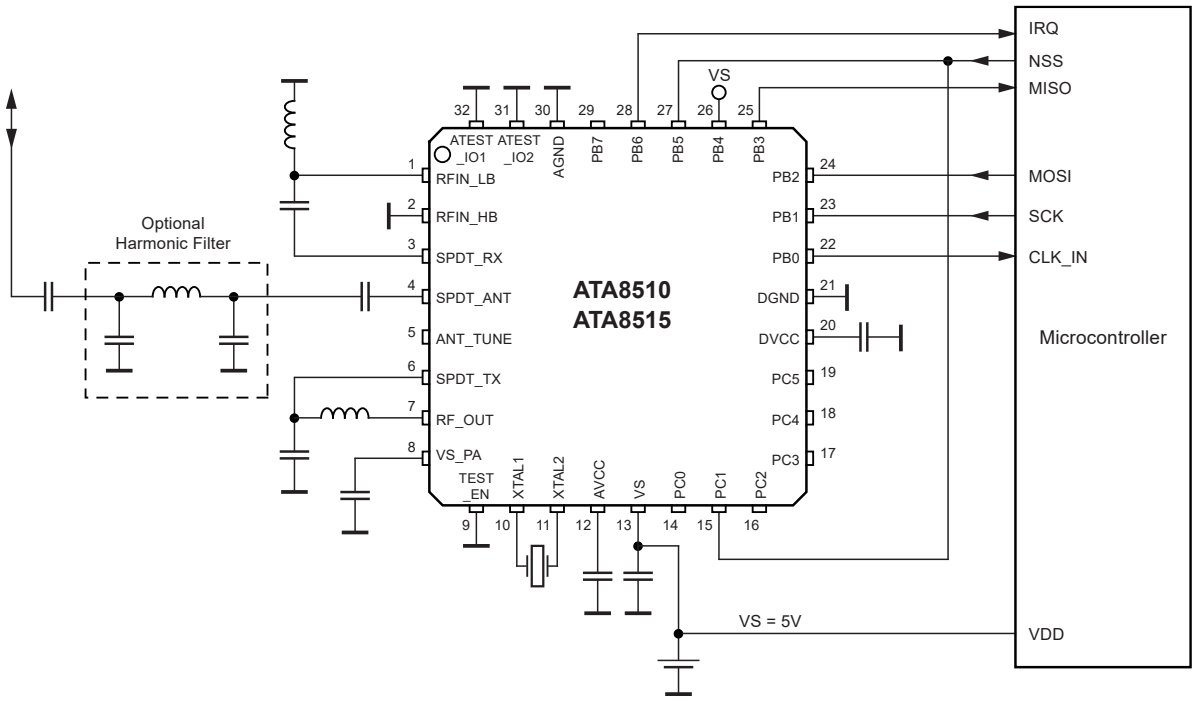
Use the user application software within the 20-Kbyte Flash (ATA8510) to control the ATA8510 transceiver together with the firmware in the 24-Kbyte ROM. The ATA8515 is not suitable for this application. The RF and decoupling circuitry is similar to Figure 2-3.

In this application, connect an LED to PB7. Alternatively, use an additional wake-up button on PB7 instead of an LED. The user can also connect an LED to PB4.

Note: The additional pull-down resistor connected in parallel is needed to prevent transverse currents in the OFFMode. This special case is only applicable to PB4 because of its active input characteristics (PWRON).

2.3.3 Typical 5V Application Circuit with External Microcontroller

Figure 2-5. Typical 5V Application Circuit with External Microcontroller



The preceding figure shows a typical base station side application circuit with an external host µC running from a 5V voltage regulator. In contrast to the 3V application with external µC, directly connect the pin PB4 (PWRON) to VS; the ATA8510/15 enters the IDLEMode after power-on. In this configuration, the ATA8510/15 can work autonomously and the µC stays powered down to keep the current consumption low while remaining sensitive to RF telegrams.

To achieve a low current in IDLEMode, configure the ATA8510/15 in the EEPROM to work with the RC oscillators. Also, configure the ATA8510/15 for autonomous multi-channel and multi-application PollingMode. The external µC is notified by an event on pin 28 (EVENT) if an appropriate RF message is received. Until this event, the ATA8510/15 periodically switches to RXMode, checks the different services and channels configured in the EEPROM, and returns to power-down while the external host µC is still in Deep Sleep mode to keep the average current low. Upon valid RF message reception, the embedded receive buffer of the ATA8510/15 contains the message. After which, the transceiver can trigger a wake-up event for the external µC to retrieve this data for further processing.

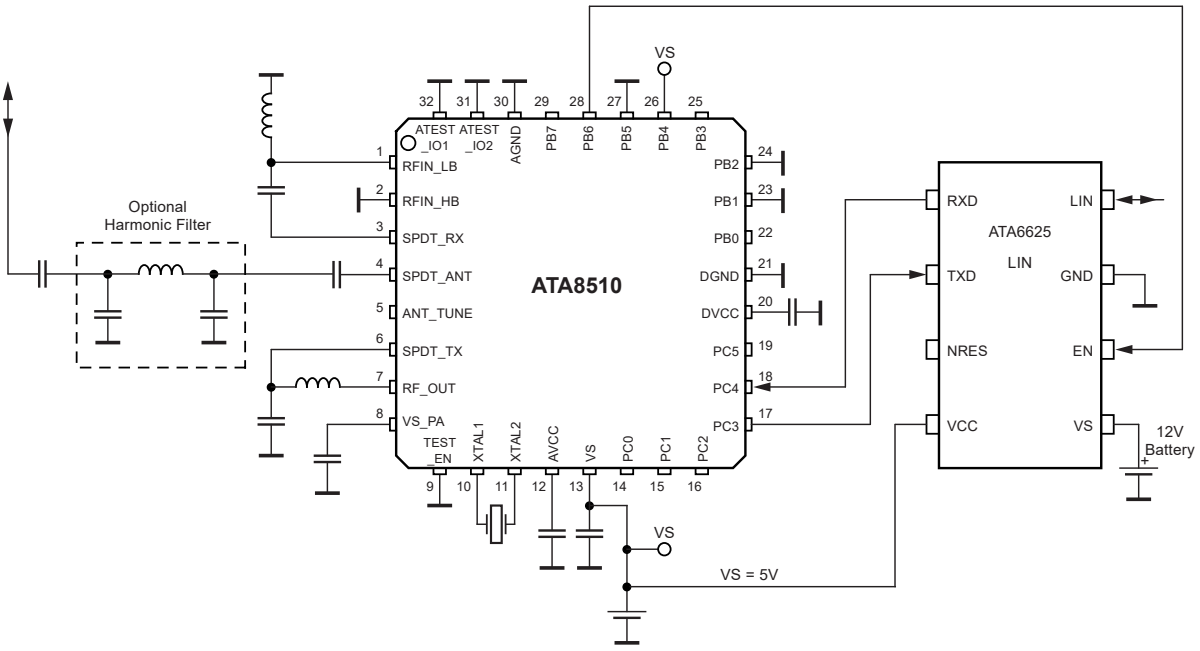
In applications using the 2.4-5.5V supply (VS), it is important to note that only the ATA8510/15 ports PB0..PB7, PC0..PC5, and the external host µC use this supply. The power amplifier of the ATA8510/15 is limited to 3.6V; therefore, an internal LDO delivers a 2.2V or 3.0V supply voltage in TXMode on pin VS_PA. The capacitor on pin VS_PA is needed to stabilize this regulator and decouple the power amplifier supply voltage. The ports PC0..PC5 have internal 50 kΩ pull-up resistors and can be left open. The ANT_TUNE pin must be left open because the application example uses a non-loop antenna.

Independent of the type of application, match the RF_OUT and RF_IN to SPDT_TX and SPDT_RX by absorbing the parasitics of the SPDT switch into the matching network; hence, the SPDT_ANT is a 50Ω RX and TX port. Improve the harmonic suppression by using an optional filter on the antenna side.

For example, if the transmit path uses a SAW filter, the user must ensure that the RF peak voltage on the pins SPDT_ANT and SPDT_TX stays in the range between -0.3V and VS_PA + 0.3V. For more details, refer to 5.6. RF Transmit Characteristics, parameters 12.45 and 12.50.

2.3.4 Typical 5V Application Circuit with One-Wire-Control

Figure 2-6. Typical 5V Application Circuit with One-Wire-Control



The preceding figure shows a typical 12V one-wire bus application circuit running from a 5V voltage regulator contained within the LIN transceiver ATA6625 device. In this application, directly connect the pin PB4 (PWRON) to VS; the ATA8510/15 enters the IDLEMode after power-up of the ATA6625 and stays there after the software in the Flash asserts the EN pin on the ATA6625 to HIGH. The system can be completely switched ON or OFF with a command via the one-wire bus. Use this application only when there is a need to separate the external host µC over a certain distance from the ATA8510/15. In these scenarios, the ATA8510/15 can work autonomously and communicate to the external host µC via a one-wire bus.

Together with 24-Kbyte ROM firmware, use the application software within the Flash for controlling the ATA8510/15 and the ATA6625. Use a simplified LIN-compliant physical layer for one-wire communication because the ATA8510/15 does not natively support one-wire commands. However, implement the one-wire communication through the use of application Flash software (ATA8510). The ATA8515 is not suitable for this application.

The ports PC0..PC2 have internal 50-kΩ pull-up resistors and can be left open. However, connect the ports PB1, PB2 and PB5 to ground. The ANT_TUNE pin must be left open because the application example uses a non-loop antenna. For more details regarding the use of a 2.4-5.5V supply and its distribution within the ATA8510/15, refer to 2.3.3. Typical 5V Application Circuit with External Microcontroller.

3. System Functional Description

3.1 Overview

3.1.1 Service-Based Concept

The ATA8510/15 is a highly configurable UHF transceiver. The configuration is stored in an internal 1024 byte EEPROM. The system control is performed by firmware. General chip-wide settings are loaded from the EEPROM to hardware registers during system initialization. During the start-up of a transmit or receive mode, the specific settings are loaded from the EEPROM or SRAM to the current service in the SRAM and from there, to the corresponding hardware registers.

A complete configuration set of the transceiver is called “service” and includes RF settings, demodulation settings and telegram handling information. Each service contains three channels that differ in the RF receive or transmit frequencies.

The ATA8510/15 supports five services that can be configured in various ways to meet customer requirements. Three service configurations are located in the EEPROM space. They are fixed configurations that must not be changed during run-time.

Two service configurations are located in the SRAM space and can be modified by USER SW in a Flash application or by an SPI command during IDLEMode.

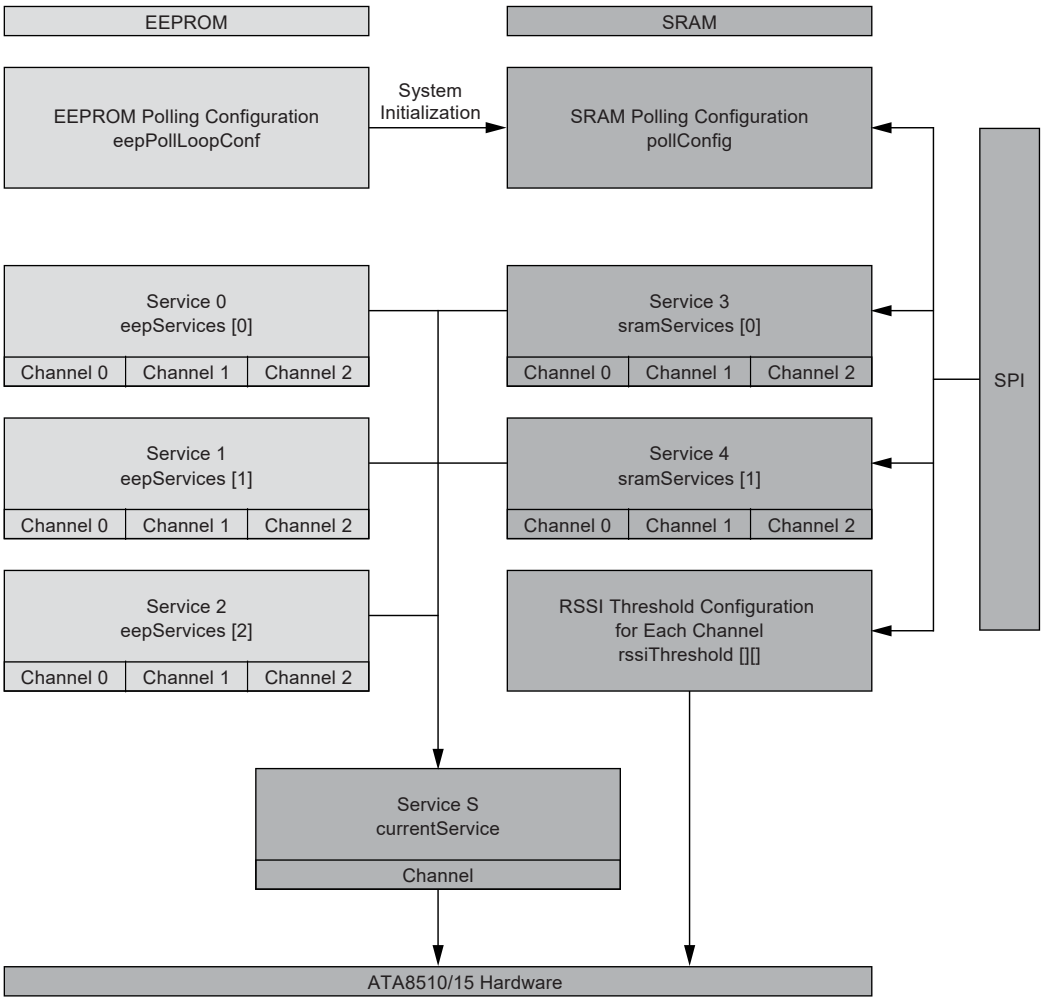
A service consists of:

- One service-specific configuration part
- Three channel-specific configuration parts

Further configurations for PollingMode and RSSI are available and can be modified in IDLEMode via an SPI command and/or User SW.

The following figure shows an overview of the service-based concept.

Figure 3-1. Service-Based Concept Overview



3.1.2 Supported Telegrams

3.1.2.1 Telegram Structure

The ATA8510/15 supports the transmission and reception of a wide variety of telegrams and protocols. Generally, no special structure is required from a telegram to be received or transmitted by the ATA8510/15. However, designated hardware and software features are built in for the blocks that are depicted in the following figure. Using this structure or parts of it can increase the sensitivity and robustness of the broadcast.

Figure 3-2. Telegram Structure

Desync	Preamble	Data Payload	Checksum	Stop Sequence

Desync:

The de-synchronization is usually a coding violation with a length of several symbols that provokes a defined restart of the receiver. The use of a de-synchronization leads to more deterministic receiver behavior, reducing the required preamble length. This can be favorable in timing-critical and energy-critical applications.

Preamble:

The preamble is a pattern that is sent before the actual data payload to synchronize the receiver and provide the starting point of the payload. A very regular pattern (e.g., 1-0-1-0...) is recommended for synchronization (“wake-up pattern, WUP”, sometimes also called “pre-burst”) while a unique, well-defined pattern of up to 32 symbols is required

to mark the start of the data payload (“start frame identifier, SFID” or “start bit”). In polling scenarios, the WUP can be tens or hundreds of ms long.

Data Payload:

The data payload contains the actual information content of the telegram. It can be NRZ or Manchester-coded. The length of the payload is application-dependent, typically 1..64 bytes.

Checksum:

A checksum can be calculated across the data payload to verify that the data were received correctly. A typical example is an 8-bit CRC checksum. Data bits at the beginning of the payload can be excluded from the CRC calculation.

Stop Sequence:

The stop sequence is a short data pattern (typically 2 to 6 symbols) to mark the end of the telegram. A coding violation can be used to prevent additional (non-deterministic) data from being received.

3.1.2.2 NRZ and Manchester Coding

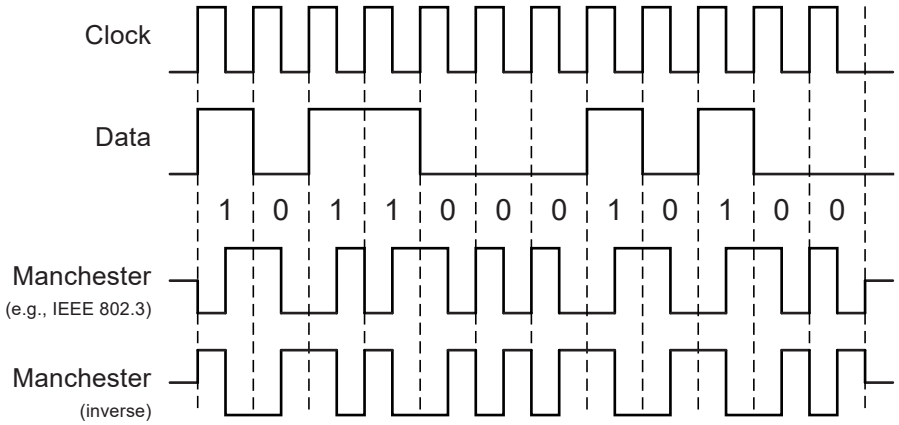
Within this document the following wording is used:

The expression data “bit” describes the real information content that will be broadcast. This information can be coded in “symbols” (sometimes also called “chips”) that are then physically transmitted from sender to receiver. The receiver has to decode the “symbols” back into data “bits” to access the information. The “symbol rate” is, therefore, always greater than or equal to the “bit rate”.

The ATA8510/15 supports two coding modes: Manchester coding and non-return-to-zero (NRZ) coding. NRZ coding is implemented in a straightforward manner: one bit is represented by one symbol.

Manchester coding implements two symbols per data bit. There is always a transition between the two symbols of one data bit so that one data bit always consists of a ‘0’ and a ‘1’. The polarity can be either way, as shown in the following figure.

Figure 3-3. Manchester Code

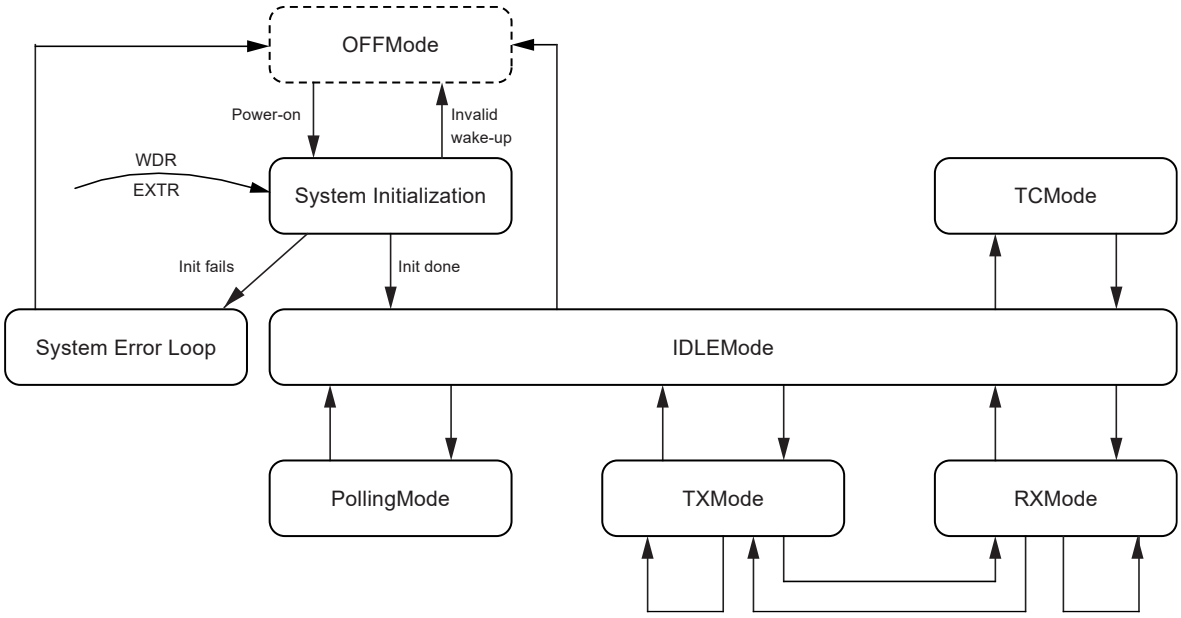


Manchester coding has many advantages, such as simple clock recovery, no DC component and error detection by code violation. Drawbacks are the coding/decoding effort and the increased symbol rate, which is twice the data rate.

3.2 Operating Modes Overview

This section gives an overview of the operating modes supported by the ATA8510/15 (see the following figure).

Figure 3-4. Operating Modes Overview



After connecting the supply voltage to the VS pin, the ATA8510/15 always starts in OFFMode. Disconnect all internal circuits from the power supply. Therefore, no SPI communication is supported. The user can wake up the ATA8510/15 by activating the PWRON pin or one of the NPWRONx pins. This triggers the power-on sequence. After the system initialization, the ATA8510/15 reaches the IDLEMode.

The IDLEMode is the basic system mode supporting the SPI communication and transitions to all other operating modes. There are two options of the IDLEMode requiring configuration in the EEPROM settings:

- IDLEMode(RC) with low power consumption using the fast RC (FRC) oscillator for processing
- IDLEMode(XTO) with active crystal oscillator for high accuracy clock output or timing measurements

The Transmit mode (TXMode) enables data transmission using the selected service/channel configurations. The `Set System Mode` SPI command enables the TXMode, or directly after power-on, when selected in the EEPROM setting. For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142).

The Receive mode (RXMode) provides data reception on the selected service/channel configuration. The precondition for data reception is a valid preamble. The receiver continuously scans for a valid telegram and receives the data if all pre-configured checks are successful. The RXMode can be enabled by the `Set System Mode` SPI command or directly after power-on when selected in the EEPROM setting. For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142).

In PollingMode, the user activates the receiver for a short period of time to check for a valid telegram on the selected service/channel configurations. The user deactivates the receiver if there is no valid telegram and a sleep period with very low power consumption elapses. This process is repeated periodically in accordance with the polling configuration. The initial settings (stored in the EEPROM) are copied to the SRAM during the firmware initialization. This allows modification of the PollingMode timing and service/channel configuration during IDLEMode.

The Tune and Check mode (TCMode) offers a calibration and self-checking functionality for the Voltage Controlled Oscillator (VCO) and Fast Resistor Capacitor (FRC) oscillators as well as for antenna tuning, temperature measurement and polling cycle accuracy. Use the `Calibrate and Check` SPI command to activate this mode. When selected in the EEPROM settings, use the tune and check tasks during the system initialization after the power-on. Furthermore, the user can activate them periodically during PollingMode. For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142).

The following table shows the relations between the operating modes and their corresponding power supplies, clock sources and Sleep mode settings.

Table 3-1. Operating Modes versus Power Supplies and Oscillators

Operation Mode	AVR Sleep Mode	DVCC	AVCC	VS_PA	XTO	SRC	FRC
OFFMode	—	OFF	OFF	OFF	OFF	OFF	OFF
IDLEMode(RC)	Active mode Power-down(1)	ON	OFF OFF	OFF OFF	OFF OFF	ON ON	ON OFF
IDLEMode(XTO)	Active mode Power-down(1)		ON ON	OFF OFF	ON ON	ON ON	OFF OFF
TXMode	Active mode		ON	ON(2)	ON	ON	OFF
RXMode	Active mode		ON	OFF	ON	ON	OFF
PollingMode(RC) • Active period • Sleep period	Active mode Power-down(1)		ON OFF	OFF OFF	ON OFF	ON ON	ON OFF
PollingMode(XTO) • Active period • Sleep period	Active mode Power-down(1)		ON ON	OFF OFF	ON ON	ON ON	OFF OFF

Notes:

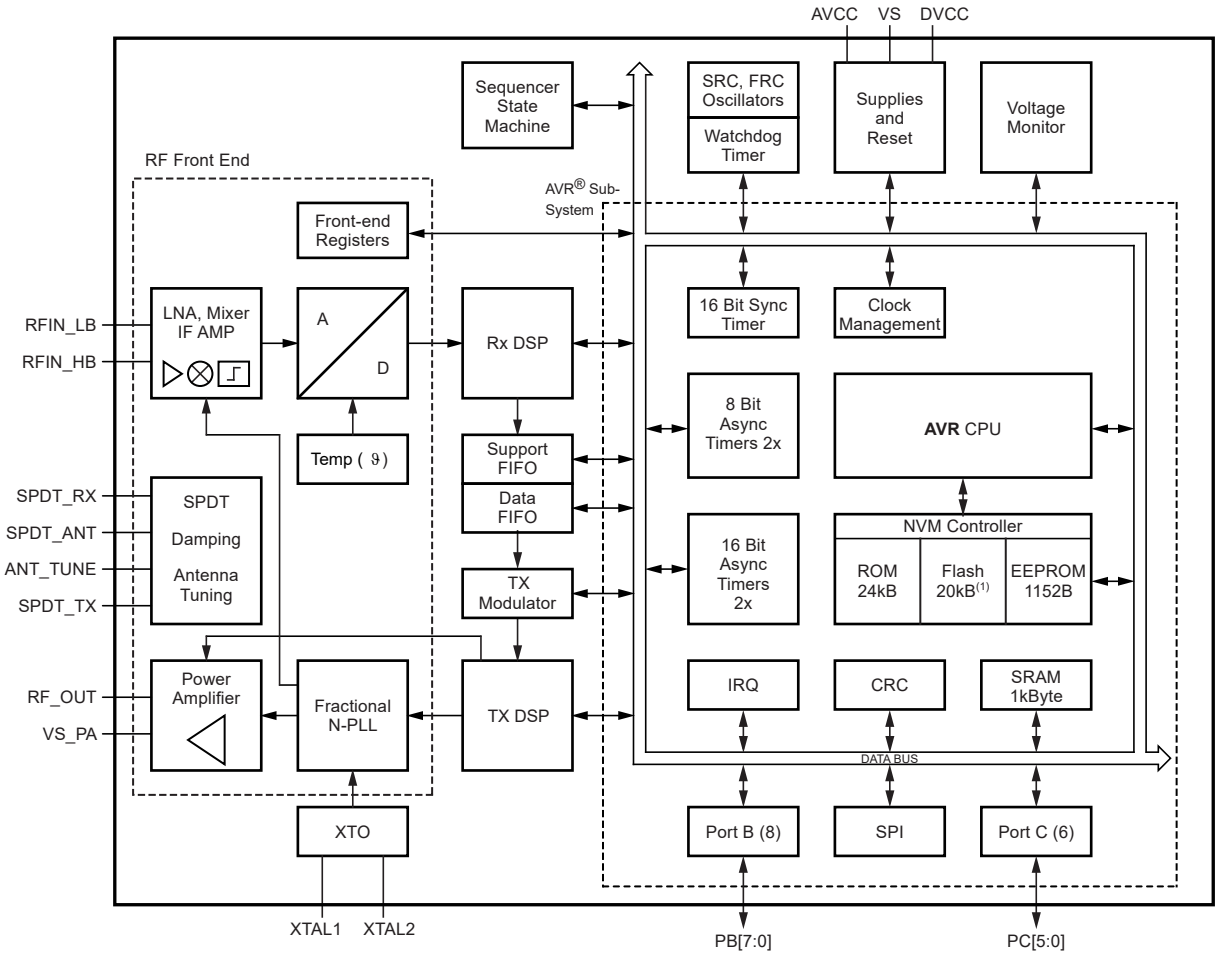
1. During the IDLEMode(RC) and the IDLEMode(XTO), the AVR microcontroller enters into Sleep mode to reduce current consumption. The Sleep mode of the microcontroller section can be defined in the EEPROM. The Power-down mode is recommended for keeping current consumption low.
2. Only activated in the 5V application after setting the VS5V bit. This is selectable in the EEPROM setting. For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142).

4. Hardware

4.1 Overview

The ATA8510/15 consists of an analog front end, digital signal processing blocks (DSP), an 8-bit AVR sub-system and various supply modules such as oscillators and power regulators. A hardware block diagram of the ATA8510/15 shows in the following figure.

Figure 4-1. Block Diagram



(1) 20kByte Flash for ATA8510, no user memory for ATA8515

Together with the fractional-N PLL, the crystal oscillator (XTO) generates the local oscillator (LO) signal for the mixer in RXMode. The RF signal comes either from the Low-Band input (RFIN_LB) or from the High-Band input (RFIN_HB) and is amplified by the low-noise amplifier (LNA) and down-converted by the mixer to the intermediate frequency (IF) using the LO signal. A 10 dB IF amplifier with low-pass filter characteristic is used to achieve enhanced system sensitivity without affecting blocking performance.

After the mixer, the IF signal is sampled using a high-resolution analog-to-digital converter (ADC).

Within the RX digital signal processing (RX DSP), the received signal from the ADC is filtered by a digital channel filter and demodulated. Two data receive paths, path A and path B, are included in the RX DSP after the digital channel filter. In addition, the receive path can be configured to provide the digital output of an internal temperature sensor (Temp(ϑ)).

In TXMode, the fractional-N PLL generates the TX frequency. The power amplifier (PA) generates an RF output power signal programmable from -10 dBm to +14 dBm at RF_OUT. The FSK modulation is performed by changing the frequency setting of the fractional-N PLL dynamically with TX digital signal processing (TX DSP). Digital preemphasis and digital Gauss filtering can be activated in the TX DSP to achieve higher data rates or reduce occupied bandwidth. The ASK modulation is performed by switching the power amplifier on and off. An ASK shaping filter is available to reduce the transmitted bandwidth of the modulated PA output signal. The shaping filter can also be used at the start and end of an FSK transmission.

With the single pole double throw (SPDT) switch, the RF signal from the antenna is switched to RFIN in RXMode and from RF_OUT to the antenna in TXMode. An adjustable capacitor and an RF level detector on ANT_TUNE are used to tune the center frequency of loop antennas to reduce tolerances and capacitive proximity effects.

The system is controlled by an AVR CPU with 24 KB firmware ROM and 20 KB user Flash for the ATA8510. 1024-byte EEPROM, 1024-byte SRAM and other peripherals are supporting the transceiver handling. Two GPIO ports, PB[7:0] and PC[5:0], are available for external digital connections, for example, as an alternate function the SPI interface is connected to port B. The ATA8510/15 is controlled by the EEPROM configuration and SPI commands and the functional behavior is mainly determined by firmware in the ROM. Much of the configuration can be modified by the EEPROM settings. The firmware running on the AVR gives access to the hardware functionality of the ATA8510/15. Extensions to this firmware can be added in the 20 KB of Flash memory for the ATA8510. The RX DSP and TX DSP registers are addressed directly and accessible from the AVR. A set of sequencer state machines is included to perform RX and TX path operations (such as enable, disable, receive, transmit) which require a defined timing parallel to the AVR program execution.

The power management contains low-dropout (LDO) regulators and reset circuits for the supply voltages VS, AVCC, DVCC and VS_PA of the ATA8510/15. In OFFMode, all the supply voltages AVCC, DVCC and VS_PA (only use VS_PA for 2.5-5.5V operation) are switched off to achieve very low current consumption. The ATA8510/15 can be powered up by activating the PWRON pin or one of the NPWRON[6:1] pins because they are still active in OFFMode. The AVCC domain can be switched on and off independently from DVCC. The ATA8510/15 includes two idle modes. In IDLEMode(RC), only the DVCC voltage regulator, the FRC and SRC oscillators are active, and the AVR uses a power-down mode to achieve low current consumption. The same power-down mode can be used during the inactive phases of the PollingMode. In IDLEMode(XTO), the AVCC voltage domain as well as the XTO are additionally activated.

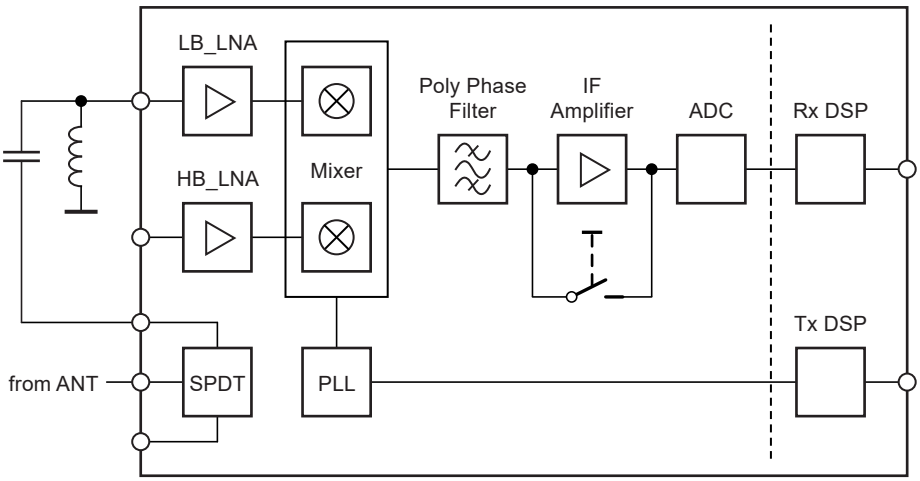
An integrated watchdog timer is available to restart the ATA8510/15 when it is not served within the configured time-out period.

4.2 Receive Path

4.2.1 Overview

The receive path consists of a low-noise amplifier (LNA), mixer, IF amplifier, analog-to-digital converter (ADC) and an RX digital signal processor (RX DSP), as shown in the following figure. The fractional-N PLL and the XTO deliver the local oscillator frequency in RXMode. The receive path is controlled by the RF front-end registers.

Figure 4-2. RX Path Overview



Two separate LNA inputs, one for Low-Band and one for High-Band, are provided to obtain optimum performance matching for each frequency range and to allow multi-band applications. A radio frequency (RF) level detector at the LNA output and a switchable damping included into the single-pole double-trough (SPDT) switch is used in the presence of large blockers to achieve enhanced system-blocking performance.

The mixer converts the received RF signal to a low intermediate frequency (IF) of about 250 kHz. A double-quadrature architecture is used for the mixer to achieve high image rejection. Additionally, the third-order suppression of the local oscillator (LO) harmonics makes receiving without a front-end SAW filter less critical, such as in a car key fob application.

An IF amplifier provides additional gain and improves the receiver sensitivity by 2-3 dB. Because of built-in filter function, the in-band compression is degraded by 10 dB, while the out-of-band compression remains unchanged.

The ADC converts the IF signal into the digital domain. Due to the high effective resolution of the ADC, the channel filter and received signal strength indicator (RSSI) can be realized in the digital signal domain. Therefore, no analog gain control (AGC) potentially leading to critical timing issues or analog filtering is required in front of the ADC. This leads to a receiver front end with excellent blocking performance up to the 1 dB compression point of the LNA and mixer, and a steep digital channel filter can be used.

The RX DSP performs the channel filtering and converts the digital output signal of the ADC to the baseband for demodulation. Due to the digital realization of these functions, the RX DSP can be adapted to the needs of many different applications. Channel bandwidth, data rate, modulation type, wake-up criteria, signal checks, clock recovery and many other properties are configurable. The RSSI value is realized completely in the digital signal domain, enabling very high relative and absolute accuracy that is only deteriorated by the gain errors of the LNA, mixer and ADC.

Two independent receive paths, A and B, are integrated in the RX DSP after the channel filter, and allow the use of different data rates, modulation types and protocols without the need to power up the receive path more than once to determine which signal will be received. This results in a reduced polling current in several applications.

The integration of different applications (remote access, temperature sensors and more) into one module is simplified because completely different protocols can be supported and a low polling current is achieved. It is even possible to configure different receive RF bands for different applications by using the two LNA inputs.

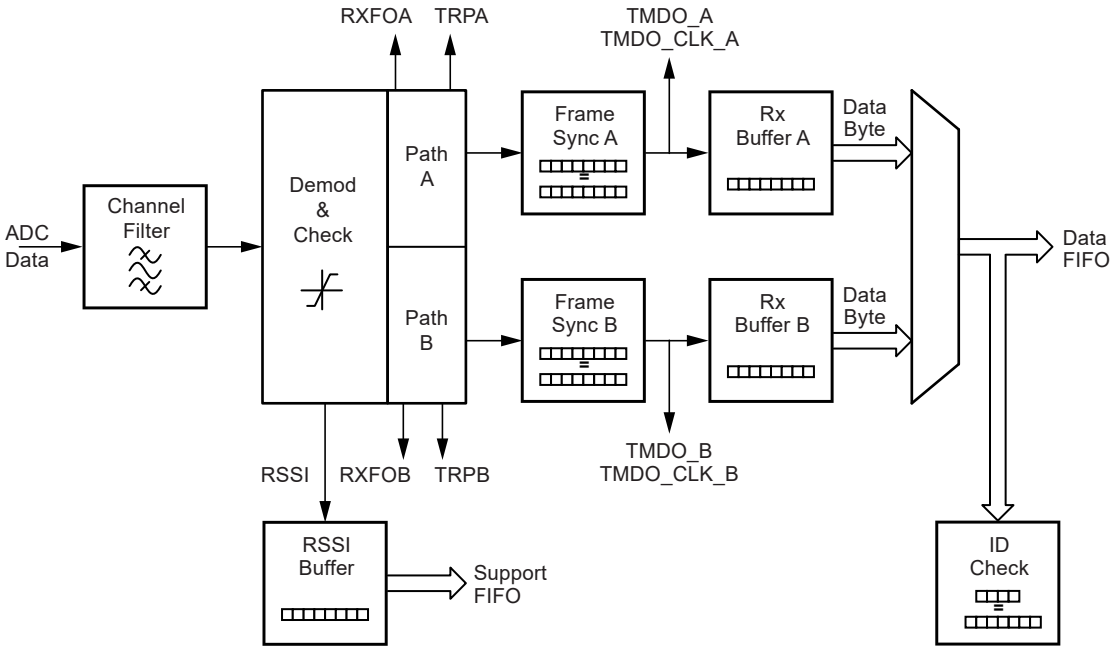
4.2.2 RX Digital Signal Processing (RX DSP)

The RX digital signal processing (DSP) block performs the digital filtering, decoding, checking and byte-wise buffering of the RX samples that are derived from the ADC, as shown in the following figure. The RX DSP provides the following outputs:

- Raw demodulated data at the TRPA/B pins
- Decoded data at the TMDO and TMDO_CLK pins
- Buffered data bytes toward the data FIFO and ID check block

- Auxiliary information about the signal such as the received signal strength indication (RSSI) and the frequency offset of the received signal from the selected center frequency (RXFOA/B)

Figure 4-3. RX DSP Overview



The channel filter determines the receiver bandwidth. Its output is used for both receiving paths A and B, making it necessary to configure the filter to match both paths. The receiving paths A and B are identical and consist of an ASK/FSK demodulator with attached signal checks, a frame synchronizer that supports pattern-based searches for the telegram start and a 1-byte hardware buffer with integrated CRC checker for the received data.

Depending on the signal checks, one path is selected that writes the received data to the data FIFO and optionally to the ID check block.

The RSSI values are determined by the demodulator and written via the RSSI buffer to the support FIFO where the latest 16 values are stored for further processing.

4.3 Transmit Path Overview

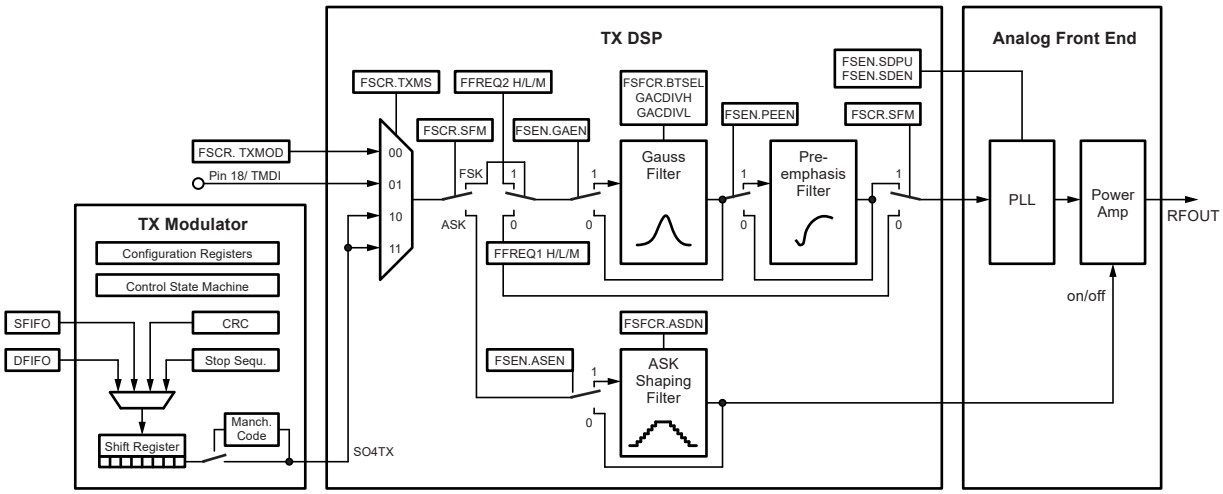
The ATA8510/15 integrates a transmitter that is capable of sending data with various options:

- Frequency bands: 310-318 MHz, 418-477 MHz and 836-956 MHz
- Data rates up to 80 kBit/s Manchester coding or 120 Ksym/s Non-return-to-zero (NRZ) coding in Buffered and Transparent mode
- ASK or FSK modulation
- Transparent or Buffered mode
- ASK shaping filter
- Gauss-shaping digital filter

This section describes the hardware blocks that are integrated to perform the transmit functionality. For detailed information on system and software flows, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142).

The following figure illustrates the block diagram of transmit data path.

Figure 4-4. Transmit Data Path



The user can select the transmission data source from a register bit. The transparent input pin 18 (TMDI) and the TX modulator fetches the data from the DFIFO and SFIFO.

If ASK/On Off Keying (OOK) modulation is selected, use the data stream to directly switch the power amplifier ON and OFF. The transmitted carrier frequency is set by the PLL frequency synthesizer.

If FSK modulation is selected, use the data stream to switch between two frequencies that are generated by the PLL frequency synthesizer. The power amplifier is constantly on. Use the power ramping (ASK shaping) during ON and OFF switching. To reduce the occupied bandwidth, enable the digital Gauss-shaping filter. For data rates above 20 kHz Manchester or 40 kHz NRZ-coding, enable the digital preemphasis filter to compensate for the Phase Locked Loop (PLL) loop filter.

4.4 AVR Controller

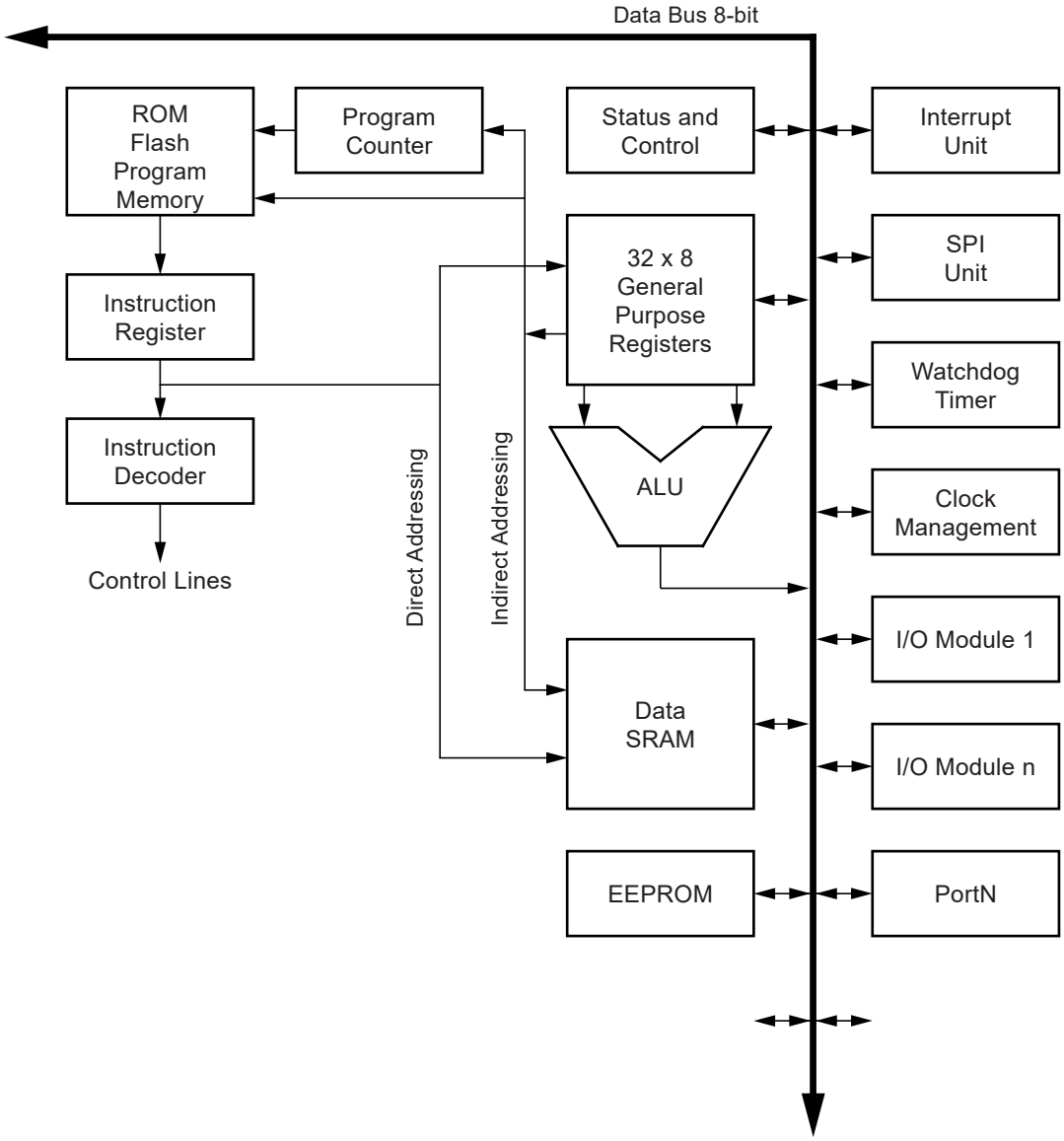
4.4.1 AVR Controller Sub-System Overview

The AVR controller sub-system consists of the AVR CPU core, its program memory and a data bus with data memory and peripheral blocks attached. The receive path and the transmit path also have their user interfaces connected to the data bus.

4.4.2 CPU Core Architectural Overview

This section discusses the AVR core architecture in general. The main function of the CPU core is to ensure correct program execution. For this reason, the CPU core must be able to access memories, perform calculations, control peripherals and handle interrupts.

Figure 4-5. Overview of Architecture



To maximize performance and parallelism, the AVR uses a Harvard architecture with separate memories and buses for program and data. Instructions in the program memory are executed with single-level pipelining. While one instruction is being executed, the next instruction is prefetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system reprogrammable Flash memory and ROM.

The fast-access register file contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This allows a single-cycle arithmetic and logic unit (ALU) operation. In a typical ALU operation, two operands are output from the register file, the operation is executed and the result is stored back in the register file in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for data space addressing, enabling efficient address calculations. One of these address pointers can also be used as an address pointer for Look-up Tables in the Flash program memory. Referred to as ‘X’, ‘Y’ and ‘Z’ registers, these higher 16-bit function registers are described later in this section.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations can also be executed in the ALU. After an arithmetic operation, the status register is updated to reflect information about the result of the operation.

The program flow is provided by conditional and unconditional jump and call instructions which are able to directly address the entire address space. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

The program memory space is divided in two sections, the boot program section and the application program section. Both sections have dedicated lock bits for write and read/write protection. The store program memory (SPM) instruction that writes into the application Flash memory section must reside in the boot program section.

During interrupts and subroutine calls, the return address of the program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM; the stack size is, thus, only limited by the total SRAM size and use of the SRAM. All user programs must initialize the stack pointer (SP) in the reset routine before subroutines or interrupts are executed. The SP is read/write accessible in the I/O space. The data SRAM can easily be accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All interrupts have a separate interrupt vector in the interrupt vector table. The interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

The I/O memory space contains 64 addresses for CPU peripheral functions as control registers, SPI and other I/O functions. The I/O memory can be accessed directly, or as the data space locations following those of the register file, 0x20 – 0x5F. In addition, the circuit has extended I/O space from 0x60 – 0x1FF and SRAM where only the ST/STS/STD and LD/LDS/LDD instructions can be used.

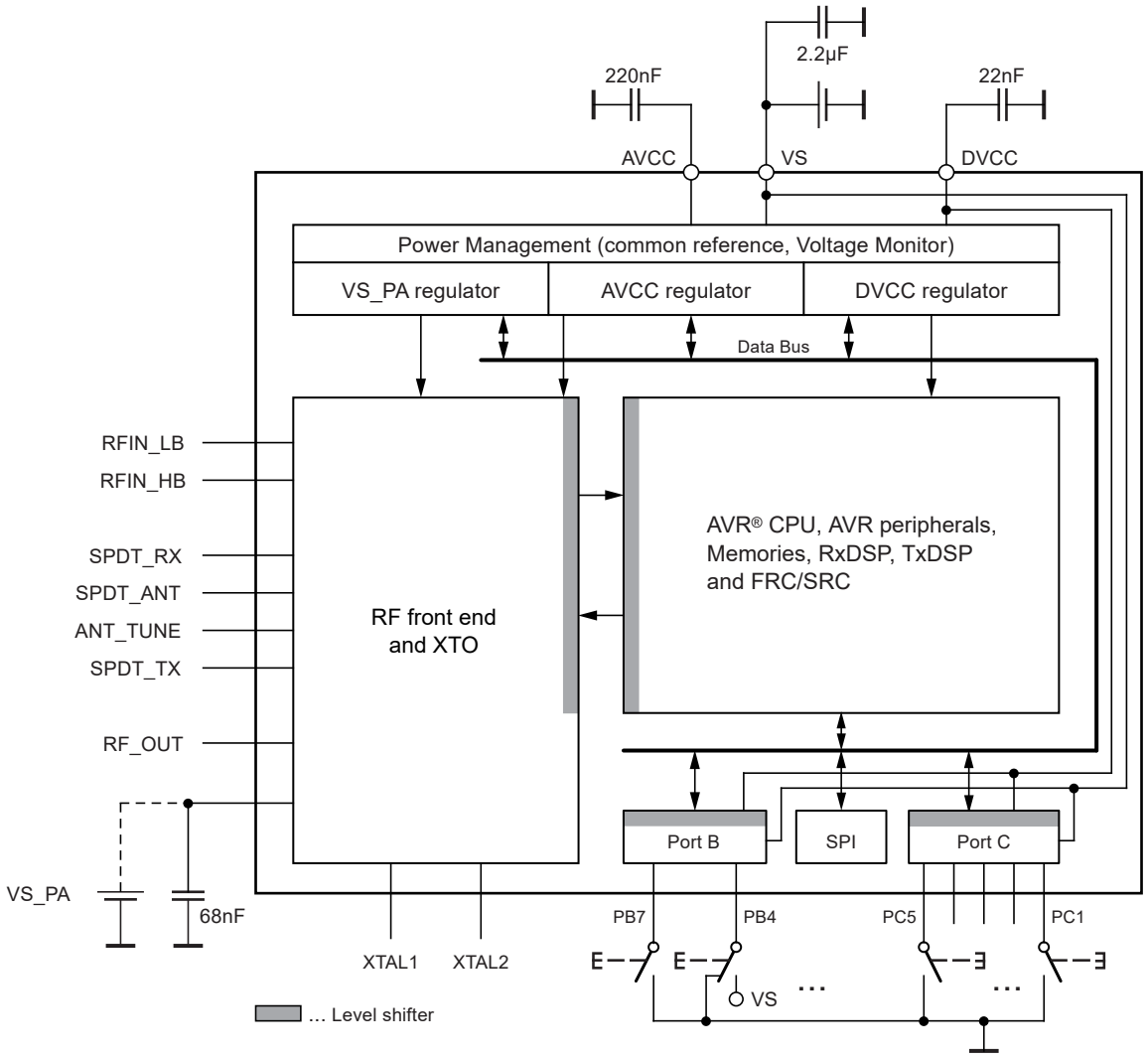
4.5 Power Management Overview

The IC has four power domains:

1. VS – Unregulated battery voltage input
2. DVCC – Internally regulated digital supply voltage. Typical value is 1.35V.
3. AVCC – Internally regulated RF front end and XTO supply. Typical value is 1.85V.
4. VS_PA – Power amplifier supply: Depending on the battery voltage range (VS), the following application modes are available:
   - Connected externally to the battery in 3V applications (VS = VS_PA = 1.9-3.6V)
   - Generated by an internal 3V regulator
     - VS = 3.2-5.5V; VS_PA = 3V
     - VS = 1.9-3.2V; VS_PA = VS – 200 mV
   - Generated by an internal 2.2V regulator in 3V/5V applications
     - VS = 2.4-5.5V; VS_PA = 2.2V
     - VS = 1.9-2.4V; VS_PA = VS – 200 mV

Operate the ATA8510/15 from VS = 1.9-3.6V (3V application) and from VS = 2.4-5.5V (5V application); program the Operating mode in the SUPCR.PVEN.

Figure 4-6. Power Supply Management

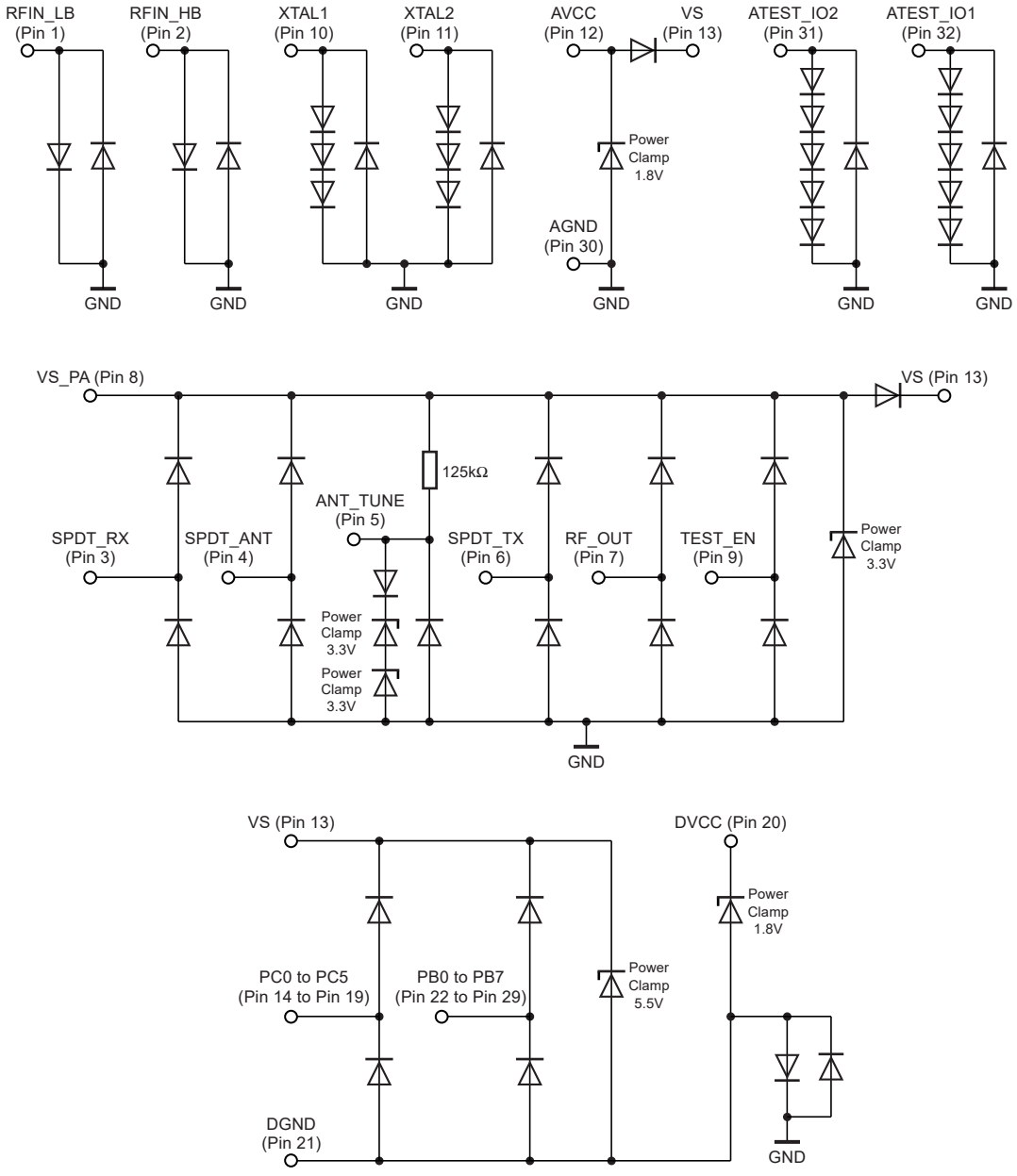


5. Electrical Characteristics

5.1 ESD Protection Circuits

GND is the exposed die pad of the ATA8510/15, which is internally connected to AGND (pin 30). All Zener diodes shown in the following figure (marked as power clamps) are realized with dynamic clamping circuits and not physical Zener diodes. Therefore, DC currents are not clamped to the shown voltages.

Figure 5-1. ATA8510/15 ESD Protection Circuit



5.2 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5-1. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Junction temperature	Tj	—	+150	°C
Storage temperature	Tstg	-55	+125	°C
Ambient temperature	Tamb	-40	+85	°C
Supply voltage	V_{VS}	-0.3	6.0	V
Supply voltage PA (1.9..3.6V application)	V_{VS_PA}	-0.3	4.0	V
Maximum input level (input matched to 50Ω)	P_{in_max}	—	+10	dBm
ESD (Human Body Model) all pins	HBM	-4	+4	kV
ESD (Machine Model) all pins	MM	-200	+200	V
ESD (Field Induced Charged Device Model) all pins	FCDM	-750	+750	V
Maximum RF amplitude at pin 5 (ANT_TUNE)(1)	ANTTUNE	—	4.0	Vp
Maximum peak voltage at pin 4 (SPDT_ANT)(1)	SPDTANT	-0.3	VS + 0.3	V
Maximum peak voltage at pin 6 (SPDT_TX)(1)	SPDTTX	-0.3	VS + 0.3	V

Note:

1. The customer application needs to be designed properly.

5.3 Thermal Resistance

Table 5-2. Thermal Resistance Parameters

Parameters	Symbol	Value	Unit
Thermal Resistance, Junction Ambient, Soldered according to JEDEC	R_{th_JA}	35	K/W

5.4 Supply Voltages and Current Consumption

All parameters refer to GND (backplane) and are valid for T_{amb} = -40°C to +85°C, V_{VS} = 1.9-3.6V (3V application) and 2.4-5.5V (5V application) over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 5V, T_{amb} = 25°C and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305 MHz. Standard EEPROM settings are used unless marked with *1.

Table 5-3. Supply Voltages and Current Consumption

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.00	Supply voltage range VS	3V application*1	13	V_{VS}	1.9	3.0	3.6	V	A
		5V application			2.4	5.0	5.5		
1.05	Supply voltage rise time	—	13	V_{VS_rise}	—	—	1	V/µs	D
1.10	Supply voltage range VS_PA	3V application*1	8	V_{VS_PA}	1.9	3	3.6	V	A
		5V application (1)			—	3	—		B
		5V application (2)			—	2.2	—		B
1.20	OFFMode Current consumption	3V application*1	8,13	$I_{OFFMode\_3V}$	—	5	—	nA	—
		T_{amb} = 25°C					150		B
		T_{amb} = 85°C					600		B
		5V application	13	$I_{OFFMode\_5V}$			5000		B
1.30	IDLEMode(RC) Current consumption	SRC active, AVR in Power-down mode, temperature range -40°C to +65°C	13	$I_{IDLEMode(RC)}$	—	50	90	µA	B
1.40	IDLEMode(XTO) Current consumption	XTO active, AVR in Power-down mode	13	$I_{IDLEMode(XTO)}$	—	250	400	µA	B
1.60	IDLEMode(XTO) Current consumption	With active CLK_OUT $f_{XTO}/6$ = 4.05 MHz $C_{LOAD\_CLK\_OUT}$ = 10 pF V_{VS} = 5.5V AVR running with $f_{XTO}/4$ = 6.076 MHz	13,22	$I_{IDLEMode(XTO)\_CLK\_OUT2}$	—	1.3	2.5	mA	B
1.80	RXMode Current consumption	AVR running with $f_{XTO}/4$	13	$I_{RXMode1}$	—	—	—	mA	—
		f_{RF} = 315 MHz*1				9.2	12.7		B
		f_{RF} = 433.92 MHz				9.8	13.2		A
		f_{RF} = 868.3 MHz*1				10.4	14.6		A
		fRF = 915 MHz*1				10.5	14.7		B

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
2.00	TXMode Current consumption	V_{VS} = 3V	(7), 8, 13	I_{TXMode}	—	—	—	mA	—
		P_{out} = +6 dBm				—	—		—
		f_{RF} = 315 MHz*1				8.9	11		B
		f_{RF} = 433.92 MHz				9.4	12		B
		fRF = 868.3 MHz*1				11.5	14.5		B
		f_{RF} = 915 MHz*1				11.7	15		B
		P_{out} = +10 dBm*1				—	—		—
		f_{RF} = 315 MHz*1				13.1	17		B
		f_{RF} = 433.92 MHz				13.8	18.5		B
		f_{RF} = 868.3 MHz*1				17.4	22.5		B
		f_{RF} = 915 MHz*1				17.4	23		B
		P_{out} = +14 dBm*1				—	—		—
		f_{RF} = 315 MHz*1				24.3	33		B
		f_{RF} = 433.92 MHz				26.3	36		B
		f_{RF} = 868.3 MHz*1				32.7	45		B
		f_{RF} = 915 MHz*1				33.5	46		B

Note: *1 Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples and D = Design parameter. A pin number in brackets means that they are measured matched to 50Ω on the application board.

5.5 RF Receiving Characteristics

All parameters refer to GND (backplane) and are valid for T_{amb} = -40°C to +85°C, V_{VS} = 1.9-3.6V (3V application) and 2.4-5.5V (5V application) over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 5V, T_{amb} = 25°C and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305 MHz. Standard EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
Frequency Ranges and Frequency Resolution of PLL for RXMode, TXMode and PollingMode									
3.00	RF operating frequency range 315 MHz Low-band	FECR.LBNHB = 1 FECR.S4N3 = 0	1, 7	$f_{Range\_LB1\_315}$	310	315	318	MHz	A
3.10	RF operating frequency range 433 MHz Low-band	FECR.LBNHB = 1 FECR.S4N3 = 1	1, 7	$f_{Range\_LB2\_433}$	418	433.92	477	MHz	B
3.30	RF operating frequency range High-band	FECR.LBNHB = 0 FECR.S4N3 = 0	2, 7	$f_{Range\_B4\_868}$	836	868.3	956	MHz	B
3.40	Frequency resolution PLL	Low-band $f_{XTO}/2^{18}$	1, 2, 7	DF_{PLL}	—	92.72	—	Hz	B
		High-band $f_{XTO}/2^{17}$				185.43			B

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
RXMode and PollingMode Receive Characteristics **IF bandwidth specifications are examples usable for parameter extrapolation if other IF bandwidth values are used**									
4.00	Receiver 3 dB bandwidth	Programmable digital IF filter	1, 2	BW_{IF}	25	—	366	kHz	B
4.10	ASK and FSK transparent mode data rate Manchester mode	at 25 kHz IF-BW	1, 2	DR_{TM}	0.25	—	7	Kbit/s	B
		at 50 kHz IF-BW					14		B
		at 80 kHz IF-BW					20		B
		at 165 kHz IF-BW					50		B
		at 237 kHz IF-BW					80		B
		at 366 kHz IF-BW					80		B
4.20	Modulation index FSK	η = frequency_deviation/ symbol_rate recommended	1, 2	η	0.5 0.75	1	360 1.25	—	B B
4.30	Frequency deviation	Maximum usable frequency deviation is base-band clock dependant f_{DEV_Max} = CLK_BB/8	1, 2	f_{DEV}	—	–	—	kHz	—
		at 25 kHz IF-BW			±0.375		±9		B
		at 50 kHz IF-BW			±0.75		±18		B
		at 80 kHz IF-BW			±1.2		±26		B
		at 165 kHz IF-BW			±2.5		±60		B
		at 237 kHz IF-BW			±3.5		±93		B
		at 366 kHz IF-BW			±5.4		±93		B
4.40	ASK and FSK transparent mode symbol rate NRZ mode	Used to receive NRZ, Keyloq, PPM, 1/3 2/3 Coded telegrams	1, 2	SR_{TM_OPT}	0.5	—	—	Ksym/s	—
		at 25 kHz IF-BW					14		B
		at 50 kHz IF-BW					28		B
		at 80 kHz IF-BW					40		B
		at 165 kHz IF-BW					100		B
		at 237 kHz IF-BW					160		B
		at 366 kHz IF-BW					160		B
4.70	Data rate tolerance FSK and ASK	Loss of sensitivity <1 dB	1, 2	DR_{TOL}	-10	—	+10	%	B

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
4.80	Buffered data rate Manchester and NRZ mode	TMDO output is buffered internally and readout via SPI interface	1, 2	$DR_{Buffered}$	—	—	—	—	—
		Manchester mode			0.25		80	Kbit/s	B
		NRZ mode			0.5		120	Ksym/s	B
4.90	FSK Sensitivity level 315MHz/433.92MHz Manchester encoded	FSK at 25 kHz IF bandwidth T_{amb} = 25°C	(1), 17, 19	—	-3dB	—	+3 dB	dBm	—
		0.75 Kbit/s ± 0.75 kHz		$SFSK_{B25\_R0.75}$		-122.5			B
		5 Kbit/s ± 2.4 kHz		$SFSK_{B25\_R5\_2.4}$		-113.5			B
5.00	Receiving100 bit Packets with 9 of 10 Packets Error Free or BER = 10^-3 Continuous RX	FSK at 80 kHz IF bandwidth T_{amb} = 25°C	(1), 17, 19	—	-3 dB	—	+3 dB	dBm	—
		2.4 Kbit/s ± 2.4 kHz		$SFSK_{B80\_R2\_4}$		-117			B
		20 Kbit/s ± 20 kHz		$SFSK_{B80\_R20}$		-108.5			B
5.10	measured at TMDO output or buffered via SPI for DR < DR Buffered	FSK at 165 kHz IF bandwidth T_{amb} = 25°C	(1), 17, 19	—	-3 dB	—	+3 dB	dBm	—
		5 Kbit/s ± 5 kHz		$SFSK_{B165\_R5}$		-114			B
		40 Kbit/s ± 40 kHz		$SFSK_{B165\_R40}$		-105.5			B

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.20	ASK Sensitivity level 315 MHz/433.92 MHz Manchester encoded Receiving 100-bit Packets with 9 of 10 Packets Error Free or BER = 10^-3 Continuous RX measured at TMDO output or buffered via SPI for DR < $DR_{Buffered}$	FSK at 366 kHz IF bandwidth T_{amb} = 25°C	(1), 17, 19	—	-3dB	—	+3 dB	dBm	—
		20 Kbit/s ± 20 kHz		$SFSK_{B366\_R20}$		-107.5			B
		80 Kbit/s ± 80 kHz		$SFSK_{B366\_R80}$		-100.5			B
5.30		ASK at 25 kHz IF bandwidth (100% ASK level of carrier value) T_{amb} = 25°C	—	—	—	—	+3 dB	dBm	—
		0.5 Kbit/s	(1), 17, 19	$SASK_{B25\_R0\_5}$	-3 dB	-125			B
		5 Kbit/s		$SASK_{B25\_R5}$		-117.5			B
5.40		ASK at 80 kHz IF bandwidth (100% ASK level of carrier value) T_{amb} = 25°C	—	—	—	—	—	—	—
		1 Kbit/s	—	$SASK_{B80\_R1}$	-3 dB	-121.5	+3 dB	dBm	B
		20 Kbit/s	(1), 17,19	$SASK_{B80\_R20}$		-110.5			B
5.50		ASK at 165 kHz IF bandwidth (100% ASK level of carrier value) T_{amb} = 25°C	—	—	-3 dB	—	+3 dB	dBm	—
		1 Kbit/s	(1), 17, 19	$SASK_{B165\_R1}$		-120.5			B
		40 Kbit/s		$SASK_{B165\_R40}$		-107.5			B
5.60		ASK at 366 kHz IF bandwidth (100% ASK level of carrier value) T_{amb} = 25°C	(1), 17,19	—	-3 dB	—	+3 dB	dBm	—
		1 Kbit/s		$SASK_{B366\_R1}$		-118.5			B
		80 Kbit/s		$SASK_{B366\_R80}$		-103.5			B
5.70	Sensitivity change High-band	High-band 868.3 MHz compared to Low-band sensitivity to be added to min/typ/max values of parameters no. 4.90 to 5.6	(2)	ΔS_{HB}	1	1	1	dB	B
5.80	Sensitivity change Full ambient temperature range	T_{amb} = -40°C to +85°C	(1) (2)	—	—	—	—	—	—
		Low-band*1		ΔS_{Tamb_LB}	-1.5	—	2	dB	C
		High-band		ΔS_{Tamb_HB}	-2		3	dB	C
		$S = S_{FSK\_ASK} + \Delta S$		—	—		—	—	—

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
5.90	Sensitivity change NRZ	Compared to Machester NRZ using no more than 8 succeeding '0' or '1' symbols	(1,2)	ΔS_{NRZ}	—	—	—	—	—
		FSK			-1	0	2	dB	C
		ASK			0	2	4		C
		S = S_{FSK_ASK}+ΔS			—	—	—		—
6.00	Sensitivity change TRPA/B raw data	Compared to matched filter TMDO signal on pin 17, Manchester encoded	(1,2), 16, 17, 19	ΔS_{RAW_DATA}	—	—	—	dB	—
		ASK				2.5			B
		FSK				1.5			B
		S = S_{FSK_ASK} +ΔS				—			—
6.20	Sensitivity change for frequency deviations lower than configured	Configured for maximum f_{DEVM}. Sensitivity degradation at $f_{DEVM}/3$ compared to f_{DEVM}, S = S_{FSK_ASK}+ΔS	(1,2)	$\Delta S_{:fdevM\_3}$	—	2	3	dB	C
6.30	Value change from ASK level to OOK level	To calculate OOK values from ASK 100% level of carrier values. For example, 2.4 Kbit at 165 kHz IF bandwidth ASK: 100% level of Carrier – 117 dBm = OOK: -111 dBm $S_{OOK} = S_{ASK}+D_{OOK}$	(1,2)	ΔOOK	6	6	6	dB	D

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
6.90	315MHz/ 433 MHz blocking Manchester encoded Useful signal level increased 3 dB above sensitivity level Blocking measured relative to useful signal level Receiving 100-bit Packets with 9 of 10 Packets Error Free or BER = 10^-3 Continuous RX Excluding spurious receiving frequencies	At 25 kHz IF bandwidth, FSK, T_{amb} = 25°C 2.4 Kbit/s ± 2.4 kHz	(1,2)	fdist.≥ 50 kHz	—	40	—	dBc	C
				fdist.≥ 100 kHz		46			C
				fdist.≥ 225 kHz		58			C
				fdist.≥ 450 kHz		64			C
				fdist.≥ 1 MHz		73			C
				fdist.≥ 4 MHz		78			C
				fdist.≥10MHz		78			C
7.00		At 80 kHz IF bandwidth, FSK, T_{amb} = 25°C 10 Kbit/s ± 10 kHz	(1,2)	fdist. ≥ 150 kHz	—	45	—	dBc	C
				fdist. ≥ 225 kHz		52			C
				fdist. ≥ 450 kHz		58			C
				fdist. ≥ 1 MHz		67			C
				fdist. ≥ 4 MHz		71			C
				fdist. ≥ 10 MHz		71			C
7.10		At 165 kHz IF bandwidth,FSK, T_{amb} = 25°C 20 Kbit/s ± 20 kHz	(1,2)	fdist. ≥ 225 kHz	—	48	—	dBc	C
				fdist. ≥ 450 kHz		54			C
				fdist. ≥ 1 MHz		64			C
				fdist.≥ 4 MHz		68			C
				fdist.≥ 10 MHz		68			C
7.20		At 366 kHz IF bandwidth, FSK, T_{amb} = 25°C 20 Kbit/s ± 20 kHz	(1,2)	fdist. ≥ 500 kHz	—	55	—	dBc	C
				fdist. ≥ 1 MHz		64			C
				fdist. ≥ 4 MHz		68			C
				fdist.≥ 10 MHz		68			C

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.30	868 MHz/915 MHz blocking Manchester encoded Useful signal level increased 3 dB above unblocked sensitivity level Blocking measured relative to useful signal level Receiving 100-bit Packets with 9 of 10 Packets Error Free or BER = 10^-3 Continuous RX Excluding spurious receiving frequencies	At 25 kHz IF bandwidth, FSK, T_{amb} = 25°C 2.4 Kbit/s ± 2.4 kHz	(1,2)	fdist. ≥ 50 kHz	—	34	—	dBc	C
				fdist.≥ 100 kHz	—	40			C
				fdist. ≥ 225 kHz		52			C
				fdist. ≥ 450 kHz		58			C
				fdist. ≥ 1 MHz		67			C
				fdist. ≥ 4 MHz		75			C
				fdist. > 10 MHz	—	75			C
7.40		At 80 kHz IF bandwidth, FSK, T_{amb} = 25°C 10 Kbit/s ± 10 kHz	—	fdist.≥ 150 kHz	—	39	—	—	C
				fdist. ≥ 225 kHz		46			C
			(1,2)	fdist.≥ 450 kHz	—	52	—	dBc	C
				fdist. ≥ 1 MHz		62			C
				fdist. ≥ 4 MHz		68			C
				fdist. > 10 MHz		68			C
7.50		At 165 kHz IF bandwidth, FSK, T_{amb} = 25°C 20 Kbit/s ± 20 kHz	(1,2)	fdist.≥ 225 kHz	—	42	—	dBc	C
				fdist. ≥ 450 kHz		48			C
				fdist. ≥ 1 MHz		58			C
				fdist. ≥ 4 MHz		65			C
				fdist. > 10 MHz		65			C
7.60		At 366 kHz IF bandwidth, FSK, T_{amb} = 25°C 20 Kbit/s ± 20 kHz	(1,2)	fdist.≥ 500 kHz	—	49	—	dBc	C
				fdist.≥ 1 MHz		58			C
				fdist. ≥ 4 MHz		65			C
				fdist. > 10 MHz		65			C
7.70	Image rejection	Low-band	(1,2)	IM_{RED}	45	55	—	dB	A
		High-band			38	47	—	dB	A
		no adaptive algorithm used; therefore,numbers valid if large disturber applied before useful signal			—	—	—	—	—
7.80	Blocking $3f_{LO}$, $5f_{LO}$	Low-band	(1,2)	BL_{NfLO}	—	—	—	dB	—
		$3*f_{LO}-f_{IF}$			27	32	37		C
		$5*f_{LO}+f_{IF}$			28	33	38		C
		High-band			—	—	—		—
		$3*f_{LO}-f_{IF}$			—	39	—		C
		$5*f_{LO}+f_{IF}$			—	45	—		C

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
7.90	Nominal IF frequency	RxDSP property depends on nominal RF frequency and DIV_IF $f_{IF} = f_{RF}/(DIV\_IF * 6)$	—	f_{IF}	242	251	276	kHz	B
8.10	System input referred compression point	No AGC is used; therefore, the full dynamic is available to receive signals at sensitivity level on pin	(1,2)	ICP_{1dB}	—	-45	—	dBm	B
8.20	System input referred 3rd-order intercept point	Low-band High-band	(1,2)	IIP3	—	-35 -37	—	dBm	C
8.30	Max, useful RX input level without damping	System works from sensitivity level up to that level with BER = 10^{-3}	(1,2)	P_{In_max1}	-10	+10	—	dBm	C
8.40	Max, useful RX input level with damping	System works from sensitivity level up to that level with BER = 10^{-3}	4	P_{In_max2}	+5	+10	—	dBm	C
8.50	Input impedance	Measured on application board,RC parallel equivalent circuit	—	Z_{in}	-20%	—	+20%	—	—
		315 MHz	1			870		Ω	C
						2.9		pF	C
		433.92 MHz	1			400		Ω	C
						2.9		pF	C
		868.3 MHz	2			340		Ω	C
						1.4		pF	C
		915 MHz	2			330		Ω	C
						1.4		pF	C
8.60	LNA amplitude detector switch level	Firmware switches SPDT to damping on if a level above $S_{Gainswitch}$ is present during start of RXMode	(1,2)	$P_{Gainswitch}$	—	-39	—	dBm	B
8.70	SPDT switch RX insertion loss	Damping-off Sensitivity matching RF_IN with SPDT to 50W compared to matching RF_IN directly to 50W	(3,4)	IL_{Switch_RX}	—	—	—	—	—
		Low-band, 433.92 MHz				0.7	1.1	dB	C
		High-band, 868 MHz				1.0	1.4	dB	C

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
8.80	SPDT switch RX damping ON	Same matching as parameter no. 8.70 This influences the blocking behavior if measured at pin 4	(3,4)	D_{switch}	—	—	—	—	—
		Low-band			14	15	16	dB	C
		High-band			17	18	19	dB	C
8.90	LO spurious at LNA input	freq > 1 GHz	(1,2)	$P_{LO\_LNA\_IN}$	—	-60	-50	dBm	C
		freq < 1 GHz			—	-86	-60	dBm	C
9.00	RSSI accuracy	$P_{RFIN\_LB(HB)}$ = -70 dBm	(1,2), 4	$RSSI_{ABS\_ACCU}$	—	—	—	dB	B
		Low-band			-5.0		+5.0		
		High-band			-5.5		+5.5		
9.10	RSSI relative accuracy	Measurement range -100 dBm to -50 dBm	(1,2), 4	$RSSI_{REL\_ACCU}$	-1	—	+1	dB	B
9.20	RSSI resolution	DSP property	(1,2), 4	$RSSI_{RES}$	—	0.5	—	dB/ value	D

Note: *1 Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples and D = Design parameter. A pin number in brackets means that they are measured matched to 50Ω on the application board.

5.6 RF Transmit Characteristics

All parameters refer to GND (backplane) and are valid for T_{amb} = -40°C to +85°C, V_{VS} = 1.9-3.6V (3V application) and 2.4-5.5V (5V application) over all process tolerances unless otherwise specified. Typical values are given at V_{VS} = 5V, T_{amb} = 25°C and for a typical process unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305 MHz. Standard EEPROM settings are used unless marked with *1.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
Frequency Ranges and Frequency Resolution of PLL									
See parameters 3.00 to 3.40.									
TXMode Transmit Characteristics									
10.00	Output power range	T_{amb} = 25°C	(7)	P_{Range}	-12	—	+14.5	dBm	B
10.10	Output power programming steps	Optimum load impedance for each power step. Up to two times higher steps for fixed load impedance.	(7)	ΔP_{OUT}	—	0.4	—	dB	—
10.20	Output power at 6 dBm	T_{amb} = 25°C using 6 dBm matching FEPAC = 35 (Low-band) FEPAC = 36 (High-band)	(7)	P_{out_6dBm}	-1.5 dB	6	+1.5 dB	dBm	B

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
Frequency Ranges and Frequency Resolution of PLL									
10.30	Output second harmonic at 6 dBm	T_{amb} = 25°C using 6 dBm matching	(7)	$HM2_{6dBm}$	—	—	—	dBc	—
		315 MHz, FEPAC = 35				-30			C
		433.92 MHz, FEPAC = 35				-36			C
		868.3 MHz, FEPAC = 36				-35			C
		915MHz, FEPAC = 36				-35			C
10.40	Output third harmonic at 6 dBm	T_{amb} = 25°C using 6 dBm matching	(7)	$HM3_{6dBm}$	—	—	—	dBc	—
		315 MHz, FEPAC = 35				-33			C
		433.92 MHz, FEPAC = 35				-41			C
		868.3 MHz, FEPAC = 36				-58			C
		915 MHz, FEPAC = 36				-58			C
10.50	TXMode current consumption at 6 dBm	6 dBm matching	(7), 8, 13	I_{TXMode_6dBm}	—	—	—	mA	—
		315 MHz, FEPAC = 35				8.7	11		B
		433.92 MHz, FEPAC = 35				9.1	12		B
		868.3 MHz, FEPAC = 36				11.5	14.5		B
		915 MHz, FEPAC = 36				11.7	15		B
10.60	Output power at 10 dBm	T_{amb} = 25°C using 10 dBm matching FEPAC = 46 (Low-band) FEPAC = 47 (High-band)	(7)	P_{out_10dBm}	-1.5dB	10	+1.5 dB	dBm	B
10.70	Output second harmonic at 10 dBm	T_{amb} = 25°C using 10 dBm matching	(7)	$HM2_{10dBm}$	—	—	—	dBc	—
		315 MHz, FEPAC = 46				-24			C
		433.92 MHz, FEPAC = 46				-28			C
		868.3 MHz, FEPAC = 47				-24			C
		915 MHz, FEPAC = 47				-27			C
10.80	Output third harmonic at 10 dBm	T_{amb} = 25°C using 10 dBm matching	(7)	$HM3_{10dBm}$	—	—	—	dBc	—
		315 MHz, FEPAC = 46				-25			C
		433.92 MHz, FEPAC = 46				-34			C
		868.3 MHz, FEPAC = 47				-50			C
		915 MHz, FEPAC = 47				-55			C

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No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
Frequency Ranges and Frequency Resolution of PLL									
10.90	TXMode current consumption at 10 dBm	10 dBm matching	(7), 8, 13	I_{TXMode_10dBm}	—	—	—	mA	—
		315 MHz, FEPAC = 46				13.1	17		B
		433.92 MHz, FEPAC = 46				13.8	18.5		B
		868.3 MHz, FEPAC = 47				17.4	22.5		B
		915 MHz, FEPAC = 47				17.4	23		B
11.00	Output power at 14 dBm	T_{amb} = 25°C using 14 dBm matching FEPAC = 56 (Low-band) FEPAC = 57 (High-band)	(7)	P_{out_14dBm}	-1.5 dB	14	+1.5 dB	dBm	B
11.10	Output second harmonic at 14 dBm	T_{amb} = 25°C using 14 dBm matching	(7)	$HM2_{14dBm}$	—	—	—	dBc	—
		315 MHz, FEPAC = 56				-30			C
		433.92 MHz FEPAC = 56				-30			C
		868.3 MHz, FEPAC = 57				-24			C
		915 MHz, FEPAC = 57				-24			C
11.20	Output third harmonic at 14 dBm	Tamb = 25°C using 14 dBm matching	(7)	$HM3_{14dBm}$	—	—	—	dBc	—
		315 MHz, FEPAC = 56				-30			C
		433.92 MHz, FEPAC= 56				-31			C
		868.3 MHz, FEPAC = 57				-50			C
		915MHz, FEPAC = 57				-51			C
11.30	TXMode current consumption at 14 dBm	14 dBm matching	(7), 8, 13	I_{TXMode_14dBm}	—	—	—	mA	—
		315 MHz, FEPAC = 56				24.3	33		B
		433.92 MHz, FEPAC = 56				26.3	36		B
		868.3 MHz, FEPAC = 57				32.7	45		B
		915 MHz, FEPAC = 57				33.5	46		B
11.40	Output power change one full temperature and supply voltage range	Low-band, High-band 0 to ≤ 10 dBm	(7)	$\Delta P_{TambVs1}$	—	—	—	dB	—
		V_{VS_PA} = 3.0V			-1.5		+1.5		C
		5V application: V_{VS_PA} = 2.7-3.3V			-3	—	+2		C
		3V application: V_{VS_PA} = 1.9-3.6V			-5.5		+2.5		C
		P = P_{out}+ΔP			—		—		—

.....continued

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
Frequency Ranges and Frequency Resolution of PLL									
11.50	Output power change two full temperature and supply voltage range	High-band> 10-14 dBm	(7)	$\Delta P_{TambVs2}$	—	—	—	dB	—
		V_{VS_PA} = 3.0V			-3		+1.5		C
		5V application: V_{VS_PA} = 2.7-3.3V			-4		2.5		C
		3V application: V_{VS_PA} = 2.1-3.6V			-6		+3		C
		P = P_{out}+ΔP			—		—		—
11.60	Spurious emission	Low-band:	(7)	SP_{TX}	—	—	—	dBc	—
		at ± f_{XTO}				-80	-65		B
		at ± f_{AVR}(f_{XTO}/4)				-85	-65		C
		at ± f_{CLK_OUT}(f_{XTO}/6)				-80	-65		C
		at ± f_{XTO}				-72	-60		B
		at ± f_{AVR} (f_{XTO}/4)				-85	-60		C
		at ± f_{CLK_OUT}(f_{XTO}/6)				-78	-60		C
11.70	TX transparent data rate in Manchester and NRZ mode	Manchester mode NRZ mode pre-emphasis enabled for symbol rates higher than 40 Kbits	18,7	$DR_{TX\_TM\_MAN}$	—	—	80	Kbit/s	B
				$DR_{TX\_TM\_NRZ}$			160	Ksym/s	B
11.80	TX buffered data rate in Manchester and NRZ mode	Manchester mode	—	$DR_{TX\_BUF\_MAN}$	—	—	80	Kbit/s	B
		NRZ mode		$DR_{TX\_BUF\_NRZ}$			120	Ksym/s	B
11.90	TX buffered data rate programming step in Manchester and NRZ mode	AVR running with f_{XTO}/4	7	ΔDR_{BUF}	—	—	1	%	D
Antenna Tuning and SPDT in TXMode									
12.00	Antenna tuning capacitor range	FEAT.ANTN[3:0] = 0-15	5	C_{TUNE_RANGE}	4	—	9	pF	B
12.10	Antenna tuning capacitor resolution	4 bits controlled with RF front-end register FEAT.ANT[3:0] available	5	C_{TUNE_RES}	—	0.16	0.2	pF	C
12.20	Antenna tuning series resistance	The series resistance influences the quality factor of the loop antenna and causes radiated TX power losses	5	$C_{TUNE\_SRESIST}$	—	2.5	4	Ω	C
12.30	Antenna tuning maximum RF amplitude	If higher levels occur in application an external capacitor to GND is needed to reduce the amplitude.	5	$C_{TUNE\_RFAMP\_MAX}$	—	—	3	V_p	D

.....continued									
No.	**Parameters**	**Test Conditions**	**Pin**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Type***
Frequency Ranges and Frequency Resolution of PLL									
12.40	SPDT insertion loss TX	Transmitted power using matching RF_OUT with SPDT to 50W compared to matching RF_OUT directly to 50W	(4,6)	IL_{Switch_TX}	—	—	—	—	—
		Low-band				0.5	1.1	dB	C
		High-band				0.7	1.2	dB	C
12.45	Maximum peak voltage on SPDT_ANT (pin4)	—	4	$V_{PEAK\_SPDT\_ANT}$	-0.3	—	VS+ 0.3	V	D
12.50	Maximum peak voltage on SPDT_TX (pin6)	—	6	$V_{PEAK\_SPDT\_TX}$	-0.3	—	VS+ 0.3	V	D

Note: *1 Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = Characterized on samples and D = Design parameter. Pin numbers in brackets mean that they are measured matched to 50Ω on the application board.

5.7 Oscillators and CLK_OUT

All parameters refer to GND (backplane) and are valid for T_{amb} = -40°C to +85°C, V_{VS} = 1.9-3.6V (3V application) and 2.4-5.5V (5V application) over all process tolerances, quartz parameters C_m = 4 fF and C_0 = 1 pF, unless otherwise specified. Typical values are given at V_{VS} = 5V, T_{amb} = 25°C and for a typical process, unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305 MHz. Standard Microchip EEPROM settings are used unless marked with *1.

Table 5-4. Oscillators and CLK_OUT

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
13.00	CLK_OUT equivalent internal capacitance	Used for current calculation	13,22	C_{CLK}	—	7.5	10	pF	C
13.10	Supply current increase CLK_OUT active	Apply calculation to all operation modes except OFFMode	13	ΔI_{CLK}	$(C_{CLK}+C_{LOAD\_CLK\_OUT}) \times V_{VS} \times f_{OUT}$			A	C
13.30	XTO frequency range	—	10, 11	f_{xto}	23.8	24.305	26.2	MHz	C
13.40	XTO pulling due to internal capacitance and XTO tolerance	C_m = 4 fF T_{amb} = 25°C	10, 11	ΔF_{XTO1}	-10	—	+10	ppm	B
13.50	XTO pulling due to temperature and supply voltage	C_m = 4 fF T_{amb} = -40°C to +85°C	10, 11	ΔF_{XTO2}	-4	—	+4	ppm	B
13.60	Maximum C_0 of XTAL	XTAL parameter	10, 11	C_{0_max}	—	1	2	pF	D
13.70	XTAL, C_m motional capacitance	XTAL parameter	10, 11	C_m	—	4	10	fF	D
13.90	XTAL,real part of XTO impedance at start-up	C_m = 4 fF C_0 = 1 pF T_{amb}<85°C	10, 11	R_{e_start2}	1100	—	—	Ω	B

.....continued									
No.	**Parameters**	**Test Conditions**	**Pin**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**	**Type***
14.00	XTAL,maximum R_m after start-up	XTAL parameter	10, 11	R_{m_max}	110	—	—	Ω	D
14.10	Internal load capacitors	Including ESD and package capacitance. Specify XTAL for 7.5 pF load capacitance (including 1 pF PCB capacitance per pin)	10, 11	C_{L1}, C_{L2}	13.3	14	14.7	pF	B
14.20	Slow RC oscillator frequency	Polling cycle can be calibrated ±2% accurate with f_{XTO}	22	f_{SRC}	-10%	125	+10%	kHz	A
14.30	Fast RC oscillator frequency	FRC oscillator can be calibrated ±2% accurate with f_{XTO}	22	f_{FRC}	-5%	6.36	+5%	MHz	A

Note: *1 Type means: A = 100% tested at voltage and temperature limits, B = 100% correlation tested, C = Characterized on samples and D = Design parameter.

5.8 I/O Characteristics for Ports PB0 to PB7 and PC0 to PC5

All parameters refer to GND (backplane) and are valid for T_{amb} = -40°C to +85°C, V_{VS} = 1.9-3.6V (3V application) and 2.4-5.5V (5V application) over all process tolerances, unless otherwise specified. Typical values are given at V_{VS} = 5V, T_{amb} = 25°C and for a typical process, unless otherwise specified. Crystal oscillator frequency f_{XTO} = 24.305 MHz. Standard Microchip EEPROM settings are used unless marked with *1.

Table 5-5. I/O Characteristics for Ports PB0 to PB7 and PC0 to PC5

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
15.00	Input low voltage	PC0 to PC5 PB0 to PB7	14-19 22-29	V_{IL}	-0.3	—	0.2x V_{VS}	V	A
15.05	Input low leakage current I/O pin	PC0 to PC5 PB0 to PB7	14-19 22-29	I_{IL}	—	—	-1	µA	A
15.10	Input high voltage	PC0 to PC5 PB0 to PB7	14-19 22-29	V_{IH}	0.8x V_{VS}	—	V_{VS}+0.3	V	A
15.15	Input high leakage current I/O pin	PC0 to PC5 PB0 to PB7	14-19 22-29	I_{IH}	—	—	1	µA	A
15.20	Output low voltage	For 3V application I_{OL} = 0.2 mA	14-19 22-29	V_{OL_3V}	—	—	0.1x V_{VS}	V	A
		For 5V application I_{OL} = 0.8 mA		V_{OL_5V}			0.1x V_{VS}	V	A
15.30	Output high voltage	For 3V application I_{OH} = -0.2 mA	14-19 22-29	V_{OH_3V}	0.9xV_{VS}	—	—	V	A
		For 5V application I_{OH} = -0.8 mA		V_{OH_5V}	0.9xV_{VS}			V	A
15.40	I/O pin pull-up resistor	OFFMode – see port B and port C	14-19 22-29	R_{PU}	30	50	70	kW	A

.....continued

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
15.50	Output low voltage for strong LED low-sided river (PB7)	Configurable on pin PB7 For 3V application I_{LOAD} = 1.5 mA	29	V_{OL_STR1}	—	—	0.1x V_{VS}	V	A
		For 5V applicationI_{LOAD} = 5 mA. For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142).					0.1x V_{VS}	V	A
15.60	Output high voltage for strong LED/LNA high-side driver (PB7, PB4)	Configurable on pin PB7 and PB4 For 3V application I_{LOAD} = -1.5 mA	26,29	V_{OH_STR1}	0.9x V_{VS}	—	—	V	A
		For 5V application I_{LOAD} = -5 mA. For more details, refer to the *ATA8510/15 Industrial User's Guide* (DS50003142)			0.9x V_{VS}			V	A
15.70	Output low voltage for strong ISP low-side driver (PB3)	Activated in ISP mode I_{OL} = 1.7 mA, V_{Vs}>2.5V T_{amb} = -40°C to +65°C	25	V_{OL_STR2}	—	—	0.1xV_{VS} 0.1x V_{VS}	V V	B B
15.80	Output high voltage for strong ISP high-side driver (PB3)	Activated in ISP mode I_{OH} = -1.7 mA, V_{Vs} >2.5V T_{amb} = -40°C to +65°C	25	V_{OH_STR2}	0.9xV_{VS} 0.9xV_{VS}	—	—	V V	B B
15.90	CLK_OUT output frequency	XTO, FRC or SRC related clock $f_{CLK\_OUT} = f_{OSC}/(2 * CLKOD)$	22	f_{CLK_OUT}	—	—	4.5	MHz	B
16.00	CLK_OUT duty cycle	$C_{LOAD\_CLK\_OUT}$ = 10 pF f_{CLK_OUT} = 4.5 MHz	22	DTY_{CLK_OUT}	45	—	55	%	A
16.10	I/O pin output delay time (rising edge)	For 3V application C_{Load} = 10 pF	14-19 22-29	$T_{del\_rise\_3V}$	13.6	17.5	22.4	ns	D
		For 5V application C_{Load} = 10 pF		$T_{del\_rise\_5V}$	9.7	12.4	15.7	ns	D
16.20	I/O pin rise time (0.1×V_{VS} to 0.9×V_{VS})	For 3V application C_{Load} = 10 pF	14-19 22-29	T_{rise_3V}	20.7	23.9	28.4	ns	D
		For 5V application C_{Load} = 10 pF		T_{rise_5V}	12.7	14.3	16.6	ns	D
16.30	I/O pin slew rate (rising edge)	For 3V application C_{Load} = 10 pF	14-19 22-29	$T_{sr\_rise\_3V}$	0.115	0.100	0.084	V/ns	D
		For 5V application C_{Load} = 10 pF		$T_{sr\_rise\_5V}$	0.315	0.280	0.240	V/ns	D

.....continued

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
16.40	I/O pin output delay time (falling edge)	For 3V application C_{Load} = 10 pF	14-19 22-29	$T_{del\_fall\_3V}$	13.7	17.4	22.7	ns	D
		For 5V application C_{Load} = 10 pF		$T_{del\_fall\_5V}$	10.4	12.2	16.0	ns	D
16.50	I/O pin fall time ($0.9\times V_{VS}$ to $0.1\times V_{VS}$)	For 3V application C_{Load} = 10 pF	14-19 22-29	T_{fall_3V}	16.2	19.2	22.5	ns	D
		For 5V application C_{Load} = 10 pF		T_{fall_5V}	10.4	12.4	13.7	ns	D
16.60	I/O pin slew rate (falling edge)	For 3V application C_{Load} = 10 pF	14-19 22-29	$T_{sr\_fall\_3V}$	0.148	0.125	0.106	V/ns	D
		For 5V application C_{Load} = 10 pF		$T_{sr\_fall\_5V}$	0.384	0.322	0.292	V/ns	D

Note: *1 Type means: A = 100% tested at voltage and temperature limits, B = 100 % correlation tested, C = Characterized on samples and D = Design parameter.

6. Ordering Information

Extended Type Number	Package	Remarks
ATA8510-GHQW	QFN32	5 mm x 5 mm, 6k tape and reel, PB-free, 20 Kbyte user Flash
ATA8515-GHQW	QFN32	5 mm x 5 mm, 6k tape and reel, PB-free

7. Package Information

This chapter provides information on package markings, dimension, and footprint of the ATA8510/15.

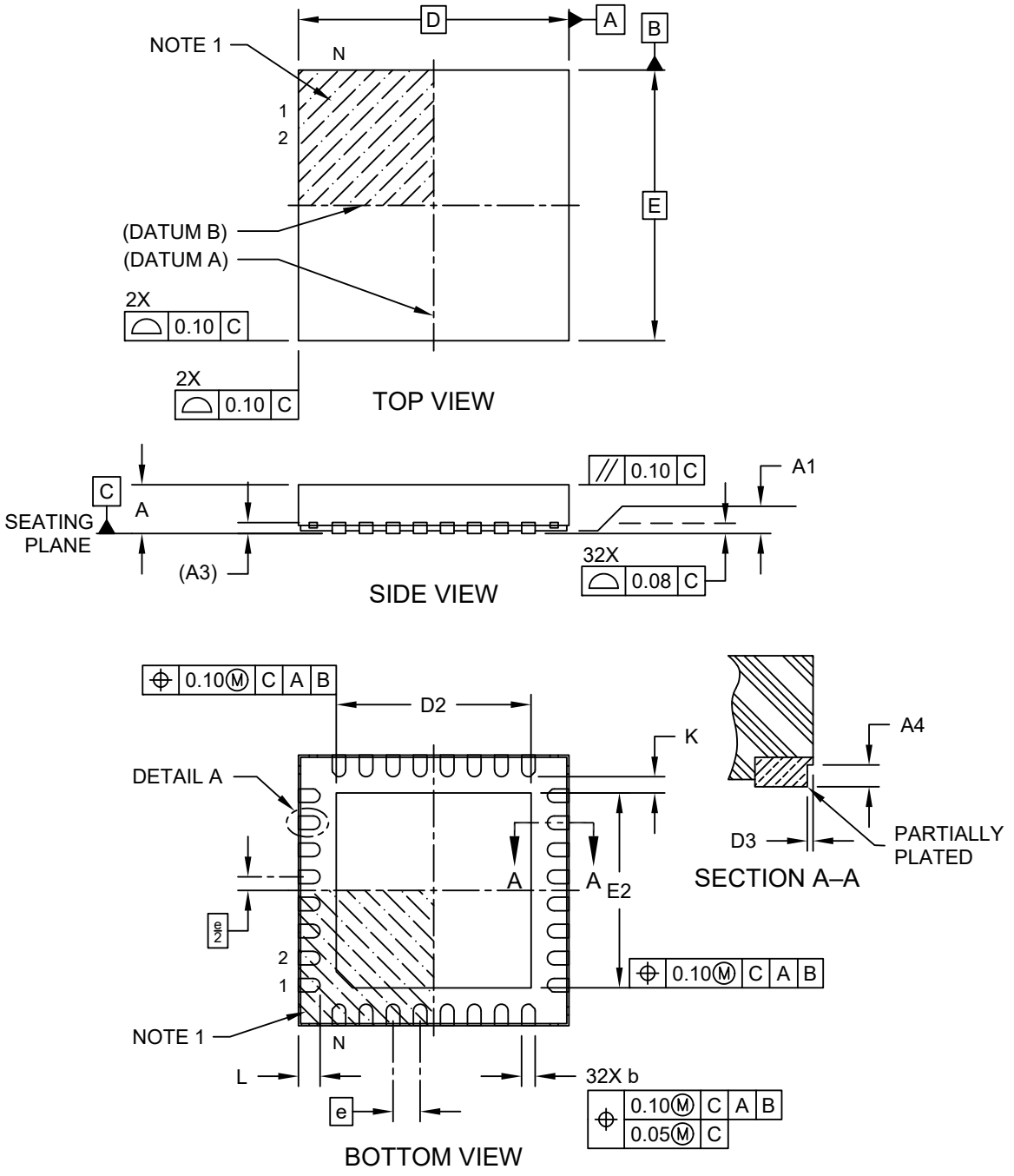
7.1 ATA8510/15 Packaging Information

For the most current package drawings, refer to the Microchip Packaging Specification located at www.microchip.com/en-us/support/package-drawings.

The following images illustrate the packaging information of the ATA8510/15, which has a 32-Lead Very Thin Plastic Quad Flat, No Lead Package (RTB) – 5x5 mm Body [VQFN] With 3.6x3.6 mm Exposed Pad and Stepped Wettable Flanks.

32-Lead Very Thin Plastic Quad Flat, No Lead Package (RTB) - 5x5 mm Body [VQFN] With 3.6x3.6 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZBS

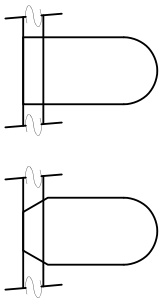
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



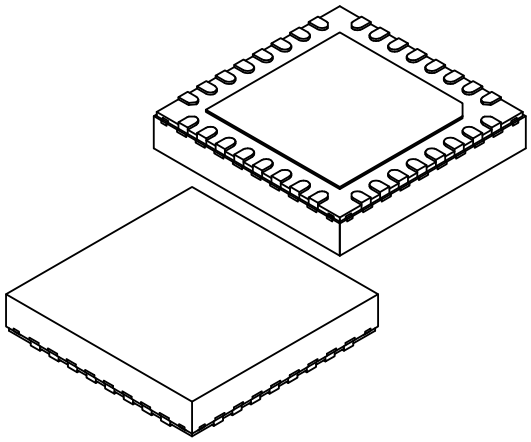
Microchip Technology Drawing C04-21391 Rev G Sheet 1 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (RTB) - 5x5 mm Body [VQFN] With 3.6x3.6 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZBS

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		32	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.50	3.60	3.70
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.50	3.60	3.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Cut Width	D3	-	-	0.085
Wettable Flank Step Cut Depth	A4	0.10	-	0.19

Dimensions D3 and A4 above apply to all new products released after November 1, and all products shipped after January 1, 2019, and supersede dimensions D3 and A4 below.
No physical changes are being made to any package; this update is to align cosmetic and tolerance variations from existing suppliers.

Wettable Flank Step Length	D3	0.035	0.06	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

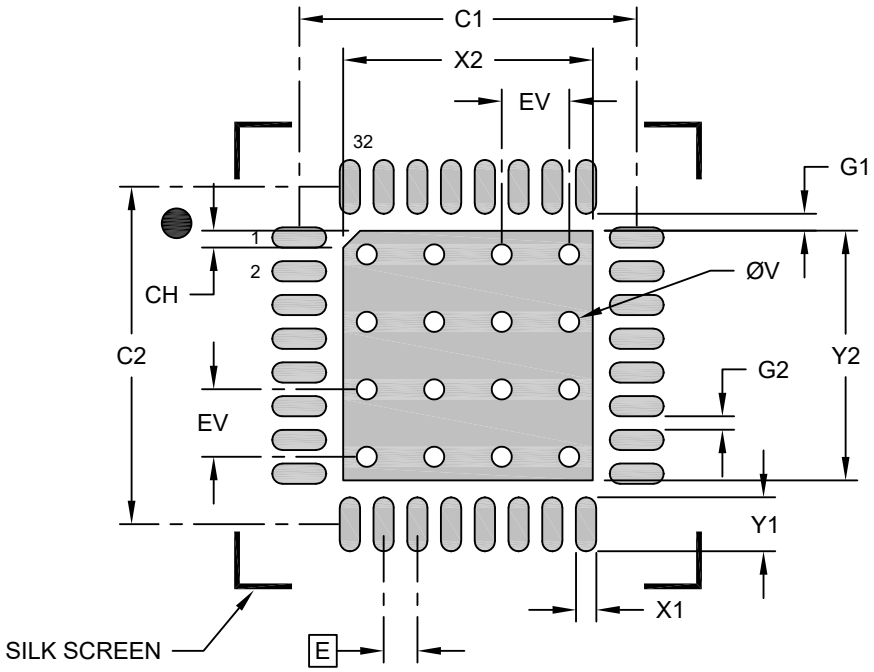
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21391 Rev G Sheet 2 of 2

32-Lead Very Thin Plastic Quad Flat, No Lead Package (RTB) - 5x5 mm Body [VQFN] With 3.6x3.6 mm Exposed Pad and Stepped Wettable Flanks; Atmel Legacy ZBS

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			3.70
Optional Center Pad Length	Y2			3.70
Exposed Pad 45° Corner Chamfer	CH		0.25	
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X32)	X1			0.30
Contact Pad Length (X32)	Y1			0.80
Contact Pad to Center Pad (X32)	G1	0.25		
Contact Pad to Contact Pad (X28)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23391 Rev G

8. Document Revision History

Table 8-1. Document Revision History

Revision	Date	Section	Description
A	07/2022	Document	Initial Revision

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