December 2012

1.0 Introduction

The goal of a clock buffer is to reproduce the input clock signal with minimal additive jitter. This requires both a well-designed buffer device and a carefully designed circuit board that minimizes the external sources of jitter on the output. One of these sources is the interfering tone produced by power supply switching. The tone can be a significant source of jitter at the buffer's output. The jitter contributed by the tone can be mitigated by external filtering and on-chip regulators. This document will show how to measure Power Supply Noise Rejection (PSNR) and allows a designer to estimate the effect of jitter on the buffer output based on the expected power supply characteristics.

2.0 Power Supply Rejection Measurement Setup

Noise sources on a power supply rail can be either random or periodic. Both can be detrimental to jitter performance of a buffer, but it is usually the periodic noise related to the power supply switching frequency (or indeed other digital noise that couples into the power supply) that dominates the jitter response. From an analysis perspective, it useful to characterize noise and the buffer's response in terms of the frequency domain. A simple test circuit can be used to inject a tone at a particular frequency on the supply rail, and then measure the response on the buffer.

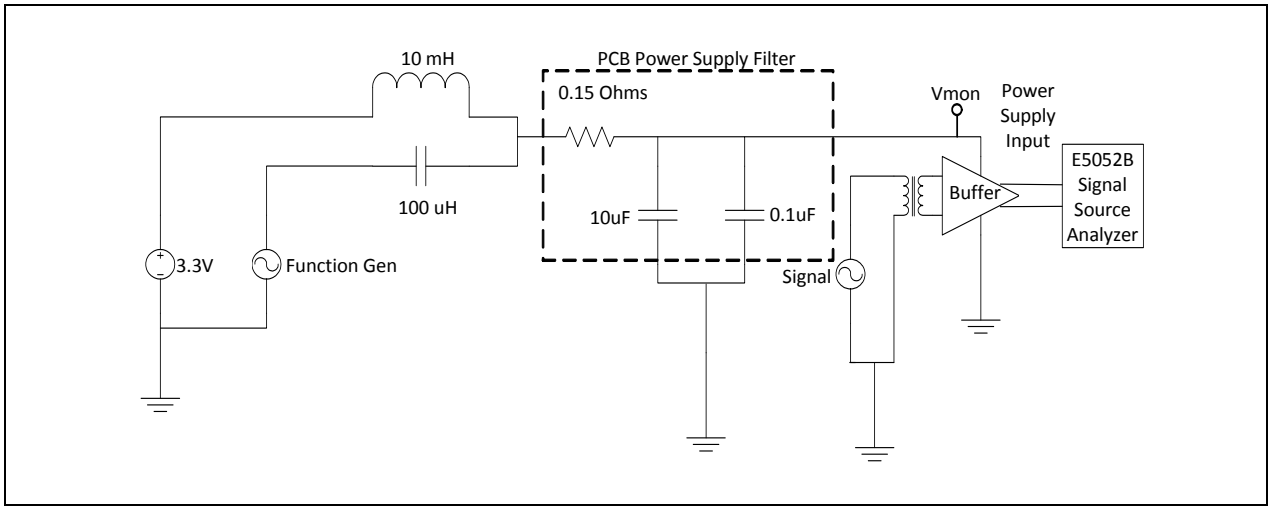

Figure 1 - PSNR Measurement Setup

Figure 1 shows the schematic for the PSNR measurement. The PCB power supply filter shown is the circuit recommended in the clock buffer datasheet. The DC source is a clean linear supply used to provide the 3.3V to the DUT. The function generator is used to inject a tone into the supply rail. The large inductor prevents AC current from the function generator propagating back into the DC source. The large capacitor prevents current from the DC supply flowing into the function generator. The PCB Power Supply Filter and the buffer are placed together on the same circuit board. The tone voltage at the input to the DUT is measured at point Vmon.

3.0 PSNR Measurement Results

Using this test setup, a tone at a particular frequency is generated, and the effect on the output signal is captured by the Agilent E5052B Signal Source Analyzer. The signal source analyzer is configured with its "Spurious" option set to display spur power in dBc (decibels relative to the carrier). The magnitude of the tone or spur is shown on the phase noise plot. The PSNR is defined as the ratio of the output tone power to the carrier power. Figure 2 shows an example of 100 kHz power supply tone on a 125MHz input signal. The power of the tone at cursor 1 is shown in the first line of the text displayed in the plot: -77.4356 dBc. This is the PSNR of the buffer for this tone frequency.

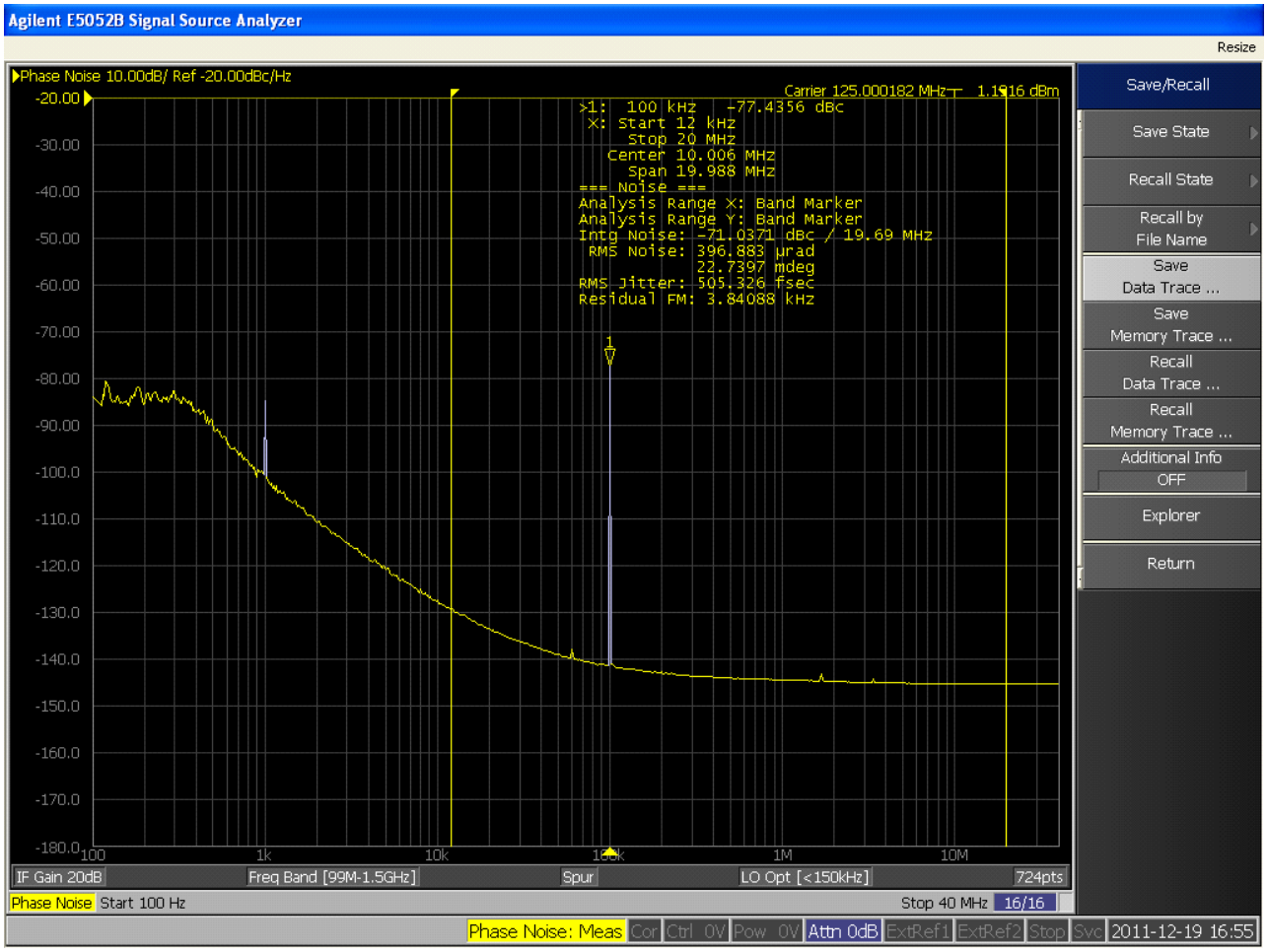

Figure 2 - Effect of Power Supply Tone on Buffer Output -- Phase Noise

Table 1 presents the additive jitter associated with a power supply tone at various frequencies for a 1:4 LVPECL clock buffer at room temperature. The carrier frequency in this case is 125 MHz, and the amplitude of the ripple is fixed at 25 mVpp at the DUT. The additive jitter is calculated from Equation 1. The buffer shows very good rejection of power supply noise. Note that the additive jitter varies in a non-linear fashion with tone frequency.

Equation 1

$$Jtone_{rms} = \frac{10^{\frac{PSNR}{20}}}{\sqrt{2} \times \pi \times Fc}$$

Where:

PSNR is the magnitude of the tone power relative to the carrier in dBc.
Fc is the frequency of the carrier in Hz.
$Jtone_{rms}$ is the additive rms jitter due to the tone.

Table 1 - Power Supply Rejection at various frequency offsets with a carrier Frequency of 125 MHz

Frequency Offset (kHz)	Amplitude of Tone at Power Supply Input (mV pp)	Power of Tone at Buffer Output relative to Carrier (PSNR in dBc)	Additive Jitter due to Power Supply Tone (fs rms)
100	25	-77.9	231
200	25	-74.1	355
300	25	-73.6	374
400	25	-76.1	281
500	25	-72.6	423

It is difficult to fix the ripple amplitude at greater than 25 mVpp at higher frequencies, as the board power filter and decoupling capacitors tend to shunt the ripple to ground (which is their intended function). Practically, this limits the upper frequency to about 500 kHz.

Measurements show that the additive jitter due to the tone at the output of the buffer is proportional to the amplitude of the tone at the input of the buffer. However, the constant of proportion is different for different tone frequencies. A plot of additive jitter vs input voltage for a 100 kHz tone is shown in Figure 3. From the graph, the amount of additive jitter can be determined based on the amplitude of the 100 kHz ripple.

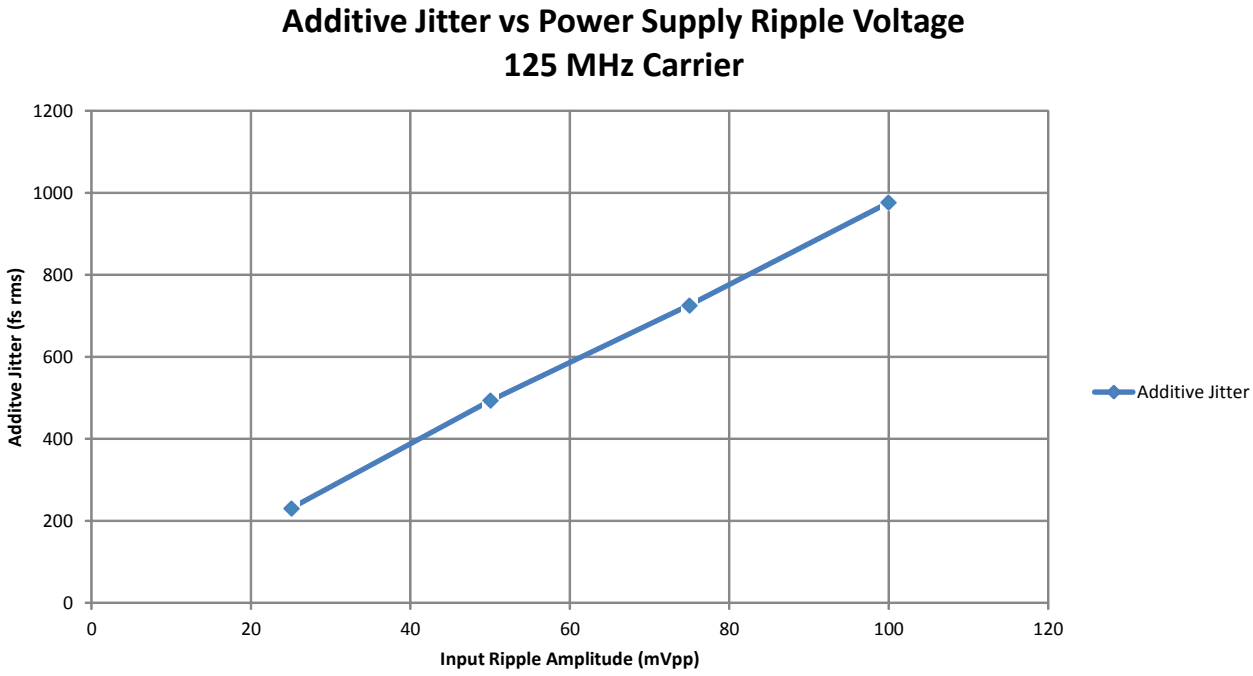

Figure 3 - Additive Jitter vs Input Ripple Amplitude (mVpp)

4.0 Additive Jitter and PSNR

It is useful to understand the impact of a particular power supply tone on the buffer's output in terms of its contribution to additive jitter. Total jitter at the buffer's output is given by Equation 2, with the assumption that the noise contributed by the tone is significantly above the random noise floor.

Equation 2

$$Jtotal_{rms} = \sqrt{Jin_{rms}^{2} + Jadd_{rms}^{2} + Jtone_{rms}^{2}}$$

Where:

Jin_{rms} is the random jitter on the input signal, with any contribution from spurs on the input removed,
$Jadd_{rms}$ is the random additive noise that the buffer contributes,
$Jtone_{rms}$ is the additive jitter contributed by the tone.

Also, in the case where there is no power supply tone, the equation reduces to:

Equation 3

$$Jtotal_{rms} = \sqrt{Jin_{rms}^{2} + Jadd_{rms}^{2}}$$

$Jtone_{rms}$ can be calculated from Equation 1 as stated earlier.

As an example, consider a 125 MHz signal source with a random jitter of 200 fs rms between 12 kHz and 20 MHz. This signal is fed to the input of a clock distribution buffer which has an additive jitter of 110 fs rms at 125 MHz in the same band. In the absence of any power supply tones, the total random jitter output from the buffer will be given by Equation 3, $\sqrt{200^2 + 110^2}$, or 228 fs rms.

Now assume a power supply tone is applied, and that its contribution can be seen on a phase noise plot of the buffer's output as a spur with -85 dBc magnitude. This is the PSNR. The contribution from the tone in terms of jitter is given by Equation 1, and results in about 101 fs rms. Therefore, the total rms random jitter, found from Equation 2, is $\sqrt{200^2 + 110^2 + 101^2}$, or 250 fs rms.

Using the above equations, it is possible to plot a graph of the total jitter vs additive jitter contributed by a tone. For example consider a case in which the input jitter is 100 fs, the additive jitter from the buffer is 110 fs. Figure 4 shows a plot of the total jitter vs increasing additive jitter due to power supply tone. The input jitter and additive jitter dominate the total jitter up to about 200 fs, then the rising jitter contributed by the tone begins to dominate.

Figure 4 - Total Jitter vs Tone Contribution

5.0 Designing for Power Supply Rejection

The PCB power supply filtering also contributes to overall Power Supply Rejection. Figure 5 shows the ideal transfer function of the filter components outlined in Figure 1. The 3dB frequency is given by $1/(2\pi RC)$, which is about 100kHz.

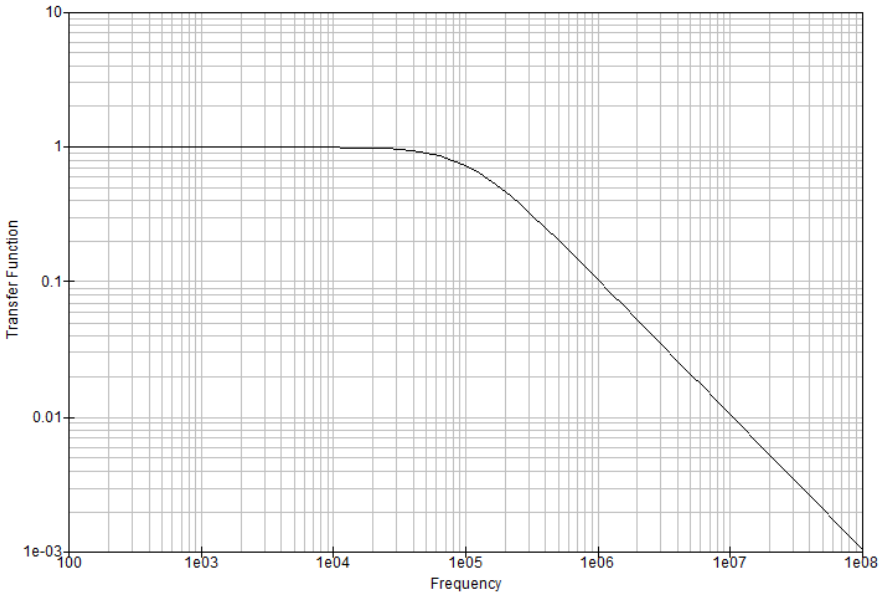

Figure 5 - Transfer Function of Power Supply Filter

The total Power Supply Noise Rejection is a combination of the attenuation due to the filter and the attenuation due to the buffer's intrinsic PSNR.

To appropriately manage power supply tones, the following jitter budgeting procedure can be used:

- The total jitter allowed at the output must be defined.
- The additive jitter of the buffer (J_{add}) and the expected jitter of the input signal (J_{in}) should be established.
- The maximum jitter allowed to be contributed from a tone is then given from a derivative of Equation 2:

$$Jtone_{rms} = \sqrt{Jtotal_{rms}^2 - Jin_{rms}^2 - Jadd_{rms}^2}$$

- The maximum jitter is translated into a maximum tone voltage at the input of the buffer using a plot of additive jitter vs. input power supply ripple, as in Figure 3.
- The maximum voltage at the buffer's input is translated to the maximum ripple voltage on the power supply using Figure 5.

For example, consider a system with a Jin of 300 fs rms and a Jadd of 110 fs rms (at 125 MHz). The maximum tolerable jitter at the output is 500 fs rms. From Equation 2, we have Jtone = 384 fs rms (maximum). Assume the concerning tone is generated by the power supply's switching frequency, which is 100 kHz. From Figure 3, it can be seen that the maximum voltage on the input ripple must be less than ~40 mVpp. From Figure 3, at 100 kHz, the PCB filtering circuit attenuation factor is about 0.7. Therefore the ripple on the power supply must be less than 40 mVpp/0.7 = 57 mVpp to achieve the 500 fs rms budget at the output. This is relatively easily achieved as most power supplies limit ripple below 30 mV pp.

6.0 Conclusion

Power supply selection is an important consideration in low-jitter clock buffer design. To achieve the desired jitter targets, the board designer needs to consider the periodic voltage components on the supply rail, the PCB power supply filter design, and the clock buffer's intrinsic power supply rejection. Microsemi clock buffers provide robust intrinsic power supply rejection. When they are used with the recommended power supply filter, significant attenuation of power supply ripple can be achieved. This allows board designers a wide degree of flexibility in power supply selection, while still maintaining the output jitter targets.

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