SY58021U

4 GHz, 1:4 LVPECL Fanout Buffer/Translator with Internal Termination

Features

- Precision 1:4 LVPECL Fanout Buffer
- Low Jitter Performance
  - 70 fs_{RMS} Phase Jitter (Typical)
- Accepts an Input Signal as Low as 100 mV
- Unique Input Termination and VT Pin Accept DC-Coupled and AC-Coupled Differential Inputs: LVPECL, LVDS, and CML
- 100K LVPECL-Compatible 800 mV Swing Output
- Power Supply 2.5V ±5% and 3.3V ±10%
- –40°C to +85°C Temperature Range
- Available in 16-Lead, 3 mm x 3 mm VQFN Package

Applications

- All SONET and GigE Clock Distribution
- Fibre Channel Clock and Data Distribution
- Backplane Distribution
- High-End, Low-Skew, Multiprocessor, Synchronous Clock Distribution

General Description

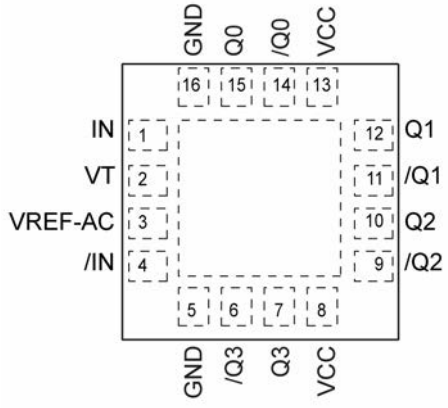
The SY58021U is a 2.5V/3.3V precision, high-speed, fully differential 1:4 LVPECL fanout buffer. Optimized to provide four identical output copies with less than 15 ps output skew and only 70 fs_{RMS} phase jitter, the SY58021U can process clock signals as fast as 4 GHz.

The differential input includes Microchip's unique, 3-pin input termination architecture interfaces to differential LVPECL, CML, and LVDS signals (AC- or DC-coupled) as small as 100 mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage (V_{REFAC}) is provided to bias the VT pin. The outputs are 100K LVPECL compatible, with extremely fast rise/fall times guaranteed to 70 ps.

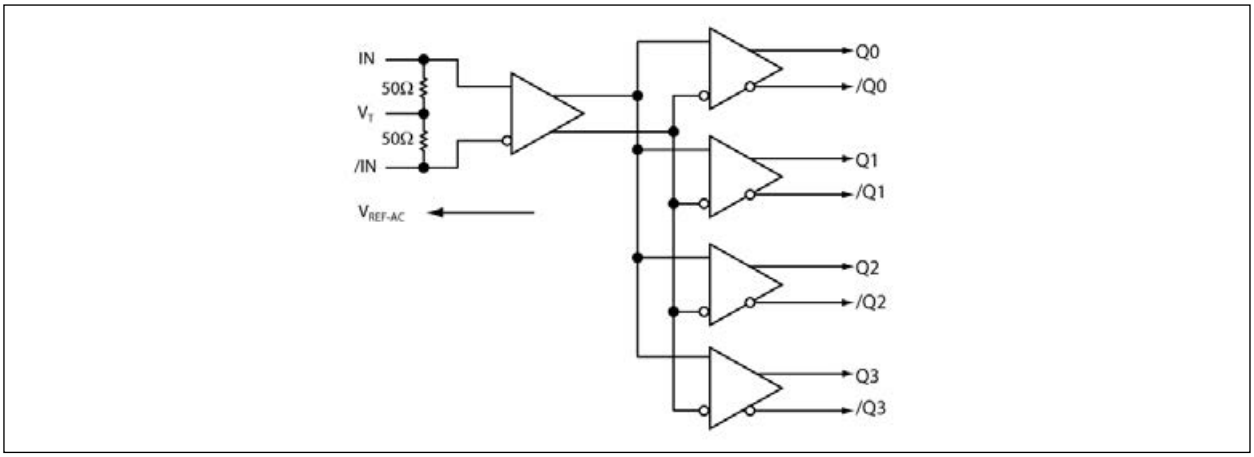
The SY58021U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require faster rise/fall times, or greater bandwidth, consider the SY58022U 1:4 fanout buffer with 400 mV LVPECL output swing, or the SY58020U 1:4 CML fanout buffer. The SY58021U is part of Microchip's high-speed, Precision Edge® product line.

Package Type

SY58021U
16-Lead VQFN (M)
(Top View)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Power Supply Voltage (V_{CC}) ..... –0.5V to +4V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
LVPECL Continuous Output Current (I_{OUT}) ..... 50 mA
LVPECL Surge Output Current (I_{OUT}) ..... 100 mA
Source or Sink Current on VT Pin ..... ±100 mA
Source or Sink Current on IN, /IN Pins ..... ±50 mA
Source or Sink Current on VREF-AC Pin (Note 1) ..... ±1.5 mA

Operating Ratings ‡

Power Supply Voltage (V_{CC}) ..... +2.375V to +3.60V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

INPUT DC ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{CC}	2.375	2.5	2.625	V	V_{CC} = 2.5V
		3.0	3.3	3.6		V_{CC} = 3.3V
Power Supply Current	I_{CC}	—	125	160	mA	No load, V_{CC} = maximum
Input High Voltage	V_{IH}	V_{CC} – 1.6	—	V_{CC}	V	IN, /IN (Note 2)
Input Low Voltage	V_{IL}	0	—	V_{IH} – 0.1	V	IN, /IN
Input Voltage Swing	V_{IN}	0.1	—	1.7	V	IN, /IN (See Figure 1-1)
Differential Input Voltage Swing	V_{DIFF_IN}	0.2	—	—	V	IN, /IN (See Figure 1-2)
IN-to-VT Resistance	R_{IN}	40	50	60	Ω	—
IN-to-VT Voltage	V_{T_IN}	—	—	1.28	V	—
Output Reference Voltage	V_{REF-AC}	V_{CC} – 1.3	V_{CC} – 1.2	V_{CC} – 1.1	V	—

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

2: $V_{IH(MIN)}$ not lower than 1.2V.

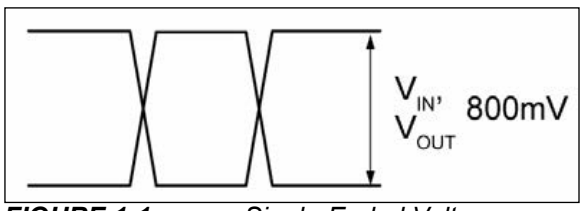


FIGURE 1-1: *Single-Ended Voltage Swing.*

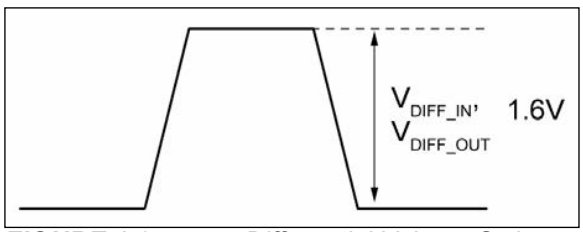


FIGURE 1-2: *Differential Voltage Swing.*

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10% or 2.5 ±5%; R_L = 50Ω to V_{CC} − 2V; T_A = –40°C to +85°C, unless otherwise stated. Note 1

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output High Voltage	V_{OH}	V_{CC} – 1.145	—	V_{CC} – 0.895	V	—
Output Low Voltage	V_{OL}	V_{CC} – 1.945	—	V_{CC} – 1.695	V	—
Output Voltage Swing	V_{OUT}	550	780	1050	mV	See Figure 1-1
Differential Output Voltage Swing	V_{DIFF_OUT}	1100	1560	2100	mV	See Figure 1-2

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3 ±10%; R_L = 50Ω to V_{CC} − 2V; T_A = –40°C to +85°C, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Operating Frequency	f_{MAX}	4	—	—	GHz	Clock, V_{OUT} ≥ 400 mV
		—	5	—	Gbps	Data, V_{OUT} ≥ 400 mV
Propagation Delay	t_{PD}	150	220	300	ps	—
Channel-to-Channel Skew	t_{CHAN}	—	4	15	ps	Note 1
Part-to-Part Skew	t_{SKEW}	—	—	30	ps	Note 2
RMS Phase Jitter	t_{JITTER}	—	70	—	fs	Output: 622 MHz, Integration Range: 12 kHz to 20 MHz
Output Rise/Fall Time (20% to 80%)	t_r,t_f	35	75	110	ps	At full swing.

Note 1: Skew is measured between outputs of the same bank under identical transitions.

2: Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature Range	T_S	–65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Operating Temperature Range	T_A	–40	—	+85	°C	—
Package Thermal Resistances						
Thermal Resistance, VQFN 16-Ld	θ_{JA}	—	60	—	°C/W	Still-Air
	θ_{JA}	—	54	—	°C/W	500 lfpm
	Ψ_{JB}	—	33	—	°C/W	Junction-to-Board Resistance, Note 1

Note 1: Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

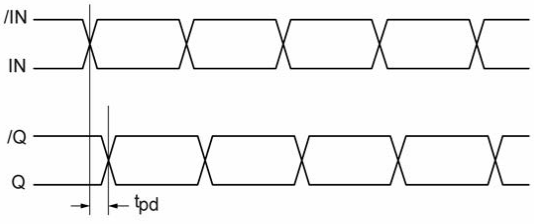


FIGURE 1-3: *Timing Diagram.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

V_{CC} = 2.5V, GND = 0V, V_{IN} = 100 mV, T_A = +25°C, unless otherwise stated.

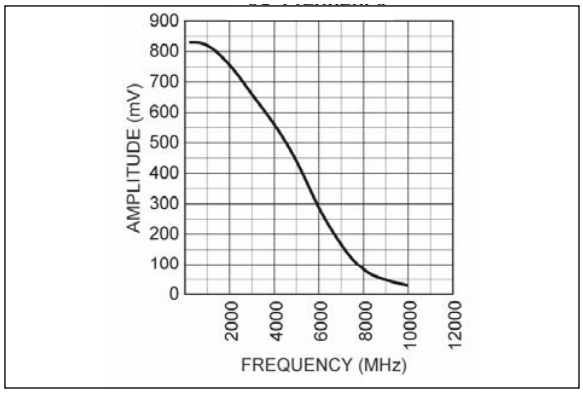


FIGURE 2-1: *Amplitude vs. Frequency.*

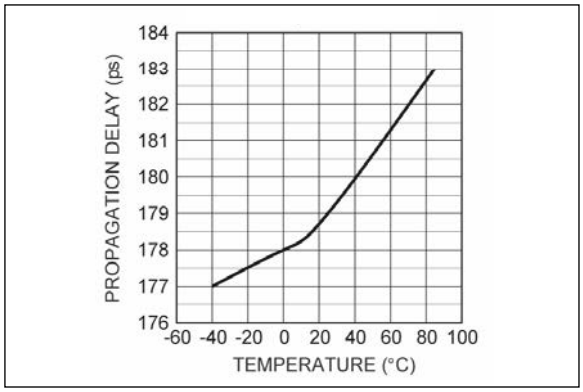


FIGURE 2-4: *Propagation Delay vs. Temperature.*

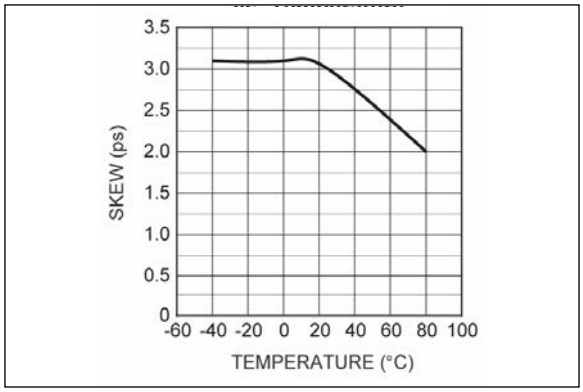


FIGURE 2-2: *Skew vs. Temperature.*

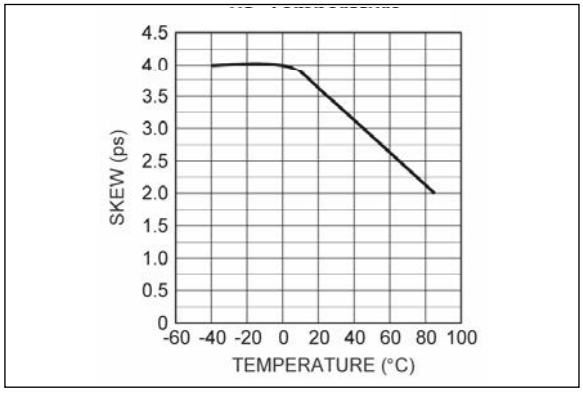


FIGURE 2-5: *Skew vs. Temperature.*

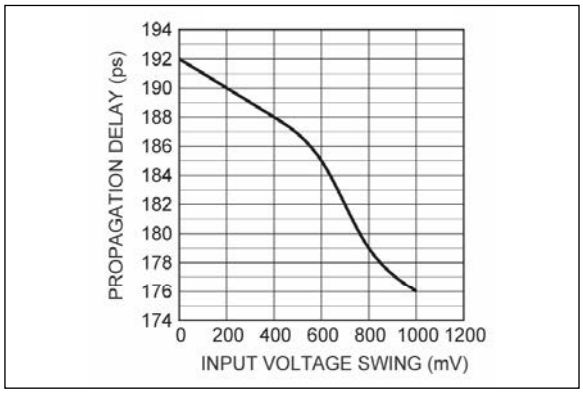


FIGURE 2-3: *Propagation Delay vs. Input Voltage Swing.*

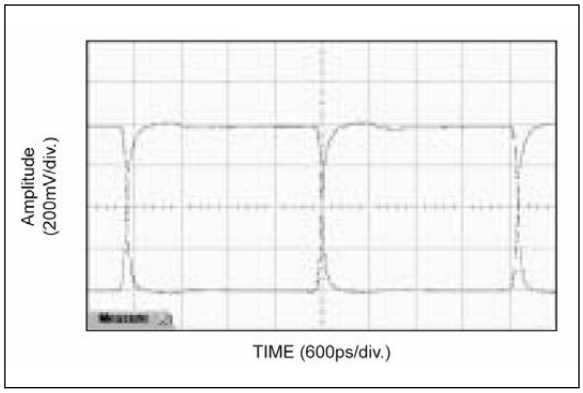


FIGURE 2-6: *200 MHz Output.*

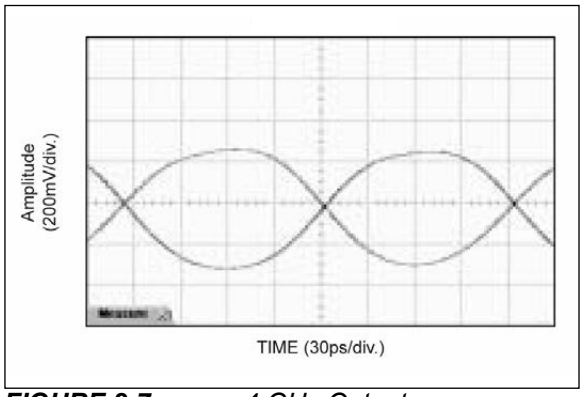


FIGURE 2-7: *4 GHz Output.*

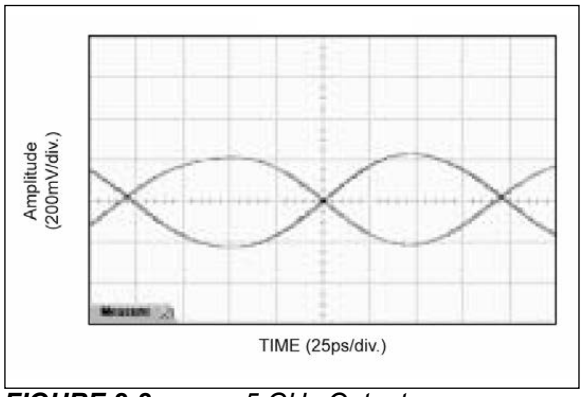


FIGURE 2-8: *5 GHz Output.*

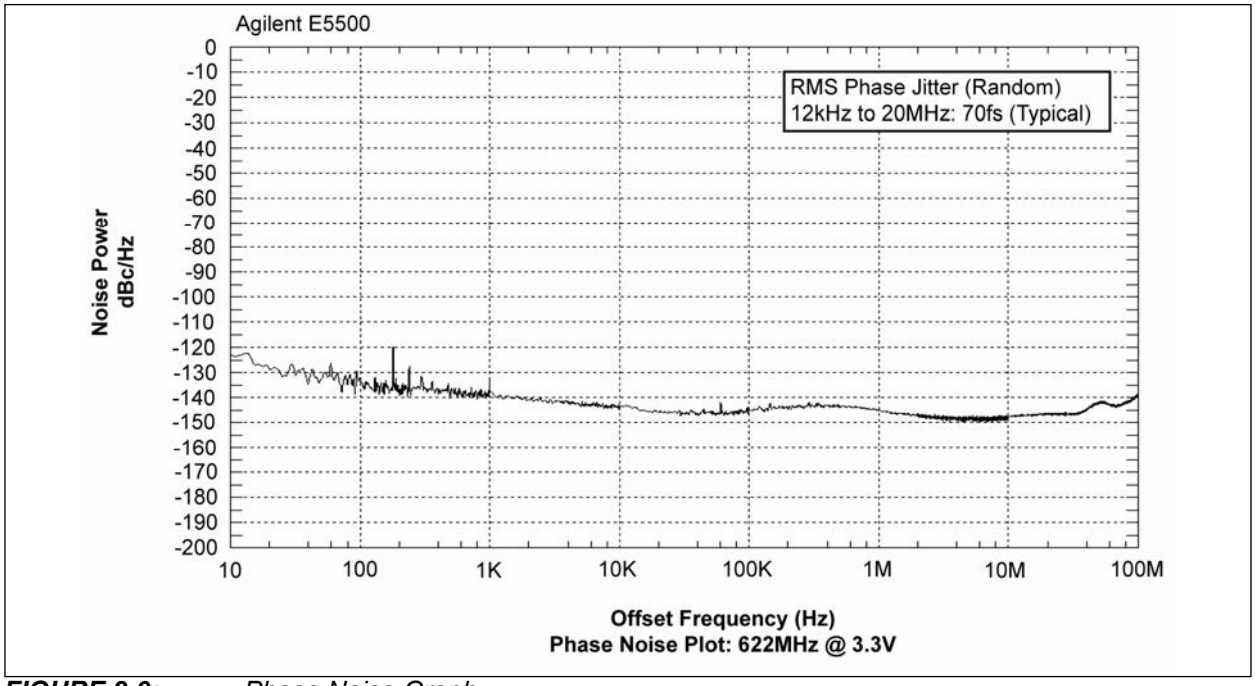


FIGURE 2-9: *Phase Noise Graph.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1, 4	IN, /IN	Differential Input: This input pair receives the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the VT pin. Note that this input will default to an indeterminate state if left open. See the “Input Interface Applications” section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See the “Input Interface Applications” section.
3	VREF-AC	Reference Output Voltage: This output biases to V_{CC} – 1.2V. It is used when AC-coupling to differential inputs. Connect VREF-AC directly to the VT pin. Bypass with 0.01 µF low ESR capacitor to VCC. See the “Input Interface Applications” section.
8, 13	VCC	Positive Power Supply: Bypass with 0.1 µF//0.01 µF low-ESR capacitors as close to the VCC pins as possible.
5, 16	GND, ePAD	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
14, 15, 11, 12, 9, 10, 6, 7	/Q0, Q0, /Q1, Q1, /Q2. Q2, /Q3, Q3	LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 800 mV Proper termination is 50Ω to V_{CC} – 2V at the receiving end. Unused output pairs may be left floating with no impact on jitter or skew. See the “LVPECL Output Termination” section.

Input Stage

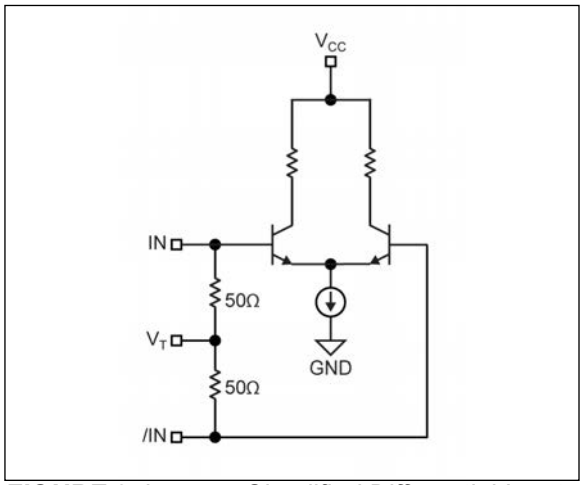


FIGURE 3-1: *Simplified Differential Input Buffer.*

4.0 INPUT INTERFACE APPLICATIONS

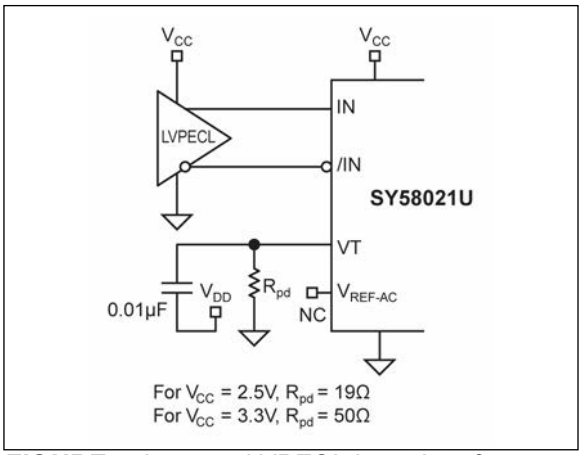


FIGURE 4-1: *LVPECL Input Interface.*

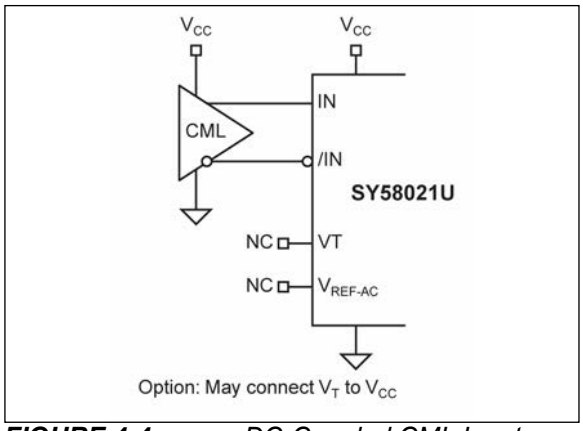


FIGURE 4-4: *DC-Coupled CML Input Interface.*

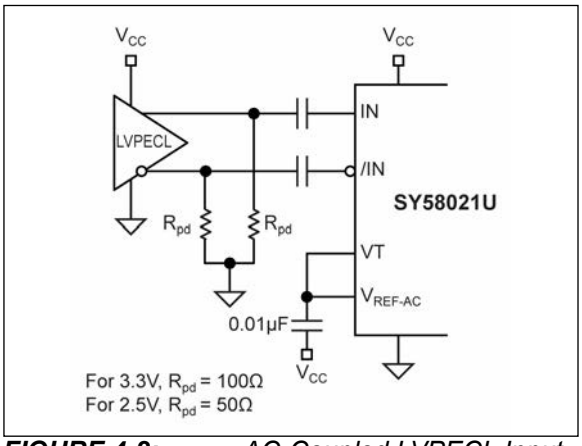


FIGURE 4-2: *AC-Coupled LVPECL Input Interface.*

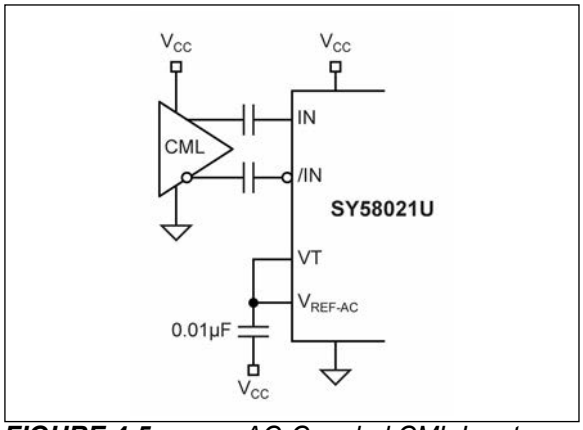


FIGURE 4-5: *AC-Coupled CML Input Interface.*

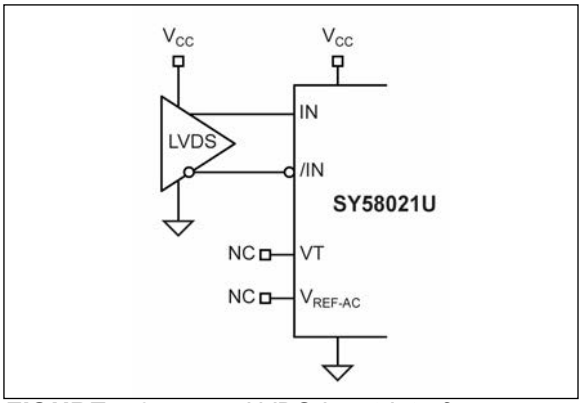
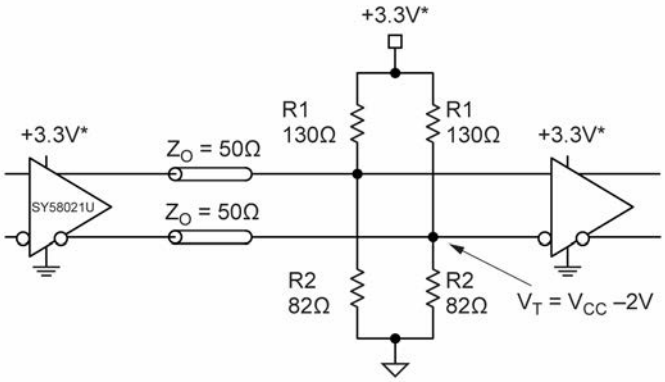


FIGURE 4-3: *LVDS Input Interface.*

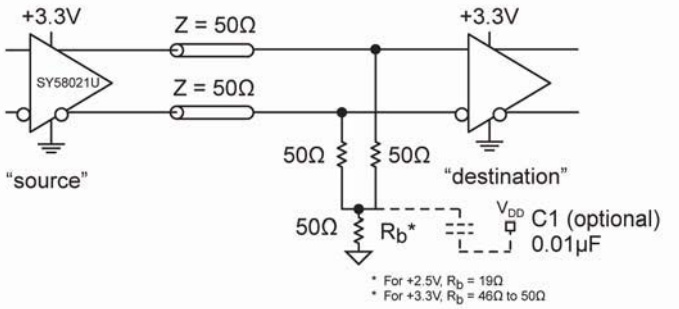
5.0 LVPECL OUTPUT

LVPECL outputs have very-low output impedance (open emitter) and small signal swing, which results in low EMI. LVPECL is ideal for driving 50Ω- and 100Ω-controlled impedance transmission lines. There are several techniques in terminating the LVPECL output (Figure 5-1 through Figure 5-3).



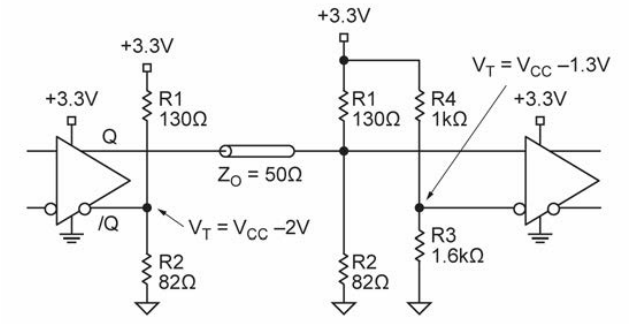
Note:
1. For +2.5V systems, R1 = 250Ω, R2 = 62.5Ω.

FIGURE 5-1: *Parallel Termination: Thevenin Equivalent.*



Notes:
1. Power-saving alternative to Thevenin termination.
2. Place termination resistors as close to destination inputs as possible.
3. Rb resistor sets the DC bias voltage, equal to VT.

FIGURE 5-2: *Parallel Termination: Three-Resistor.*



Notes:
1. Unused output (/Q) must be terminated to balance the output.
2. For +2.5V systems: R1 = 250, R2 = 62.5, R3 = 1.25k, R4 = 1.2k
   For +3.3V systems: R1 = 130, R2 = 82, R3 =1k, R4 = 1.6k
3. Unused output pairs (Q and /Q) may be left floating.

FIGURE 5-3: *Terminating Unused I/O.*

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

16-Lead VQFN*

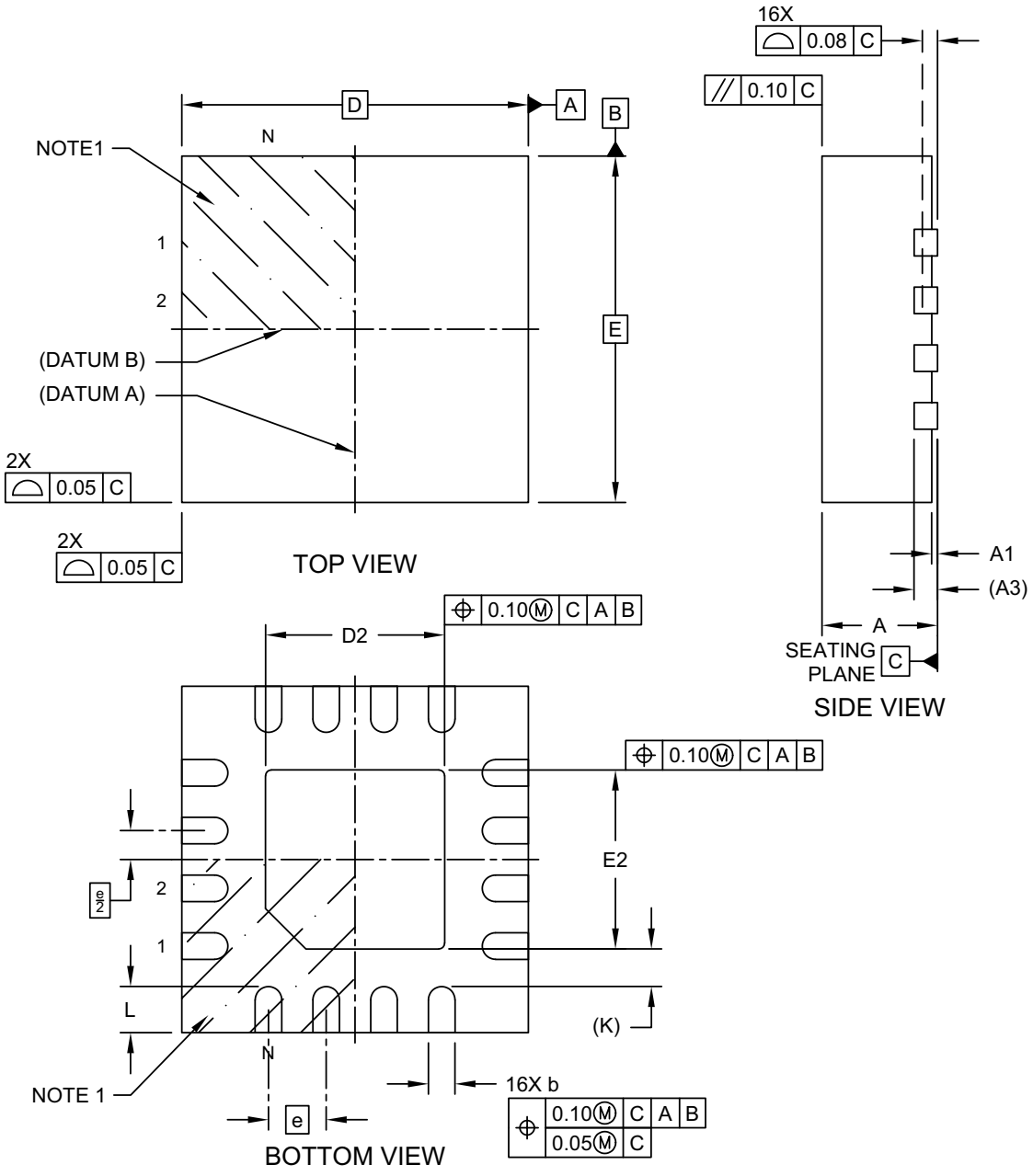
Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad; Micrel Legacy Package QFN33-16LD-PL-1

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev C Sheet 1 of 2

16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad; Micrel Legacy Package QFN33-16LD-PL-1

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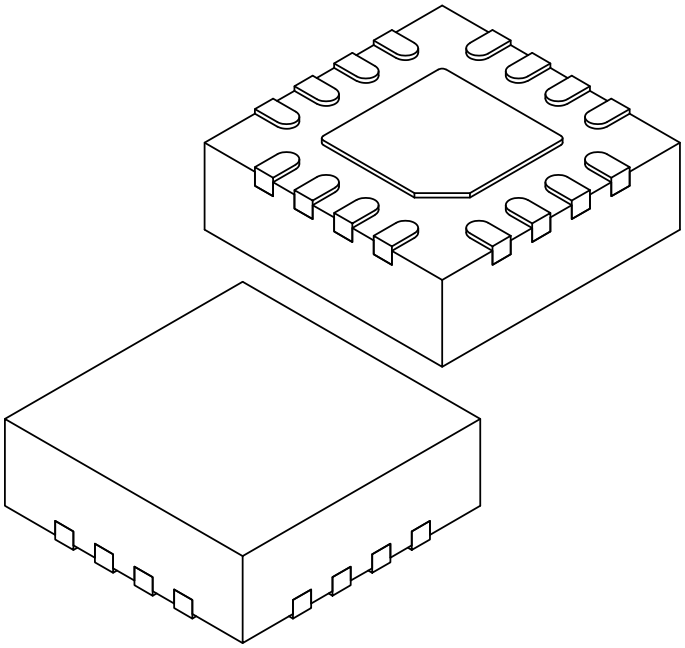


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.50	1.55	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.33 REF	

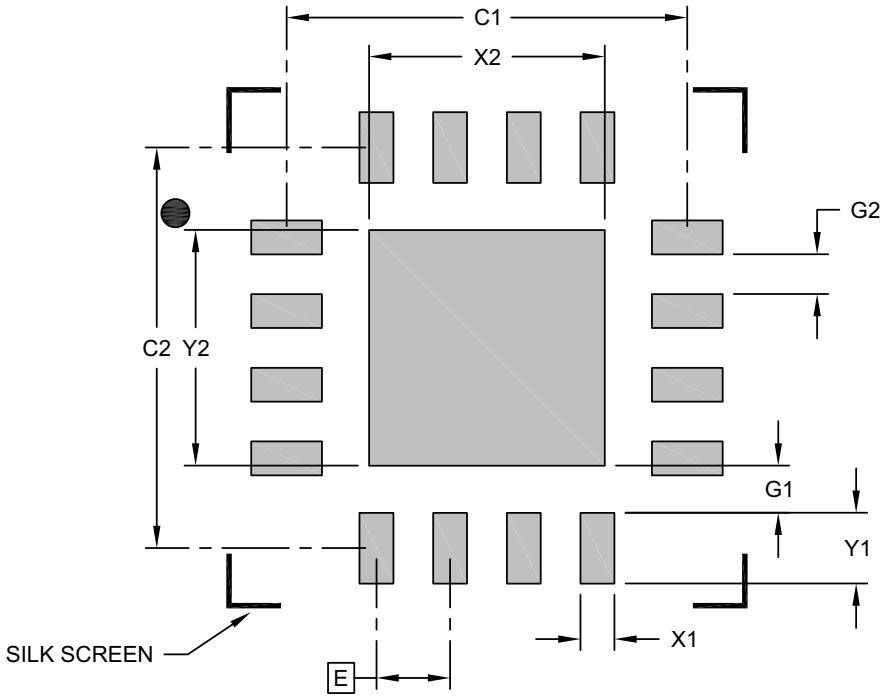
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev C Sheet 2 of 2

16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad; Micrel Legacy Package QFN33-16LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.72	
Contact Pad Spacing	C2		2.72	
Contact Pad Width (Xnn)	X1			0.23
Contact Pad Length (Xnn)	Y1			0.48
Contact Pad to Center Pad (Xnn)	G1	0.32		
Contact Pad to Contact Pad (Xnn)	G2	0.27		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3103-NCA Rev C

APPENDIX A: REVISION HISTORY

Revision A (October 2023)

- Converted Micrel document SY58021U to Microchip data sheet template DS20006822A.
- Minor text changes throughout.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Part No.	X	X	X	[-XX]
Device	Supply Voltage	Package	Temperature Range	Media Type

Device:	SY58021:	4 GHz, 1:4 LVPECL Fanout Buffer/Translator with Internal Termination	
Supply Voltage:	U	=	2.5V/3.3V
Package:	M	=	16-Lead 3 mm x 3 mm VQFN
Temperature Range:	G	=	–40°C to +85°C
Media Type:	<blank> TR	= =	100/Tube 1,000/Reel

Examples:

a) SY58021UMG:

SY58021, 2.5V/3.3V Supply Voltage, 16-Lead VQFN, –40°C to +85°C Temperature Range, 100/Tube

b) SY58021UMG-TR:

SY58021, 2.5V/3.3V Supply Voltage, 16-Lead VQFN, –40°C to +85°C Temperature Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

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