KSZ8851SNL

Hardware Design Checklist

1.0 INTRODUCTION

This document provides a hardware design checklist for Microchip KSZ8851SNL 10/100BASE-T/TX Ethernet controller that has one copper port and one uplink port that support SPI interface. These checklist items should be followed when utilizing the KSZ8851SNL in a new design. A summary of these items is provided in Section 11.0, "Hardware Checklist Summary," on page 11. Detailed information on these subjects can be found in the corresponding section:

- Section 2.0, "General Considerations"
- Section 3.0, "Power"
- Section 4.0, "Ethernet Signals"
- Section 5.0, "Clock Circuit"
- Section 6.0, "System Application"
- Section 7.0, "Digital Interfaces"
- Section 8.0, "Startup"
- Section 9.0, "Configuration Pins (Strapping Options)"
- Section 10.0, "Miscellaneous"

2.0 GENERAL CONSIDERATIONS

2.1 Required Reference

The KSZ8851SNL implementor should have the following documents on hand:

- *KSZ8851SNL Data Sheet* (www.microchip.com/DS00002381)
- *KSZ8851 Silicon Errata and Data Sheet Clarification* (www.microchip.com/DS80000716)
- *KSZ8851SNL_HP (Rev1.1).zip* (www.microchip.com/KSZ8851)

2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

2.3 Ground

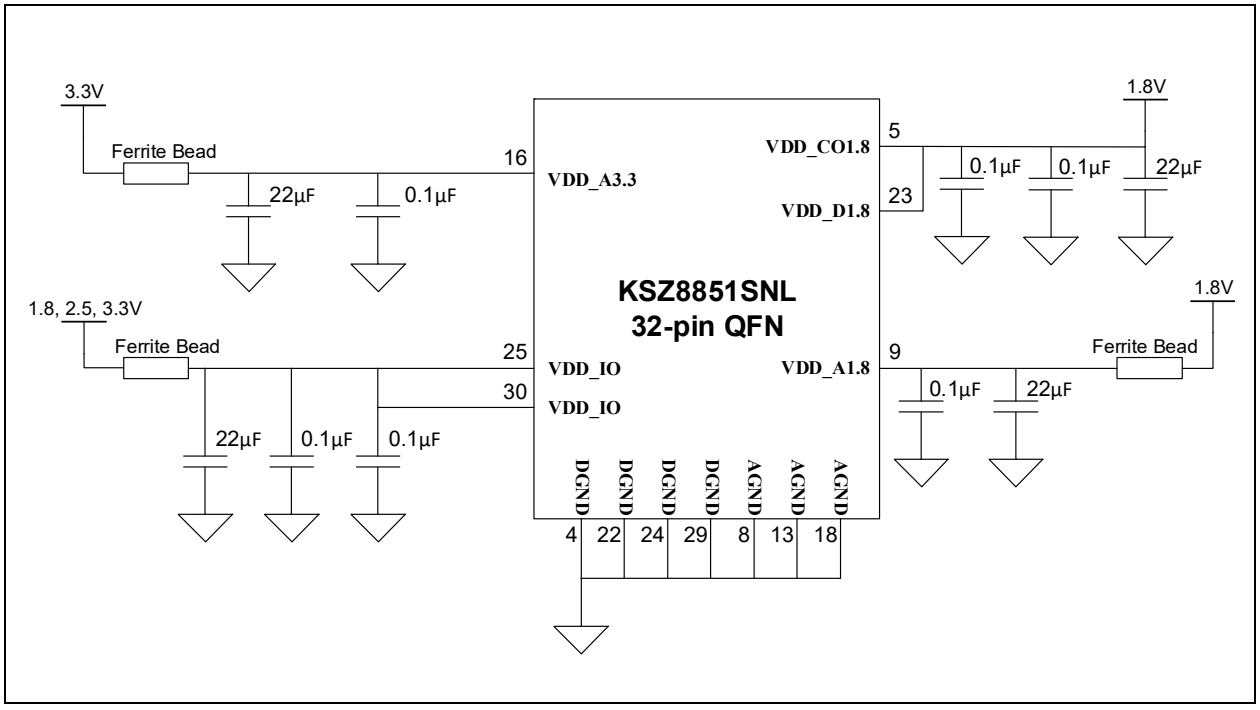
- The ground pins (**GND**) should be connected to the digital ground, and the analog ground should be connected to the solid contiguous ground plane as system ground on the board. Separate digital ground and analog ground planes are not recommended.
- If using the magnetics and RJ45 connector, a chassis ground should be used for the line side of the magnetics and the metal case of the RJ45 connector. The system ground and the chassis ground should be tied together by a ferrite bead. The ferrite bead should be placed far away from the Ethernet device for better ESD and EMI.

3.0 POWER

- The analog supply (**VDD_A3.3**) pin on the KSZ8851SNL is pin 16, which requires a connection to VDD_A3.3 (created from +3.3V through a ferrite bead).
- KSZ8851SNL VDDIO supports three VDDIO voltages of 1.8V, 2.5V, and 3.3V. Pins 25 and 30 (**VDD_IO**) should be connected to one of three VDDIO voltages through a ferrite bead.
- The analog 1.8V core power pin is pin 9, and the digital 1.8V core power pin is pin 23. A ferrite bead is required between analog 1.8V and digital 1.8V power rail.
- There are two ways to provide 1.8V power: (1) from the internal 1.8V LDO output pin 5 when VDDIO is 3.3V or 2.5V and (2) from the external 1.8V LDO when VDDIO is 1.8V power. When using the external 1.8V LDO, the **VDD_CO1.8** pin 5 should be left floating.
- Be sure to place bulk capacitors on each side of the ferrite beads, and use 0.1 µF capacitors to decouple the device for all power pins. The capacitor size should be SMD_0603 or smaller.

The power and ground connections are shown in Figure 3-1.

FIGURE 3-1: POWER AND GROUND CONNECTIONS



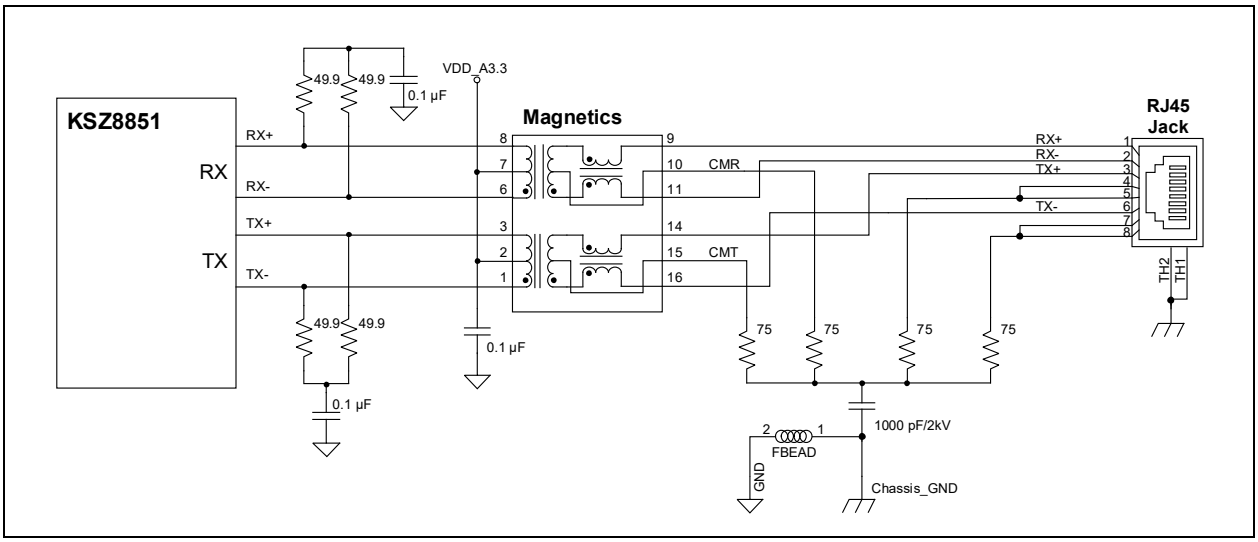
4.0 ETHERNET SIGNALS

The KSZ8851SNL has one integrated PHY that is fully compliant with IEEE 802.3u standard to support 10/100BASE-T/TX Ethernet copper ports.

4.1 KSZ8851SNL Copper Ports Connection

- KSZ8851SNL has one Ethernet copper port. The port is a current driver with external termination resistors and DC biasing power on the magnetics. Each port connection between KSZ8851SNL and magnetics is illustrated in Figure 4-1.
- Both center taps, receive (RX) and transmit (TX), of the magnetics on the chip side should be tied to 3.3V analog power.
- In the Ethernet controller, the RX +/- differential pair should be connected to RJ45 connector pins 1 and 2 through magnetics, and the TX +/- differential pair should be connected to RJ45 connector pins 3 and 6 through magnetics.
- Two 49.9Ω termination resistors and one 0.1 µF capacitor to ground for each differential pair of RX and TX.

FIGURE 4-1: ETHERNET PORT CONNECTION WITH MAGNETICS



4.2 Chip-Side Magnetics Connection

- The center tap connection on the KSZ8851SNL side for the TX channel should not be connected to **VDD_A3.3**. The TX channel center tap and the RX channel center tap of the magnetics should be connected together and connected to the system ground through common-mode capacitor only. The common-mode capacitor value can be from 0.1-10 µF.
- When using the KSZ8851SNL device in the Auto-MDI/MDIX mode of operation, use a magnetics module with identical TX and RX paths.

4.3 RJ45 Connector Line-Side Magnetics Connection

- In the Controller design:
  - Pin 1 of the RJ45 should connect to RX+ of the KSZ8851SNL, and pin 2 of the RJ45 should connect to RX- of the KSZ8851SNL.
  - Pin 3 of the RJ45 should connect to TX+ of the KSZ8851SNL, and pin 6 of the RJ45 should connect to TX- of the KSZ8851SNL.
- Each center tap connection on the cable side (RJ45) for the TX channel and for the RX channel should each be terminated with a 75Ω resistor through the same 1000 pF, 2 kV capacitor to chassis ground.
- RJ45 pins 4 and 5 should be shorted and then terminated with a 75Ω resistor through the 1000 pF capacitor
- to the chassis ground.
- RJ45 pins 7 and 8 should be shorted and then terminated with a 75Ω resistor through the 1000 pF capacitor
- to the chassis ground.
- Only one 1000 pF, 2 kV capacitor to chassis ground is required. It is shared by both TX and RX center taps and four 75Ω resistors.
- The RJ45 connector shield should be tied directly to the chassis ground.

4.4 Alternative Termination Selection for RJ45 Connector

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods of accomplishing this:
  - Pins 4 and 5 can be connected with two 49.9Ω resistors. The common connection of these resistors should be linked through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. An equivalent circuit is created by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 kV capacitor. There are two methods for accomplishing this:
  - Pins 7 and 8 can be connected with two 49.9Ω resistors. The common connection of these resistors should be linked through a third 49.9Ω resistor to the 1000 pF, 2 kV capacitor.
  - For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. An equivalent circuit is created by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 kV capacitor to chassis ground.
- The RJ45 connector shield should be attached directly to the chassis ground.

4.5 Utilization of RJ45 with Integrated LED

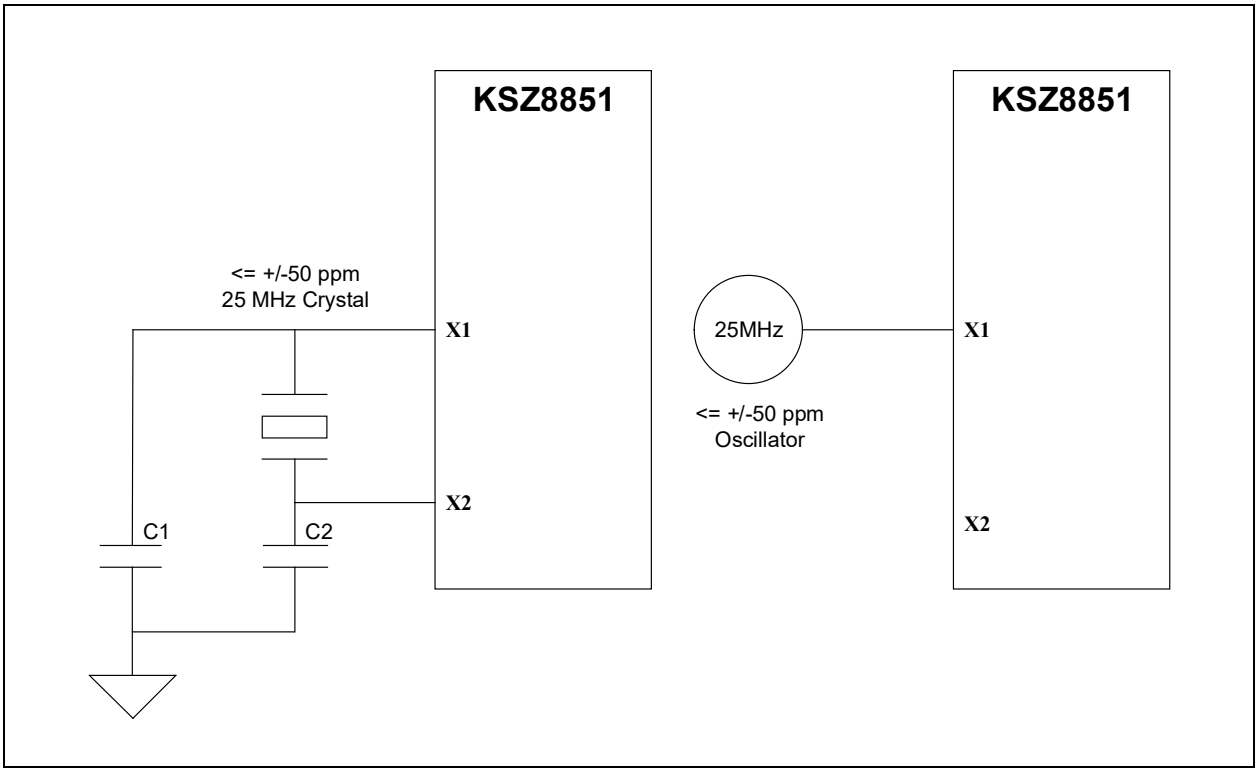
- The user can utilize the RJ45 connector with integrated LED components if the product working environment is not very noisy.
- If the designed product works in an electrically noisy outside environment, it is not recommended to use RJ45 with integrated LED. This is because the outside interference signal or voltage can be coupled to the LED circuit through the line side of RJ45, and the LED circuit is directly connected to chip and system power or ground. It is better to use independent LED components.
- If the user needs to utilize the RJ45 with an integrated LED circuit in an electrically noisy environment, consider adding TVS diodes to protect the chip.

5.0 CLOCK CIRCUIT

5.1 Crystal and External Oscillator/Clock Connections

- **X1** (pin 20) is the clock circuit input for the KSZ8851SNL device. This pin requires a capacitor to ground when a crystal is used. One side of the crystal connects to this pin.
- **X2** (pin 21) is the clock circuit output for the KSZ8851SNL device. This pin requires a capacitor to ground when a crystal is used. One side of the crystal connects to this pin.
- Since every system design is unique, the capacitor values are system-dependent, based on the C_L specification of the crystal and the stray capacitance value. Refer to the crystal data sheet for the C_L required. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.
- Alternately, a 25.000 MHz clock oscillator may be used to provide the clock source for the KSZ8851SNL. When using a single-ended clock source, **X1** connects to a 3.3V tolerant oscillator. **X2** should be left floating as No Connect (NC). See Figure 5-1.

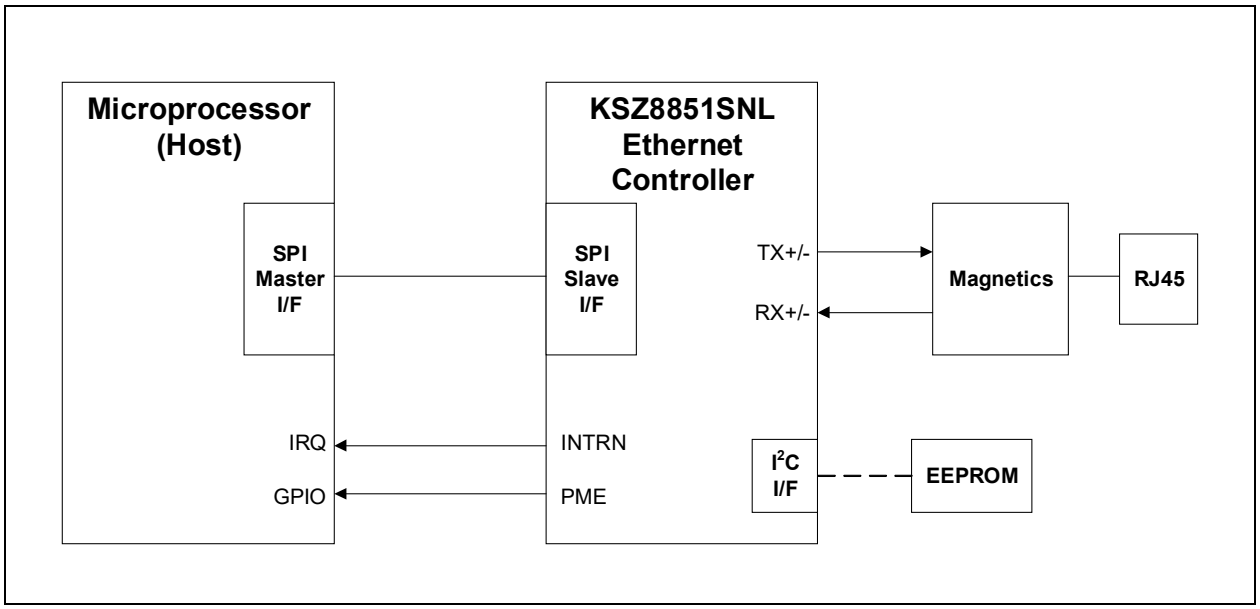
FIGURE 5-1: CRYSTAL AND OSCILLATOR CONNECTIONS FOR KSZ8851SNL



6.0 SYSTEM APPLICATION

In the system design, EEPROM is an option. If the host software or firmware can provide the host MAC address, EEPROM does not have to be used in the system design. Otherwise, EEPROM should be designed in this system.

FIGURE 6-1: TYPICAL APPLICATION DIAGRAM



7.0 DIGITAL INTERFACES

7.1 SPI Interface Signals and Connection

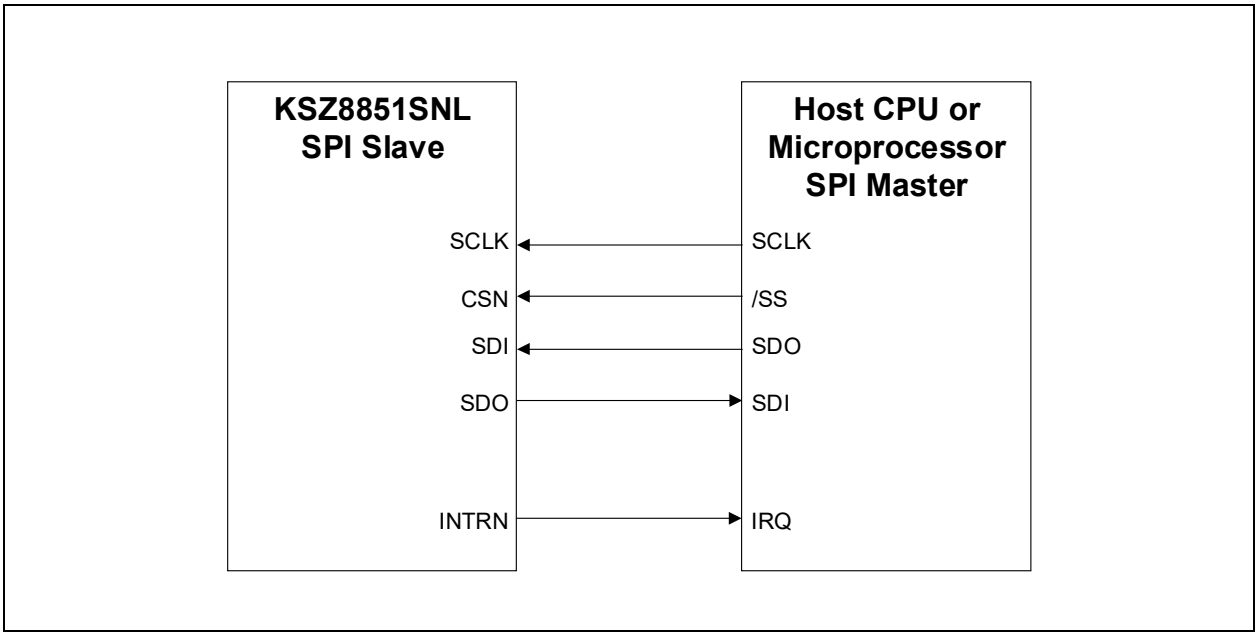
- See Table 7-1 for KSZ8851SNL SPI pin descriptions.

TABLE 7-1: SPI PIN DESCRIPTIONS

Pin Number	SPI Signals	Descriptions
4	SCLK	Serial clock input from the host CPU for SPI interface. This clock speed can run up to 40 MHz maximum.
6	SI	Serial data in from host CPU for SPI interface
8	CSN	Chip Select Enable (Active low) from host CPU for SPI interface
10	SO	Serial data out to host CPU for SPI interface

- The KSZ8851SNL SPI as a slave SPI interface can be connected to a host master SPI for Ethernet packets transmission. In SPI Slave mode, an external SPI master device (microcontroller or CPU) supplies the operating serial clock (SCLK), chip select (CSN), and serial input data (SI) that is clocked in on the rising edge of SCLK to the KSZ8851SNL device. Serial output data (SO) is driven out by the KSZ8851SNL on the falling edge of SCLK to the external SPI master device. The falling edge of CSN is starting the SPI operation, and the rising edge of CSN is ending the SPI operation. The SCLK stays in Low state when SPI operation is idle. The connection is shown in the Figure 7-1.

FIGURE 7-1: HOST CPU SPI MASTER AND KSZ8851SNL SPI SLAVE CONNECTIONS



7.2 KSZ8851SNL SPI Interface Request

- For the signal integrity, the SCLK signal needs a series termination resistor at drive pin.
- The KSZ8851SNL SPI Serial data output (SO) pin is tri-stated when CSN is negated and this pin must have an external 1 kΩ to 4.7 kΩ pull-up resistor. It is recommended to use a 1 kΩ pull-up resistor if the SCLK frequency is higher than 10 MHz, and a 4.7 kΩ pull-up resistor if the SCLK frequency is equal or lower than 10 MHz. The SPI SCLK clock speed can run up to 40 MHz at maximum.
- Provisions should be made for series resistors for all outputs on the SPI interface. Series resistors will enable the designer to closely match the output driver impedance of the KSZ8851SNL and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application-dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors are 22Ω. See Table 7-2.

TABLE 7-2: SERIES TERMINATIONS FOR SPI INTERFACE

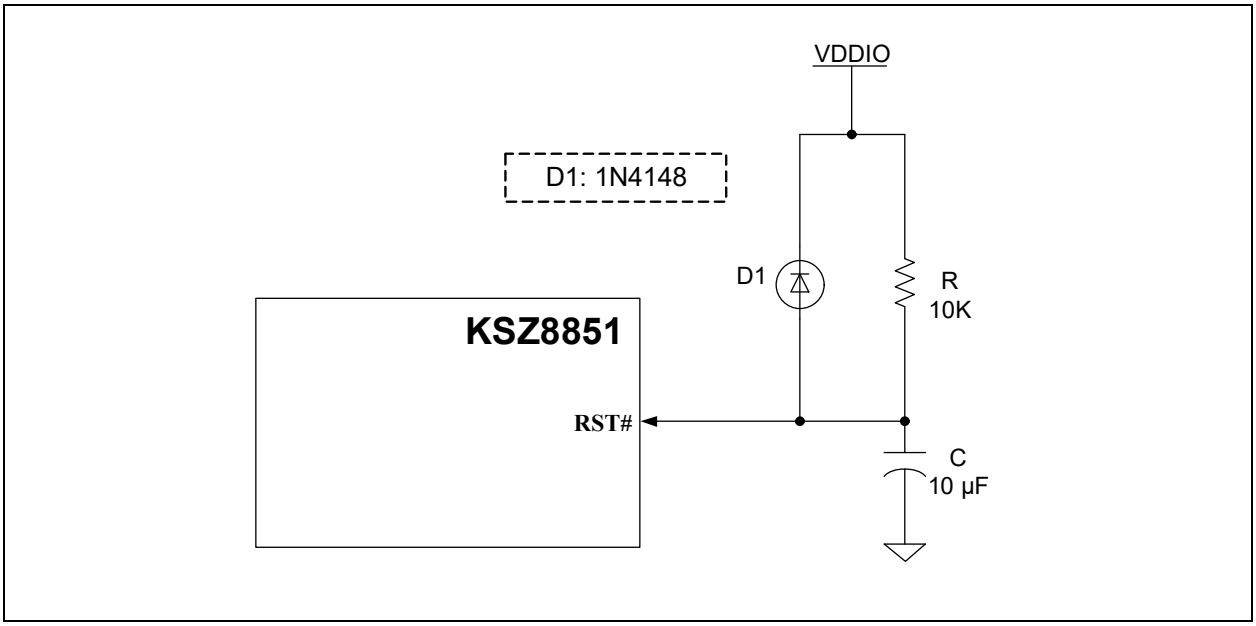
Signals for SPI Interface Slave Signals/Master Signals	Series Resistors at KSZ8851SNL SPI Slave Side	Series Resistors at the Host CPU/ Microprocessor SPI Master Side
SCLK	—	22Ω
SO/SDI	22Ω	—
SI/SDO	—	22Ω
CSN/SS#	—	—

8.0 STARTUP

8.1 Reset Circuit

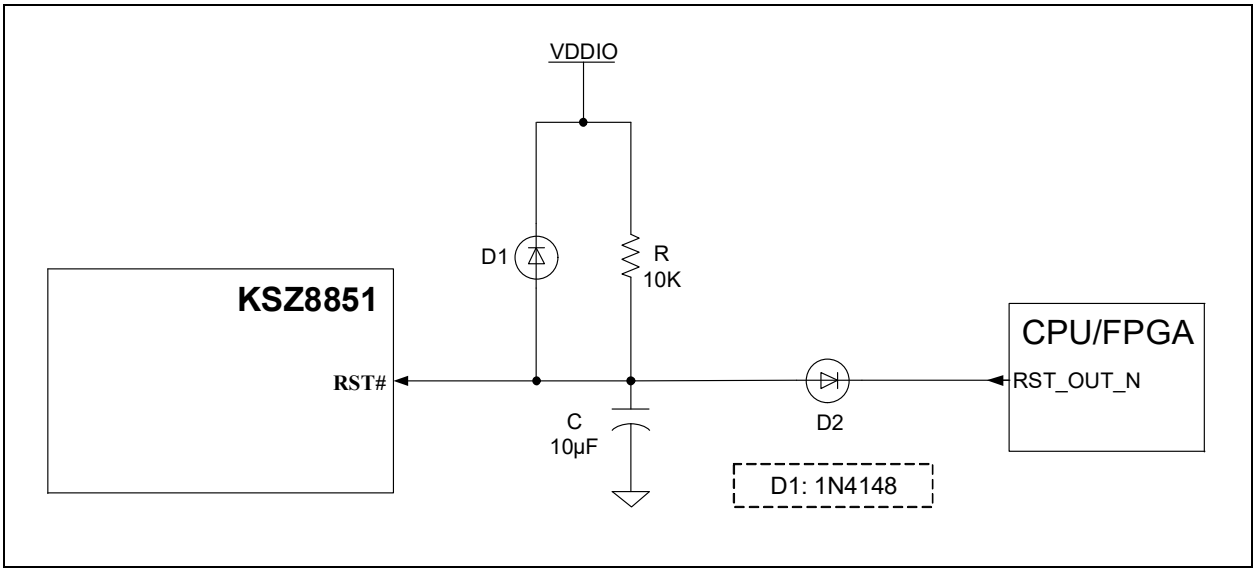
- **RST_N** (pin 19) is an active-low reset input. This signal resets all logic and registers within the KSZ8851SNL. A hardware reset (RST_N assertion) is required following power-up. Please refer to the latest copy of the *KSZ8851SNL Data Sheet* for reset timing requirements. Figure 8-1 shows a recommended reset circuit for powering up the KSZ8851SNL device when reset is triggered by the power supply.

FIGURE 8-1: R/C RESET CIRCUIT FOR KSZ8851SNL POWER-UP RESET



- The reset circuit interface with CPU/FPGA reset output pin shows the recommended reset circuit for applications where reset is driven by an external CPU or FPGA. The reset-out pin, RST_OUT_N, from CPU/FPGA provides the warm reset after a power-up reset is done. If the Ethernet device and CPU/FPGA use the same VDDIO voltage, D2 can be removed and both reset pins can be connected directly. See Figure 8-2.

FIGURE 8-2: RESET CIRCUIT INTERFACE WITH CPU/FPGA RESET OUTPUT



9.0 CONFIGURATION PINS (STRAPPING OPTIONS)

There are some strap-in pins to help with the KSZ8851SNL configuration after power-up or hardware reset. The *KSZ8851SNL Data Sheet* has complete details on the operation of strapping pins.

9.1 General Strap-In Pins and Others

The recommended pull-up and pull-down resistors values for strap pins are 4.7 kΩ and 1 kΩ, respectively. Users are highly discouraged from directly executing a pull-up to power and pull-down to ground without pull-up and pull-down resistors.

10.0 MISCELLANEOUS

10.1 ISET Resistor

ISET (pin 17) on the KSZ8851SNL should connect to the system ground through a 3.01 kΩ resistor with a tolerance of 1.0%. This **ISET** pin is used to set up critical bias currents for the embedded 10/100 Ethernet physical devices.

10.2 Other Considerations

- Incorporate an SMD ferrite bead footprint to connect the chassis ground to the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a ferrite bead or a capacitor. Users are required to place the capacitor/ferrite bead far from the KSZ8851SNL device in PCB layout placement for better ESD.
- Make sure that enough bulk capacitors (4.7-22 µF) are incorporated in each power rail.

11.0 HARDWARE CHECKLIST SUMMARY

TABLE 11-1: HARDWARE DESIGN CHECKLIST

Section	Check	Explanation	√	Notes
Section 2.0, "General Considerations"	Section 2.1, "Required Reference"	All necessary documents are on hand.		
	Section 2.2, "Pin Check"	The pins match the data sheet.		
	Section 2.3, "Ground"	Verify if the digital ground and the analog ground are tied together. Check if there is a chassis ground for the line-side ground.		
Section 3.0, "Power"	Section 3.0, "Power"	Check the power connection in Figure 3-1 for the ferrite beads and the decouple capacitors. The bulk capacitors in 10 µF to 47 µF values are for each power rail, while 0.1 µF capacitors are attached to each power pin and power rail. If using 2.5V or 3.3V as VDDIO, can use internal 1.8V LDO and output 1.8V from pin 5. If using 1.8V as VDDIO, must be use an external 1.8V LDO to provide 1.8V voltage.		
Section 4.0, "Ethernet Signals"	Section 4.1, "KSZ8851SNL Copper Ports Connection"	Verify if there are 49.9Ω termination resistors on TX and RX pairs and refer to Figure 4-1 for the copper port connection.		
	Section 4.2, "Chip-Side Magnetics Connection"	Verify if the center taps of the magnetics on the KSZ8851SNL chip side are connected to the VDD_A3.3 3.3V analog power. The center taps of the magnetics on the chip side should also have the common mode capacitor to ground.		
	Section 4.3, "RJ45 Connector Line-Side Magnetics Connection"	Verify if the line side of the magnetics has two 75Ω resistors through a 1000 pF, 2 kV capacitor connected to chassis ground that is also linked to the metal case of the RJ45 for the line side.		
	Section 4.4, "Alternative Termination Selection for RJ45 Connector"	If using the solution in Section 4.3, "RJ45 Connector Line-Side Magnetics Connection", it is not required to check Section 4.4, "Alternative Termination Selection for RJ45 Connector" that uses smith termination with 50Ω + 25Ω resistors.		
	Section 4.5, "Utilization of RJ45 with Integrated LED"	Use RJ45 with integrated LED if the product working environment is not very noisy. Otherwise, use an independent LED solution.		
Section 5.0, "Clock Circuit"	Section 5.1, "Crystal and External Oscillator/Clock Connections"	Verify the usage of 25 MHz max. ±50 ppm crystal. The drive level should be about 100 µW or above (preferably higher). If using 25 MHz oscillator with maximum ±50 ppm, it is better to use 3.3V power for the oscillator power.		
Section 6.0, "System Application"	Section 6.0, "System Application"	Refer to Figure 6-1 for design requirement to decide whether EEPROM is needed.		
Section 7.0, "Digital Interfaces"	Section 7.1, "SPI Interface Signals and Connection"	Refer to Table 7-1 and Figure 7-1 to check the signal connections from output pins to input pins correctly.		
	Section 7.2, "KSZ8851SNL SPI Interface Request"	Check if the pull-up resistors are correct. Check if the series terminations resistors are correct based on Table 7-2.		

TABLE 11-1: HARDWARE DESIGN CHECKLIST (CONTINUED)

Section	Check	Explanation	√	Notes
Section 8.0, "Startup"	Section 8.1, "Reset Circuit"	Verify if R/C reset circuit is used for a power-up reset. A 10 kΩ resistor and a 10 µF capacitor are recommended. For the cost-down, the D1 in Figure 8-1 and Figure 8-2 can be ignored because the RST_N pin has an internal protection diode. For a warm reset from CPU/FPGA to KSZ8851SNL, D2 can be removed from Figure 8-1 and Figure 8-2 if KSZ8851SNL and CPU/FPGA are using the same VDDIO voltage.		
Section 9.0, "Configuration Pins (Strapping Options)"	Section 9.1, "General Strap-In Pins and Others"	It is generally recommended to use 4.7 kΩ pull-up and 1kΩ pull-down resistor. Avoid pulling up/down to power or ground directly. If not specified, NC pin should have no connection.		
Section 10.0, "Miscellaneous"	Section 10.1, "ISET Resistor"	Check that pin 17 ISET resistor (3.01 kΩ, 1%) has no any capacitor in parallel.		
	Section 10.2, "Other Considerations"	Incorporate an SMD footprint (SMD_0805-1210) to connect the chassis ground to the system ground. The SMD footprint should be placed far from the KSZ8851SNL device in PCB layout placement. Incorporate sufficient power plane bulk capacitors (4.7-22 µF) for each power rail.		

APPENDIX A: REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00003436A (03-27-20)	Initial release.	

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