

# SY58022U

### 5.5 GHz, 1:4 Fanout Buffer/Translator with 400 mV LVPECL Outputs and Internal Input Termination

### Features

- Precision 1:4, 400 mV LVPECL Fanout Buffer
- Ensured AC Performance over Temperature and Voltage:
  - >5.5 GHz f<sub>MAX</sub> Clock
  - <80 ps t<sub>r</sub>/t<sub>f</sub> Times
  - <250 ps (V<sub>IN</sub> ≥300 mV) t<sub>PD</sub>
  - <15 ps Maximum Skew
- Low Jitter Performance: 60 fs<sub>RMS</sub> Phase Jitter
- Accepts an Input Signal as Low as 100 mV
- Unique Input Termination and VT Pin Accepts DCand AC-Coupled Differential Inputs: LVPECL, LVDS, and CML
- 400 mV LVPECL Compatible Outputs
- Power Supply: 2.5V ±5% and 3.3V ±10%
- –40°C to +85°C Temperature Range
- Available in a 16-Lead 3 mm x 3 mm VQFN Package

### Applications

- All SONET and All GigE Clock Distribution
- Fibre Channel Clock and Data Distribution
- Backplane Distribution
- Data Distribution: OC-48, OC-48+FEC, XAUI
- High-End, Low-Skew, Multiprocessor Synchronous Clock Distribution

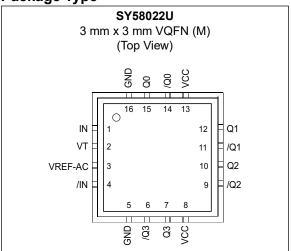
### **General Description**

The SY58022U is a 2.5V/3.3V precision, high-speed, fully differential 1:4 LVPECL fanout buffer. Optimized to provide four identical output copies with less than 15 ps of skew and less than 10  $p_{SPP}$  total jitter, the SY58022U can process clock signals as fast as 5.5 GHz.

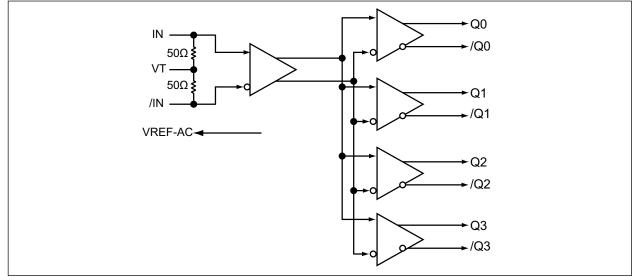
The differential input includes Microchip's unique, 3-pin input termination architecture interfaces to differential LVPECL, CML, and LVDS signals (AC- or DC-coupled) as small as 100 mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage ( $V_{REF-AC}$ ) is provided to bias the VT pin. The outputs are 400 mV LVPECL compatible with extremely fast rise/fall times ensured to be less than 80 ps.

The SY58022U operates from a 2.5V  $\pm$ 5% supply or 3.3V  $\pm$ 10% supply and is ensured over the full industrial temperature range (-40°C to +85°C). For applications that require greater output swing or CML compatible outputs, consider the SY58021U 1:4 fanout buffer with LVPECL outputs, or the SY58020U 1:4 fanout buffer with 400 mV CML outputs.

### Package Type



### **Functional Block Diagram**



### 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Power Supply Voltage (V <sub>CC</sub> )	
Input Voltage (V <sub>IN</sub> )	–0.5V to V <sub>CC</sub>
Continuous Output Current (I <sub>OUT</sub> )	
Surge Output Current (I <sub>OUT</sub> )	100 mA
Source or Sink Current on VT Pin	±100 mA
Source or Sink Current on (IN, /IN) Pins	±50 mA
Source or Sink Current on VREF-AC Pin (Note 1)	±1.5 mA

### **Operating Ratings ††**

**† Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

**††** Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 1: Due to the limited drive capability, use for input of the same package only.

### DC ELECTRICAL CHARACTERISTICS

T <sub>A</sub> = -40°C to +85°C. Note 1							
Parameters	Symbol	Min.	Тур.	Max.	Units	Conditions	
	N	2.375	2.5	2.625	V	V <sub>CC</sub> = 2.5V	
Power Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V	V <sub>CC</sub> = 3.3V	
Power Supply Current	I <sub>CC</sub>	—	125	160	mA	No load, V <sub>CC</sub> = Max.	
Input High Voltage	V <sub>IH</sub>	1.2	_	V <sub>CC</sub>	V	—	
Input Low Voltage	V <sub>IL</sub>	0	_	V <sub>IH</sub> – 0.1	V	IN, /IN	
Input Voltage Swing	V <sub>IN</sub>	0.1	_	3.6	V	IN, /IN; See Figure 4-1	
Differential Input Voltage	V <sub>DIFF_IN</sub>	0.2	_	3.4	V	IN, /IN; See Figure 4-2	
IN-to-VT Resistance	R <sub>IN</sub>	40	50	60	Ω	—	
Output Reference Voltage	V <sub>REF-AC</sub>	V <sub>CC</sub> – 1.3	V <sub>CC</sub> – 1.2	V <sub>CC</sub> – 1.1	V	—	
IN-to-VT Voltage	V <sub>T_IN</sub>	_	_	1.28	V	_	

**Note 1:** The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

### LVPECL DC ELECTRICAL CHARACTERISTICS

$V_{CC}$ = 3.3V ±10% or $V_{CC}$ = 2.5 ±5%; $R_L$ = 50 $\Omega$ to $V_{CC}$ – 2V; $T_A$ = –40°C to +85°C, unless otherwise stated. Note 1								
Parameter	Symbol	Min.	Тур.	Max.	Units	Condition		
Output High Voltage	V <sub>OH</sub>	V <sub>CC</sub> – 1.145	V <sub>CC</sub> – 1.020	V <sub>CC</sub> – 0.895	V	—		
Output Low Voltage	V <sub>OL</sub>	V <sub>CC</sub> – 1.545	V <sub>CC</sub> – 1.420	V <sub>CC</sub> – 1.295	V	—		
Output Voltage Swing	V <sub>OUT</sub>	150	400	650	mV	See Figure 4-1		
Differential Output Swing	V <sub>DIFF_OUT</sub>	300	800	1300	mV	See Figure 4-2		

Note 1: The circuit is designed to meet the DC specifications shown in the table above after thermal equilibrium has been established.

### **AC ELECTRICAL CHARACTERISTICS**

 $V_{CC}$  = 2.5V ±5% or 3.3V ±10%;  $R_L$  = 50 $\Omega$  to  $V_{CC}$  – 2V;  $T_A$  = –40°C to +85°C, unless otherwise stated.

Parameter	Symbol	Min.	Тур.	Max.	Units	Condition
Maximum Operating Frequency	f	5.5	—	—	GHz	Clock, V <sub>OUT</sub> ≥ 200 mV
Maximum Operating Frequency	f <sub>MAX</sub>	—	10	—	Gbps	NRZ Data
Propagation Delay	t <sub>PD</sub>	130	200	280	ps	—
Channel-to-Channel Skew	t <sub>CHAN</sub>	_	4	15	ps	Note 1
Part-to-Part Skew	t <sub>SKEW</sub>	—	—	50	ps	Note 2
RMS Phase Jitter	t <sub>JITTER</sub>	_	60	_	fs	Output = 622 MHz, Integration range: 12 kHz to 20 MHz
Output Rise/Fall Time	t <sub>r</sub> /t <sub>f</sub>	20	50	80	ps	20% to 80%, At full swing

Note 1: Skew is measured between outputs of the same bank under identical transitions.

2: Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

### **TEMPERATURE SPECIFICATIONS**

Parameters	Symbol	Min.	Тур.	Max.	Units	Conditions	
Temperature Ranges							
Operating Temperature Range	T <sub>A</sub>	-40		+85	°C	—	
Lead Temperature	—	—	_	+260	°C	Soldering, 20 sec.	
Storage Temperature Range	T <sub>S</sub>	-65	_	+150	°C	—	
Package Thermal Resistances							
	0		60	_	°C/W	Still-air	
Thermal Resistance, 3x3 VQFN 16-Ld	$\theta_{JA}$	_	54			500 lpfm	
	$\theta_{JB}$		33	_	°C/W	Junction-to-board, Note 1	

Note 1: Thermal performance assumed exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

### 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

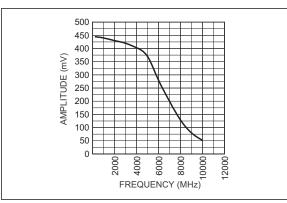


FIGURE 2-1:

Amplitude vs. Frequency.

 $V_{CC}$  = 3.3V,  $V_{EE}$  = 0V,  $V_{IN}$  = 100 mV,  $T_A$  = +25°C, unless otherwise stated.

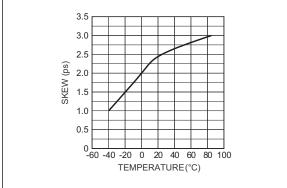


FIGURE 2-2:



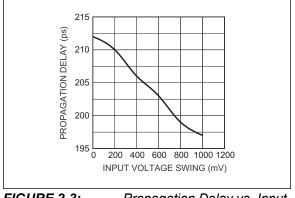


FIGURE 2-3: Voltage Swing.

Propagation Delay vs. Input

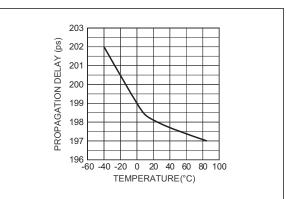


FIGURE 2-4: Temperature.

Propagation Delay vs.

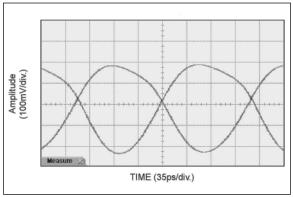


FIGURE 2-5: 4 GHz

4 GHz Output.

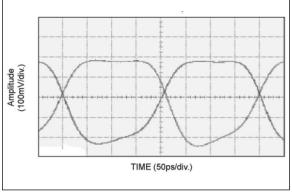


FIGURE 2-6:

2.5 GHz Output.

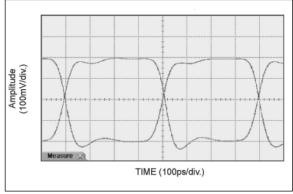


FIGURE 2-7: 1.25 GHz Output.

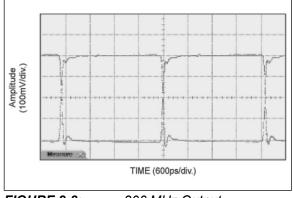


FIGURE 2-8: 200 MHz Output.

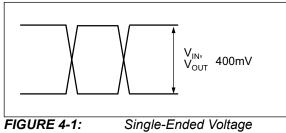
### 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

Pin Number	Pin Name	Description
1, 4	IN, /IN	Differential Input: This input pair receives the signal to be buffered. Each pin is internally terminated with $50\Omega$ to the VT pin. Note that this input will default to an indeterminate state if left open. See the Input Interface Applications section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See the Input Interface Applications section.
3	VREF-AC	Reference Output Voltage: This output biases to V <sub>CC</sub> – 1.2V. It is used when AC-coupling to differential inputs. Connect VREF-AC directly to the VT pin. Bypass with 0.01 $\mu$ F low ESR capacitor to VCC. See the Input Interface Applications section.
8, 13	VCC	Positive Power Supply: Bypass with 0.1 $\mu$ F//0.01 $\mu$ F low-ESR capacitors as close to the pins as possible. A 0.01 $\mu$ F capacitor should be as close to the VCC pin as possible.
5, 16	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
14, 15 11, 12 9, 10 6, 7	/Q0, Q0 /Q1, Q1 /Q2, Q2 /Q3, Q3	LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 400 mV. Proper termination is $50\Omega$ to V <sub>CC</sub> – 2V at the receiving end. Unused output pairs may be left floating with no impact on jitter or skew. See the Output Termination Recommendations section.

TABLE 3-1: PIN FUNCTION TABLE

### 4.0 SINGLE-ENDED AND DIFFERENTIAL SWINGS



Swing.

Single-Ended Voltage

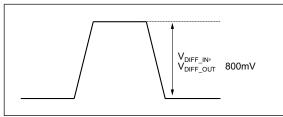


FIGURE 4-2:

Differential Voltage Swing.

### 5.0 TIMING DIAGRAM

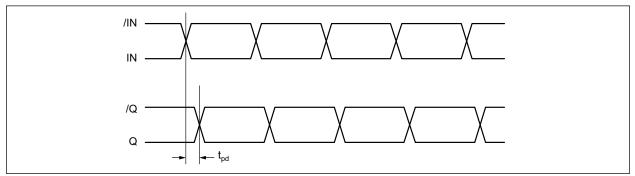
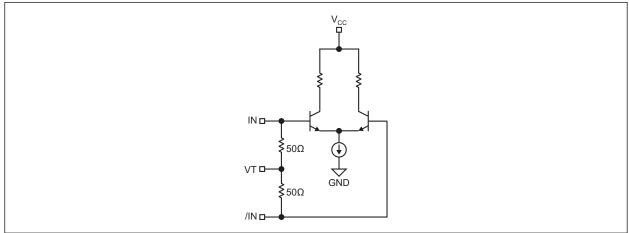


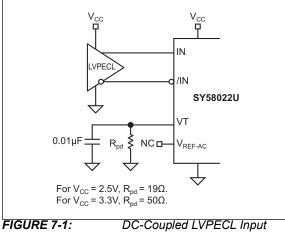
FIGURE 5-1: Timing Diagram.

### 6.0 INPUT STAGE





#### 7.0 INPUT INTERFACE APPLICATIONS



Interface.

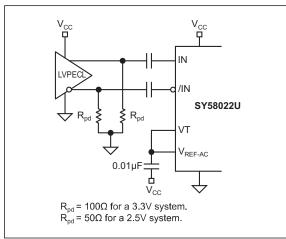


FIGURE 7-2: AC-Coupled LVPECL Input Interface.

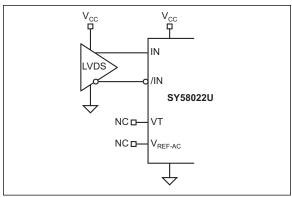


FIGURE 7-3:

LVDS Input Interface.

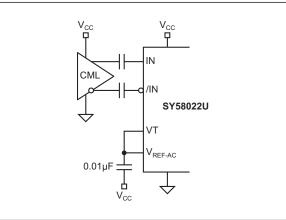


FIGURE 7-4: Interface.

AC-Coupled CML Input



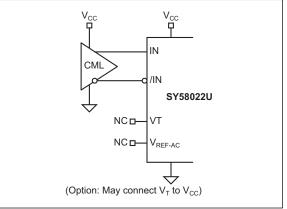


FIGURE 7-5:

CML Input Interface.

### 8.0 OUTPUT TERMINATION RECOMMENDATIONS

LVPECL outputs have very low output impedance (open emitter), and small signal swing which results in low EMI (electro-magnetic interference). The LVPECL is ideal for driving  $50\Omega$ -controlled and  $100\Omega$ -controlled impedance transmission lines. In addition, LVPECL is compatible for driving standard PECL inputs because PECL inputs require only 100 mV input swing. Further, there are several techniques in terminating the LVPECL outputs, as shown in Figure 8-1 through Figure 8-3.

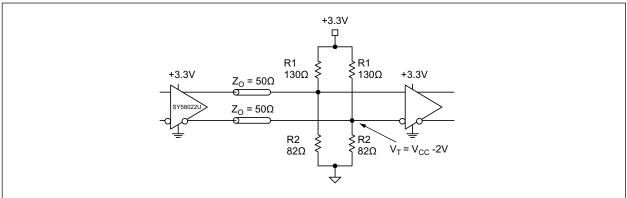
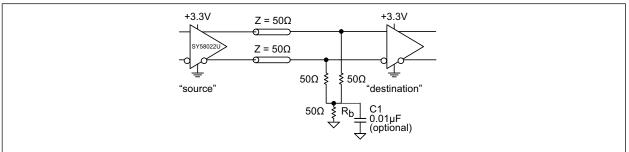
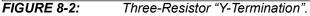


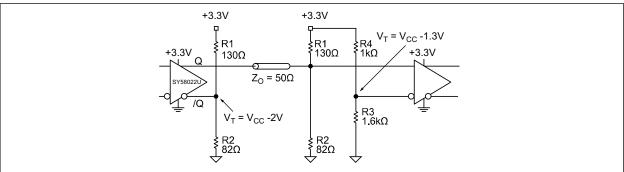
FIGURE 8-1: Parallel Termination – Thevenin Equivalent.

Note: For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω. For +3.3V systems: R1 = 130Ω, R2 = 83Ω.





**Note:** Power-saving alternative to Thevenin termination. Place termination resistors as close to destination inputs as possible.  $R_b$  resistor sets the DC bias voltage, equal to  $V_T$ . For +2.5V systems,  $R_b = 19\Omega$ . For 3.3V systems,  $R_b = 46\Omega$  to  $50\Omega$ . C1 is an optional bypass capacitor intended to compensate for any  $t_r/t_f$  mismatches.

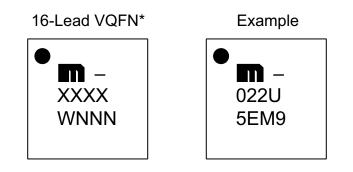




**Note:** Unused output (/Q) must be terminated to balance the output. For +2.5V systems: R1 =  $250\Omega$ , R2 =  $62.5\Omega$ , R3 =  $1.25 k\Omega$ , R4 =  $1.2 k\Omega$ . For +3.3V systems: R1 =  $130\Omega$ , R2 =  $82\Omega$ , R3 =  $1 k\Omega$ , R4 =  $1.6 k\Omega$ . Unused output pairs (Q and /Q) may be left floating.

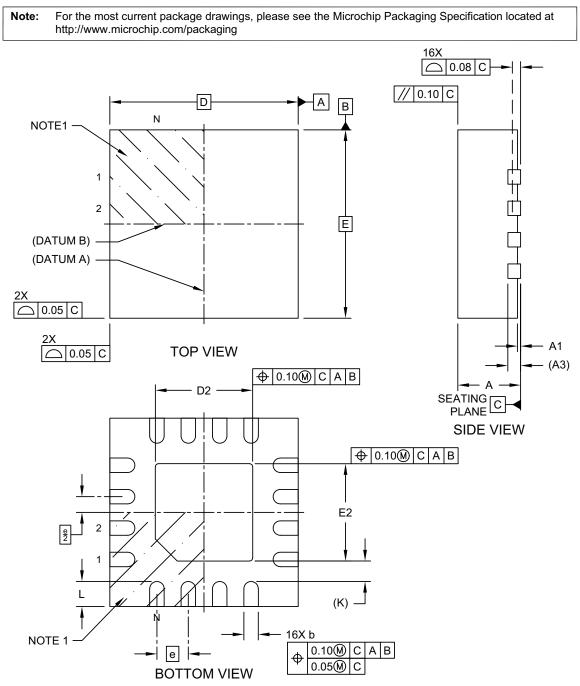
### 9.0 PACKAGING INFORMATION

### 9.1 Package Marking Information



Legend:	Y YY WW NNN @3 *	Product code or customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC <sup>®</sup> designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. Pin one index is identified by a dot, delta up, or delta down (triangle
b c tł	e carriec haracters he corpora	nt the full Microchip part number cannot be marked on one line, it will d over to the next line, thus limiting the number of available for customer-specific information. Package may or may not include ate logo. (_) and/or Overbar ( <sup>-</sup> ) symbol may not be to scale.

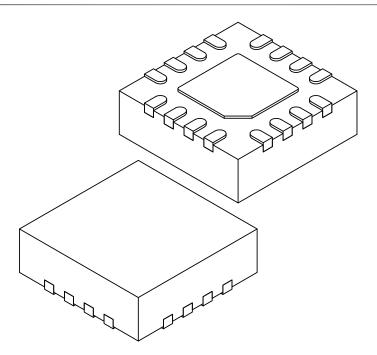
## 16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad; Micrel Legacy Package QFN33-16LD-PL-1



Microchip Technology Drawing C04-1103-NCA Rev C Sheet 1 of 2

#### 16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad; Micrel Legacy Package QFN33-16LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units				
Dimension	Limits	MIN	NOM	MAX	
Number of Terminals	Ν		16		
Pitch	е		0.50 BSC		
Overall Height	А	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Terminal Thickness	A3	0.203 REF			
Overall Length	D	3.00 BSC			
Exposed Pad Length	D2	1.50	1.55	1.60	
Overall Width	E		3.00 BSC		
Exposed Pad Width	E2	1.50	1.55	1.60	
Terminal Width	b	0.18	0.23	0.28	
Terminal Length	L	0.35	0.40	0.45	
Terminal-to-Exposed-Pad	К		0.33 REF		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

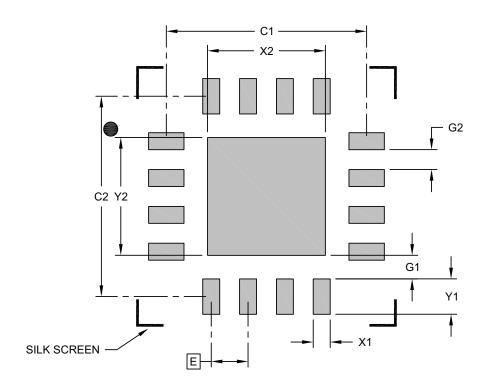
2. Package is saw singulated

 Dimensioning and tolerancing per ASME Y14.5M BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev C Sheet 2 of 2

#### 16-Lead Very Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN] With 1.55 mm Exposed Pad; Micrel Legacy Package QFN33-16LD-PL-1

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### **RECOMMENDED LAND PATTERN**

	MILLIMETERS			
Dimension	Limits	MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.72	
Contact Pad Spacing	C2		2.72	
Contact Pad Width (Xnn)	X1			0.23
Contact Pad Length (Xnn)	Y1			0.48
Contact Pad to Center Pad (Xnn)	G1	0.32		
Contact Pad to Contact Pad (Xnn)	G2	0.27		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3103-NCA Rev C

### APPENDIX A: REVISION HISTORY

### Revision A (August 2023)

- Converted Micrel document SY58022U to Microchip data sheet template DS20006800A.
- Swapped Figure 7-4 and Figure 7-5. These were sorted incorrectly in the legacy document.
- Minor text changes throughout.

NOTES:

### **PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device       Supply Voltage       Package       Temperature Range       Media Type Media Type:       a) SY58022UMG:         Device:       SY58022:       5.5 GHz 1:4 Fanout Buffer/Translator with 400 mV LVPECL Outputs and Internal Input Termination       SY58022:       S.5 GHz 1:4 Fanout Buffer/Translator with 400 mV LVPECL Outputs and Internal Input Termination       SY58022:       S.5 GHz 1:4 Fanout Buffer/Translator with 400 mV LVPECL Outputs and Internal Input Termination       SY58022:       S.7 Size       Sys8022:       SY58022:       S.5 GHz 1:4 Fanout Buffer/Translator with 400 mV LVPECL Outputs and Internal Input Termination       SY58022:       SY58022:       S.5 GHz 1:4 Fanout Buffer/Translator with 400 mV LVPECL Outputs and Internal Input Termination       SY58022:       SY58022:       S.5 GHz 1:4 Fanout Buffer/Translator with 400 mV LVPECL Outputs and Internal Input Termination       SY58022:       S.5 GHz 1:4 Fanout Buffer/Translator with 400 mV LVPECL Outputs and Internal Input Termination       SY58022:       S.5 Sidez 2:       SY58022:       SY5802:       SY58022:       SY5802:       SY58022:       SY5802:       SY5802:	Part No.	X	X	X	- <u>XX</u>	Exampl	es:
SY58022, 2.5V/3.3V Supply Voltage, 16- Lead VQFN, -40°C to +85°C Temperature Range, 100/Tube         Device:       5.5 GHz 1:4 Fanout Buffer/Translator with 400 mV LVPECL Outputs and Internal Input Termination         Supply Voltage:       U = 2.5V/3.3V         Package:       M = 3 mm x 3 mm 16-Lead VQFN         Temperature Range:       G = -40°C to +85°C         Media Ture: <blank> = 100/Tube</blank>	Device		Package	•	Media Type	a) SY58	3022UMG:
Supply Voltage:       U       =       2.5V/3.3V       Supply Voltage, 16-Lead VQFN, -40°C to +85°C Temperature Range, 1,000/Reel         Package:       M       =       3 mm x 3 mm 16-Lead VQFN       Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.         Media Ture: <blank> =       100/Tube</blank>	Device:		400 mV LVP	Fanout Buffer/Tran		b) SY58	Lead VQFN, -40°C to +85°C Temperature Range, 100/Tube
Temperature Range:       G = -40°C to +85°C       catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.         Media Type: <blank> = 100/Tube</blank>	Supply Voltage:	U =					Lead VQFN, -40°C to +85°C Temperature
Temperature Range:       G = -40°C to +85°C       the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.         Media Type: <blank> = 100/Tube</blank>	Package:	M =	3 mm x 3 mm	16-Lead VQFN		Note 1:	catalog part number description. This identifier is
		G =	–40°C to +85	°C			the device package. Check with your Microchip Sales Office for package availability with the Tape
	Media Type:						

NOTES:

#### Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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