Application Note
APT-0402 Rev A
March 25, 2004

Eliminating Parasitic Oscillation between Parallel MOSFETs

Based in part on a paper presented at Power Electronics Technology 2003 conference titled "Issues with Paralleling MOSFETs and IGBTs" by

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Introduction

Parasitic oscillation is a problem that unfortunately has not gone away as MOSFETs have evolved over the years and remains one of the main problems that can occur when paralleling MOSFETs. Parasitic oscillation can however be effectively eliminated with the use of a ferrite bead combined with a resistor on the gate of each MOSFET. This application note describes the nature of parasitic oscillation and explains why the ferrite bead solution is so effective. Although only MOSFETs are discussed, the phenomenon of parasitic oscillation and techniques for its elimination equally affect IGBTs.

Nature of Parasitic Oscillation

It has been shown [1], [2] that parasitic oscillation occurs during a switching transient when the drain voltage transitions.

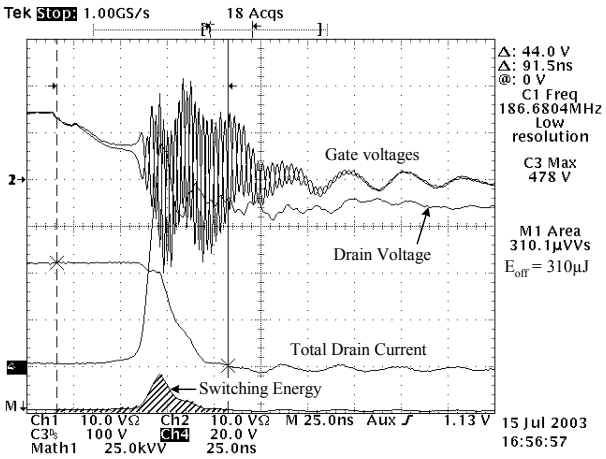

Figure 1 Parasitic oscillation between MOSFETs

Figure 1 shows parasitic oscillation between two parallel APT5024BLL Power MOS7® MOSFETs from Advanced Power Technology, rated at 500 Volts, 22 Amps. Each MOSFET has a 10Ω gate resistor between its gate and the gate driver. The applied drain-source voltage is 333 Volts, total current is 44 Amps, temperature is 25 °C, and gate drive supply voltage is 15 Volts. A single Micrel MIC4452 gate driver is used with symmetrical gate connection layout.

As seen in Figure 1, the oscillation on the gate is at very high frequency. Parasitic oscillation frequencies are typically in the range of 50MHz to 250MHz. Such an oscillation condition is unacceptable because it can cause over-voltage transients on the gate, radio frequency noise emission, high switching losses, and can even lead to uncontrolled, sustained oscillation and destruction of one or more devices.

Figure 1 shows oscillation during turn-off, but turn-on oscillation was also present in this case. Quite often the conditions for oscillation are different for turn-on than for turn-off, and oscillation will only occur at one or the other. Die size, capacitances, gain, and circuit parasitic elements are some of the factors that affect parasitic oscillation.

Parasitic oscillation is most easily detected on the gates but also exists in the drain currents and drain voltages, even through the drains are "shorted together". Parasitic oscillation is a push-pull situation where the voltages and currents oscillate out of phase between devices.

Parasitic oscillation can be very intermittent in nature, compounded by the fact that the impedance of test probes may in some cases eliminate it, making it difficult to prove its existence. Also, the same MOSFETs that won't oscillate in one circuit may oscillate in another due to differences in circuit layout.

In general, the conditions for oscillation are:

- Gain > 1
- Phase shift = 180°

The MOSFET has plenty of gain, and there is 180° phase shift. Also the dramatically varying voltage-dependent gate to drain capacitance provides non-linear feedback. Certainly all the conditions necessary for oscillation can be present when paralleling.

It is important to note that energy for parasitic oscillation comes from the drain and not from the gate. The rapid change in drain-source voltage during a switching transient induces a current from the drain through the reverse transfer capacitance to the gate circuitry. If the dv/dt is high enough, the magnitude of current injected to the gate can be sufficient to build up voltage across gate impedances (equivalent gate resistance in the MOSFET, bond wires in the package, stray inductances in the circuit, and the gate resistance). This can cause one of the MOSFETs to become more fully enhanced (turn itself on), causing a sudden imbalance in current sharing and also in the drain voltage at the die of each MOSFET. This variation in drain voltage is supported across stray inductances between the MOSFET dice. This sudden imbalance excites the oscillation of a resistive-inductive-capacitive (RLC) tank circuit involving the capacitances of each MOSFET die, the parasitic inductances in their interconnections, and the gate resistances.

Increasing the gate resistance dampens the tank circuit and is often effective in preventing oscillation in the first place because of reduced dv/dt. Unfortunately higher gate resistance also slows down the switching. The increased gate resistance sufficient to prevent oscillation sometimes results in unacceptably high switching losses.

The susceptibility for parasitic oscillation is related to peak drain dv/dt because this affects the peak drain-gate current during switching. figures 2 and 3 show peak drain dv/dt and di/dt values respectively for various gate resistance values, measured on a single APT5024BLL MOSFET. Note that dv/dt and di/dt are not constant during switching, and Figures 2 and 3 show only the maximum values of each. Rise and fall times of drain voltage and current (measured between 10% and 90% of final values) are roughly proportional to gate resistance as are switching energies, which are

shown in Figure 4. All measurements were made at room temperature with an applied drain-source voltage of 333 Volts, a gate drive supply of 15 Volts, and switching 22 Amps. E_{on} includes diode reverse recovery current from a 600 Volt, 30 Amp fast recovery diode.

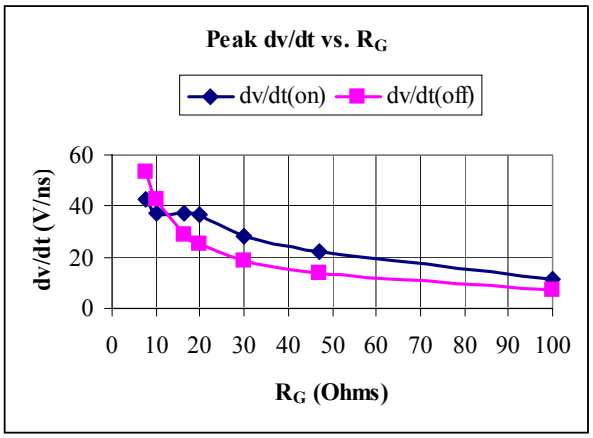

Figure 2 Peak drain dv/dt vs. gate resistance

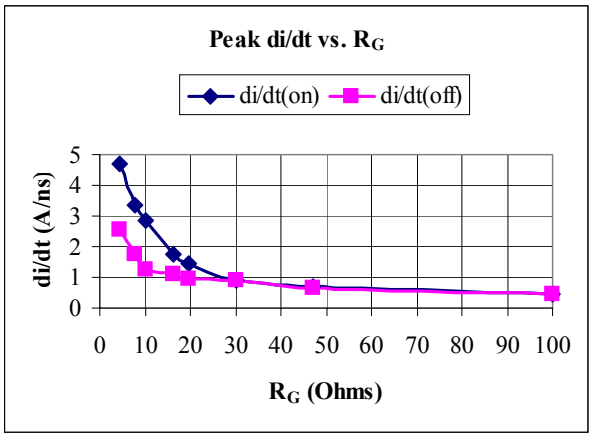

Figure 3 Peak drain di/dt vs. gate resistance

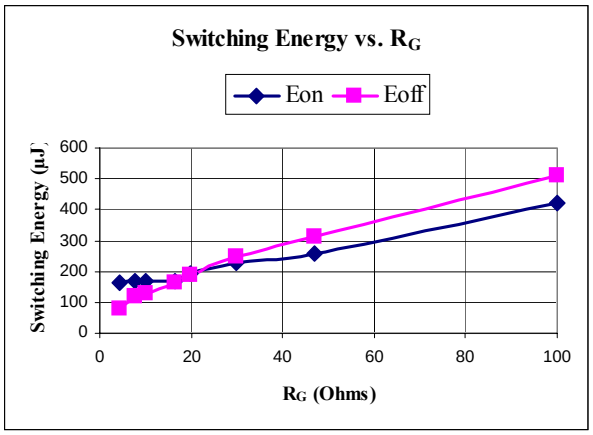

Figure 4 Switching energies vs. gate resistance

Peak drain dv/dt at turn-off is very sensitive to gate resistance, as well as peak di/dt at both turn-on and turn-off. Beyond the "knee" of these curves, increasing the gate resistance yields diminishing benefits in terms of limiting energy induced into the oscillating circuit, but the switching energies increase steadily. If oscillations persist even with large values of gate resistance, some other technique may be required to eliminate the oscillation while keeping switching losses at an acceptable level.

Ferrite Beads

It has been found that a ferrite bead combined with a resistor on each MOSFET gate eliminates parasitic oscillation while minimizing switching losses. In fact, adding a ferrite bead is more effective than using gate resistance alone because the impedance of the ferrite bead is directly proportional to frequency. The bandwidth of the gate drive signal is about 2MHz, whereas parasitic oscillation frequency is many times higher, from about 50MHz to 250MHz. So the impedance of the ferrite bead to oscillation noise is 25 to 125 times higher than its impedance to the gate drive signal. This high impedance is extremely effective at blocking drain to gate noise current. Given enough inductance in the ferrite bead combined with sufficient damping from the gate resistance, parasitic oscillation can be completely and reliably eliminated.

A ferrite bead can also be used with a single MOSFET that is not connected in parallel with any other MOSFETs. The effect is the same; high frequency noise on the gate is blocked, eliminating any tendency for oscillations.

Figure 5 shows the clean turn-off switching transient of the same parallel pair of APT5024BLL MOSFETs that were oscillating in Figure 1. The difference is that a ferrite

bead was added in series with a 4.3Ω resistor on each MOSFET gate.

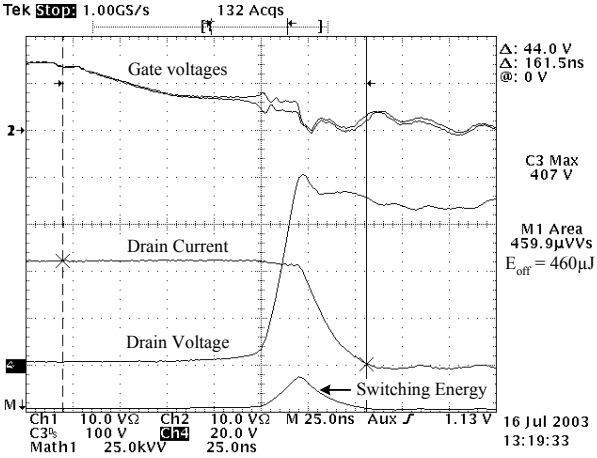

Figure 5 APT5024BLL Turn-off, 4.3Ω with series ferrite bead on each gate, 333V, 44A, 25 °C

Turn-on of these paralleled MOSFETs has just as dramatic a change as turn-off.

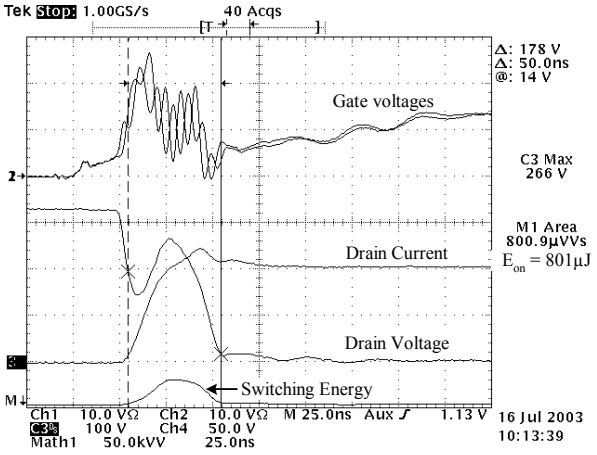

Figure 6 APT50M65LLL Turn-on, 4.3Ω resistor only on each gate, 333V, 100A, 25 °C

In Figure 6, two parallel APT50M65LLL MOSFETs are oscillating during turn-on, each with a 4.3Ω resistor on the gate. The same MOSFETs were used in Figure 7, this time with only a 1Ω resistor in series with a small ferrite bead on each gate. The oscillation is eliminated at the expense of about 8% increase in E_{on}. Turn-on delay increased very slightly.

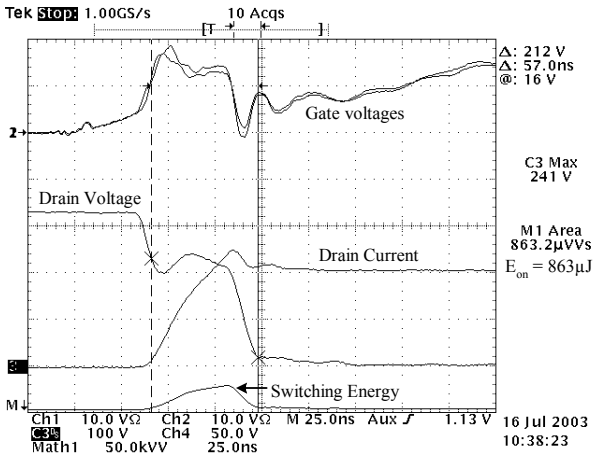

Figure 7 APT50M65LLL Turn-on, 1Ω with series ferrite bead on each gate, 333V, 100A, 25 °C

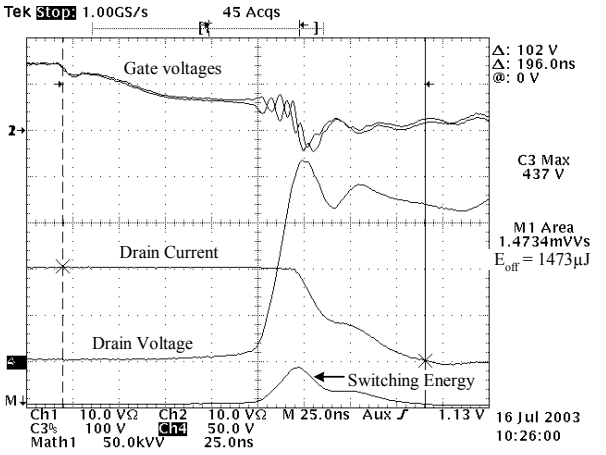

Figure 8 APT50M65LLL Turn-off, 4.3Ω resistor only on each gate, 333V, 100A, 25 °C

Figures 8 shows turn-off just beginning to oscillate, and in Figure 9 the oscillation is gone. The same 4.3Ω resistor and 1Ω resistor with series ferrite bead combinations were used as in Figures 6 and 7. This time the ferrite bead with small series resistance resulted in a *decrease* in E_{off}, in spite of the fact that turn-off delay is increased. Note that the gates in Figure 9 are on the verge of oscillating, so a slight increase in gate impedances would be optimum.

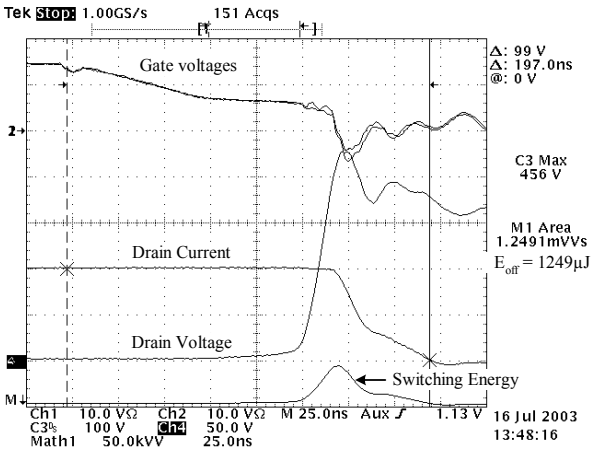

Figure 9 APT50M65LLL Turn-off, 1Ω with series ferrite bead on each gatge, 333V, 100A, 25 °C

If resistance alone were used to eliminate the oscillations shown in Figures 1, and 6, the switching energies would be higher than with the use of ferrite beads (and a lower resistance) on each gate.

Ferrite beads are a very attractive solution. They are inexpensive, small, and simple to use. There are a variety of ferrite beads available with different characteristics. Switching energies can be optimized by experimenting with different combinations of resistance and bead inductance. Some ferrite beads have very flat inductive reactance with steadily increasing resistance with increasing frequency. If the ferrite beads are large and lossy enough, the gate resistors can be eliminated.

It may seem odd that adding inductance to the gate drive circuit solves the parasitic oscillation problem. Best design practice dictates minimizing the gate drive inductance by using a very tight circuit layout. The key with gate drive layout however isn't so much inductance but rather loop area [3]. The problem with a large loop area is the loop acts as an antenna, which can pick up high frequency noise. In [1] and [2], long gate drive lead lengths actually eliminated parasitic oscillation due to the increased stray gate drive inductance.

Zener Clamp Diodes

It is a common practice to install a zener diode between the gate and source leads. This can be effective at reducing noise at low switching frequencies and with long gate drive lead lengths, as in many motor drives. Zener diodes are however ineffective at absorbing noise at frequencies of tens of megahertz.

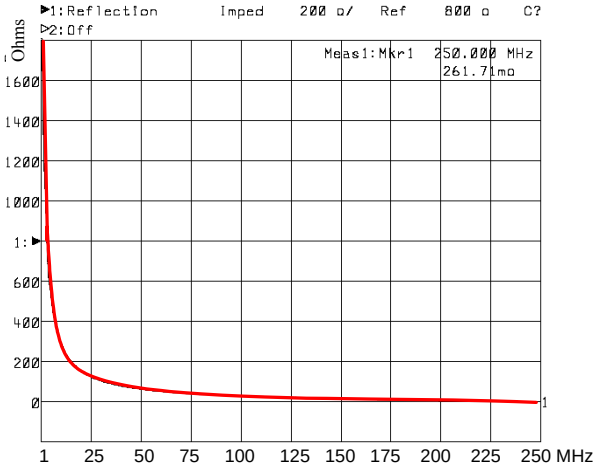

Figure 10 Zener Impedance vs. Frequency, DO-41 Package

Figure 10 shows the measured frequency response of a 15 Volt zener diode in a DO-41 package. The leads were cut off to about 5 mm length, about what is needed to solder through a circuit board. The impedance is purely capacitive up to about 250MHz, and at higher frequency the package inductance dominates, making the zener diode act like an inductor. Just like a regular diode, the zener diode capacitance reduces with increasing reverse bias voltage.

The presence of a zener diode attached to the gate adds a small, voltage and frequency dependent capacitance to the RLC tank circuit where parasitic oscillation can occur. The added capacitance usually makes no difference though because the zener diode capacitance is small compared to the input capacitance of a MOSFET.

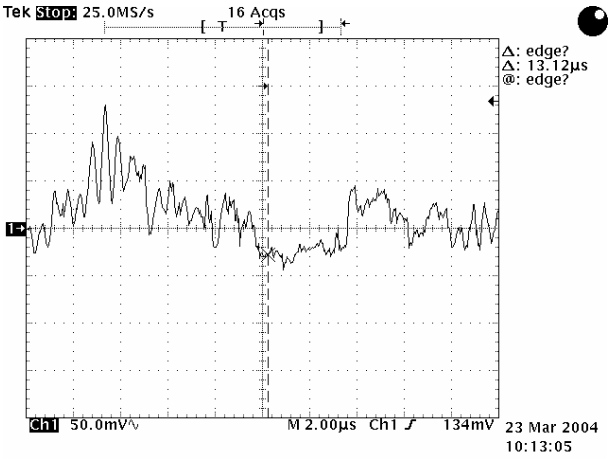

Figure 11 Zener Oscillation at Breakdown Voltage

Figure 11 shows oscillation of a zener with cathode-anode voltage at the zener breakdown voltage. A 15V, 0.5W zener in a DO-41 package was connected in series with a 1kΩ resistor, and voltage was applied across the zener and resistor combination. The scope probe was attached across the zener diode with the trigger set for AC coupling. With a slight change in applied voltage, either lower or higher, the oscillation stops. The zener diode only oscillates as it begins to avalanche. This zener oscillation was found in at least one case to actually increase the susceptibility of paralleled MOSFETs to go into parasitic oscillation. Whether this happens depends of course on the circuit parasitic impedances and components.

Since adding a gate-source zener diode does not effectively restrict high frequency noise and parasitic oscillation, it is best to leave them out. They can however be useful for suppressing low frequency noise, such as in a motor drive application with long gate drive lead lengths.

Conclusions

- Parasitic oscillation between parallel transistors is unacceptable because of greatly reduced reliability, possibly reduced efficiency, and radio frequency noise.
- Peak drain dv/dt and di/dt are non-linear functions of gate resistance. The effectiveness of reducing peak dv/dt and di/dt decreases but switching energies steadily increase with increasing gate resistance.
- Ferrite beads are very effective at eliminating parasitic oscillation while minimizing switching losses because they act like a frequency-dependent gate resistor.
- Installing a zener diode between gate and source does not control parasitic oscillation.

References

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