Million Cycle Endurance

Application Note
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INTRODUCTION

Some data storage applications require flash memory endurance, i.e., the number of Erase and Program cycles, to be at least 1,000,000 cycles, while still meeting the standard endurance cumulative failure rate of less than 1% (ref. IEEE-Std-1005-1998). This would mean cycling every sector within the device about once every 5 minutes for 10 years of continuous operation. In reality, most applications only require that some portion of the address space be cycled 1,000,000 or more times; the rest of the address space will be cycled far fewer times. This application note will show how the standard SST memory, with a guaranteed 10,000 cycle failure rate of less than 1%, can be used in applications where a portion of the memory requires 1,000,000 endurance cycles.

Endurance Specification

In order to guarantee endurance, the manufacturer must specify both a number of cycles for endurance and the associated failure rate. The lot acceptance guarantee means that if a customer samples a shipment and the sample fails, the entire shipment may be returned to the manufacturer. Endurance cycling is a time consuming test; for instance, to cycle a flash device 10,000 times takes a full day for an SST device, while other manufacturers' devices will take a month or longer. Customers rarely actually perform incoming lot acceptance inspections for endurance. Therefore, even if a flash memory vendor provides a lot acceptance guarantee, the user has a difficult and time consuming task to actually perform the sample lot acceptance endurance testing in a practical time frame.

The most important value is the actual endurance failure rate of the device in the application. This value can vary significantly from technology to technology and per manufacturer for a given technology. See Figure 1 for an example of how a "higher endurance number" does not mean a better system failure rate. As long as the system does not actually erase and program the device into the "wear-out" region, the device with the lower failure rate provides better system reliability.

SST is able to provide a true lot acceptance guarantee (where the customer can accept/reject an entire lot based on the results of a sample, tested under JEDEC defined conditions) of the endurance of all SST SuperFlash memory devices. This is possible because SST's proprietary SuperFlash technology allows the testing of each and every memory cell of each and every device for endurance during the standard product testing operation.

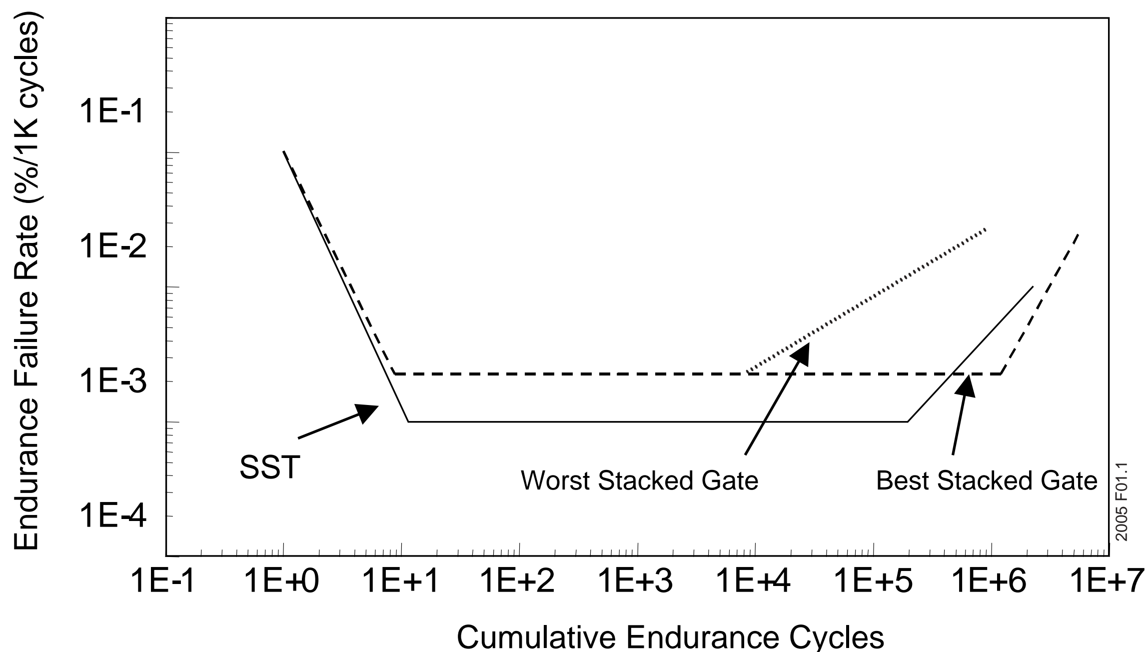

FIGURE 1: SST's Split-Gate and Others' Stacked Gate Cells use FN tunneling for Erase and CHE for Program

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System Operation and Impact on System Reliability

Flash memories are used to store many types of code and data. Most code, e.g., firmware, is changed infrequently (<1000 times). Some code, e.g., configuration, may be changed very frequently (>100,000 times). Although most data is changed frequently (>1,000 times), only some data is changed very frequently (>100,000 times). Most applications only use the flash memories for code or not very frequently changed data. Therefore, during the useful life of less than 10,000 endurance cycles, the figure of paramount importance is a low failure rate (<0.01%/1000 cycles), not the total number of cycles (which are not going to be required anyway). However, there is an increasing number of applications where a portion of the total flash memory space is required for very frequently changed code or data.

Device Erase/Program Operation

Flash memories typically erase by sectors, e.g., a segment of memory larger than the minimum read element (byte or word) and program byte-by-byte or word-by-word. Erase sectors can be of various sizes, even within the same device. There are some devices with a page program feature; however, the page size is less than the erase sector size. Endurance is limited by the number of times the sector is erased and programmed.

A flash memory sector can be programmed many times between erases, as long as each byte (word) within the sector is only programmed once. For example, an SST flash device with a 4 KByte sector can have all 4 KByte programmed byte-by-byte in one Program operation time or can have each byte programmed with its own Program operation until all 4,096 locations have been programmed. Each Erase operation plus the Program operations (1 to 4096 times of Byte-Program) after the erase, makes one endurance (Erase and Program) cycle.

Technology Comparisons

The limitation on flash memories endurance is controlled by two major factors:

1. The Time-Dependent-Dielectric-Breakdown characteristics of the charge transfer oxides used for erase and program.
2. The charge-trapping characteristics of the charge transfer oxides used for erase and program.

Which factor is most significant and the magnitude of the factor as affecting erase or program capability are functions of the process technology and cell design.

SST's SuperFlash technology uses relatively thick oxides for charge transfer both to erase and program; therefore, is much less susceptible to the dielectric breakdown issues of the thin oxide used in the alternative technologies, e.g., stacked gate.

Both SuperFlash and thin oxide alternative technologies are susceptible to charge trapping effects on erase and program, although with SuperFlash the effects on program are virtually undetectable. All flash memory cells are similarly affected by charge trapping which reduces the erase margin; therefore, closing the window between the programmed and erased states. Extended erase times or higher erase voltages can overcome the window closing caused by charge trapping.

Some memory locations in SST flash devices will eventually fail due to single bits failing to erase, i.e., stuck “0”, due to charge trapping effect. These single bits are readily apparent after an Erase operation, so suitable corrective actions at the system level can take place.

Unlike the SST SuperFlash, the alternative technologies using thin oxide stacked gate, not only fail due to single bit failure to erase, but more importantly fail for another distinctly dissimilar failure mode of over-erase. Over-erase causes the catastrophic failure of an entire column; therefore, there is no suitable corrective action available at the system level. In order to minimize the catastrophic over-erase failure rate, the thin oxide stacked gate manufacturers must employ complicated erase algorithms. The logic for these algorithms occupies silicon area, but more importantly, execution of these algorithms takes a long time. Since execution of the algorithm already takes a long time, thin oxide stacked gate manufacturers allow additional extensions of the erase time to increase the number of possible endurance cycles. Therefore, the Sector-Erase time of a stacked gate flash memories starts at about 1 second and increases to tens of seconds through the lifetime of the device.

Recognizing that most applications do not require very frequent changing of the memory contents and that time to re-write is of critical importance during system testing and in field usage, SST has chosen to use a fixed, short duration Sector-Erase time. This fixed erase time does not increase over the life of the application. The short 10s of milliseconds (at most, depending on device), not seconds, allows cost effective system testing and field updating.

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Constraint

Since SST has chosen to use a fixed short Sector-Erase time, the device failure rate for all devices in all lots is not guaranteed to meet IEEE standard criteria of less than 1% at 1,000,000 cycles. This is not a limitation of the technology, just that SST has chosen not to penalize all customers by forcing a long erase time, just to satisfy those few applications that require high number of cycles.

Solution

The typical endurance of an SST device is greater than 100,000 cycles with the fixed short erase time specification. Therefore, any given 4 KByte sector endurance is greater than 100,000 cycles. If 10 sectors are allocated to take turns storing 4 KByte of data, effectively 1,000,000 cycles or more of data changes can be supported. This only uses 40 KByte of address space, which is still less than the block size (64 KByte) of many stacked gate devices. So as long as the amount of very frequently changed data is less than 4 KByte, the actual memory space utilization is the same or better with the SST device.

Implementation

To implement the use of additional sectors to achieve higher endurance, the following algorithm is recommended (note, this concept can be implemented in a variety of “address pointing” algorithms):

1. Select 10 sectors to be used, preferably consecutive addresses.
2. Establish an address pointer location.
3. Have the address pointer identify the address of the first sector, e.g., the same sector address that is used for the Sector-Erase command. This same address forms part of the address of the first byte in the sector to be programmed.
4. Program the sector until all 4 KByte are used. This is the sector containing the valid data.
5. Erase the sector.
6. Verify the sector is erased.
7. If the sector erases correctly, then start programming new data in the sector. Continue steps 4 to 6 until the sector fails to verify. When this sector fails to verify, program all locations in the sector to “0” to further indicate the sector is no longer usable.
8. When the sector fails to verify, then move the address pointer to the next sector and continue steps 4 through 8.

Since the typical number of endurance cycles per sector is 100,000; the total number of available Erase/Program operations for the 10 sectors will be greater than 1,000,000 cycles.

Summary

This application note provides a methodology to use SST’s standard guaranteed 10,000 endurance cycle MPF SuperFlash memory in applications that require a portion of the memory space to be cycled 1,000,000 times or more. The benefits of SST’s fast and fixed erase times is maintained, while still allowing a portion of the memory to be cycled many times.

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