SY87700AL

Low-Power, 3.3V, 32 Mbps to 208 Mbps AnyRate® Clock and Data Recovery

Features

- 3.3V Power Supply
- SONET/SDH/ATM Compatible
- Clock and Data Recovery from 32 Mbps Up to 208 Mbps NRZ Data Stream; Clock Generation from 32 Mbps to 208 Mbps
- Two On-Chip PLLs: One for Clock Generation and Another for Clock Recovery
- Selectable Reference Frequencies
- Differential PECL High-Speed Serial I/O
- Line Receiver Input: No External Buffering Needed
- Link Fault Indication
- 100K ECL-Compatible I/O
- Industrial Temperature Range: –40°C to +85°C
- Low Power: Fully Compatible SY87700V, but Consumes 30% Less Power
- Available in a 32-Lead ePAD TQFP Package

Applications

- SONET/SDH/ATM OC-1 and OC-3
- Fast Ethernet, SMPTE 259
- Proprietary Architecture Up to 208 Mbps

General Description

The SY87700AL is a complete clock recovery and data re-timing integrated circuit for data rates from 32 Mbps up to 208 Mbps NRZ. The device is ideally suited for SONET/SDH/ATM applications and other high-speed data transmission systems.

Clock recovery and data re-timing is performed by synchronizing the on-chip VCO directly to the incoming data stream. The VCO center frequency is controlled by the reference clock frequency and the selected divide ratio. On-chip clock generation is performed through the use of a frequency multiplier PLL with a byte rate source as reference.

The SY87700AL also includes a link fault detection circuit.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN})..... –0.5V to V_{CC}
Output Current (I_{OUT})
Continuous .....±50 mA
Surge.....±100 mA

Operating Ratings ‡

Input Voltage (V_{CC}) ..... –3.15V to +3.45V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

DC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{CC}	3.15	3.3	3.45	V	—
Power Supply Current	I_{CC}	—	120	160	mA	—

PECL 100K DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; $T_A = –40°C$ to $+85°C$, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input HIGH Voltage	V_{IH}	$V_{CC} – 1.165$	—	$V_{CC} – 0.880$	V	—
Input LOW Voltage	V_{IL}	$V_{CC} – 1.810$	—	$V_{CC} – 1.475$	V	—
Output HIGH Voltage	V_{OH}	$V_{CC} – 1.075$	—	$V_{CC} – 0.830$	V	50Ω to $V_{CC} – 2V$
Output LOW Voltage	V_{OL}	$V_{CC} – 1.860$	—	$V_{CC} – 1.570$	V	50Ω to $V_{CC} – 2V$
Input LOW Current	I_{IL}	0.5	—	—	µA	$V_{IN} = V_{IL(MIN)}$

TTL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; $T_A = –40°C$ to $+85°C$, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Input HIGH Voltage	V_{IH}	2.0	—	V_{CC}	V	—
Input LOW Voltage	V_{IL}	—	—	0.8	V	—
Output HIGH Voltage	V_{OH}	2.0	—	—	V	$I_{OH} = –0.4$ mA
Output LOW Voltage	V_{OL}	—	—	0.5	V	$I_{OL} = 4$ mA
Input HIGH Current	I_{IH}	–175	—	—	µA	$V_{IN} = 2.7V$, V_{CC} = Max.
		—	—	100	µA	$V_{IN} = V_{CC}$, V_{CC} = Max.
Input LOW Current	I_{IL}	–300	—	—	µA	$V_{IN} = 0.5V$, V_{CC} = Max.
Output Short-Circuit Current	I_{OS}	–15	—	–100	mA	$V_{OUT} = 0V$, (Max., 1 sec.)

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = V_{CCO} = V_{CCA} = 3.3V \pm 5\%$; $T_A = –40°C$ to $+85°C$, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
VCO Center Frequency	f_{VCO}	750	—	1250	MHz	f_{REFCLK} x Byte Rate
VCO Center Frequency Tolerance	Δf_{VCO}	—	5	—	%	Nominal
Acquisition Lock Time	t_{ACQ}	—	—	15	µs	50Ω to $V_{CC} – 2$
REFCLK Pulse Width HIGH	t_{CPWH}	4	—	—	ns	50Ω to $V_{CC} – 2$
REFCLK Pulse Width LOW	t_{CPWL}	4	—	—	ns	$V_{IN} = V_{IL}$ (Min.)
REFCLK Input Rise Time	t_{IR}	—	0.5	2	ns	—
Output Duty Cycle (RCLK/TCLK)	t_{ODC}	45	—	55	% of UI	—
ECL Output Rise/Fall Time (20% to 80%)	t_r/t_f	100	—	400	ps	50Ω to $V_{CC} – 2$
Recovered Clock Skew	t_{SKEW}	–200	—	200	ps	—
Data Valid	t_{DV}	$1/(2xf_{RCLK}) – 200$	—	—	ps	—
Data Hold	t_{DH}	$1/(2xf_{RCLK}) – 200$	—	—	ps	—

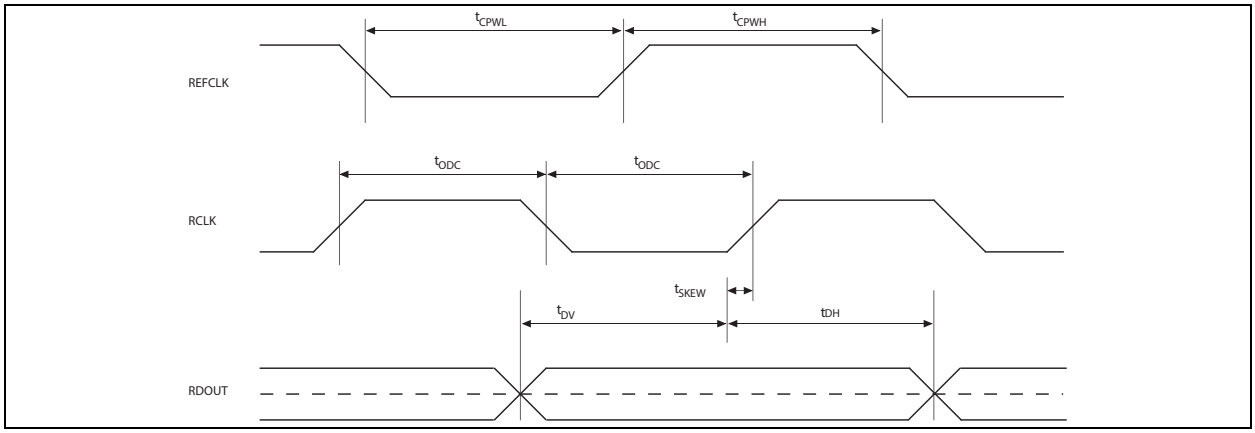
TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature	T_S	–65	—	+150	°C	—
Package Thermal Resistance						
Thermal Resistance, TQFP 32-Ld, Note 2	θ_{JA}	—	27.6	—	°C/W	0 lfpm airflow
	θ_{JA}	—	22.6	—	°C/W	200 lfpm airflow
	θ_{JA}	—	20.7	—	°C/W	500 lfpm airflow

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +85°C rating. Sustained junction temperatures above +85°C can impact the device reliability.

2: Using JEDEC standard test boards with die attach pad soldered to PCB. See www.amkor.com for additional package details.

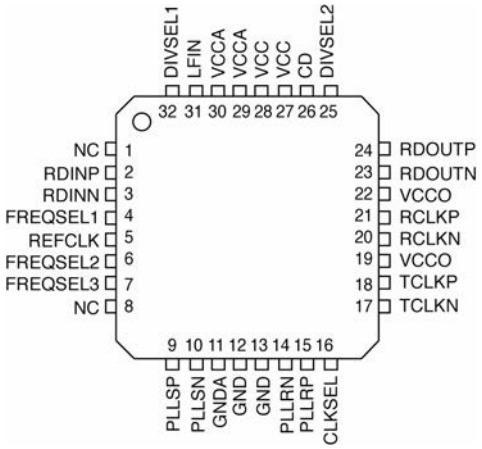
Timing Waveforms



2.0 PIN DESCRIPTIONS

Package Type

SY87700AL
32-Lead TQFP (M)
(Top View)



The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
Inputs		
2 3	RDINP RDINN	Serial Data Input. Differential PECL: These built-in line receiver inputs are connected to the differential receive serial data stream. An internal receive PLL recovers the embedded clock (RCLK) and data (RDOUT) information. The incoming data rate can be within one of eight frequency ranges depending on the state of the FREQSEL pins. See “Frequency Selection” Table.
5	REFCLK	Reference Clock. TTL Input: This input is used as the reference for the internal frequency synthesizer and the “training” frequency for the receiver PLL to keep it centered in the absence of data coming in on the RDIN inputs
26	CD	Carrier Detect. PECL Input: This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output of optical modules or from external transition detection circuitry. When this input is HIGH the input data stream (RDIN) is recovered normally by the Receive PLL. When this input is LOW the data on the inputs RDIN will be internally forced to a constant LOW, the data outputs RDOUT will remain LOW, the Link Fault Indicator output LFIN forced LOW and the clock recovery PLL forced to lock onto the clock frequency generated from REFCLK.
4 6 7	FREQSEL1 FREQSEL2 FREQSEL3	Frequency Select. TTL Inputs: These inputs select the output clock frequency range as shown in the “Frequency Selection” Table.
32 25	DIVSEL1 DIVSEL2	Divider Select. TTL Inputs: These inputs select the ratio between the output clock frequency (RCLK/TCLK) and the REFCLK input frequency as shown in the “Reference Frequency Selection” Table.
16	CLKSEL	Clock Select. TTL Input: This input is used to select either the recovered clock of the receiver PLL (CLKSEL = HIGH) or the clock of the frequency synthesizer (CLKSEL = LOW) to the TCLK outputs.

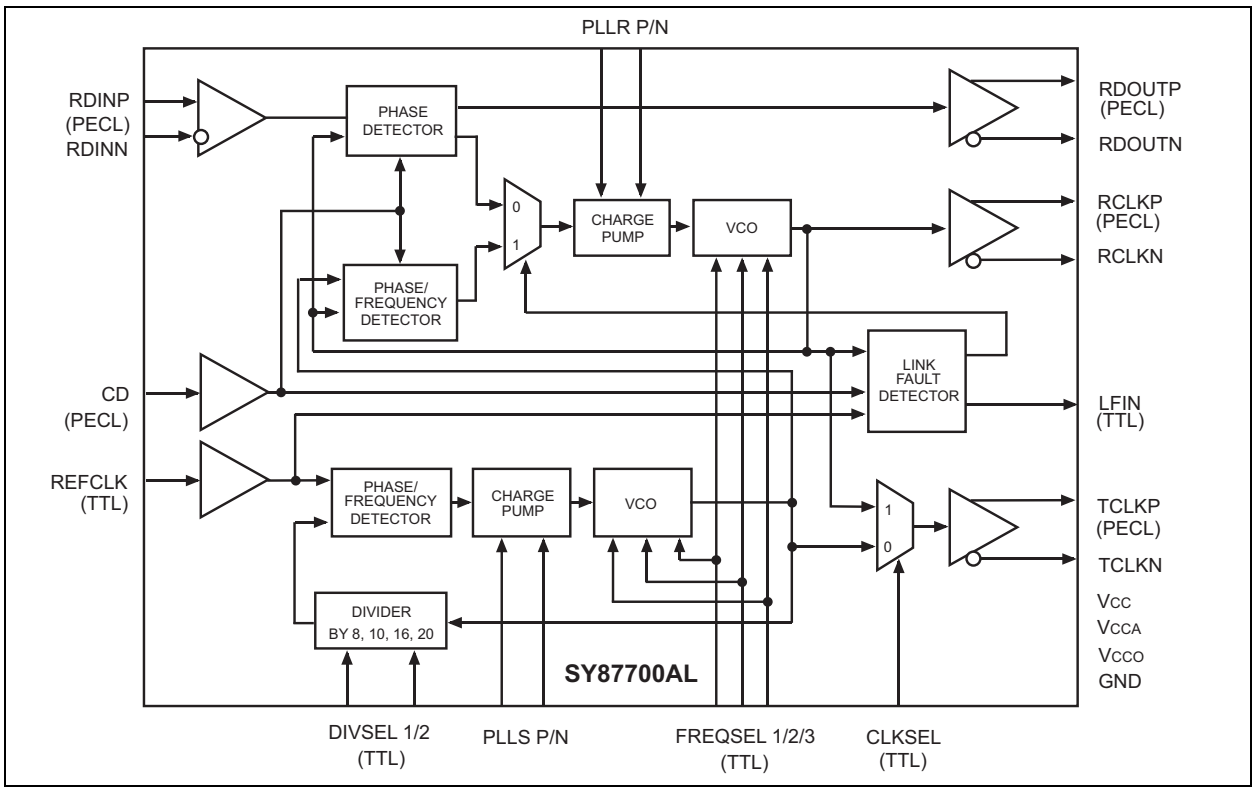
TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
Outputs		
31	LFIN	Link Fault Indicator. TTL Output: This output indicates the status of the input data stream RDIN. Active HIGH signal is indicating when the internal clock recovery PLL has locked onto the incoming data stream. LFIN will go HIGH if CD is HIGH and RDIN is within the frequency range of the Receive PLL (1000 ppm). LFIN is an asynchronous output.
24 23	RDOUTP RDOUTN	Receive Data Output. Differential PECL: These ECL 100k outputs represent the recovered data from the input data stream (RDIN). This recovered data is specified against the rising edge of RCLK.
21 20	RCLKP RCLKN	Clock Output. Differential PECL: These ECL 100k outputs represent the recovered clock used to sample the recovered data (RDOUT).
18 17	TCLKP TCLKN	Clock Output. Differential PECL: These ECL 100k outputs represent either the recovered clock (CLKSEL = HIGH) used to sample the recovered data (RDOUT) or the transmit clock of the frequency synthesizer (CLKSEL = LOW).
9 10	PLLSP PLLSN	Clock Synthesis PLL Loop Filter: External loop filter pins for the clock synthesis PLL.
15 14	PLLRP PLLRN	Clock Recovery PLL Loop Filter: External loop filter pins for the receiver PLL.
Power and Ground		
27, 28	VCC	Supply Voltage(Note 1)
29, 30	VCCA	Analog Supply Voltage(Note 1)
19, 22	VCCO	Output Supply Voltage(Note 1)
12, 13	GND	Ground.
1, 8	NC	No connect.
11	GNDA	Analog Ground.

Note 1: VCC, VCCA, VCCO must be the same value.

3.0 FUNCTIONAL DESCRIPTION

Functional Block Diagram



3.1 Clock Recovery

Clock recovery, as shown in the block diagram, generates a clock that is at the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency detector. Output pulses from the detector indicate the required direction of phase correction. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability, without incoming data, is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the frequency of the incoming signal varies by greater than approximately 1000 ppm with respect to the synthesizer frequency, the PLL will be declared out of lock, and the PLL will lock to the reference clock.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal. This transfer function yields a 30 µs data stream of continuous 1's or 0's for random incoming NRZ data.

3.2 Lock Detect

The SY87700AL contains a link fault indication circuit, which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, then the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by more than approximately 1000 ppm, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within approximately 1000 ppm, the PLL will be declared in lock and the lock detect output will go active.

During the interval when the CDR is not locked onto the RDIN input, the LFIN output will not be a static LOW, but will be changing.

TABLE 3-1: FREQUENCY SELECTION TABLE

FREQSEL1	FREQSEL2	FREQSEL3	f_{VCO}/f_{RCLK}	f_{RCLK} Data Rates
0	1	1	6	125 Mbps to 208 Mbps
1	0	0	8	94 Mbps to 156 Mbps
1	0	1	12	63 Mbps to 104 Mbps
1	1	0	16	47 Mbps to 78 Mbps
1	1	1	24	32 Mbps to 52 Mbps
0	1	0	—	Undefined
0	0	X (Note 2)	—	Undefined

Note 1: SY87700AL operates from 32 MHz to 208 MHz. For higher speed applications, the SY87701AL operates from 28 MHz to 1300 MHz.

2: X is a Don't Care.

TABLE 3-2: REFERENCE FREQUENCY SELECTION

DIVSEL1	DIVSEL2	f_{RCLK}/f_{REFCLK}
0	0	8
0	1	10
1	0	16
1	1	20

Note: Suggested values. Values may vary for different applications.

FIGURE 3-1: *Loop Filter Components.*

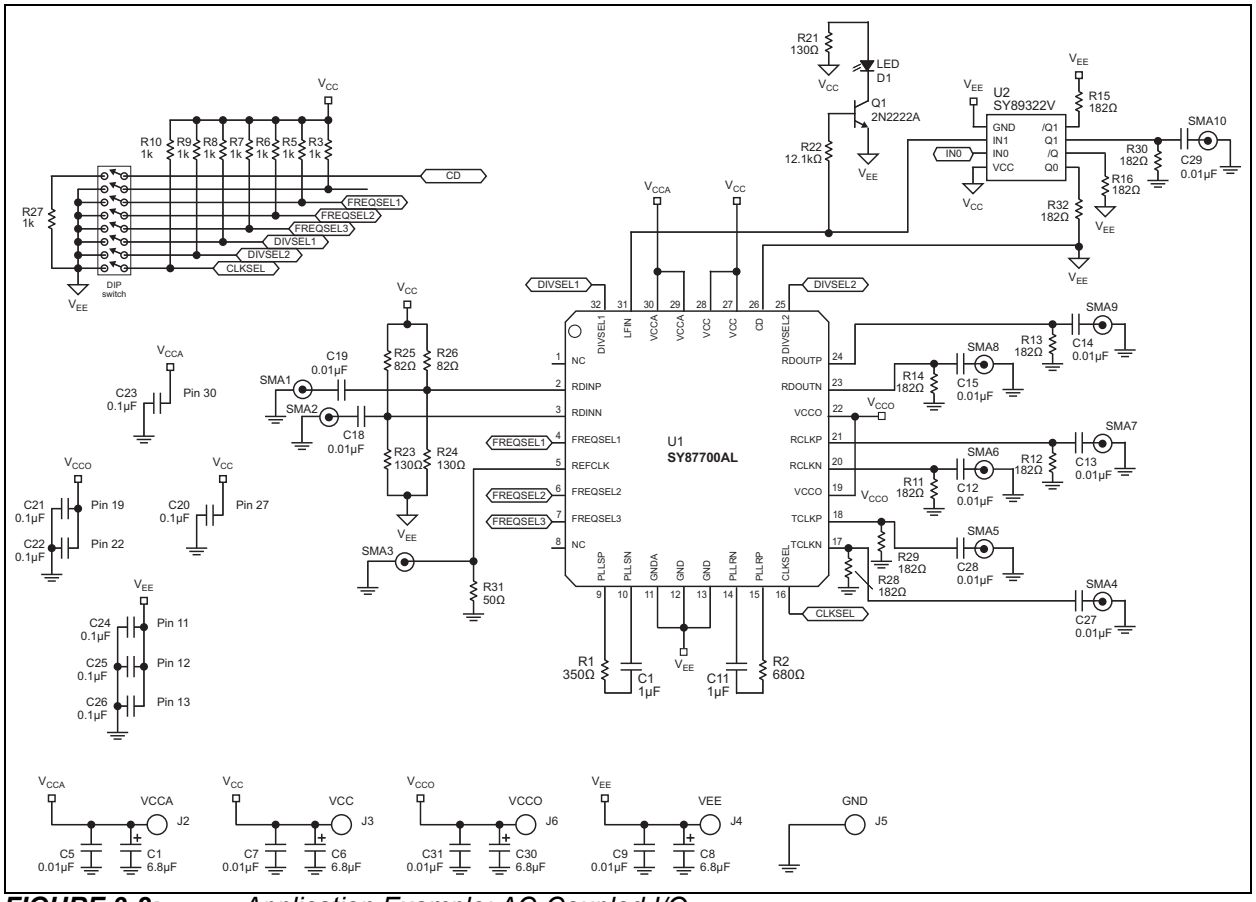


FIGURE 3-2: *Application Example: AC-Coupled I/O.*

TABLE 3-3: BILL OF MATERIALS (AC-COUPLED)

Item	Part Number	Manufacturer	Description	Qty.
C6	293D685X0025B2T	Vishay	6.8 µF, 25V, Tantalum Capacitor, Size B	1
C7	VJ206Y103JXJAT	Vishay	0.01 µF Ceramic Capacitor, Size 1206, X7R Dielectric	1
C10, C11	VJ0603Y105JXJAT	Vishay	1.0 µF Ceramic Capacitor, Size 0603, X7R Dielectric	2
C12 - C15, C18, C19, C27, C28	VJ0402Y104JXJAT	Vishay	0.1 µF Ceramic Capacitor, Size 0402, X7R Dielectric	8
C20 - C26	VJ0402Y104JXJAT	Vishay	0.01 µF Ceramic Capacitor, Size 1206, X7R Dielectric	7
D1	P301-ND	Panasonic	LED Diode, T-1 3/4, Red Clear	1
D2	P300-ND/P301-ND	Vishay	T-1 3/4, Red LED	1
J2, J3, J4, J6	111-0702-001	Johnson Components	Red, Insulated Thumb Nut Binding Post (Jumped Together)	4
J5	BLM21A102F	Murata	Black, Insulated Thumb Nut Binding Post, GND (Jumped to V_{EE})	1
Q1	459-2598-5-ND	NTE	2N2222A Buffer/Driver Transistor, NPN	1
R1	CRCW04023500F	Vishay	350Ω Resistor, 2%, Size 0402	1
R2	CRCW04026800F	Vishay	680Ω Resistor, 2%, Size 0402	1
R3 - R10	CRCW04021001F	Vishay	1 kΩ Pull-up Resistor, 2%, Size 1206	8
R11 - R16, R28 - R30, R32	CRCW04021820F	Vishay	182Ω Resistor, 2%, Size 0402	10
R21	CRCW06031300F	Vishay	130Ω Resistor, 2%, Size 0603	1
R22	CRCW04021820F	Vishay	12.1 kΩ Resistor, 2%, Size 1206	1
R23, R24	CRCW04022825F	Vishay	82Ω Resistor, 2%, Size 0402	2
R25, R26	CRCW04021300F	Vishay	130Ω Resistor, 2%, Size 0402	2
R27	CRCW0402OOR0F	Vishay	0Ω Resistor, 2%, Size 0402	1
R31	CRCW04025000F	Vishay	50Ω Resistor, 2%, Size 0402	1
SMA1 - SMA10	142-0701-851	Johnson Components	End Launch SMA Jack	10
SP1 - SP6	—	—	Solder Jump Option	6
SW1	CT2068-ND	CTS	8-Position, Top Actuated Slide Dip Switch	1
U1	SY87700AL	Microchip	Low-Power 3.3V 28 Mbps to 216 Mbps AnyRate® Clock and Data Recovery	1
U2	SY89322V	Microchip	3.3/5V Dual LVTTL/LVCMOS-to-Differential LVPECL Translator	1

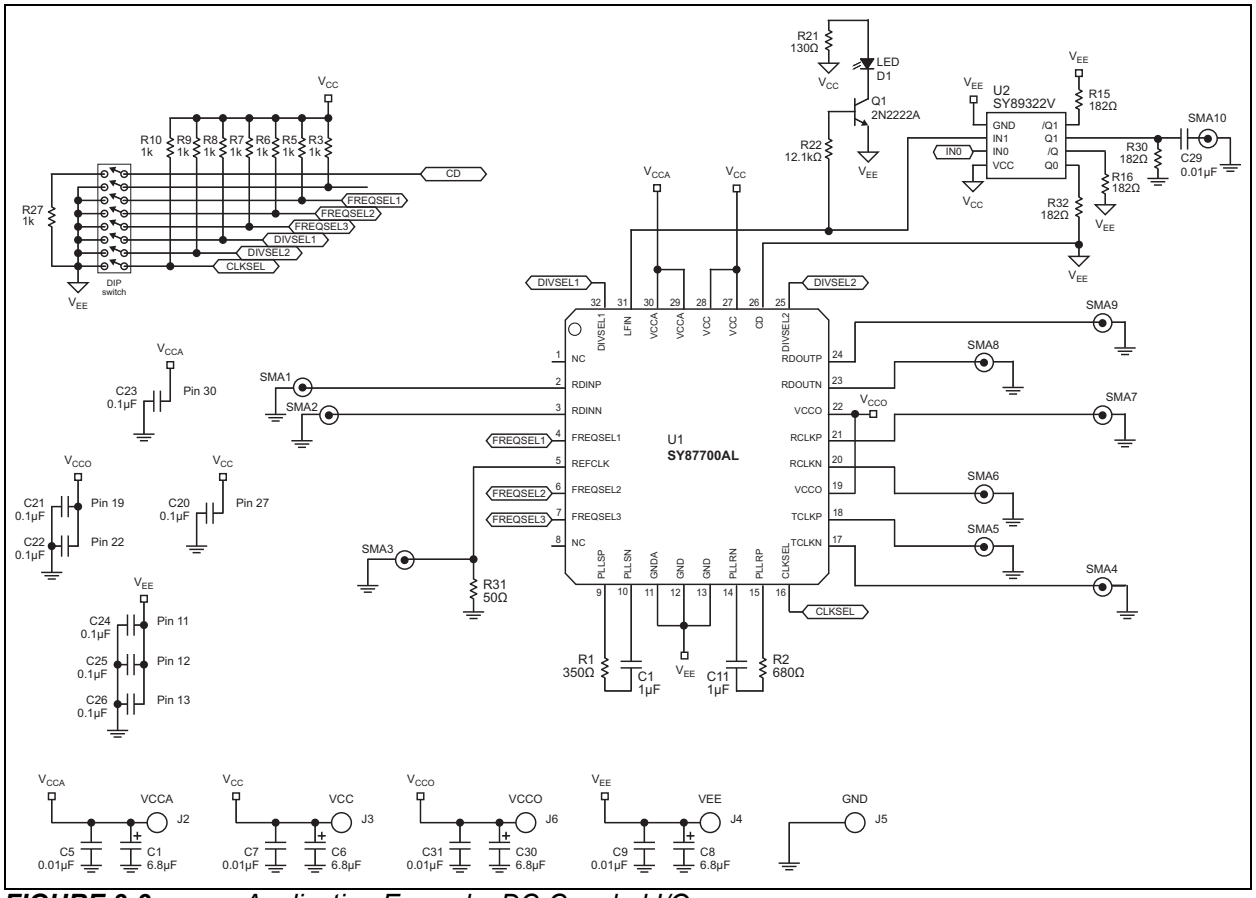


FIGURE 3-3: *Application Example: DC-Coupled I/O.*

TABLE 3-4: BILL OF MATERIALS (DC-COUPLED)

Item	Part Number	Manufacturer	Description	Qty.
C6	293D685X0025B2T	Vishay	6.8 µF, 25V, Tantalum Capacitor, Size B	1
C7	VJ206Y103JXJAT	Vishay	0.01 µF Ceramic Capacitor, Size 1206, X7R Dielectric	1
C10, C11	VJ0603Y105JXJAT	Vishay	1.0 µF Ceramic Capacitor, Size 0603, X7R Dielectric	2
C12 - C15, C18, C19, C27, C28	VJ0402Y104JXJAT	Vishay	0.1 µF Ceramic Capacitor, Size 0402, X7R Dielectric	8
C20 - C26	VJ0402Y104JXJAT	Vishay	0.01 µF Ceramic Capacitor, Size 1206, X7R Dielectric	7
D1	P301-ND	Panasonic	LED Diode, T-1 3/4, Red Clear	1
D2	P300-ND/P301-ND	Vishay	T-1 3/4, Red LED	1
J2, J3, J4, J6	111-0702-001	Johnson Components	Red, Insulated Thumb Nut Binding Post (Jumped Together)	4
J5	BLM21A102F	Murata	Black, Insulated Thumb Nut Binding Post, GND (Jumped to V_{EE})	1
Q1	459-2598-5-ND	NTE	2N2222A Buffer/Driver Transistor, NPN	1
R1	CRCW04023500F	Vishay	350Ω Resistor, 2%, Size 0402	1
R2	CRCW04026800F	Vishay	680Ω Resistor, 2%, Size 0402	1
R3 - R10	CRCW04021001F	Vishay	1 kΩ Pull-up Resistor, 2%, Size 1206	8
R15, R16, R30, R32	CRCW04021820F	Vishay	182Ω Resistor, 2%, Size 0402	4
R21	CRCW06031300F	Vishay	130Ω Resistor, 2%, Size 0603	1
R22	CRCW04021820F	Vishay	12.1 kΩ Resistor, 2%, Size 1206	1
R23, R24	CRCW04022825F	Vishay	82Ω Resistor, 2%, Size 0402	2
R27	CRCW0402OOR0F	Vishay	0Ω Resistor, 2%, Size 0402	1
R31	CRCW04025000F	Vishay	50Ω Resistor, 2%, Size 0402	1
SMA1 - SMA10	142-0701-851	Johnson Components	End Launch SMA Jack	10
SP1 - SP6	—	—	Solder Jump Option	6
SW1	CT2068-ND	CTS	8-Position, Top Actuated Slide Dip Switch	1
U1	SY87700AL	Microchip	Low-Power 3.3V 28 Mbps to 216 Mbps AnyRate® Clock and Data Recovery	1
U2	SY89322V	Microchip	3.3/5V Dual LVTTL/LVCMOS-to-Differential LVPECL Translator	1

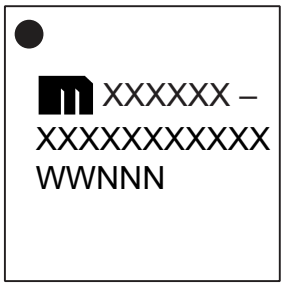
4.0 LAYOUT AND GENERAL SUGGESTIONS

- Establish controlled impedance stripline, microstrip, or coplanar construction techniques.
- Signal paths should have approximately the same width as the device pads.
- All differential paths are critical timing paths, where skew should be matched to within ±10 ps.
- Signal trace impedance should not vary more than ±5%. If in doubt, perform TDR analysis of all high-speed signal traces.
- Maintain compact filter networks as close to filter pins as possible. Provide ground plane relief under filter path to reduce stray capacitance. Be careful of crosstalk coupling into the filter network.
- Maintain low jitter on the REFCLK input. Isolate the XTAL oscillator from power supply noise by adequately decoupling. Keep XTAL oscillator close to device, and minimize capacitive coupling from adjacent signals.
- Higher speed operation may require use of fundamental-tone (third-overtone typically has more jitter) crystal-based oscillator for optimum performance. Evaluate and compare candidates by measuring TXCLK jitter.
- All unused outputs must be terminated. To conserve power, unused PECL outputs can be terminated with a 1 kΩ resistor to V_{EE}.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information

32-Lead TQFP*



Example

Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

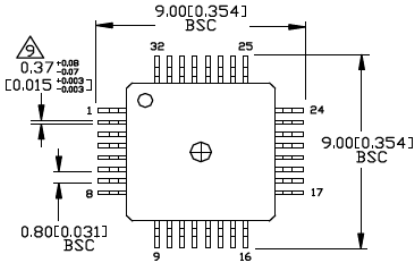
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

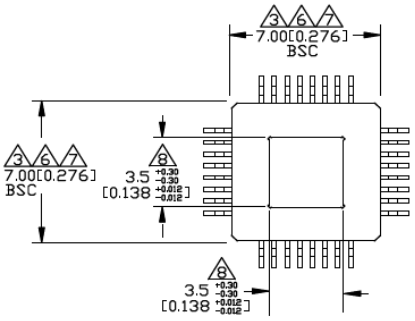
32-Lead TQFP Package Outline and Recommended Land Pattern

TITLE
32 LEAD TQFP 7X7 mm EPAD PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

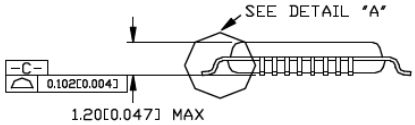
DRAWING #	TQFPEP7X7-32LD-PL-1	UNIT	MM [INCH]



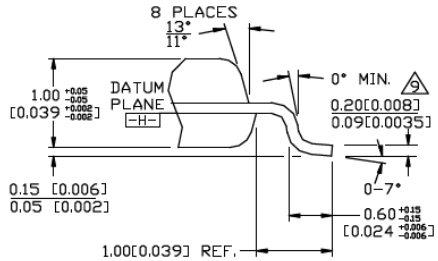
TOP VIEW



BOTTOM VIEW

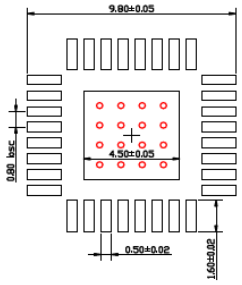


SIDE VIEW



DETAIL "A"

NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
8. EXPOSED PAD SHALL BE COPLANAR WITH PACKAGE BOTTOM WITHIN 0.05mm
EXPOSED PAD: Cu WITH Sn/Pb PLATING
9. DIMENSION INCLUDES LEAD FINISH.
10. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIAS. RECOMMENDED SIZE IS 0.30MM DIAMETER, CONNECT TO GND



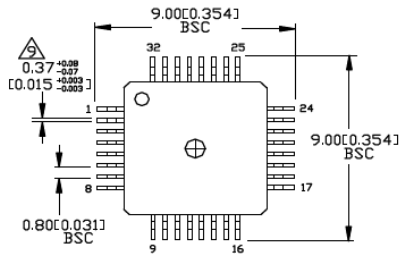
RECOMMENDED LAND PATTERN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

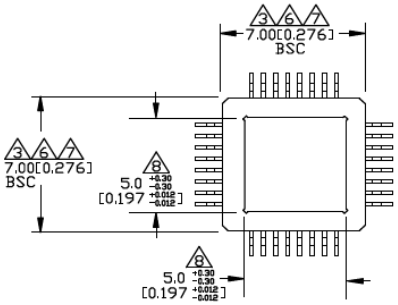
TITLE

32 LEAD TQFP 7X7 mm EPAD PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

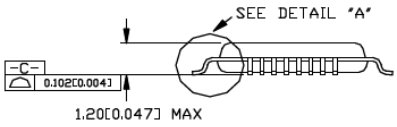
DRAWING #	TQFPEP7X7-32LD-PL-2	UNIT	MM [INCH]
Lead Frame	Copper	Lead Finish	Matte Tin



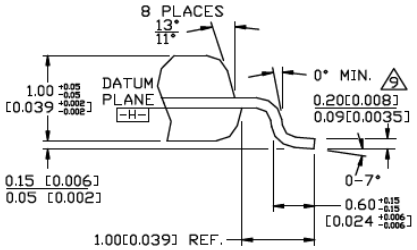
TOP VIEW



BOTTOM VIEW



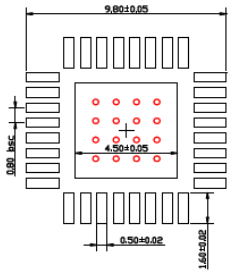
SIDE VIEW



DETAIL "A"

NOTES:

1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.254 [0.010].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN.
6. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H-
7. PACKAGE TOP DIMENSIONS ARE SMALLER THAN BOTTOM DIMENSIONS AND TOP OF PACKAGE WILL NOT OVERHANG BOTTOM OF PACKAGE.
8. EXPOSED PAD SHALL BE COPLANAR WITH PACKAGE BOTTOM WITHIN 0.05mm
   EXPOSED PAD: Cu WITH Sn/Pb PLATING
9. DIMENSION INCLUDES LEAD FINISH.
10. RED CIRCLES IN LAND PATTERN REPRESENT THERMAL VIAS. RECOMMENDED SIZE IS 0.30MM DIAMETER, CONNECT TO GND



RECOMMENDED LAND PATTERN

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (November 2021)

- Converted Micrel document SY87700AL to Microchip data sheet DS20006628A.
- Removed all reference to the EOL'd 28-Lead SOIC package option.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART No.	X	X	X	-XX
Device	Supply Voltage	Package	Temperature Range	Media Type

Device:	SY87700A:	Low-Power, 3.3V, 32 Mbps to 208 Mbps AnyRate® Clock and Data Recovery
Supply Voltage:	L =	3.3V
Package:	H =	32-Lead TQFP
Temperature Range:	G =	–40°C to +85°C
Media Type:	(blank)=	250/Tray
	TR =	1,000/Reel

Examples:

a) SY87700ALHG: SY87700A, 3.3V Supply Voltage, 32-Lead TQFP, –40°C to +85°C Temp. Range, 250/Tray

b) SY87700ALHG-TR: SY87700A, 3.3V Supply Voltage, 32-Lead TQFP, –40°C to +85°C Temp. Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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