SY88053CL/SY88063CL Evaluation Board

1G to 12.5G Limiting Post Amplifiers with Programmable Decision Threshold (053CL) Digital Offset Correction (063CL)

General Description

The SY88053CL/063CL evaluation board enables fast and thorough evaluation of the SY88053CL/063CL limiting amplifiers.

The board is an easy-to-use, single-supply design, driven by a high-speed pattern generator and terminated to a 50Ω scope. The board features simple user adjustability of the LOS threshold, through the adjustment of an on-board potentiometer and different setting options selections using jumpers.

The SY88053CL/063CL are part of Micrel's industry leading family of ultra-small high-speed fiber-optic ICs.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Features

- Multi-rate operation from 1.0625Gbps to 12.5Gbps
- External crosspoint adjustment (053CL)
- Digital offset correction (063CL)
- Wide differential input range ($5mV_{PP}$ to $1800mV_{PP}$)
- Wide SD de-assert or LOS assert threshold range
  - $3mV_{PP}$ to $30mV_{PP}$
  - 4dB typical electrical hysteresis
- Fast SD assert and LOS de-assert times
  - 75ns typical; 120ns maximum
- Selectable LOS or SD status signal indicator
- Selectable RXOUT+/RXOUT– polarity (053CL)
- TTL-compatible JAM input with internal pull-up
- Low-noise CML data inputs with integrated 50Ω termination impedance to internal reference V_{REF}
- Low-noise CML data outputs with integrated 50Ω termination impedance
  - 25ps typical rise/fall times
- Wide range power supply: 3.3V ±10%
- Industrial temp range: –40°C to +85°C
- Available in a tiny 3mm x 3mm QFN package

Applications

- Asymmetrical/Symmetrical 10GEPON and XGPON
- 10G Gigabit Ethernet,
- 8G and 10G Fibre Channel
- SONET OC192; SDH STM64
- WDM/DWDM systems
- OBSAI, CPRI

Markets

- PON/FTTx
- Telecom, datacom/enterprise
- Storage area networks
- High-performance computing
- Wireless

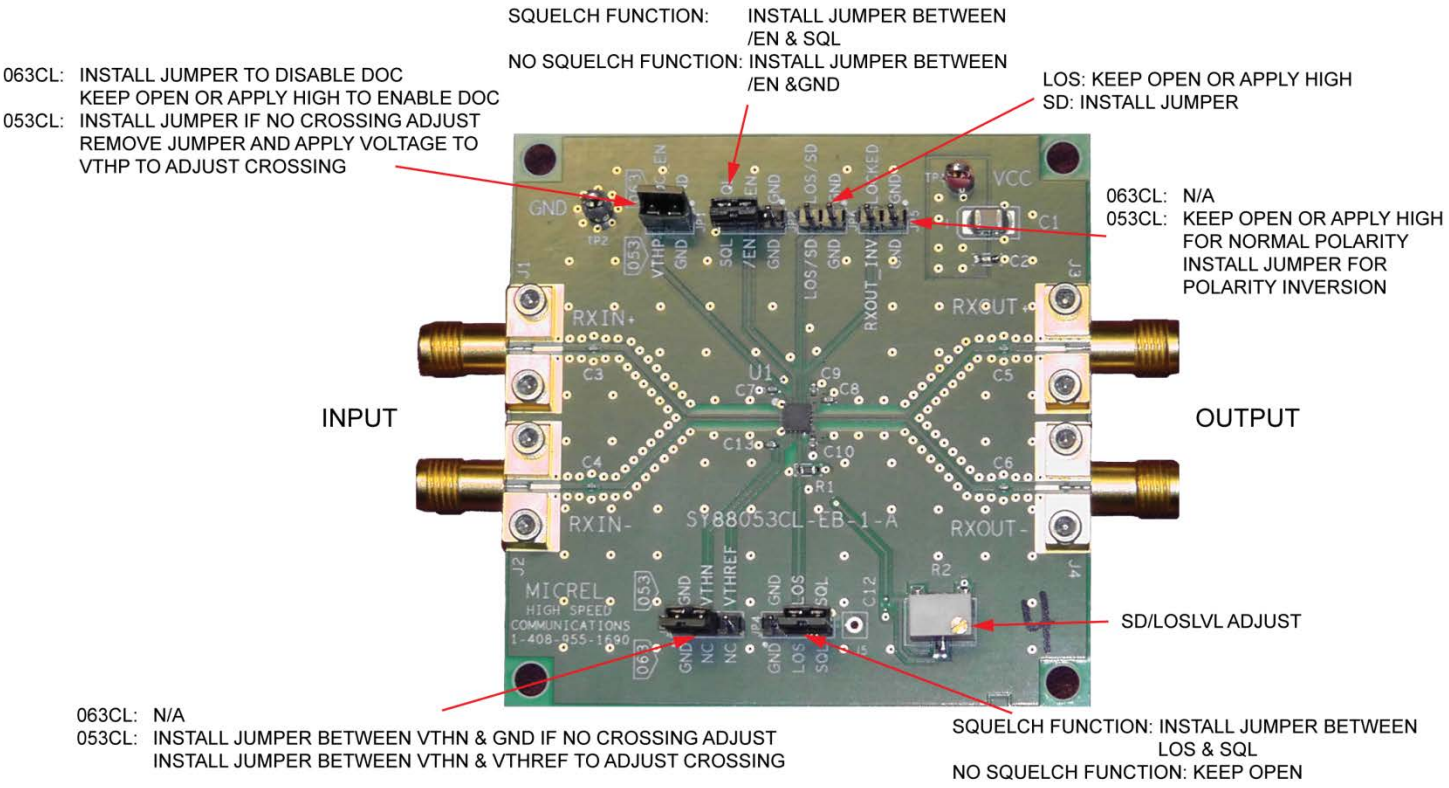
Ordering Information[1]

Ordering Part Number	PCB Revision	Description
SY88053CL-EVAL	SY88053CL-EB-1-A	Evaluation board for 1.0625G to 12.5G Limiting Post Amplifier with Programmable Decision Threshold
SY88063CL-EVAL	SY88053CL-EB-1-A	Evaluation board for 1.0625G to 12.5G Limiting Post Amplifier with Digital Offset Correction

Note:

1. The same evaluation board (SY88053CL-EB-1-A) is used for both SY88053CL and SY88063CL.

Evaluation Board



Evaluation Board Description

The SY88053CL/063CL evaluation board is designed to operate with a single 3.3V ±10% power supply and is configured with AC-coupled inputs and outputs. The high-speed input and output signals are brought out to SMA connectors through matched length AC-coupled differential traces.

AC-Coupled Input

The AC-coupled inputs are internally biased as follows:

For the SY88053CL, the internal 50Ω resistors are terminated to V_{CC} − 1.2V. For the SY88063CL, the internal 50Ω resistors are terminated to V_{CC} − 0.9V.

AC-Coupled Output

The board is configured with AC-coupled outputs to interface directly with 50Ω load equipment inputs. If only one output is used, the unused complementary output must be terminated with 50Ω to ground.

Coupling Capacitors Selection

The coupling capacitor value should be carefully selected, especially when the same circuit is used for multi-rate applications, for instance in 1G/10G or 2.5G/10G PON applications.

The RC time constant created by the capacitor and the input termination resistor can cause a baseline DC droop if the selected capacitor value is too small for the data rate and the data pattern contains long strings of Consecutive Identical Digits (CID). It can also cause pattern dependent jitter if the selected value is too large for the data rate. Choose the coupling capacitor value to get an optimized low-frequency cutoff that minimizes the two problems together.

For 1G/10G or 2.5G/10G application range, 10nF would be a good choice, but be sure to optimize the coupling capacitor value for the specific application.

Measurements

Evaluating RXOUT+ and RXOUT–

1. Set a DC power supply to +3.3V and turn it off.
2. Connect the positive lead to V_{CC} post and the negative lead to GND post.
3. Connect the /EN input to GND (jumper between pin1 and pin 2 of JP2) to enable the RXOUT+ and RXOUT− output buffers.
4. For SY88063CL: Do not install jumpers on JP1 and JP3.
5. For SY88053CL: Connect VTHN and VTHP to GND (install jumper on JP1 and jumper between pins 1 and 2 of JP3) to turn off the crosspoint adjustment or connect VTHN to VTHREF (jumper between pin 2 and pin 3 of JP3) and apply a voltage to VTHP (JP1 open) to adjust the eye crossing (start with a voltage close to VTHREF).
6. Set the desired frequency on a pattern generator with amplitude between 5mV_{PP} and 1800mV_{PP}. Typical data patterns are $2^7 - 1$ or $2^{23} - 1$ PRBS patterns, depending on the application. Because the inputs to the board are AC-coupled, the voltage offset of the pattern generator is not significant and can be set between GND and VCC.
7. Connect the pattern generator with differential outputs as a data source to the RXIN+ and RXIN− inputs on the SY88053CL/063CL evaluation board. Use matched length differential cables.
8. Turn the power supply on.
9. Observe RXOUT+ and RXOUT− outputs on a 50Ω input scope.

Adjusting Crosspoint (053CL)

1. As mentioned in step 5 above, to adjust crosspoint, move the jumper on JP3 to connect VTHN to VTHREF.
2. Remove the jumper from JP1.
3. Apply a 1.25V DC voltage to TP1 and adjust it slightly to set crossing at 50%, higher or lower.

Digital Offset Correction (DOC) (063CL)

The DOC circuit corrects for internal offset and may not be able to fully compensate for offset that external circuits and/or driving devices such TIA may impose at the inputs of the device.

To enable the DOC function in the SY88063CL, leave JP1 open or apply a high signal to DOC_EN (pin 2 of JP1).

To disable the DOC function, install a jumper on JP1.

LOS/SD Timing Measurements

The board comes with 10nF coupling capacitors at the inputs and outputs. To minimize the effect of the input RC time constant on the signal delay from the SMA connectors to the input of the device, the caps must be replace with lower values caps (100pF or lower). This delay may increase the measured LOS/SD assert/de-assert time.

LOS Hysteresis Measurements

The SY88053CL/063CL evaluation board provides a potentiometer (R2) to allow for convenient adjustment of SD/LOSLVL without the need for an extra power supply. SD/LOSLVL taps off a potentiometer connected between V_{CC} and V_{REF}. V_{REF} is an internal reference voltage of approximately V_{CC} − 1.3V. So, SD/LOSLVL can be set to any voltage between V_{CC} and V_{CC} − 1.3V, as specified in the SY88053CL and SY88063CL datasheets. The potentiometer creates a voltage divider. Thus the SD/LOSLVL can be calculated using Equation 1.

$$SD/LOSLVL = V_{CC} - \frac{1.3 \times R}{R + 1.5} \quad \text{Eq. 1}$$

R is the resistance (in kΩ) of the potentiometer from V_{CC} to the tap at SD/LOSLVL. Follow the steps below to measure the LOS/SD hysteresis as a function of the input voltage swing at the RXIN+ and RXIN− inputs.

Minimum Input Swing Hysteresis Measurement

The minimum acceptable BER input swing for the SY88053CL and SY88063CL is $5mV_{PP}$.

1. Set a DC power supply to +3.3V and turn it off. Connect the positive lead to the V_{CC} post and the negative lead to the GND post.
2. Connect the /EN input to GND (jumper between pin 1 and pin 2 of JP2) to enable the RXOUT+ and RXOUT− output buffers.
3. Connect a DMM or similar voltage-measurement device between the LOS_{LVL} pin and V_{CC}.
4. Connect a second DMM, or similar voltage-measurement device between the LOS output and GND. From here on, this DMM will be referred to as the LOS DMM. To use a scope instead of the LOS DMM, move the jumper from /EN-GND to /EN-SQL (from pin 1 and pin 2 to pin 2 and pin 3 of JP2), install a jumper from LOS to SQL (between pin 2 and pin 3 of JP4) to set the squelch function, and observe the output waveform (RXOUT+ and/or RXOUT−) on the scope instead of measuring LOS with DMM.
5. Connect the pattern generator with differential outputs as a data source to RXIN+ and RXIN− inputs on the SY88053CL evaluation board. Use matched length differential cables.
6. Turn the power supply on.
7. Adjust the trim pot R2 so the voltage at the SD/LOSLVL pin is around 1.3V below V_{CC}. This sets the LOS for maximum sensitivity. At this level the LOS output should go high or low (measured with the LOS DMM), as the input voltage swing at RXIN+ and RXIN− is varied up and down around $5mV_{PP}$.
8. Adjust the trim pot to set the sensitivity to a desired level and lower the amplitude of the input signal until LOS is asserted high, then increase the input signal until the LOS de-asserts Low.
9. The hysteresis between the assert and de-assert levels can be calculated using Equation 2:

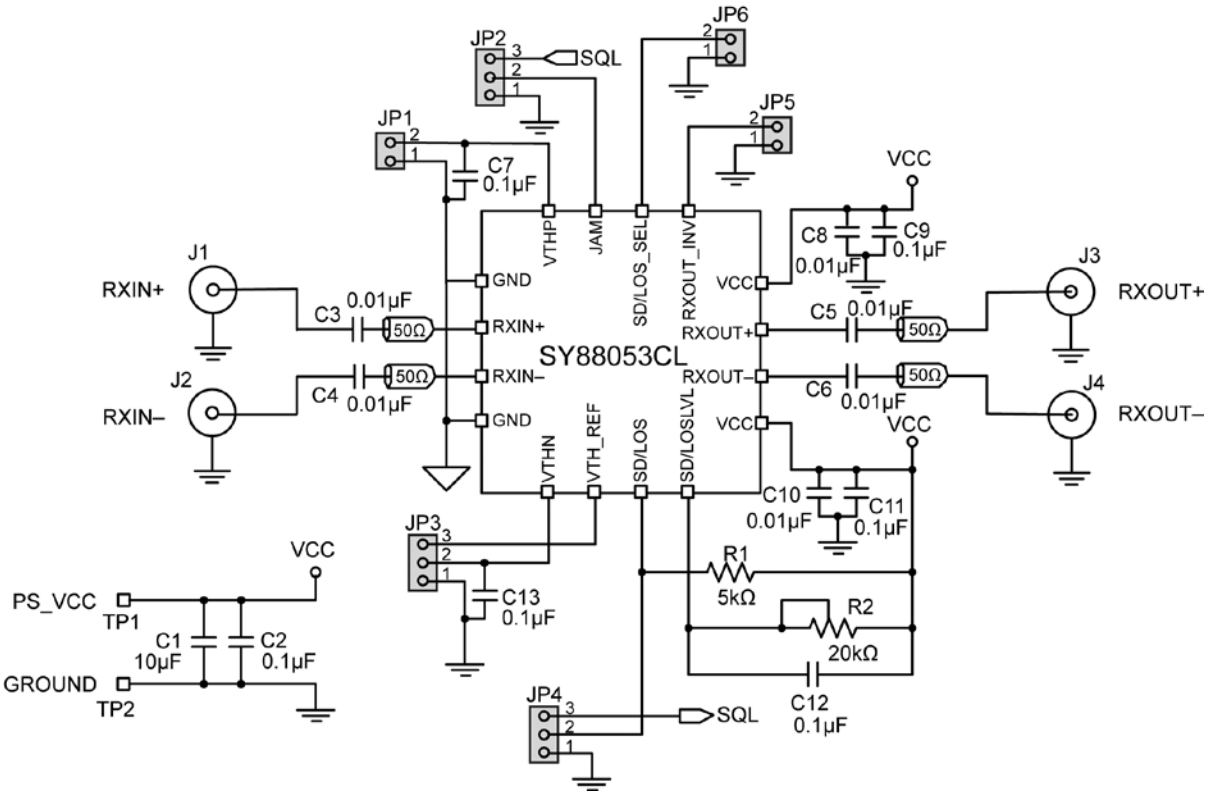
$$Hysteresis(dB) = 20Log\frac{LOS\text{-}D}{LOS\text{-}A} \quad \text{Eq. 2}$$

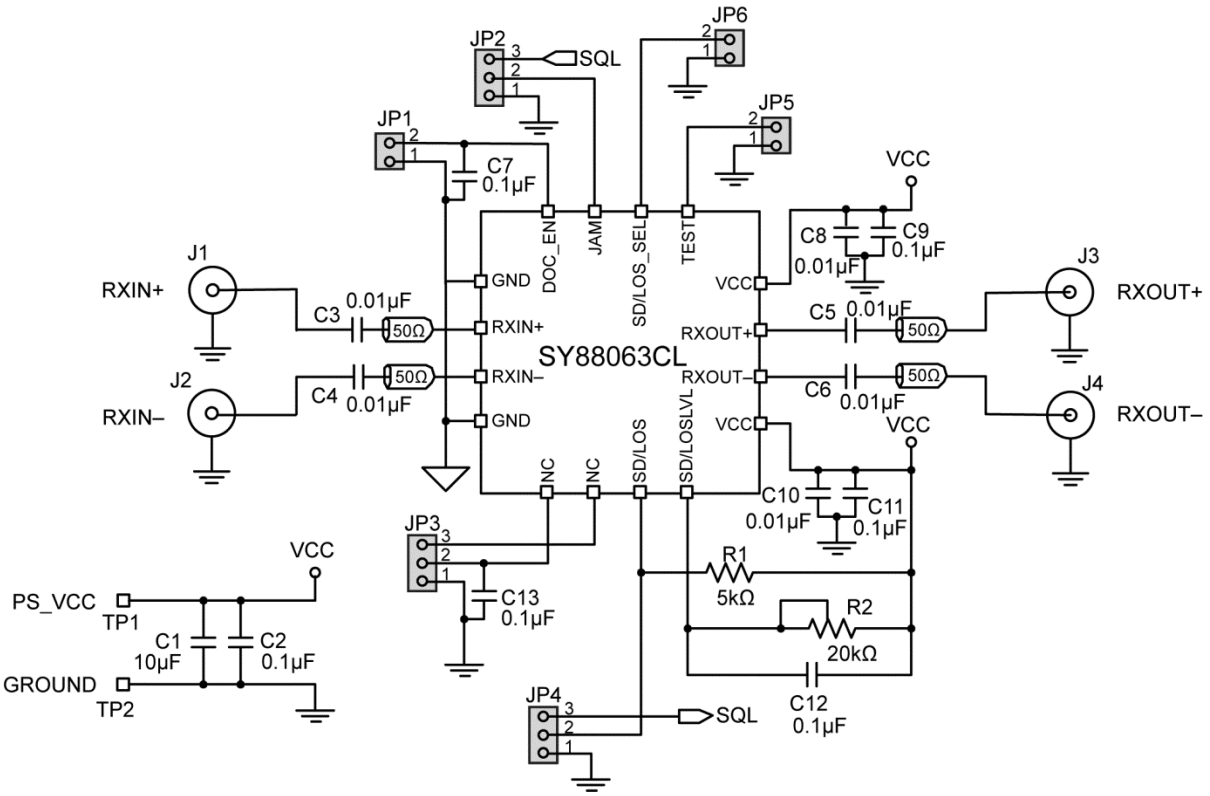
Where:

LOS-D is the LOS de-assert input level and LOS-A is the LOS assert input level.

This hysteresis should be >3dB.

Evaluation Board Schematics[1]





Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C3–6, C8, C10	C1005X7R1C103K050BC	TDK[2]	CAP CER 0.1µF 16V 10% X7R 0402	6
C2, C7, C9, C11–C13	C1005X7R1C104K050BC	TDK	CAP CER 0.1µF 16V 10% X7R 0402	5
C1	C3216X5R0J106K/1.60	TDK	CAP CER 10UF 6.3V 10% X5R 1206	1
JP1–JP6	TSW-103-07-S-S	Samtec[3]	0.1mil Center through hole terminal strip	5
R1	CRCW04025001F	Vishay[4]	5kΩ, 10%, 1/16W Resistor SMD, Size 0402	1
R2	3269W-1-153G	Bourns[5]	20kΩ Trimpot	1
TP2	5011	Keystone[6]	Color Coded PCB test point, Black	1
TP1	5010	Keystone	Color Coded PCB test point, Red	1
J1–J4	32K243-40ML5	Rosenberger[7]	End Launch SMA	4
U1	**SY88053CL/063CL**	**Micrel, Inc.**[8]	**Post Amplifier**	1

Notes:

2. TDK: www.tdk.com.
3. Samtec: www.samtec.com.
4. Vishay: www.vishay.com
5. Bourns, Inc.: www.bourns.com.
6. Keystone Electronics Corp.: www.keyelco.com.
7. Rosenberger: www.rosenberger.com.
8. **Micrel, Inc.:** www.micrel.com.

TCG Support

Hotline: 408-955-1690

Email Support: HBWHelp@micrel.com

Application Hints and Notes

For application notes about high-speed termination on high-bandwidth FOM and clock synthesizer products, SONET jitter measurement, and other TCG products, go to Micrel's website at: http://www.micrel.com.

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