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## Automotive USB Port Power Controller with Charger Emulation

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### Features

- Port Power Switch with Two Current Limit Behaviors
  - 2.9V to 5.5V Source Voltage Range
  - Up to 3.0A Current (2.85A typical) with 55 mΩ on Resistance
  - Overcurrent Trip or Constant Current Limiting
  - Soft Turn-On Circuitry
  - Programmable Current Limit
  - Dynamic Thermal Management
  - Undervoltage and Overvoltage Lockout
  - Back-Drive, Back-Voltage Protection
  - Latch or Auto-Recovery (Low Test Current) Fault Handling
  - Selectable Active-High or Active-Low Power Switch Enable
  - BC1.2 V<sub>BUS</sub> Discharge Port Renegotiation Function
- Selectable/Automatic Cycling of Universal Serial Bus (USB) Data Line Charger Emulation Profiles
  - USB-IF BC1.2 Charging Downstream Port (CDP) and Dedicated Charging Port (DCP) modes, Chinese Telecommunications Industry Standard YD/T 1591-2009 and most Apple<sup>®</sup> Inc. and RIM<sup>®</sup> Protocols Standard; others as defined via the SMBus 2.0/I<sup>2</sup>C Protocol
  - Supports 12W Charging Emulation
  - USB 2.0 Compliant High-Speed Data Switch (in Data Pass-Through, SDP and CDP modes)
  - Nine Preloaded Charger Emulation Profiles for Maximum Compatibility Coverage of the Peripheral Devices
  - One Custom-Programmable Charger Emulation Profile for Portable Device Support for Fully Host-Controlled Charger Emulation
- Supports Active Cables
- Self-Contained Current Monitoring and Rationing for Power-Allocation Applications
- Low-Power Attach Detection and Open-Drain (A\_DET#) Pin
- Ultra Low-Power Sleep State
- Optional Split Supply Support for V<sub>S</sub> and V<sub>DD</sub> for Low-Power in System Standby States
- Wake on Attach USB
- SMBus 2.0/I<sup>2</sup>C Communications
  - Supports Block Write and Read
  - Multiple SMBus Addresses
- Wide Operating Temperature Range: -40°C to +85°C
- IEC61000-4-2 8/15 kV Electrostatic Discharge (ESD) Immunity
- Passes Automotive AEC-Q100 Reliability Testing

### General Description

The UCS81003 provides a USB port power switch for precise control of up to 3.0A continuous current (2.85A typical) with Overcurrent Limit (OCL), dynamic thermal management, latch or auto-recovery (low-test current) fault handling, selectable active-low or active-high enable, undervoltage and overvoltage lockout, back-drive protection and back-voltage protection.

Split supply support for V<sub>S</sub> and V<sub>DD</sub> is an option for low power in system standby states. This gives battery-operated applications (such as on-board computers) the ability to detect attachments from a Sleep or OFF state. After the Attach Detection is flagged, the system can decide to wake-up or provide charging, or both.

In addition to Power Switching and Current Limiting modes, the UCS81003 automatically charges a wide variety of portable devices, including USB-IF BC1.2, YD/T-1591 (2009), most Apple Inc. and RIM, and many others. Nine preloaded charger emulation profiles maximize the compatibility coverage of the peripheral devices. Additionally, a customizable charger emulation profile is available to accommodate unique existing and future portable device handshaking/signature requirements.

The UCS81003 also provides current monitoring to enable intelligent management of system power and charge rationing for controlled delivery of current, regardless of the host power state. This is especially important for battery-operated applications to provide power and not to excessively drain the battery.

The UCS81003 is available in a 5 mm x 5 mm 28-pin VQFN package.

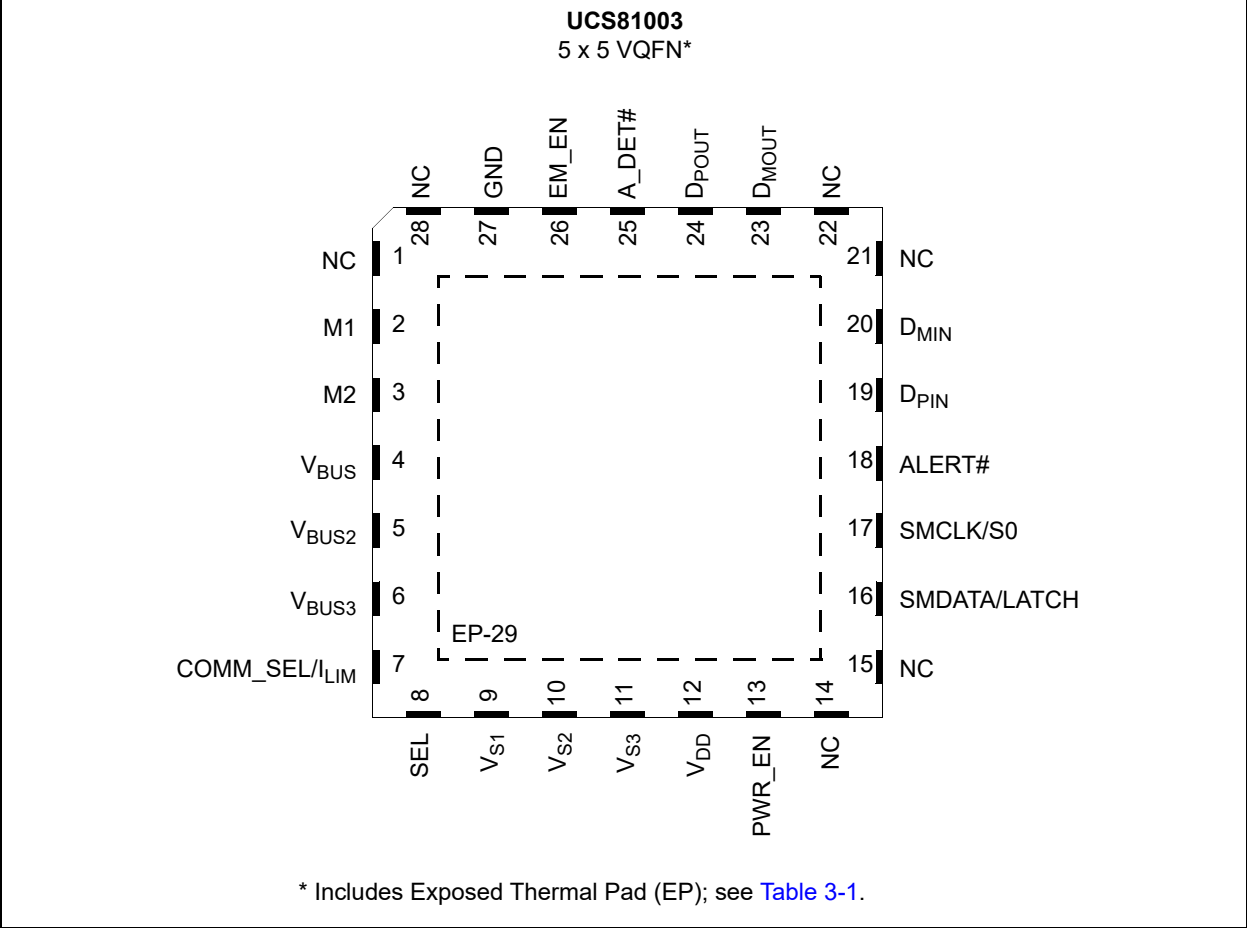
The UCS81003 is AEC-Q100 qualified for automotive applications.

### Applications

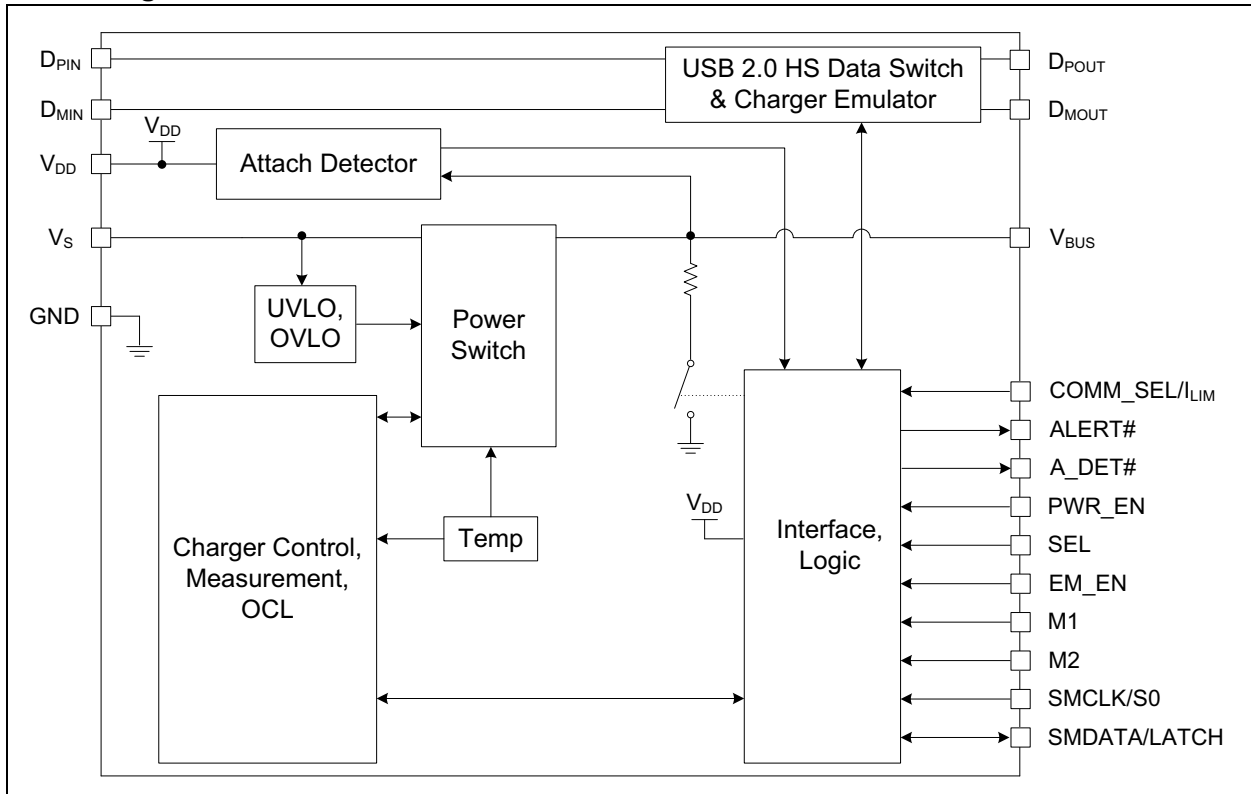
- DC Power Socket Replacement
- Consumer USB Port Protection
- Consumer Device Charging Port
- Auxiliary Box Charging Feature
- Rear Seat Entertainment Consumer Access Point

# UCS81003

## Package Type



## Block Diagram



# UCS81003

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Voltage on $V_{DD}$ , $V_S$ and $V_{BUS}$ pins .....	-0.3 to 6V
Pull-Up Voltage ( $V_{PULLUP}$ ) .....	-0.3 to $V_{DD} + 0.3V$
Data Switch Current ( $I_{HSW\_ON}$ ), Switch On .....	$\pm 50$ mA
Port Power Switch Current .....	Internally limited
Data Switch Pin Voltage To Ground ( $D_{POUT}$ , $D_{PIN}$ , $D_{MOUT}$ , $D_{MIN}$ ); ( $V_{DD}$ powered or unpowered) .....	-0.3 to $V_{DD} + 0.3V$
Differential Voltage Across Open Data Switch ( $D_{POUT} - D_{PIN}$ , $D_{MOUT} - D_{MIN}$ , $D_{PIN} - D_{POUT}$ , $D_{MIN} - D_{MOUT}$ ) .....	$V_{DD}$
Voltage on any Other Pin to Ground .....	-0.3 to $V_{DD} + 0.3V$
Current on any Other Pin .....	$\pm 10$ mA
Package Power Dissipation .....	Table 1-1
Maximum Junction Temperature Under Bias .....	+125°C
Storage Temperature Range .....	-55°C to +150°C

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: POWER DISSIPATION SUMMARY**

Board	Package	$\theta_{JC}$	$\theta_{JA}$	De-rating Factor Above +25°C	$T_A < +25^\circ C$ Power Rating	$T_A < +70^\circ C$ Power Rating	$T_A < +85^\circ C$ Power Rating
High K (see Note 1)	28-pin VQFN 5 x 5 mm	4°C/W	32°C/W	31.3 mW°C	2470 mW	1220 mW	800 mW
Low K (see Note 1)	28-pin VQFN 5 x 5 mm	4°C/W	51°C/W	19.6 mW°C	1620 mW	800 mW	530 mW

**Note 1:** Junction to ambient ( $\theta_{JA}$ ) is dependent on the design of the thermal vias. Without thermal vias and thermal landing, the  $\theta_{JA}$  is approximately 77°C/W, including localized PCB temperature increase. This  $\theta_{JA}$  value is an estimate for a JEDEC® compliant 2S2P PCB with thermal vias.

**TABLE 1-2: ELECTRICAL CHARACTERISTICS**

<b>Electrical Characteristics:</b> Unless otherwise specified, $V_{DD} = 4.5V$ to $5.5V$ , $V_S = 2.9V$ to $5.5V$ , $V_{PULLUP} = 3V$ to $5.5V$ , $T_J = -40^\circ C$ to $+125^\circ C$ ; all Typical values at $V_{DD} = V_S = 5V$ , $T_J = +27^\circ C$ .						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	4.5	5	5.5	V	Note 1
Source Voltage	$V_S$	2.9	5	5.5	V	Note 1
Supply Current in Active ( $I_{DD\_ACTIVE} + I_{VS\_ACT}$ )	$I_{ACTIVE}$	—	650	750	$\mu A$	Average current $I_{BUS} = 0$ mA, $T_J < +85^\circ C$

- Note 1:** For split supply systems using the Attach Detection feature,  $V_S$  must not exceed  $V_{DD} + 150$  mV.
- This parameter is ensured by design and is not 100% tested.
  - This parameter is characterized, but not 100% production tested.
  - The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above  $I_{LIM}$  (if  $I_{BUS\_R2MIN} \leq I_{LIM}$ ) or above  $I_{BUS\_R2MIN}$  (if  $I_{BUS\_R2MIN} > I_{LIM}$  and  $I_{LIM} \leq 1.68A$ ).
  - The minimum and maximum values represent the boundaries of a programmable range. Each value in the range is typical.

**TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)**

<b>Electrical Characteristics:</b> Unless otherwise specified, $V_{DD} = 4.5V$ to $5.5V$ , $V_S = 2.9V$ to $5.5V$ , $V_{PULLUP} = 3V$ to $5.5V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ; all Typical values at $V_{DD} = V_S = 5V$ , $T_J = +27^{\circ}C$ .						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Current in Sleep ( $I_{DD\_SLEEP} + I_{VS\_SLEEP}$ )	$I_{SLEEP}$	—	5	15	$\mu A$	Average current $V_{PULLUP} \leq V_{DD}$ , $T_J < +85^{\circ}C$
Supply Current in Detect ( $I_{DD\_DETECT} + I_{VS\_DETECT}$ )	$I_{DETECT}$	—	175	—	$\mu A$	Average current, no portable device attached
<b>Power-On Reset</b>						
$V_S$ Low Threshold	$V_{S\_UVLO}$	—	2.5	—	V	$V_S$ voltage increasing
$V_S$ Low Hysteresis	$V_{S\_UVLO\_HYST}$	—	100	—	mV	$V_S$ voltage decreasing
$V_{DD}$ Low Threshold	$V_{DD\_TH}$	—	4	—	V	$V_{DD}$ voltage increasing
$V_{DD}$ Low Hysteresis	$V_{DD\_TH\_HYST}$	—	500	—	mV	$V_{DD}$ voltage decreasing
<b>Pins</b>						
<b>I/O Pins – SMCLK, SMDATA, EM_EN, M1, M2, PWR_EN, S0, LATCH, ALERT#, A_DET# – DC Parameters</b>						
Output Low Voltage	$V_{OL}$	—	—	0.4	V	$I_{SINK\_IO} = 8\text{ mA}$ SMDATA, ALERT#, A_DET#
Input High Voltage	$V_{IH}$	2.1	—	—	V	PWR_EN, EM_EN, M1, M2, LATCH, S0, SMDATA, SMCLK
Input Low Voltage	$V_{IL}$	—	—	0.8	V	PWR_EN, EM_EN, M1, M2, LATCH, S0, SMDATA, SMCLK
Leakage Current	$I_{LEAK}$	—	—	$\pm 5$	$\mu A$	Powered or unpowered, $V_{PULLUP} \leq V_{DD}$ , $T_J < +85^{\circ}C$
<b>Interrupt Pins – AC Parameters</b>						
ALERT#, A_DET# Pin Blanking Time	$t_{BLANK}$	—	25	—	ms	
ALERT# Pin Interrupt Masking Time	$t_{MASK}$	—	5	—	ms	
<b>SMBus/I<sup>2</sup>C Timing</b>						
Input Capacitance	$C_{IN}$	—	5	—	pF	
Clock Frequency	$f_{SMB}$	10	—	400	kHz	
Spike Suppression	$t_{SP}$	—	—	50	ns	<a href="#">Note 2</a>
Bus Free Time Stop to Start	$t_{BUF}$	1.3	—	—	$\mu s$	
Start Setup Time	$t_{SU:STA}$	0.6	—	—	$\mu s$	
Start Hold Time	$t_{HD:STA}$	0.6	—	—	$\mu s$	
Stop Setup Time	$t_{SU:STO}$	0.6	—	—	$\mu s$	
Data Hold Time	$t_{HD:DAT}$	0	—	—	$\mu s$	When transmitting to the Master
Data Hold Time	$t_{HD:DAT}$	0.3	—	—	$\mu s$	When receiving from the Master
Data Setup Time	$t_{SU:DAT}$	0.6	—	—	$\mu s$	
Clock Low Period	$t_{LOW}$	1.3	—	—	$\mu s$	

**Note 1:** For split supply systems using the Attach Detection feature,  $V_S$  must not exceed  $V_{DD} + 150\text{ mV}$ .

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# UCS81003

**TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)**

<b>Electrical Characteristics:</b> Unless otherwise specified, $V_{DD} = 4.5V$ to $5.5V$ , $V_S = 2.9V$ to $5.5V$ , $V_{PULLUP} = 3V$ to $5.5V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ; all Typical values at $V_{DD} = V_S = 5V$ , $T_J = +27^{\circ}C$ .						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock High Period	$t_{HIGH}$	0.6	—	—	$\mu s$	
Clock/Data Fall Time	$t_{FALL}$	—	—	300	ns	Min = $20 + 0.1 C_{LOAD}$ ns, <a href="#">Note 3</a>
Clock/Data Rise Time	$t_{RISE}$	—	—	300	ns	Min = $20 + 0.1 C_{LOAD}$ ns, <a href="#">Note 3</a>
Capacitive Load	$C_{LOAD}$	—	—	400	pF	Per bus line, <a href="#">Note 2</a>
Timeout	$t_{TIMEOUT}$	25	—	35	ms	Disabled by default, <a href="#">Note 2</a>
Idle Reset	$t_{IDLE\_RESET}$	350	—	—	$\mu s$	Disabled by default, <a href="#">Note 2</a>
High-Speed Data Switch						
High-Speed Data Switch – DC Parameters						
Switch Leakage Current	$I_{HSW\_OFF}$	—	$\pm 0.5$	—	$\mu A$	Switch open – $D_{PIN}$ to $D_{POUT}$ , $D_{MIN}$ to $D_{MOUT}$ , or all four pins to ground. $V_{DD} \leq V_S$
Charger Resistance	$R_{CHG}$	—	2	—	$M\Omega$	$D_{POUT}$ or $D_{MOUT}$ to $V_{BUS}$ or ground (see <a href="#">Figure 1-2</a> ), BC1.2 DCP charger emulation active
On Resistance	$R_{ON\_HSW}$	—	2	—	$\Omega$	Switch closed, $V_{DD} = 5V$ test current = 8 mA, test voltage = 0.4V, see <a href="#">Figure 1-2</a>
On Resistance	$R_{ON\_HSW\_1}$	—	5	—	$\Omega$	Switch closed, $V_{DD} = 5V$ , test current = 8 mA, test voltage = 3.0V, see <a href="#">Figure 1-2</a>
Delta-On Resistance	$\Delta R_{ON\_HSW}$	—	$\pm 0.3$	—	$\Omega$	Switch closed, $V_{DD} = 5V$ , $I_{TST} = 8$ mA, $V_{TST} = 0$ to 1.5V, see <a href="#">Figure 1-2</a>
High-Speed Data Switch – AC Parameters						
$D_P$ , $D_M$ Capacitance to Ground	$C_{HSW\_ON}$	—	4	—	pF	Switch closed, $V_{DD} = 5V$
$D_P$ , $D_M$ Capacitance to Ground	$C_{HSW\_OFF}$	—	2	—	pF	Switch open, $V_{DD} = 5V$
Turn-Off Time	$t_{HSW\_OFF}$	—	400	—	$\mu s$	Time from state control (EM_EN, M1, M2) switch ON to switch OFF, $R_{TERM} = 50\Omega$ , $C_{LOAD} = 5$ pF
Turn-On Time	$t_{HSW\_ON}$	—	400	—	$\mu s$	Time from state control (EM_EN, M1, M2) switch OFF to switch ON, $R_{TERM} = 50\Omega$ , $C_{LOAD} = 5$ pF

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Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Propagation Delay	$t_{PD}$	—	0.25	—	ns	$R_{TERM} = 50\Omega$ , $C_{LOAD} = 5$ pF
Propagation Delay Skew	$\Delta t_{PD}$	—	25	—	ps	$R_{TERM} = 50\Omega$ , $C_{LOAD} = 5$ pF
Rise/Fall Time	$t_{F/R}$	—	10	—	ns	$R_{TERM} = 50\Omega$ , $C_{LOAD} = 5$ pF
$D_P - D_M$ Crosstalk	$X_{TALK}$	—	-40	—	dB	$R_{TERM} = 50\Omega$ , $C_{LOAD} = 5$ pF
Off Isolation	$O_{IRR}$	—	-30	—	dB	$R_{TERM} = 50\Omega$ , $C_{LOAD} = 5$ pF, $f = 240$ MHz
-3 dB Bandwidth	BW	—	1100	—	MHz	$R_{TERM} = 50\Omega$ , $C_{LOAD} = 5$ pF, $V_{DPOUT} = V_{DMOUT} = 350$ mV DC
Total Jitter	$t_J$	—	200	—	ps	$R_{TERM} = 50\Omega$ , $C_{LOAD} = 5$ pF, Rise Time = Fall Time = 500 ps at 480 Mbps (PRBS = $2^{15} - 1$ )
Skew of Opposite Transitions of the Same Output	$t_{SK(P)}$	—	20	—	ps	$R_{TERM} = 50\Omega$ , $C_{LOAD} = 5$ pF
Port Power Switch						
Port Power Switch – DC Parameters						
Overvoltage Lockout	$V_{S\_OV}$	—	6	—	V	
On Resistance	$R_{ON\_PSW}$	—	55	—	m $\Omega$	$4.75V < V_S < 5.25V$
$V_S$ Leakage Current	$I_{LEAK\_VS}$	—	2.22	—	$\mu A$	Sleep state into $V_S$ pin
Back-Voltage Protection Threshold	$V_{BV\_TH}$	—	150	—	mV	$V_{BUS} > V_S$ , $V_S > V_{S\_UVLO}$
Back-Drive Current	$I_{BD\_1}$	—	0	3	$\mu A$	$V_{DD} < V_{DD\_TH}$ , Any powered power pin to any unpowered power pin. Current out of unpowered pin (Note 3).
	$I_{BD\_2}$	—	0	2	$\mu A$	$V_{DD} < V_{DD\_TH}$ , Any powered power pin to any unpowered power pin, except for $V_{DD}$ to $V_{BUS}$ in Detect power state and $V_S$ to $V_{BUS}$ in Active power state. Current out of unpowered pin (Note 3).

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Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Selectable Current Limits	$I_{LIM1}$	—	570	—	mA	$I_{LIM}$ Resistor = 0 or 47 k $\Omega$ (minimum mA setting)
	$I_{LIM2}$	—	1000	—		$I_{LIM}$ Resistor = 10 k $\Omega$ or 56 k $\Omega$
	$I_{LIM3}$	—	1130	—		$I_{LIM}$ Resistor = 12 k $\Omega$ or 68 k $\Omega$
	$I_{LIM4}$	—	1350	—		$I_{LIM}$ Resistor = 15 k $\Omega$ or 82 k $\Omega$
	$I_{LIM5}$	—	1680	—		$I_{LIM}$ Resistor = 18 k $\Omega$ or 100 k $\Omega$
	$I_{LIM6}$	—	2050	—		$I_{LIM}$ Resistor = 22 k $\Omega$ or 120 k $\Omega$
	$I_{LIM7}$	—	2280	—		$I_{LIM}$ Resistor = 27 k $\Omega$ or 150 k $\Omega$
	$I_{LIM8}$	—	2850	3000		$I_{LIM}$ Resistor = 33 k $\Omega$ or $V_{DD}$
Pin Wake Time	$t_{PIN\_WAKE}$	—	3	—	ms	
SMBus Wake Time	$t_{SMB\_WAKE}$	—	4	—	ms	
Idle Sleep Time	$t_{IDLE\_SLEEP}$	—	200	—	ms	
Thermal Regulation Limit	$T_{REG}$	—	110	—	$^{\circ}C$	Die Temperature at which current limit is reduced.
Thermal Regulation Hysteresis	$T_{REG\_HYST}$	—	10	—	$^{\circ}C$	Hysteresis for $t_{REG}$ functionality. Temperature must drop by this value before $I_{LIM}$ value restored to normal operation.
Thermal Shutdown Threshold	$T_{TSD}$	—	135	—	$^{\circ}C$	Die Temperature at which port power switch turns OFF.
Thermal Shutdown Hysteresis	$T_{TSD\_HYST}$	—	35	—	$^{\circ}C$	After shutdown due to $T_{TSD}$ being reached, a die temperature drop is required before port power switch can be turned ON again.
Auto-Recovery Test Current	$I_{TEST}$	—	190	—	mA	Portable device attached, $V_{BUS} = 0V$ , Die Temp < $T_{TSD}$
Auto-Recovery Test Voltage	$V_{TEST}$	—	750	—	mV	Portable device attached, $V_{BUS} = 0V$ before application, Die Temp < $T_{TSD}$ Programmable, 250-1000 mV, default listed
Discharge Impedance	$R_{DISCHARGE}$	—	100	—	$\Omega$	

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**TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)**

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Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>Port Power Switch – AC Parameters</b>						
Turn-On Delay	$t_{ON\_PSW}$	—	0.75	—	ms	PWR_EN active toggle to switch on time, $V_{BUS}$ discharge not active.
Turn-Off Time	$t_{OFF\_PSW\_INA}$	—	0.75	—	ms	PWR_EN inactive toggle to switch off time $C_{BUS} = 120 \mu F$
Turn-Off Time	$t_{OFF\_PSW\_ERR}$	—	1	—	ms	Overcurrent Error, $V_{BUS}$ Min Error, or Discharge Error to switch off, $C_{BUS} = 120 \mu F$
Turn-Off Time	$t_{OFF\_PSW\_ERR}$	—	100	—	ns	TSD or back-drive error to switch off, $C_{BUS} = 120 \mu F$
$V_{BUS}$ Output Rise Time	$t_{R\_BUS}$	—	1.1	—	ms	Measured from 10% to 90% of $V_{BUS}$ , $C_{LOAD} = 220 \mu F$ , $I_{LIM} = 1.0A$
Soft Turn-On Rate	$\Delta I_{BUS}/\Delta t$	—	100	—	mA/ $\mu s$	
Temperature Update Time	$t_{DC\_TEMP}$	—	200	—	ms	Programmable 200-1600 ms, default listed
Short-Circuit Response Time	$t_{SHORT\_LIM}$	—	1.5	—	$\mu s$	Time from detection of short to current limit applied. No $C_{BUS}$ applied.
Short-Circuit Detection Time	$t_{SHORT}$	—	6	—	ms	Time from detection of short to port power switch disconnect and ALERT# pin assertion.
Latched Mode Cycle Time	$t_{UL}$	—	7	—	ms	From PWR_EN edge transition from inactive to active to begin error recovery.
Auto-Recovery Mode Cycle Time	$t_{CYCLE}$	—	25	—	ms	Time delay before error condition check. Programmable 10-25 ms, default listed.
Auto-Recovery Delay	$t_{RST}$	—	20	—	ms	Portable device attached, $V_{BUS}$ must be $\geq V_{TEST}$ after this time. Programmable 10-25 ms, default listed.
Discharge Time	$t_{DISCHARGE}$	—	200	—	ms	Amount of time discharge resistor applied. Programmable 100-400 ms, default listed.

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- 3:** This parameter is characterized, but not 100% production tested.
- 4:** The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above  $I_{LIM}$  (if  $I_{BUS\_R2MIN} \leq I_{LIM}$ ) or above  $I_{BUS\_R2MIN}$  (if  $I_{BUS\_R2MIN} > I_{LIM}$  and  $I_{LIM} \leq 1.68A$ ).
- 5:** The minimum and maximum values represent the boundaries of a programmable range. Each value in the range is typical.

# UCS81003

**TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)**

<b>Electrical Characteristics:</b> Unless otherwise specified, $V_{DD} = 4.5V$ to $5.5V$ , $V_S = 2.9V$ to $5.5V$ , $V_{PULLUP} = 3V$ to $5.5V$ , $T_J = -40^{\circ}C$ to $+125^{\circ}C$ ; all Typical values at $V_{DD} = V_S = 5V$ , $T_J = +27^{\circ}C$ .						
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>Port Power Switch Operation With Trip Mode Current Limiting</b>						
Region 2 Current Keep-Out	$I_{BUS\_R2MIN}$	—	0.12	—	A	
Minimum $V_{BUS}$ ed at Output	$V_{BUS\_MIN}$	1.5	2.0	2.25	V	Note 5
<b>Port Power Switch Operation with Constant Current Limiting (Variable Slope)</b>						
Region 2 Current Keep-Out	$I_{BUS\_R2MIN}$	—	1.68	—	A	
Minimum $V_{BUS}$ Allowed at Output	$V_{BUS\_MIN}$	1.5	2.0	2.25	V	Note 5
<b>Current Measurement</b>						
<b>Current Measurement – DC Parameters</b>						
Current Measurement Range	$I_{BUS\_M}$	0	—	2988.6	mA	Range 0-255 LSB (see Note 4)
Reported Current Measurement Resolution	$D_{IBUS\_M}$	—	11.72	—	mA	1 LSB
Current Measurement Accuracy	—	—	$\pm 2$	—	%	$180\text{ mA} < I_{BUS} < I_{LIM}$
		—	$\pm 2$	—	LSB	$I_{BUS} < 180\text{ mA}$
<b>Current Measurement – AC Parameter</b>						
Sampling Rate	—	—	500	—	$\mu s$	
<b>Charge Rationing</b>						
<b>Charge Rationing – DC Parameters</b>						
Accumulated Current Measurement Accuracy	—	—	$\pm 4.5$	—	%	
<b>Charge Rationing – AC Parameter</b>						
Current Measurement Update Time	$t_{PCYCLE}$	—	1	—	s	
<b>Attach/Removal Detection</b>						
<b><math>V_{BUS}</math> Bypass – DC Parameters</b>						
On Resistance	$R_{ON\_BYP}$	—	50	—	$\Omega$	
Leakage Current	$I_{LEAK\_BYP}$	—	—	3	$\mu A$	Switch off, $T_A < +85^{\circ}C$ , Note 2
Current Limit	$I_{DET\_CHG}/I_{BUS\_BYP}$	—	2	—	mA	$V_{DD} = 5V$ and $V_{BUS} > 4.75V$
<b>Attach/Removal Detection – DC Parameters</b>						
Attach Detection Threshold	$I_{DET\_QUAL}$	—	800	—	$\mu A$	Programmable 200-1000 $\mu A$ , default listed.

- Note 1:** For split supply systems using the Attach Detection feature,  $V_S$  must not exceed  $V_{DD} + 150\text{ mV}$ .
- 2:** This parameter is ensured by design and is not 100% tested.
- 3:** This parameter is characterized, but not 100% production tested.
- 4:** The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above  $I_{LIM}$  (if  $I_{BUS\_R2MIN} \leq I_{LIM}$ ) or above  $I_{BUS\_R2MIN}$  (if  $I_{BUS\_R2MIN} > I_{LIM}$  and  $I_{LIM} \leq 1.68A$ ).
- 5:** The minimum and maximum values represent the boundaries of a programmable range. Each value in the range is typical.

**TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)**

**Electrical Characteristics:** Unless otherwise specified,  $V_{DD} = 4.5V$  to  $5.5V$ ,  $V_S = 2.9V$  to  $5.5V$ ,  $V_{PULLUP} = 3V$  to  $5.5V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ ; all Typical values at  $V_{DD} = V_S = 5V$ ,  $T_J = +27^{\circ}C$ .

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Primary Removal Detection Threshold	$I_{REM\_QUAL\_ACT}$	—	700	—	$\mu A$	Programmable 100-900 $\mu A$ , default listed, Active power state
		—	800	—	$\mu A$	Programmable 200-1000 $\mu A$ , default listed, Detect power state (see <a href="#">Section 8.4</a> "Removal Detection").
<b>Attach/Removal Detection – AC Parameters</b>						
Attach Detection Time	$t_{DET\_QUAL}$	—	100	—	ms	Time from Attach to A_DET# assert
Removal Detection Time	$t_{REM\_QUAL}$	—	1000	—	ms	
Allowed Charge Time	$t_{DE-T\_CHARGE}$	—	800	—	ms	$C_{BUS} = 500 \mu F$ maximum, Programmable 200-2000 ms, default listed.
<b>Charger Emulation Profile</b>						
<b>General Emulation – DC Parameters</b>						
Charging Current Threshold	$I_{BUS\_CHG}$	—	175.8	—	mA	Default
Charging Current Threshold Range	$I_{BUS\_CHG\_RNG}$	11.72	—	175.8	mA	<a href="#">Note 5</a>
DP-DM Shunt Resistor Value	$R_{DCP\_RES}$		—	200	$\Omega$	Connected between $D_{P\_OUT}$ and $D_{M\_OUT}$ , $0V < D_{P\_OUT} = D_{M\_OUT} < 3V$
Response Magnitude (voltage divider option resistance range)	$SX\_RXMAG\_DVDR$	93	—	200	$k\Omega$	<a href="#">Note 5</a>
Resistor Ratio Range (voltage divider option)	$SX\_RATIO$	0.25	—	0.66	V/V	<a href="#">Note 5</a>
Resistor Ratio Accuracy (voltage divider option)	$SX\_RATIO\_ACC$	—	$\pm 0.5$	—	%	Average over range
Response Magnitude (resistor option range)	$SX\_RXMAG\_RES$	1.8	—	150	$k\Omega$	<a href="#">Note 5</a>
Internal Resistor Tolerance (resistor option)	$SX\_RXMAG\_RES\_ACC$	—	$\pm 10$	—	%	Average over range
Response Magnitude (voltage option range)	$SX\_RXMAG\_VOLT$	0.4	—	2.2	V	<a href="#">Note 5</a>
Voltage Option Accuracy	$SX\_RXMAG\_VOLT\_ACC$	—	$\pm 1$	—	%	No load, average over range
Voltage Option Accuracy	$SX\_RXMAG\_VOLT\_ACC_{150}$	—	-6	—	%	150 $\mu A$ load, average over range
Voltage Option Accuracy	$SX\_RXMAG\_VOLT\_ACC_{250}$	—	-10	—	%	250 $\mu A$ load, average over range

- Note 1:** For split supply systems using the Attach Detection feature,  $V_S$  must not exceed  $V_{DD} + 150$  mV.
- Note 2:** This parameter is ensured by design and is not 100% tested.
- Note 3:** This parameter is characterized, but not 100% production tested.
- Note 4:** The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above  $I_{LIM}$  (if  $I_{BUS\_R2MIN} \leq I_{LIM}$ ) or above  $I_{BUS\_R2MIN}$  (if  $I_{BUS\_R2MIN} > I_{LIM}$  and  $I_{LIM} \leq 1.68A$ ).
- Note 5:** The minimum and maximum values represent the boundaries of a programmable range. Each value in the range is typical.

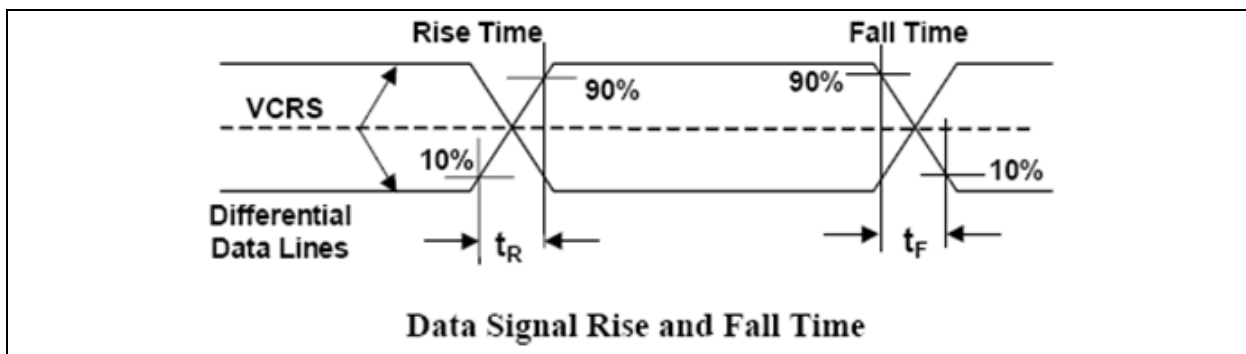
# UCS81003

**TABLE 1-2: ELECTRICAL CHARACTERISTICS (CONTINUED)**

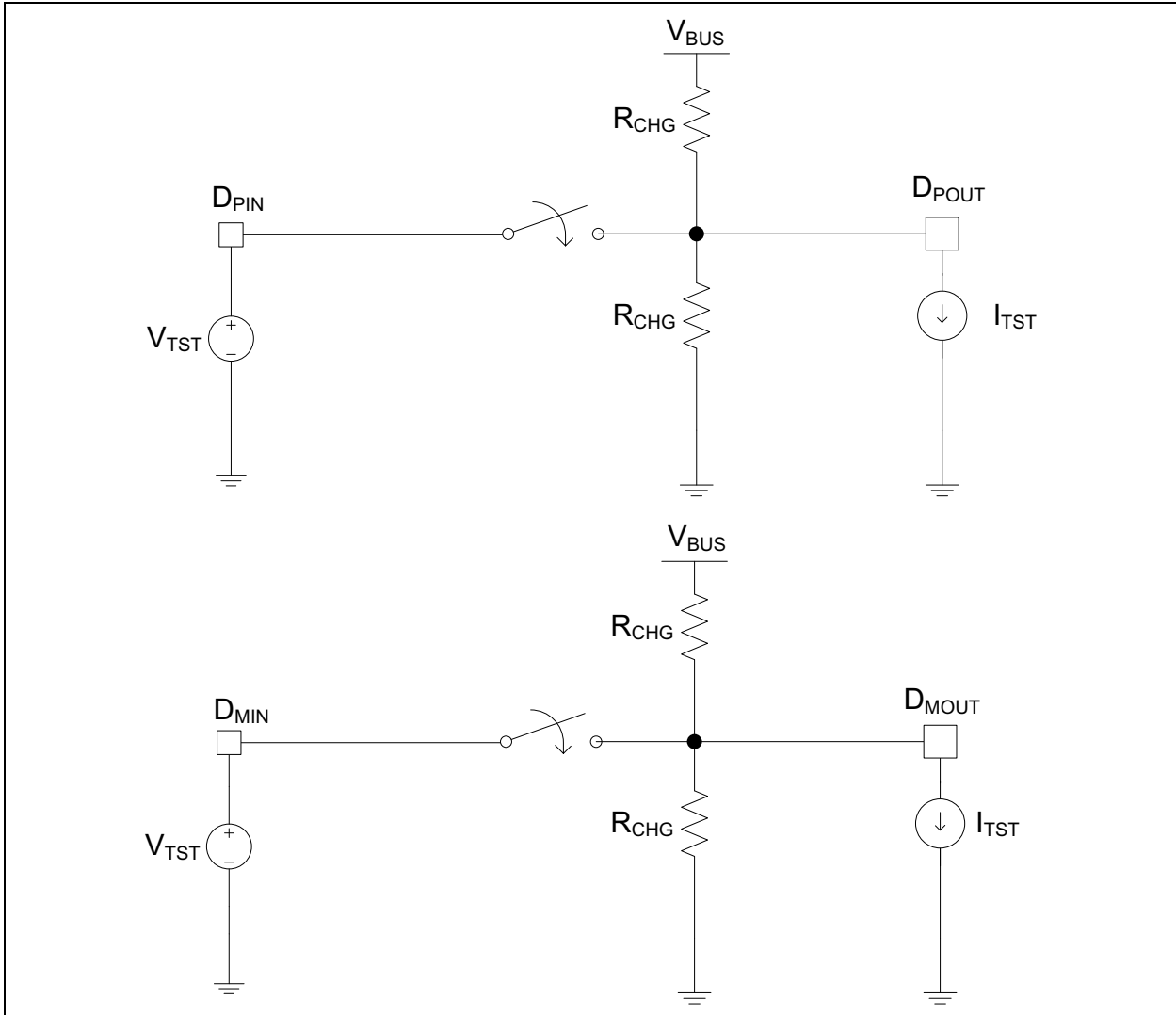
**Electrical Characteristics:** Unless otherwise specified,  $V_{DD} = 4.5V$  to  $5.5V$ ,  $V_S = 2.9V$  to  $5.5V$ ,  $V_{PULLUP} = 3V$  to  $5.5V$ ,  $T_J = -40^{\circ}C$  to  $+125^{\circ}C$ ; all Typical values at  $V_{DD} = V_S = 5V$ ,  $T_J = +27^{\circ}C$ .

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Voltage Option Output	SX_RXMAG_VOLT_BC	0.5	—	—	V	$D_{MOUT} = 0.6V$ , 250 $\mu A$ load, <a href="#">Note 3</a>
Response Magnitude (Zero Volt Option Range)	SX_PUPD	10	—	150	$\mu A$	$SX\_RXMAG\_VOLT = 0$ <a href="#">Note 5</a>
Pull-Down Current Accuracy	SX_PUPD_ACC_3p6	—	$\pm 5$	—	%	$D_{POUT}$ or $D_{MOUT} = 3.6V$ Compliance voltage
Pull-Down Current	SX_PUPD_ACC_BC	50	—	—	$\mu A$	Setting = 100 $\mu A$ $D_{POUT}$ or $D_{MOUT} = 0.15V$ Compliance voltage, <a href="#">Note 3</a>
Stimulus Voltage Threshold Range	SX_TH	0.3	—	2.2	V	<a href="#">Note 5</a>
Stimulus Voltage Accuracy	SX_TH_ACC	—	$\pm 2$	—	%	Average over range
Stimulus Voltage Accuracy	SX_TH_ACC_BC	0.25	—	—	V	At $SX\_TH = 0.3V$ , <a href="#">Note 3</a>
<b>General Emulation – AC Parameters</b>						
Emulation Reset Time	$t_{EM\_RESET}$	—	50	—	ms	Default
Emulation Reset Time Range	$t_{EM\_RESET\_RNG}$	50	—	175	ms	<a href="#">Note 5</a>
Emulation Timeout Range	$t_{EM\_TIMEOUT}$	0.8	—	12.8	s	<a href="#">Note 5</a>
Stimulus Delay, SX_TD Range	$t_{STIM\_DEL}$	0	—	100	ms	<a href="#">Note 5</a>
Emulation Delay	$t_{RES\_EM}$	—	—	0.5	s	Time from set impedance to impedance appears on $D_P/D_M$ , <a href="#">Note 3</a> .

- Note 1:** For split supply systems using the Attach Detection feature,  $V_S$  must not exceed  $V_{DD} + 150$  mV.
- Note 2:** This parameter is ensured by design and is not 100% tested.
- Note 3:** This parameter is characterized, but not 100% production tested.
- Note 4:** The current measurement full-scale range maximum value is 3.0A. However, the UCS81003 cannot report values above  $I_{LIM}$  (if  $I_{BUS\_R2MIN} \leq I_{LIM}$ ) or above  $I_{BUS\_R2MIN}$  (if  $I_{BUS\_R2MIN} > I_{LIM}$  and  $I_{LIM} \leq 1.68A$ ).
- Note 5:** The minimum and maximum values represent the boundaries of a programmable range. Each value in the range is typical.



**FIGURE 1-1:** USB Rise Time/Fall Time Measurement.



**FIGURE 1-2:** Description of DC Terms.

**TABLE 1-3: TEMPERATURE SPECIFICATIONS**

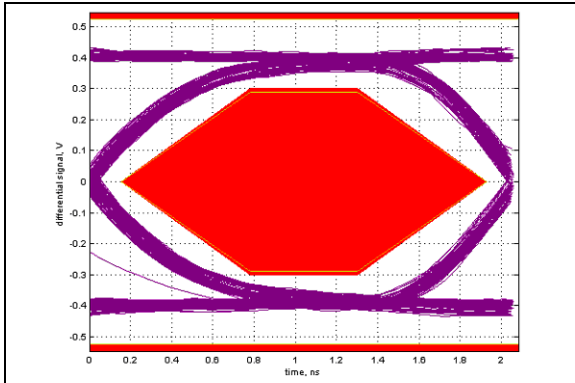
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
<b>Temperature Ranges</b>						
Operating Temperature Range	$T_A$	-40	—	+85	°C	
Storage Temperature Range	$T_A$	-55	—	+150	°C	
<b>Thermal Package Resistances – see Table 1-1</b>						

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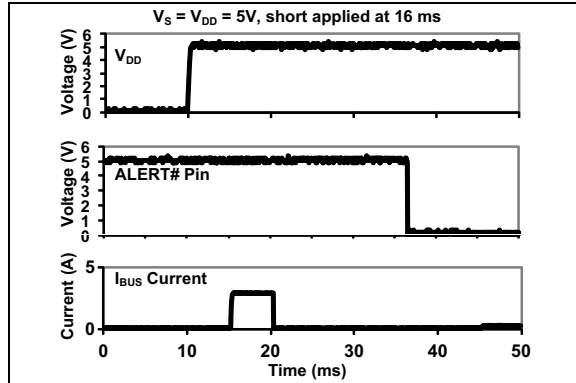
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (for example, outside specified power supply range) and therefore outside the warranted range.

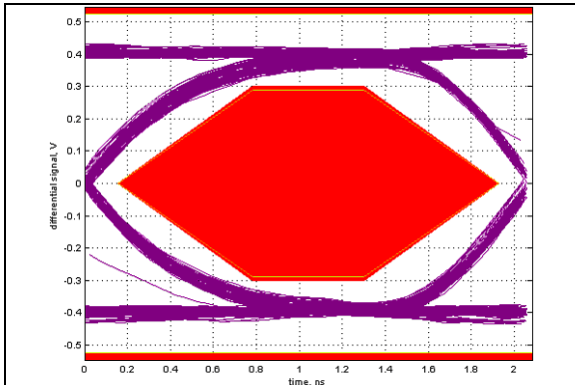
**Note:** Unless otherwise indicated,  $V_{DD} = V_S = 5V$ ,  $T_J = +27^\circ C$ .



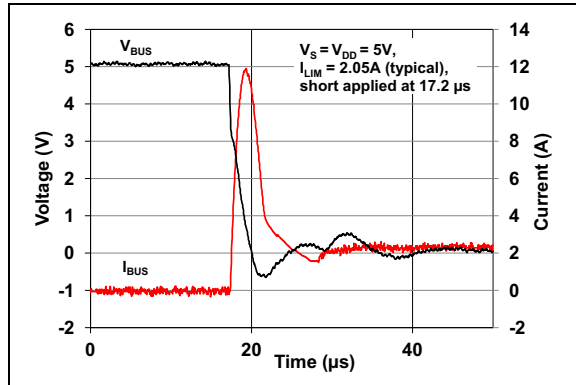
**FIGURE 2-1:** USB-IF High-Speed Eye Diagram (Without Data Switch).



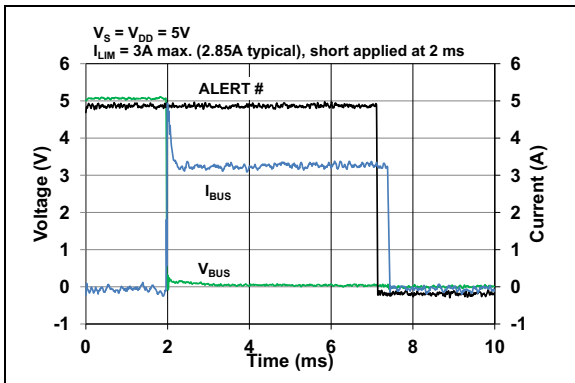
**FIGURE 2-4:** Power-Up Into a Short.



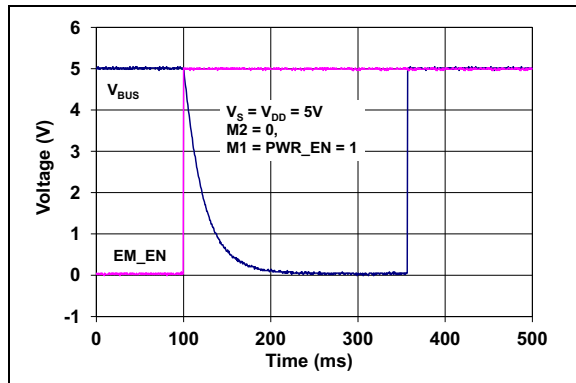
**FIGURE 2-2:** USB-IF High-Speed Eye Diagram (With Data Switch).



**FIGURE 2-5:** Internal Power Switch Short Response.

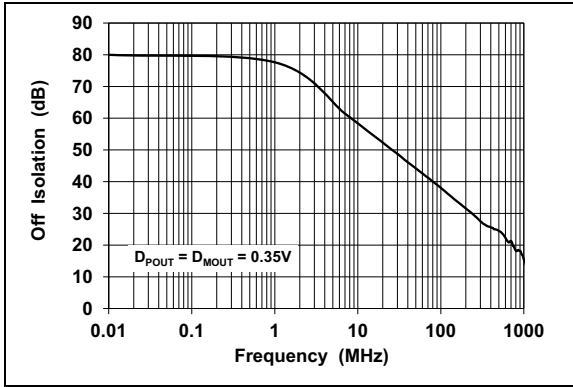


**FIGURE 2-3:** Short Applied After Power-Up.

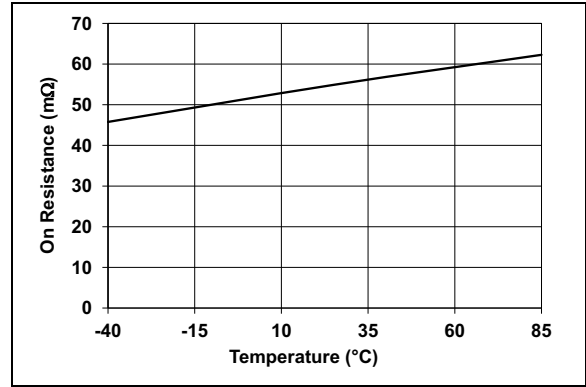


**FIGURE 2-6:**  $V_{BUS}$  Discharge Behavior.

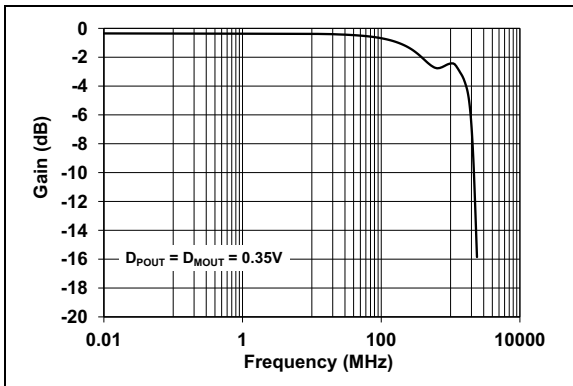
**Note:** Unless otherwise indicated,  $V_{DD} = V_S = 5V$ ,  $T_J = +27^\circ C$ .



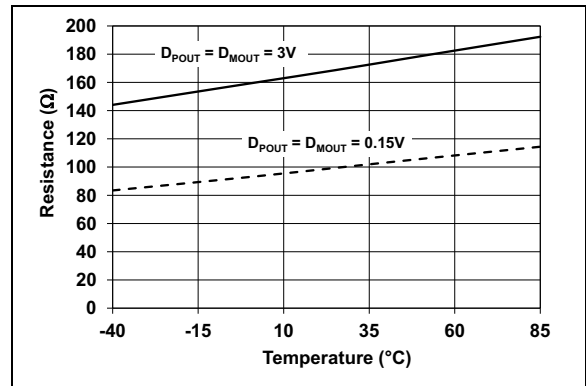
**FIGURE 2-7:** Data Switch Off Isolation vs. Frequency.



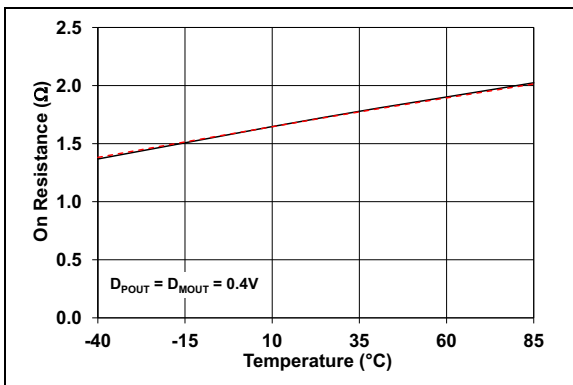
**FIGURE 2-10:** Power Switch On Resistance vs. Temperature.



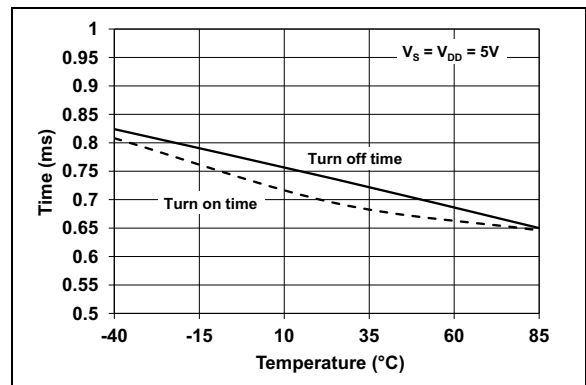
**FIGURE 2-8:** Data Switch Bandwidth vs. Frequency.



**FIGURE 2-11:**  $R_{DCP\_RES}$  Resistance vs. Temperature.



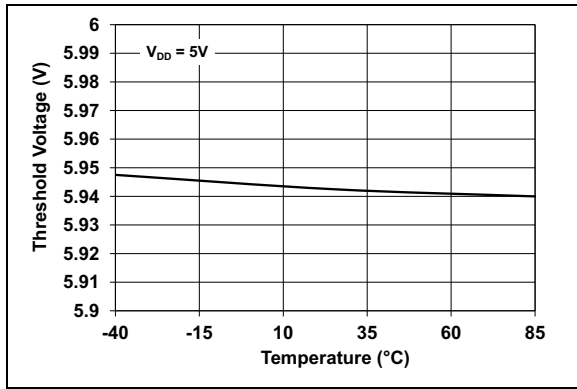
**FIGURE 2-9:** Data Switch On Resistance vs. Temperature.



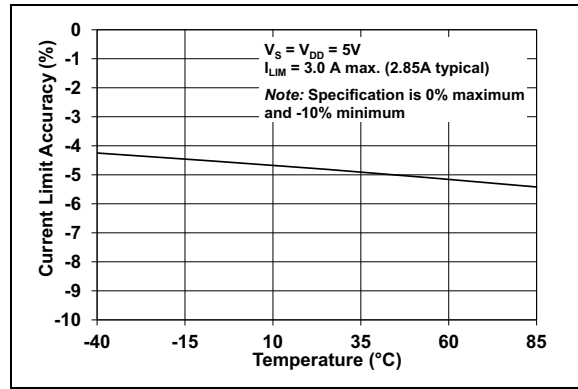
**FIGURE 2-12:** Power Switch On/Off Time vs. Temperature.

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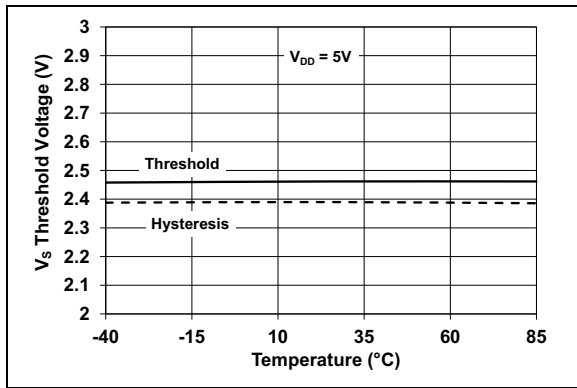
Note: Unless otherwise indicated,  $V_{DD} = V_S = 5V$ ,  $T_J = +27^\circ C$ .



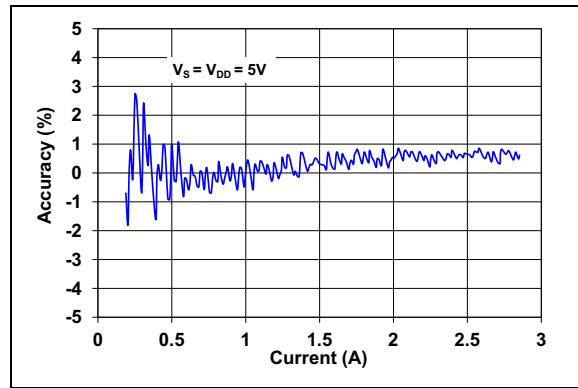
**FIGURE 2-13:**  $V_S$  Overvoltage Threshold vs. Temperature.



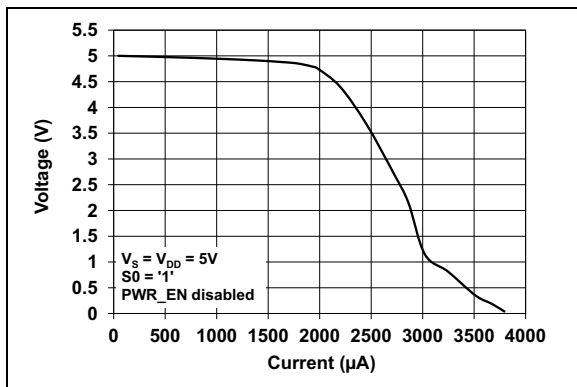
**FIGURE 2-16:** Trip Current Limit Operation vs. Temperature.



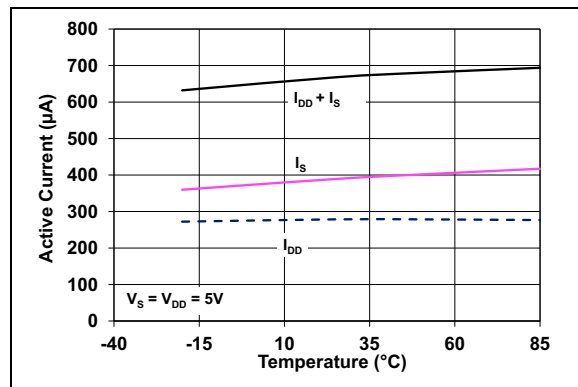
**FIGURE 2-14:**  $V_S$  Undervoltage Threshold vs. Temperature.



**FIGURE 2-17:**  $I_{BUS}$  Measurement Accuracy.



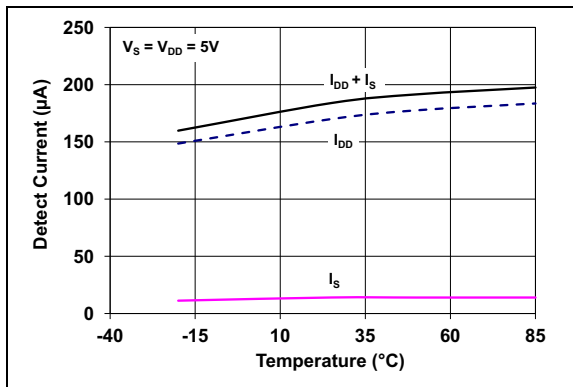
**FIGURE 2-15:** Detect State  $V_{BUS}$  vs.  $I_{BUS}$ .



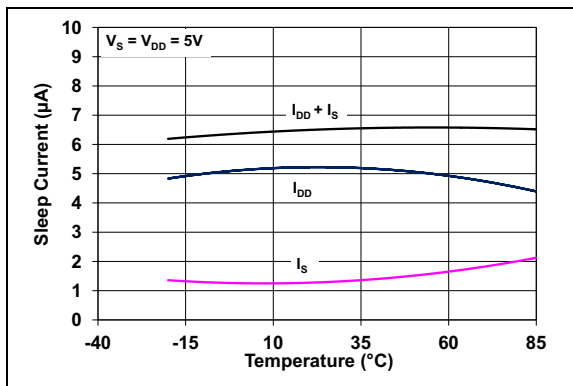
**FIGURE 2-18:** Active State Current vs. Temperature.



**Note:** Unless otherwise indicated,  $V_{DD} = V_S = 5V$ ,  $T_J = +27^\circ C$ .



**FIGURE 2-19:** Detect State Current vs. Temperature.



**FIGURE 2-20:** Sleep State Current vs. Temperature.

### 3.0 PIN DESCRIPTION

The function of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

UCS81003 5x5 VQFN	Symbol	Function	Pin Type	Connection Type if Pin Not Used
1	NC	Not internally connected	n/a	Leave open
2	M1	Active mode selector input #1	DI	Connect to ground or $V_{DD}$ (see <a href="#">Note 3</a> )
3	M2	Active mode selector input #2	DI	Connect to ground or $V_{DD}$ (see <a href="#">Note 3</a> )
4	$V_{BUS1}$	Voltage output from Power Switch	Hi-Power <a href="#">Note 1</a>	Leave open
5	$V_{BUS2}$	These pins are internally connected and must be tied together.		
6	$V_{BUS3}$			
7	COMM_SEL/ $I_{LIM}$	<b>COMM_SEL</b> – selects SMBus or Stand-Alone mode of operation (see <a href="#">Table 11-1</a> ). <b><math>I_{LIM}</math></b> – selects the hardware current limit at power-up.	AIO	n/a
8	SEL	Selects polarity of PWR_EN control and SMBus address (see <a href="#">Table 11-2</a> ).	AIO	n/a
9	$V_{S1}$	Voltage input to Power Switch. These pins are internally connected and must be tied together.	Hi-Power	Connect to ground
10	$V_{S2}$			
11	$V_{S3}$			
12	$V_{DD}$	Main power supply input for chip functionality	Power	n/a
13	PWR_EN	Port power switch enable input. Polarity is determined by SEL pin.	DI	Connect to ground or $V_{DD}$ (see <a href="#">Note 3</a> )
14	NC	Not internally connected	n/a	Leave open
15	NC	Not internally connected	n/a	Leave open

- Note 1:** Total leakage current from pins 4, 5 and 6 ( $V_{BUS}$ ) to ground must be less than 100  $\mu$ A for proper attach/removal detection operation.
- 2:** It is recommended to use 2 M $\Omega$  pull-down resistors on the  $D_{POUT}$  or  $D_{MOUT}$  pin, or both if a portable device stimulus is expected when using the Customer Charger Emulation profile with the high-speed data switch open. The 2 M $\Omega$  value is based on BC1.1 impedance characteristics for Dedicated Charging Ports.
- 3:** To ensure operation, the PWR\_EN pin must be enabled, as determined by the SEL pin decode, when it is not driven by an external device. Furthermore, one of the M1, M2 or EM\_EN pins must be connected to  $V_{DD}$  if all three are not driven from an external device. If the PWR\_EN pin is disabled or all of the M1, M2, and EM\_EN pins are connected to ground, the UCS81003 remains in the Sleep or Detect state unless activated via the SMBus.

TABLE 3-1: PIN FUNCTION TABLE

UCS81003 5x5 VQFN	Symbol	Function	Pin Type	Connection Type if Pin Not Used
16	SMDATA/LATCH	<b>SMDATA</b> - SMBus data input/output (requires pull-up resistor)	DIOD	n/a
		<b>LATCH</b> - In Stand-Alone mode, Latch/Auto-Recovery Fault Handling mechanism selection input (see <a href="#">Section 7.5 “Fault Handling Mechanism”</a> )	DI	
17	SMCLK/S0	<b>SMCLK</b> - SMBus Clock Input (requires pull-up resistor)	DI	n/a
		<b>S0</b> - In Stand-Alone mode, enables Attach/Removal Detection feature (see <a href="#">Section 5.3.6 “S0 Input”</a> )		
18	ALERT#	Active-low error event output flag (requires pull-up resistor)	OD	Connect to ground
19	D <sub>PIN</sub>	USB data input (plus)	AIO	Connect to ground or ground through a resistor
20	D <sub>MIN</sub>	USB data input (minus)	AIO	Connect to ground or ground through a resistor
21	NC	Not internally connected	n/a	Leave open
22	NC	Not internally connected	n/a	Leave open
23	D <sub>MOU</sub> T	USB data output (minus)	AIO (see <a href="#">Note 2</a> )	Connect to ground
24	D <sub>POU</sub> T	USB data output (plus)	AIO (see <a href="#">Note 2</a> )	Connect to ground
25	A_DET#	Active-low device Attach Detection output flag (requires pull-up resistor)	OD	Connect to ground
26	EM_EN	Active mode selector input	DI	Connect to ground or V <sub>DD</sub> (see <a href="#">Note 3</a> )
27	GND	Ground	Power	n/a
28	NC	Not internally connected	n/a	Leave open
29	EP	Exposed Thermal Pad. Must be connected to the electrical ground.	EP	n/a

- Note 1:** Total leakage current from pins 4, 5 and 6 (V<sub>BUS</sub>) to ground must be less than 100  $\mu$ A for proper attach/removal detection operation.
- 2:** It is recommended to use 2 M $\Omega$  pull-down resistors on the D<sub>POU</sub>T or D<sub>MOU</sub>T pin, or both if a portable device stimulus is expected when using the Customer Charger Emulation profile with the high-speed data switch open. The 2 M $\Omega$  value is based on BC1.1 impedance characteristics for Dedicated Charging Ports.
- 3:** To ensure operation, the PWR\_EN pin must be enabled, as determined by the SEL pin decode, when it is not driven by an external device. Furthermore, one of the M1, M2 or EM\_EN pins must be connected to V<sub>DD</sub> if all three are not driven from an external device. If the PWR\_EN pin is disabled or all of the M1, M2, and EM\_EN pins are connected to ground, the UCS81003 remains in the Sleep or Detect state unless activated via the SMBus.

# UCS81003

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The description of the pin types are listed in [Table 3-2](#).

**TABLE 3-2: PIN TYPES DESCRIPTION**

Pin Type	Description
Power	This pin is used to supply power or ground to the device
Hi-Power	This pin is a high-current pin
AIO	<b>Analog Input/Output</b> – this pin is used as an I/O for analog signals.
DI	<b>Digital Input</b> – this pin is used as a digital input. This pin is glitch-free.
DIOD	<b>Open-Drain Digital Input/Output</b> – this pin is bidirectional. It is open-drain and requires a pull-up resistor. This pin is glitch-free.
OD	<b>Open-Drain Digital Output</b> – used as a digital output. It is open-drain and requires a pull-up resistor. This pin is glitch-free.
EP	Exposed Thermal Pad

## 4.0 TERMS AND ABBREVIATIONS

**Note:** The M1, M2, PWR\_EN and EM\_EN pins each have configuration bits (<pin name>\_SET in [Section 10.4.3 “Switch Configuration Register”](#)) that may be used to perform the same function as the external pin state. These bits are accessed via the SMBus/I<sup>2</sup>C and are OR'd with the respective pin. This OR'd combination of pin state and register bit is referenced as the <pin name> control.

**TABLE 4-1: TERMS AND ABBREVIATIONS**

Term/Abbreviation	Description
Active mode	Active power state operation mode: Data Pass-Through, BC1.2 SDP, BC1.2 CDP, BC1.2 DCP or Dedicated Charger Emulation Cycle.
Attach Detection	An Attach Detection event occurs when the current drawn by a portable device is greater than $I_{DET\_QUAL}$ for longer than $t_{DET\_QUAL}$ .
Attachment	The physical insertion of a portable device into a USB port that UCS81003 is controlling.
CC	Constant Current
CDM	Charged Device Model. JEDEC <sup>®</sup> model for characterizing susceptibility of a device to damage from ESD.
CDP or USB-IF BC1.2 CDP	Charging Downstream Port. The combination of the UCS81003 CDP handshake and an active standard USB host comprises a CDP. This enables a BC1.2 compliant portable device to simultaneously draw current up to 1.5A while data communication is active. The USB high-speed data switch is closed in this mode.
Charge Enable	When a charger emulation profile is accepted by a portable device and charging commences.
Charger Emulation Profile	Representation of a charger comprised of $D_{POUT}$ , $D_{MOUT}$ and $V_{BUS}$ signaling which makes a defined set of signatures or handshaking protocols.
Connection	USB-IF term which refers to establishing active USB communications between a USB host and a USB device.
Current Limiting Mode	Determines the action that is performed when the $I_{BUS}$ current reaches the $I_{LIM}$ threshold. Trip opens the port power switch. Constant Current (variable slope) enables $V_{BUS}$ to be dropped by the portable device.
DCE	Dedicated Charger Emulation. Charger emulation in which the UCS81003 can deliver power only (by default). No active USB data communication is possible when charging in this mode (by default).
DCP or USB-IF BC1.2 DCP	Dedicated Charging Port. This functions as a dedicated charger for a BC1.2 portable device. This enables the portable device to draw currents up to 1.5A with Constant Current Limiting (and beyond 1.5A with Trip Current Limiting). By default, no USB communications are possible.
DC	Dedicated Charger. A charger which inherently does not have USB communications such as an A/C wall adapter.
Disconnection	USB-IF term which refers to the loss of active USB communications between a USB host and a USB device.
Dynamic Thermal Management	The UCS81003 automatically adjusts port power switch limits and modes to lower internal power dissipation when the thermal regulation temperature value is approached.
Enumeration	A USB-specific term indicating that a host is detecting and identifying USB devices.
Handshake	Application of a charger emulation profile that requires a response. Two-way communication between the UCS81003 and the portable device.
HBM	Human Body Model
HSW	High-Speed Switch
$I_{BUS\_R2MIN}$	Current limiter mode boundary
$I_{LIM}$	The $I_{BUS}$ current threshold used in current limiting. In Trip mode, when $I_{LIM}$ is reached, the port power switch is opened. In Constant Current mode, when the current exceeds $I_{LIM}$ , operation continues at a reduced voltage and increased current; if $V_{BUS}$ voltage drops below $V_{BUS\_MIN}$ , the port power switch is opened.

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**TABLE 4-1: TERMS AND ABBREVIATIONS (CONTINUED)**

Term/Abbreviation	Description
Legacy	USB devices that require non-BC1.2 signatures must be applied on the D <sub>POUT</sub> and D <sub>MOUT</sub> pins to enable charging.
OCL	Overcurrent Limit
POR	Power-On Reset
Portable Device	USB device attached to the USB port.
Power Thief	A USB device that does not follow the handshaking conventions of a BC1.2 device or Legacy devices and draws current immediately upon receiving power (that is, a USB book light, portable fan, and so on).
Removal Detection	A Removal Detection event occurs when the current load on the V <sub>BUS</sub> pin drops to less than I <sub>REM_QUAL</sub> for longer than t <sub>REM_QUAL</sub> .
Removal	The physical removal of a portable device from a USB port controlled by the UCS81003.
Response	An action, usually in response to a stimulus, in charger emulation performed by the UCS81003 device via the USB data lines.
SDP or USB-IF SDP	Standard Downstream Port. The combination of the UCS81003 high-speed switch being closed with an upstream USB host present comprises a BC1.2 SDP. This enables a BC1.2 compliant portable device to simultaneously draw current up to 0.5A while data communication is active.
Signature	Application of a charger emulation profile without waiting for a response. One-way communication from the UCS81003 to the portable device.
Stand-Alone Mode	Indicates that the communications protocol is not active and all communications between the UCS81003 and a controller are done via the external pins only (M1, M2, EM_EN, PWR_EN, S0 and LATCH as inputs; ALERT# and A_DET# as outputs).
Stimulus	An event in charger emulation detected by the UCS81003 device via the USB data lines.

## 5.0 GENERAL DESCRIPTION

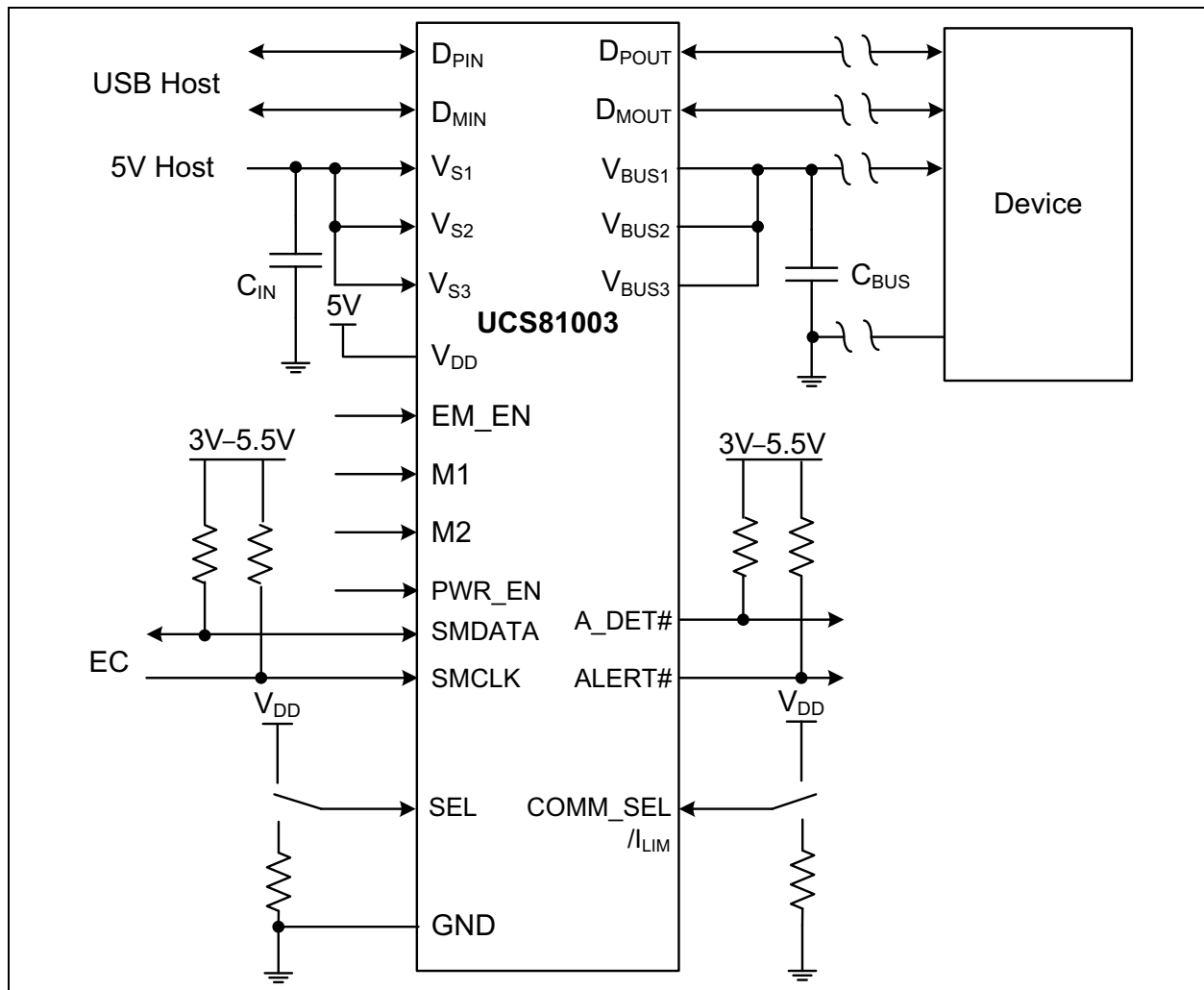
The UCS81003 provides a single USB port power switch for precise control of up to 3.0A continuous current with Overcurrent Limit (OCL), dynamic thermal management, latch or auto-recovery fault handling, selectable active-low or active-high enable, undervoltage and overvoltage lockout, and back-voltage protection.

Split supply support for  $V_{BUS}$  and  $V_{DD}$  is an option for low power in system standby states.

In addition to power switching and current limiting, the UCS81003 provides automatic and configurable charger emulation profiles to charge a wide variety of portable devices, including USB-IF BC1.2 (CDP or DCP modes), YD/T-1591 (2009), 12W charging, most Apple and RIM portable devices and many others.

The UCS81003 also provides current monitoring to enable intelligent management of system power and charge rationing for controlled delivery of current regardless of the host power state. This is especially important for battery-operated applications that must provide power without excessively draining the battery, or require power allocation depending on application activities.

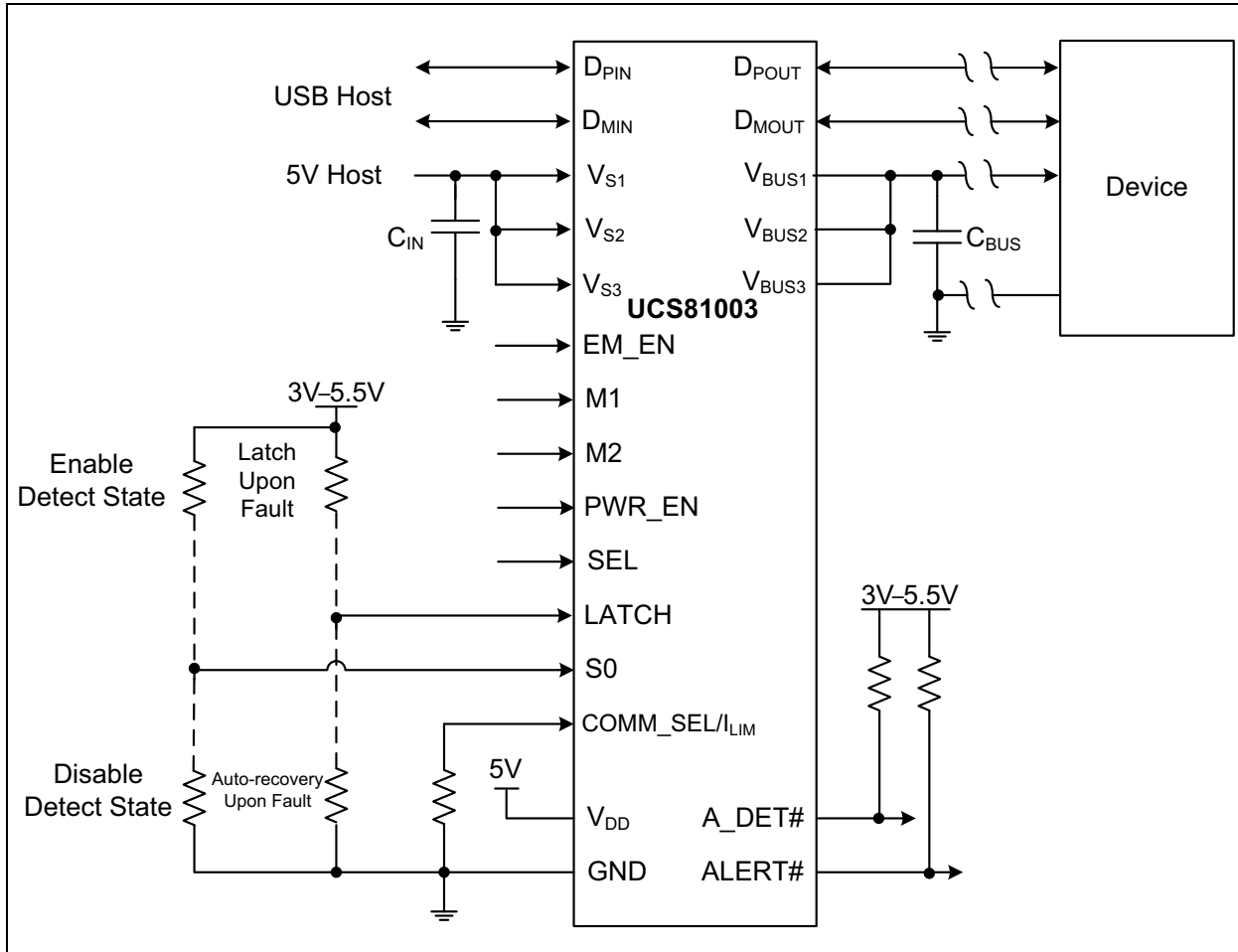
Figure 5-1 shows a UCS81003 full-featured system configuration in which the UCS81003 provides a port power switch and low-power Attach Detection with wake-up signaling (wake on USB). The current limit is established at power-up. It can be lowered if required after power-up via the SMBus/I<sup>2</sup>C. This configuration also provides configurable USB data line-charger emulation, programmable current limiting (as determined by the accepted charger emulation profile), active current monitoring, and port charge rationing.



**FIGURE 5-1:** UCS81003 System Configuration (with Charger Emulation, SMBus Control and USB Host).

# UCS81003

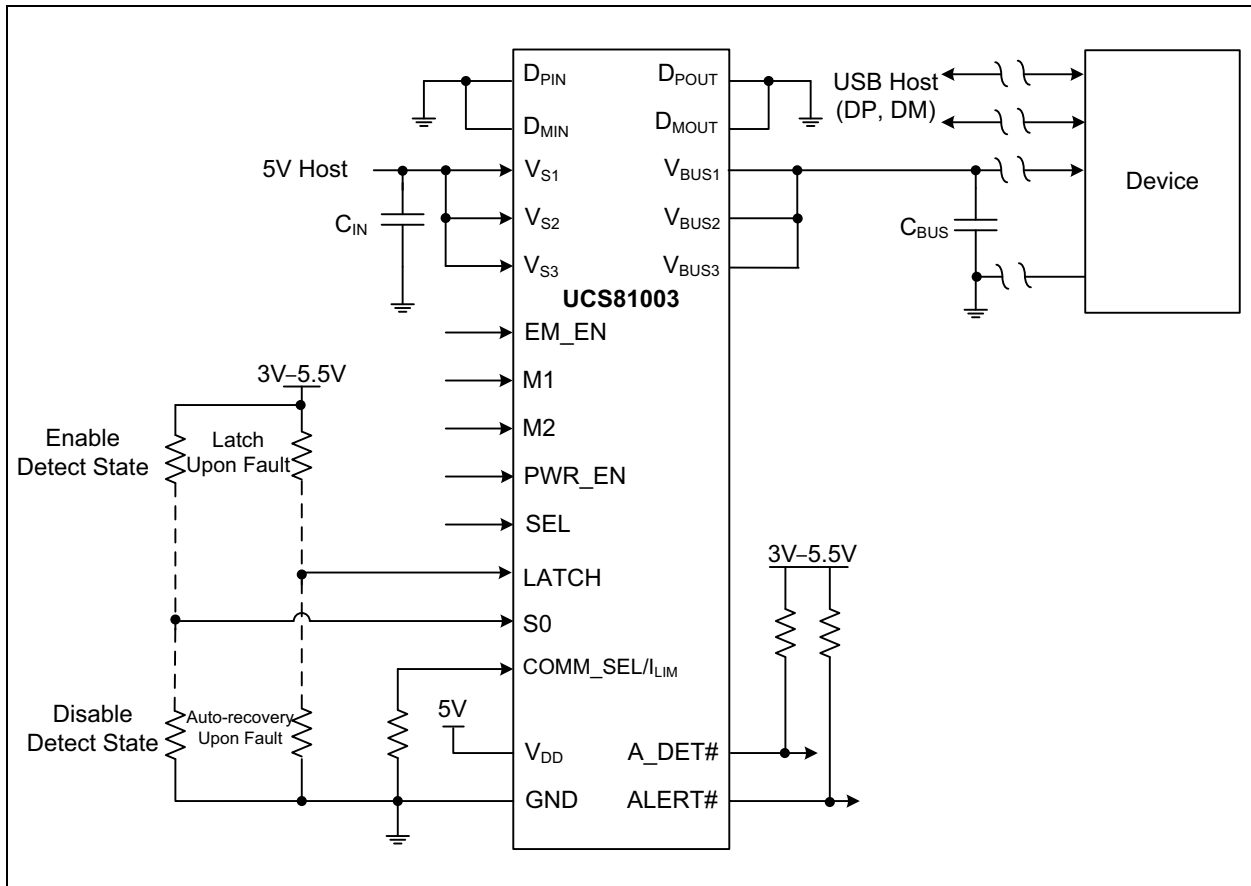
Figure 5-2 shows a system configuration in which the UCS81003 provides a USB data switch, port power switch, low-power Attach Detection and portable device Attach/Removal Detection signaling. This configuration does not include configurable data line charger emulation, programmable current limiting or current monitoring and rationing.



**FIGURE 5-2:** UCS81003 System Configuration (Charger Emulation, No SMBus, with USB Host).



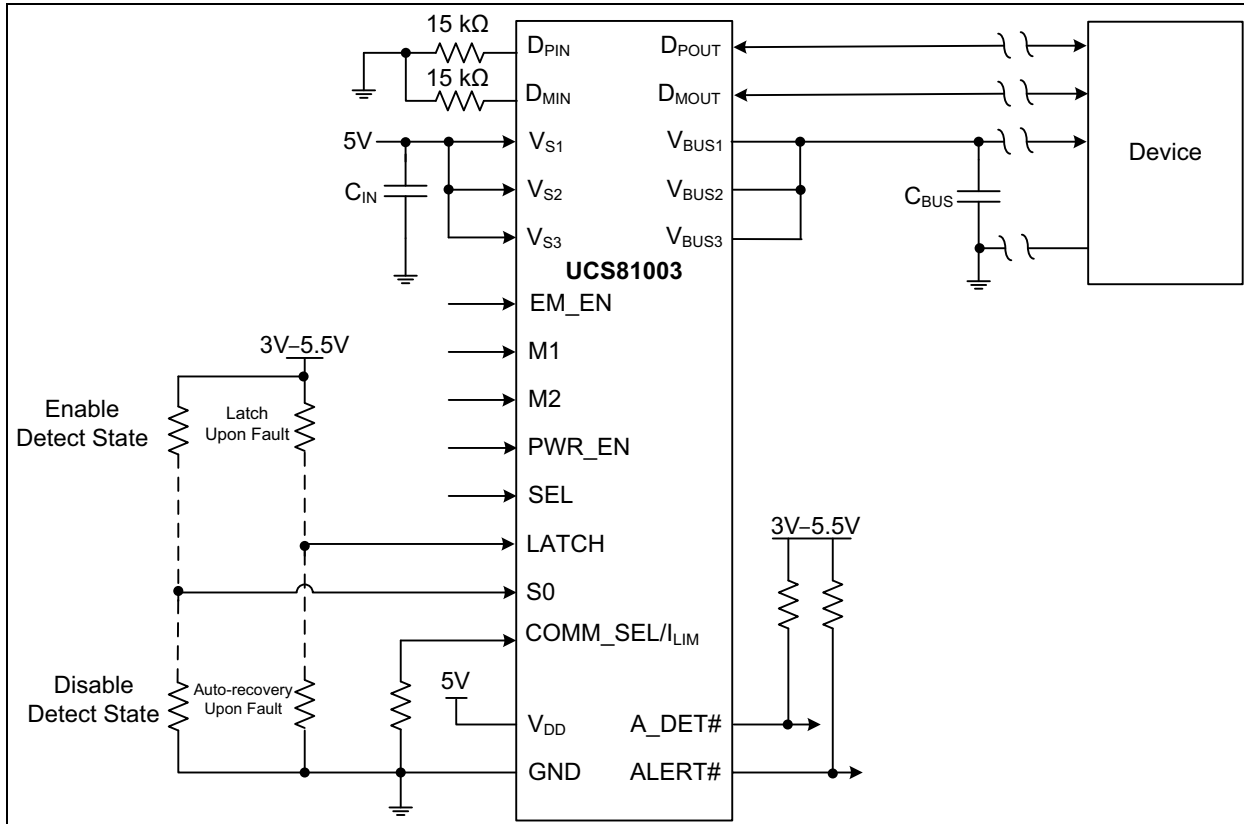
Figure 5-3 shows a system configuration in which the UCS81003 provides a port power switch, low-power Attach Detection and portable device attachment detected signaling. This configuration is useful for applications that provide USB BC1.2 or legacy data line handshaking, or both on the USB data lines, but still require port power switching and current limiting.



**FIGURE 5-3:** UCS81003 System Configuration (No SMBus, No Charger Emulation).

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Figure 5-4 shows a system configuration in which the UCS81003 provides a port power switch, low-power Attach Detection, charger emulation (with no USB host) and portable device attachment detected signaling. This configuration is useful for wall adapter-type applications and cigarette-plug adapters.



**FIGURE 5-4:** UCS81003 System Configuration (No SMBus, No USB Host, with Charger Emulation).

## 5.1 UCS81003 Power States

The UCS81003 has the following power states:

**TABLE 5-1: POWER STATES DESCRIPTION**

State	Description
<b>OFF</b>	This power state is entered when the voltage at the $V_{DD}$ pin voltage is $< V_{DD\_TH}$ . In this state, the device is considered OFF. The UCS81003 does not retain its digital states and register contents, nor respond to SMBus/I <sup>2</sup> C communications. The port power switch, bypass switch, and the high-speed data switches are turned OFF. See <a href="#">Section 5.1.1 “Off State Operation”</a> .
<b>Sleep</b>	This is the lowest power state available. While in this state, the UCS81003 retains digital functionality, respond to changes in emulation controls and wake to respond to SMBus/I <sup>2</sup> C communications. The high-speed switch and all other functionality are disabled. See <a href="#">Section 5.1.2 “Sleep State Operation”</a> .
<b>Detect</b>	This is a low-current power state. In this state, the device is actively looking for a portable device to be attached. The high-speed switch is disabled by default. While in this state, the UCS81003 retains the configuration and charge rationing data, but does not monitor the bus current. The SMBus/I <sup>2</sup> C communications is fully functional. See <a href="#">Section 5.1.3 “Detect State Operation”</a> .
<b>Error</b>	This power state is entered when a fault condition exists. See <a href="#">Section 5.1.5 “Error State Operation”</a> .
<b>Active</b>	This power state provides full functionality. While in this state, operations include activation of the port power switch, USB data line handshaking/charger emulation, and current limiting and charge rationing. See <a href="#">Section 5.1.4 “Active State Operation”</a> .

Table 5-2 shows the settings for the various power states, except OFF and Error. If  $V_{DD} < V_{DD\_TH}$ , the UCS81003 is in the OFF state. To determine the mode of operation in the Active state, see Table 9-1.

**Note:** Using configurations that are unlisted in Table 5-2 is not recommended and may produce undesirable results.

**TABLE 5-2: POWER STATES CONTROL SETTINGS**

Power State	$V_S$	PWR_EN	S0	M1, M2, EM_EN	Portable Device Attached	Behavior
Sleep	n/a	disabled	0	Not set to Data Pass-Through. (Note 1)	n/a	<ul style="list-style-type: none"> <li>All switches disabled.</li> <li><math>V_{BUS}</math> is near ground potential.</li> <li>The UCS81003 wakes to respond to SMBus communications.</li> </ul>
	n/a	enabled	0	All = 0b	n/a	
Detect (see Section 8.0 "Detect State")	n/a	disabled	1	n/a	n/a	<ul style="list-style-type: none"> <li>High-Speed switch disabled (by default).</li> <li>Port power switch disabled.</li> <li>Host-Controlled transition to Active state (see Section 5.1.3.2 "Host-Controlled Transition from Detect to Active").</li> </ul>
	$< V_{S\_UVLO}$	enabled	1	All $\neq$ 0b	n/a	
	$> V_{S\_UVLO}$	enabled	1	All $\neq$ 0b	No	
Active (see Section 9.0 "Active State")	$> V_{S\_UVLO}$	enabled	0	All $\neq$ 0b	n/a	<ul style="list-style-type: none"> <li>High-Speed switch enabled/disabled based on mode.</li> <li>Port power switch is ON at all times.</li> <li>Attach and Removal Detection disabled. See Note 2.</li> </ul>
	$> V_{S\_UVLO}$	enabled	1	All $\neq$ 0b	Yes	

- Note 1:** In order to transition from Active State Data Pass-Through mode into Sleep with these settings, change the M1, M2 and EM\_EN pins before changing the PWR\_EN pin. See Section 9.4 "Data Pass-Through (No Charger Emulation)".
- 2:** If S0 = '0' and a portable device is not attached in DCE Cycle mode, the UCS81003 is cycling through charger emulation profiles (by default). There is no guarantee which charger emulation profile is applied first when a portable device is attached.

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## 5.1.1 OFF STATE OPERATION

The device is in the OFF state if  $V_{DD}$  is less than  $V_{DD\_TH}$ . When the UCS81003 is in the OFF state it does nothing and all circuitry is disabled. Digital register values are not stored and the device does not respond to SMBus commands.

## 5.1.2 SLEEP STATE OPERATION

When the UCS81003 is in the Sleep state, the device is in its lowest power state. The high-speed switch, bypass switch, and the port power switch are disabled. The Attach and Removal Detection feature is disabled.  $V_{BUS}$  is near ground potential. The ALERT# pin is not asserted. If asserted prior to entering the Sleep state, the ALERT# pin is released. The A\_DET# pin is released. SMBus activity is limited to single byte read or write.

When in the Sleep state, the first data byte read from the UCS81003 wakes the device; however, the data to be read returns all '0's and must be considered invalid. This is dummy read byte is meant to wake the UCS81003. Subsequent read or write bytes are normally accepted. After the dummy read, the UCS81003 is in a higher power state (see Figure 5-6). The device returns to Sleep after the last communication, or if no further communication has occurred.

Figure 5-5 shows timing diagrams for waking the UCS81003 via external pins. Figure 5-6 shows the timing for waking the UCS81003 via SMBus.

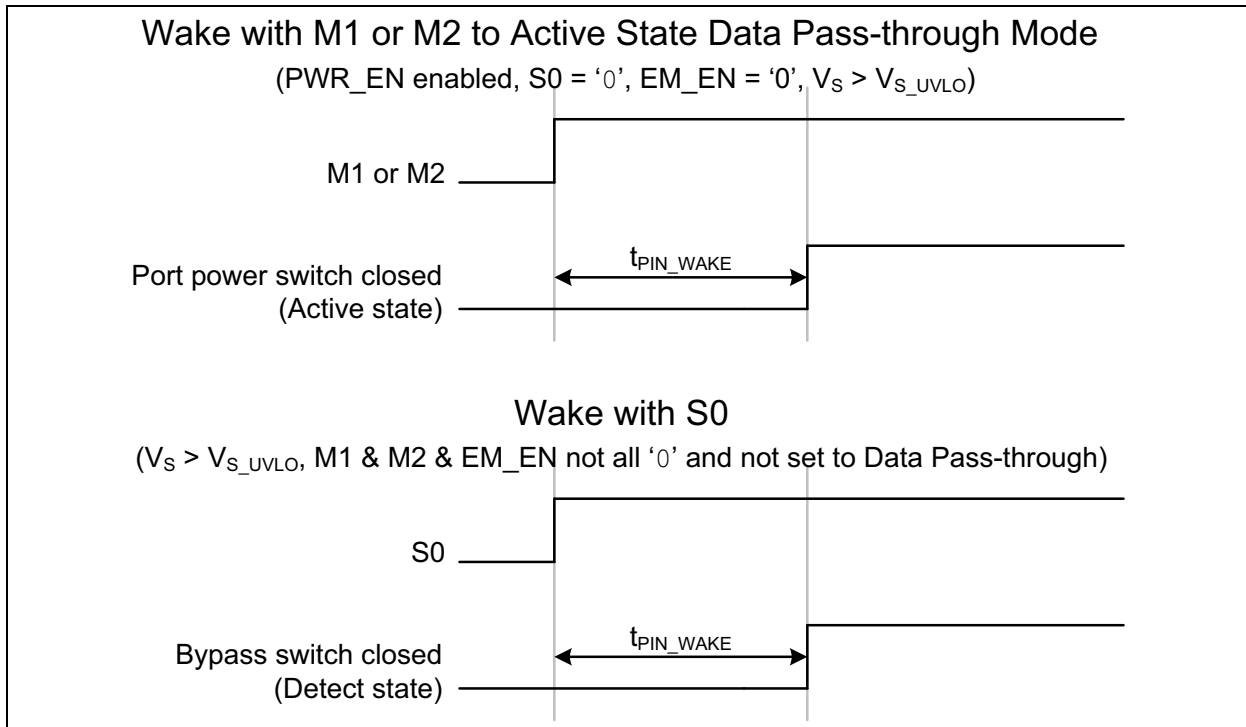


FIGURE 5-5: Wake Timing via External Pins.

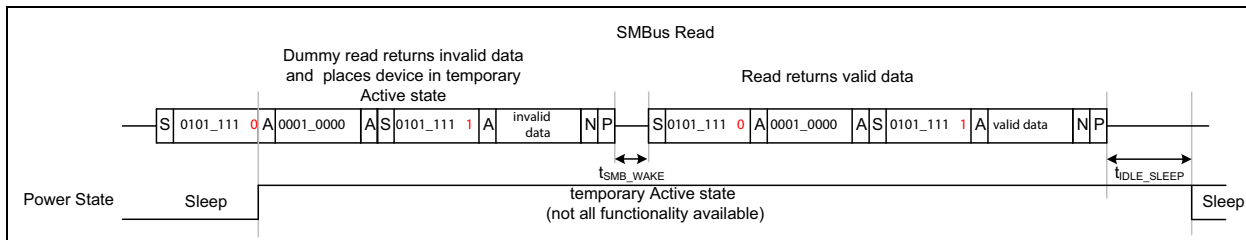


FIGURE 5-6: Wake via SMBus Read with S0 = '0'.

## 5.1.3 DETECT STATE OPERATION

When the UCS81003 is in the Detect state, the port power switch is disabled. The high-speed switch is also disabled by default. The  $V_{BUS}$  output is connected to the  $V_{DD}$  voltage by a secondary bypass switch (see [Section 8.0 “Detect State”](#)).

There is one non-recommended configuration which places the UCS81003 in the Detect state, but  $V_{BUS}$  is not discharged and a portable device attachment is not detected. For the recommended configurations, see [Table 5-2](#).

There are two methods for transitioning from the Detect state to the Active state: automatic and host-controlled.

### 5.1.3.1 Automatic Transition from Detect to Active

For the Detect state, set S0 to '1', enable PWR\_EN, set the EM\_EN, M1, and M2 controls to the desired Active mode ([Table 9-1](#)), and supply  $V_S > V_{S\_UVLO}$ . When a portable device is attached and an Attach Detection event occurs, the UCS81003 automatically transitions to the Active state and operate according to the selected Active mode.

### 5.1.3.2 Host-Controlled Transition from Detect to Active

For the Detect state, set S0 to '1', set the EM\_EN, M1, and M2 controls to the desired Active mode ([Table 9-1](#)), and configure one of the following:

- disable PWR\_EN and supply  $V_S$ , or
- enable PWR\_EN and do not supply  $V_S$ . When a portable device is attached and an Attach Detection event occurs, the host must respond to transition to the Active state.

Depending on the control settings in the Detect state, this entails:

- enabling PWR\_EN, or
- supplying  $V_S$  above the threshold.

**Note:** If S0 is '1', PWR\_EN is enabled and  $V_S$  is not present, the A\_DET# pin cycles if the current draw exceeds the current capacity of the bypass switch.

### 5.1.3.3 State Change from Detect to Active

When conditions cause the UCS81003 to transition from the Detect state to the Active state, the following occurs:

1. The Attach Detection feature is disabled and the Removal Detection feature remains enabled unless S0 is changed to '0'.
2. The bypass switch is turned OFF.
3. The discharge switch is turned ON briefly for  $t_{DISCHARGE}$ .
4. The port power switch is turned ON.

## 5.1.4 ACTIVE STATE OPERATION

Whenever the UCS81003 enters the Active state and the port power switch is closed, it enters the mode as instructed by the host controller (see [Section 9.0 “Active State”](#)). The UCS81003 cannot be in the Active state (therefore, the port power switch cannot be turned ON) if any of the following conditions exist:

- $V_S < V_{S\_UVLO}$
- PWR\_EN is disabled.
- M1, M2, and EM\_EN are all set to '0'.
- S0 is set to '1' and an Attach Detection event did not occur.

## 5.1.5 ERROR STATE OPERATION

The UCS81003 enters the Error state from the Active state when any of the following events are detected:

- Maximum allowable internal die temperature is exceeded ( $T_{TSD}$ ) (see [Section 7.2.1.2 “Thermal Shutdown”](#)).
- An overcurrent condition (see [Section 7.1.1 “Current Limit Setting”](#)).
- An undervoltage condition on  $V_{BUS}$  (see [Section 5.2.5 “Undervoltage Lockout on  \$V\_S\$ ”](#)).
- A back-drive condition (see [Section 5.2.3 “Back-voltage Detection”](#)).
- A discharge error (see [Section 7.3 “ \$V\_{BUS}\$  Discharge”](#)).
- An overvoltage condition on the  $V_S$  pins.

The UCS81003 enters the Error state from the Detect state when a back-drive condition is detected or when the maximum allowable internal die temperature is exceeded.

The UCS81003 enters the Error state from the Sleep state when a back-drive condition is detected.

When the UCS81003 enters the Error state, the port power switch,  $V_{BUS}$  bypass switch, and the high-speed switch are turned OFF, and the ALERT# pin is asserted (by default). These switches remain OFF while in this power state. The UCS81003 leaves this state as determined by the fault handling selection (see [Section 7.5 “Fault Handling Mechanism”](#)).

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When using the Latch fault handler and the user has reactivated the device by clearing the `ERR` bit (see [Section 10.3 “Status Registers”](#)), or toggling the `PWR_EN` control, the UCS81003 checks that all of the error conditions are removed. If using Auto-Recovery Fault Handler, after the  $t_{CYCLE}$  time period, the UCS81003 checks that all of the error conditions are removed.

If all of the error conditions are removed, the UCS81003 returns to the Active state or Detect state as applicable. Returning to the Active state causes the UCS81003 to restart the selected mode (see [Section 9.2 “Active Mode Selection”](#)).

If the device is in the Error state and a Removal Detection event occurs, it checks the error conditions and then returns to the power state as defined by the `PWR_EN`, `M1`, `M2`, `EM_EN`, and `S0` controls.

## 5.2 Supply Voltages

### 5.2.1 $V_{DD}$ SUPPLY VOLTAGE

The UCS81003 requires 4.5V to 5.5V to be present on the  $V_{DD}$  pin for core device functionality. Core device functionality consists of maintaining register states, wake-up upon SMBus/I<sup>2</sup>C query and Attach Detection.

### 5.2.2 $V_S$ SOURCE VOLTAGE

$V_S$  can be a separate supply and can be greater than  $V_{DD}$  to accommodate high-current applications in which current path resistances result in unacceptable voltage drops that may prevent optimal charging of some portable devices.

### 5.2.3 BACK-VOLTAGE DETECTION

Whenever the following conditions are true, the port power switch, the  $V_{BUS}$  bypass switch, and the high-speed data switch are disabled, and a back-voltage event is flagged. This causes the UCS81003 to enter the Error power state (see [Section 5.1.5 “Error State Operation”](#)).

- The  $V_{BUS}$  voltage exceeds the  $V_S$  voltage by  $V_{BV\_TH}$  and the port power switch is closed. The port power switch is immediately opened. If the condition lasts for longer than  $t_{MASK}$ , then the UCS81003 enters the Error state. Otherwise, the port power switch is turned ON as soon as the condition is removed.
- The  $V_{BUS}$  voltage exceeds the  $V_{DD}$  voltage by  $V_{BV\_TH}$  and the  $V_{BUS}$  bypass switch is closed. The bypass switch is immediately opened. If the condition lasts for longer than  $t_{MASK}$ , then the UCS81003 enters the Error state. Otherwise, the bypass switch is turned ON as soon as the condition is removed.

### 5.2.4 BACK-DRIVE CURRENT PROTECTION

If a self-powered portable device is attached, it may drive the  $V_{BUS}$  port to its power supply voltage level; however, the UCS81003 is designed such that leakage current from the  $V_{BUS}$  pins to the  $V_{DD}$  or  $V_S$  pins shall not exceed  $I_{BD\_1}$  (if the  $V_{DD}$  voltage is zero) or  $I_{BD\_2}$  (if the  $V_{DD}$  voltage exceeds  $V_{DD\_TH}$ ).

### 5.2.5 UNDERVOLTAGE LOCKOUT ON $V_S$

The UCS81003 requires a minimum voltage ( $V_{S\_UVLO}$ ) to be present on the  $V_S$  pin for Active power state.

### 5.2.6 OVERVOLTAGE DETECTION AND LOCKOUT ON $V_S$

The UCS81003 port power switch is disabled if the voltage on the  $V_S$  pin exceeds a voltage ( $V_{S\_OV}$ ) for longer than the specified time ( $t_{MASK}$ ). This causes the device to enter the Error state.

## 5.3 Discrete Input Pins

**Note:** If it is necessary to connect any of the control pins except the `COMM_SEL`/`ILIM` or `SEL` pins via a resistor to  $V_{DD}$  or `GND`, the resistor value must not exceed 100 k $\Omega$  in order to meet the  $V_{IH}$  and  $V_{IL}$  specifications.

### 5.3.1 `COMM_SEL`/`ILIM` INPUT

The `COMM_SEL`/`ILIM` input determines the initial `ILIM` settings and the communications mode as shown in [Table 11-1](#).

### 5.3.2 `SEL` INPUT

The `SEL` pin selects the polarity of the `PWR_EN` control. In addition, if the UCS81003 is not configured to operate in Stand-Alone mode, the `SEL` pin determines the SMBus address. See [Table 11-2](#). The `SEL` pin state is latched upon device power-up and further changes have no effect.

### 5.3.3 `M1`, `M2`, AND `EM_EN` INPUTS

The `M1`, `M2`, and `EM_EN` input controls determine the Active mode and affect the power state (see [Table 5-2](#) and [Table 9-1](#)). When these controls are all set to '0' and `PWR_EN` is enabled, the UCS81003 Attach and Removal Detection feature is disabled. In SMBus mode, the `M1`, `M2`, and `EM_EN` pin states are ignored by the UCS81003 if the `PIN_IGN` configuration bit is set (see [Section 10.4.3 “Switch Configuration Register”](#)); otherwise, the `M1_SET`, `M2_SET`, and `EM_EN_SET` configuration bits (see [Section 10.4.3 “Switch Configuration Register”](#)) are checked along with the pins.

## 5.3.4 PWR\_EN INPUT

The PWR\_EN control enables the port power switch to be turned ON if conditions are met and affects the power state (see [Table 5-2](#)). The port power switch cannot be closed if PWR\_EN is disabled. However, if PWR\_EN is enabled, the port power switch is not necessarily closed (see [Section 5.1.4 “Active State Operation”](#)). Polarity is controlled by the SEL pin. In SMBus mode, the PWR\_EN pin state is ignored by the UCS81003 if the PIN\_IGN configuration bit is set (see [Section 10.4.3 “Switch Configuration Register”](#)); otherwise, the PWR\_ENS configuration bit (see [Section 10.4.3 “Switch Configuration Register”](#)) is checked along with the pin.

## 5.3.5 LATCH INPUT

The Latch input control determines the behavior of the fault handling mechanism (see [Section 7.5 “Fault Handling Mechanism”](#)).

When the UCS81003 is configured to operate in Stand-Alone mode (see [Section 11.3 “Stand-Alone Operating Mode”](#)), the LATCH control is available exclusively via the LATCH pin (see [Table 11-10](#)). When the UCS81003 is configured to operate in SMBus mode, the LATCH control is available exclusively via the LATCHS configuration bit (see [Section 10.4.3 “Switch Configuration Register”](#)).

## 5.3.6 S0 INPUT

The S0 control enables the Attach and Removal Detection feature and affects the power state (see [Table 5-2](#)). When S0 is set to '1', an Attach Detection event must occur before the port power switch can be turned ON (this statement requires PWR\_EN\_BEH OTP bit is set to '1'). When S0 is set to '0', the Attach and Removal Detection feature is not enabled.

When the device is configured to operate in SMBus mode (see [Section 11.3 “Stand-Alone Operating Mode”](#)), the S0 control is available exclusively via the S0\_SET configuration bit (see [Section 10.4.3 “Switch Configuration Register”](#)). Otherwise, the S0 control is exclusively available via the S0 pin since the SMBus protocol is disabled.

## 5.4 Discrete Output Pins

### 5.4.1 ALERT# AND A\_DET# OUTPUT PINS

The ALERT# pin is an active-low open-drain interrupt to the host controller. The ALERT# pin is asserted (by default - see ALERT\_MASK in [Section 10.4.1 “General Configuration Register”](#)) when an error occurs (see [Register 10-3](#)). The ALERT# pin can also be asserted when the LOW\_CUR (portable device is pulling less current and may be finished charging) or TREG (thermal regulation temperature exceeded) bits are set and linked. As well, when charge rationing is enabled, the ALERT# pin is asserted by default when the current rationing threshold is reached as determined by RATION\_BEH<1:0> (see [Table 7-1](#)). The ALERT# pin is released when all error conditions that may assert the ALERT# pin (such as an error condition, charge rationing, and TREG and LOW\_CHG if linked) are removed or reset as necessary.

The A\_DET# pin provides an active-low open-drain output indication that a valid Attach Detection event has occurred. It remains asserted until the UCS81003 is placed into the Sleep state or a Removal Detection event occurs. For wake on USB, the A\_DET# pin assertion can be utilized by the system. If the S0 control is '0' and the UCS81003 is in the Active state, the A\_DET# pin is asserted regardless if a portable device is attached or not. If S0 is '1', PWR\_EN is enabled and  $V_S$  is not present, the A\_DET# pin cycles if the current draw exceeds the current capacity of the bypass switch.

### 5.4.2 INTERRUPT BLANKING

The ALERT# and A\_DET# pins are not asserted for a specified time (up to  $t_{BLANK}$ ) after power-up. Additionally, an error condition (except for the thermal shutdown) must be present for longer than a specified time ( $t_{MASK}$ ) before the ALERT# pin is asserted.

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## 6.0 USB HIGH-SPEED DATA SWITCH

The UCS81003 contains a series USB 2.0-compliant high-speed switch between the  $D_{PIN}$  and  $D_{MIN}$  pins and between the  $D_{POUT}$  and  $D_{MOU}$  pins. This switch is designed for high-speed, low-latency functionality to enable USB 2.0 full-speed and high-speed communications with minimal interference.

Nominally, the switch is closed in the Active state, enabling uninterrupted USB communications between the upstream host and the portable device. The switch is opened when:

- The UCS81003 is actively emulating using any of the charger emulation profiles except CDP (by default - see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)).
- The UCS81003 is operating as a dedicated charger unless the  $HSW\_DCE$  configuration bit is set (see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)).
- The UCS81003 is in the Detect state (by default) or in the Sleep state.

<b>Note:</b> If the $V_{DD}$ voltage is less than $V_{DD\_TH}$ , the high-speed data switch is disabled and opened.
---

### 6.1 USB-IF High-Speed Compliance

The USB data switch does not significantly degrade the signal integrity through the device  $D_P/D_M$  pins with USB high-speed communications.



## 7.0 USB PORT POWER SWITCH

To assure compliance to various charging specifications, the UCS81003 contains a USB port power switch that supports two current-limiting modes: Trip and Constant Current (variable slope). The current limit ( $I_{LIM}$ ) is pin selectable (and may be updated via the register set). The switch also includes soft start circuitry and a separate short-circuit current limit.

The port power switch is ON in the Active state (except when  $V_{BUS}$  is discharging).

### 7.1 Current Limiting

#### 7.1.1 CURRENT LIMIT SETTING

The UCS81003 hardware set current limit ( $I_{LIM}$ ), can be one of eight values (see [Table 11-1](#)). This resistor value is read once upon UCS81003 power-up. The current limit can be changed via the SMBus/I<sup>2</sup>C after power-up; however, the programmed current limit cannot exceed the hardware set current limit.

At power-up, the communication mode (Stand-Alone or SMBus/I<sup>2</sup>C) and hardware current limit ( $I_{LIM}$ ) are determined via the pull-down resistor (or pull-up resistor, if connected to  $V_{DD}$ ) on the COMM\_SEL/ $I_{LIM}$  pin as shown in [Table 11-1](#).

#### 7.1.2 SHORT CIRCUIT OUTPUT CURRENT LIMITING

Short circuit current limiting occurs when the output current is above the selectable current limit ( $I_{LIMx}$ ). This event is detected and the current immediately becomes limited (within  $t_{SHORT\_LIM}$  time). If the condition remains, the port power switch flags an Error condition and enters the Error state (see [Section 5.1.5 “Error State Operation”](#)).

#### 7.1.3 SOFT START

When the PWR\_EN control changes its state to enable the port power switch, or an Attach Detection event occurs in the Detect power state and the PWR\_EN control is enabled, the UCS81003 invokes a soft start routine for the duration of the  $V_{BUS}$  rise time ( $t_{R\_BUS}$ ). This soft start routine limits current flow from  $V_S$  into  $V_{BUS}$  while it is active. This circuitry prevents current spikes due to a step in the portable device current draw.

In the case when a portable device is attached while the PWR\_EN pin is enabled, if the bus current exceeds  $I_{LIM}$ , the UCS81003 current limiter responds within a specified time ( $t_{SHORT\_LIM}$ ) and operates normally at this point. The  $C_{BUS}$  capacitor delivers the extra current, if any, as required by the load change.

#### 7.1.4 CURRENT-LIMITING MODES

The UCS81003 current limiting has two modes: Trip and Constant Current (variable slope). Either mode functions at all times when the port power switch is

closed. The current limiting mode used depends on the Active state mode (see [Section 9.9 “Current Limit Mode Associations”](#)). When operating in the Detect power state (see [Section 5.1.3 “Detect State Operation”](#)), the current capacity at  $V_{BUS}$  is limited to  $I_{BUS\_BYP}$  as described in [Section 8.2 “V<sub>BUS</sub> Bypass Switch”](#).

##### 7.1.4.1 Trip Mode

When using Trip Current Limiting, the UCS81003 USB port power switch functions as a low-resistance switch and rapidly turns OFF if the current limit is exceeded. While operating using Trip Current Limiting, the  $V_{BUS}$  output voltage is held relatively constant (equal to the  $V_S$  voltage minus the  $R_{ON} \times I_{BUS}$  current) for all current values up to the  $I_{LIM}$ .

If the current drawn by a portable device exceeds  $I_{LIM}$ , the following occurs:

1. The port power switch is turned OFF (Trip action).
2. The UCS81003 enters the Error state and assert the ALERT# pin.
3. The fault handling circuitry determines subsequent actions.

Trip Current Limiting is used by default when the UCS81003 is in Data Pass-Through and Dedicated Charger Emulation Cycle (except when the BC1.2 DCP charger emulation profile is accepted), and when there is no handshake. This method is also used when charger emulation is active.

**Note:** To avoid cycling in Trip mode, set  $I_{LIM}$  higher than the highest expected portable device current draw.

##### 7.1.4.2 Constant Current Limiting (Variable Slope)

Constant Current Limiting is used when a portable device handshakes using the BC1.2 DCP charger emulation profile and the current drawn is greater than  $I_{LIM}$  (and  $I_{LIM} < 1.68A$ ). It is also used in BC1.2 CDP mode and during the DCE Cycle when a charger emulation profile is being applied and the emulation timeout is active.

In CC mode, the port power switch enables the attached portable device to reduce  $V_{BUS}$  output voltage to less than the input  $V_S$  voltage while maintaining current delivery. The V/I slope depends on the user set  $I_{LIM}$  value. This slope is held constant for a given  $I_{LIM}$  value.

# UCS81003

## 7.2 Thermal Management and Voltage Protection

### 7.2.1 THERMAL MANAGEMENT

The UCS81003 utilizes two-stage internal thermal management: Dynamic Thermal Management and Fixed Thermal Shutdown.

#### 7.2.1.1 Dynamic Thermal Management

For the first stage (active in both current limiting modes), referred to as Dynamic Thermal Management, the UCS81003 automatically adjusts port power switch limits and modes to lower power dissipation when the thermal regulation temperature value is approached as described below.

If the internal temperature exceeds the  $T_{REG}$  value, the port power switch is opened, the current limit ( $I_{LIM}$ ) is lowered by one step and a timer is started ( $t_{DC\_TEMP}$ ). When this timer expires, the port power switch is closed and the internal temperature is checked again. If it remains above the  $T_{REG}$  threshold, the UCS81003 repeats this cycle (opens port power switch and reduces the  $I_{LIM}$  setting by one step) until  $I_{LIM}$  reaches its minimum value.

**Note 1:** If the temperature exceeds the  $T_{REG}$  threshold while operating in the DCE Cycle mode after a charger emulation profile is accepted, the profile is removed. The UCS81003 does not restart the DCE Cycle until one of the control inputs changes state to restart emulation.

**2:** The UCS81003 does not actively discharge  $V_{BUS}$  as a result of the temperature exceeding  $T_{REG}$ ; however, any load current provided by a portable device or other load causes  $V_{BUS}$  to be discharged when the port power switch is opened, possibly resulting in an attached portable device resetting.

If the UCS81003 is operating using Constant Current Limiting (variable slope) and the  $I_{LIM}$  setting is reduced to its minimum set point and the temperature is still above  $T_{REG}$ , the UCS81003 switches to operating using Trip Current Limiting. This is done by reducing the  $I_{BUS\_R2MIN}$  setting to 120 mA and restoring the  $I_{LIM}$  setting to the value immediately below the programmed setting (for example, if the programmed  $I_{LIM}$  is 2.05A, the value is set to 1.68A). If the temperature continues to remain above  $T_{REG}$ , the UCS81003 continues this cycle (open the port power switch and reduce the  $I_{LIM}$  setting by one step).

If the UCS81003 internal temperature drops below  $T_{REG} - T_{REG\_HYST}$ , the UCS81003 takes action based on the following:

1. If the Current Limit mode changed from CC mode to Trip mode, then a timer is started. When this timer expires, the UCS81003 resets the port power switch operation to its original configuration, enabling it to operate using Constant Current Limiting (variable slope).
2. If the Current Limit mode did not change from CC mode to Trip mode, or has started operating in Trip mode, the UCS81003 resets the port power switch operation to its original configuration.

If the UCS81003 is operating using Trip Current Limiting and the  $I_{LIM}$  setting is reduced to its minimum set point and the temperature is above  $T_{REG}$ , the port power switch is closed and the current limit is held at its minimum setting until the temperature drops below  $T_{REG} - T_{REG\_HYST}$ .

#### 7.2.1.2 Thermal Shutdown

The second-stage thermal management consists of a hardware implemented thermal shutdown corresponding to the maximum allowable internal die temperature ( $T_{TSD}$ ). If the internal temperature exceeds this value, the port power switch immediately turns OFF until the temperature is below  $T_{TSD} - T_{TSD\_HYST}$ .

## 7.3 $V_{BUS}$ Discharge

The UCS81003 discharges  $V_{BUS}$  through an internal 100 $\Omega$  resistor when at least one of the following conditions occurs:

- The PWR\_EN control is disabled (triggered on the inactive edge of the PWR\_EN control).
- A portable device Removal Detection event is flagged.
- The  $V_S$  voltage drops below a specified threshold ( $V_{S\_UVLO}$ ) that causes the port power switch to be disabled.
- When commanded into the Sleep power state via the EM\_EN, M1, and M2 controls.
- Before each charger emulation profile is applied (UCS81003AM and UCS81003AB), unless it is a power-up condition (UCS81003AB only).
- Upon recovery from the Error state.
- When commanded via the SMBus (see [Section 10.4 “Configuration Registers”](#)) in the Active state.
- Any time that the port power switch is activated after the  $V_{BUS}$  bypass switch is ON (that is, whenever  $V_{BUS}$  voltage transitions from being driven from  $V_{DD}$  to being driven from  $V_S$ , such as going from Detect to Active power state).
- Any time that the  $V_{BUS}$  bypass switch is activated after the port power switch is ON (that is, going from Active to Detect power state).

When the  $V_{BUS}$  discharge circuitry is activated, at the end of the  $t_{DISCHARGE}$  time, the UCS81003 confirms that  $V_{BUS}$  is discharged. If the  $V_{BUS}$  voltage is not below the  $V_{TEST}$  level, a discharge error is flagged (by setting the DISCH\_ERR status bit) and the UCS81003 enters the Error state.

## 7.4 Battery Full

Delivery of bus current to a portable device can be rationed by the UCS81003. When this functionality is enabled, the host system must provide the UCS81003 with an accumulated charge maximum limit (in mAh). The charge rationing functionality works only in the Active power state. It continuously monitors the current

delivered and the time elapsed since the mode is activated (or since the data is updated). This information is compiled to generate a charge-rationing number that is checked against the host limit.

Once the programmed current-rationing limit is reached, the UCS81003 takes action as determined by the RATION\_N\_BEH bits as described in [Table 7-1](#). Note that this does not cause the device to enter the Error state.

Once the charge rationing circuitry has reached the programmed threshold, the UCS81003 maintains the desired behavior until charge rationing is reset. Once charge rationing is reset or disabled, the UCS81003 recovers as shown in [Table 7-2](#).

**TABLE 7-1: CHARGE RATIONING BEHAVIOR**

RATION_BEH<1:0>		Behavior	Actions taken	Notes
1	0			
0	0	Report	ALERT# pin asserted.	
0	1	Report and Disconnect (default)	<ol style="list-style-type: none"> <li>ALERT# pin asserted.</li> <li>Charger emulation profile removed.</li> <li>Port power switch disconnected.</li> </ol>	The HSW is not affected. All bus monitoring is still active. Changing the M1, M2, EM_EN, S0, and PWR_EN controls causes the device to change power states as defined by the pin combinations; however, the port power switch remains OFF until the rationing circuitry is reset. Furthermore, the bypass switch is not turned ON if enabled via the S0 control.
1	0	Disconnect and Go to Sleep	<ol style="list-style-type: none"> <li>Port power switch disconnected.</li> <li>Charger emulation profile removed.</li> <li>Device enters the Sleep state.</li> </ol>	The HSW is disabled. All VBUS and VS monitoring are stopped. Changing the M1, M2, EM_EN, S0, and PWR_EN controls has no effect on the power state until the rationing circuitry is reset.
1	1	Ignore	Take no further action.	

**TABLE 7-2: CHARGE RATIONING RESET BEHAVIOR**

Behavior	Reset Actions
Report	<ol style="list-style-type: none"> <li>Reset the Total Accumulated Charge registers.</li> <li>Clear the RATION status bit.</li> <li>Release the ALERT# pin.</li> </ol>
Report and Disconnect	<ol style="list-style-type: none"> <li>Reset the Total Accumulated Charge registers.</li> <li>Clear the RATION status bit.</li> <li>Release the ALERT# pin.</li> <li>Check the M1, M2, EM_EN, S0 and PWR_EN controls and enter the indicated power state if the controls changed (<a href="#">Note 1</a>).</li> </ol>

**Note 1:** Any time the charge rationing circuitry checks the pin conditions when changing rationing behavior or resetting charge rationing, if the external pin conditions changed, then charger emulation is restarted (provided emulation is enabled via the pin states). If the pin conditions did not change, the UCS81003 returns to the previous power state as if the rationing threshold is not reached (for example, it does not discharge  $V_{BUS}$  or restart emulation).

**TABLE 7-2: CHARGE RATIONING RESET BEHAVIOR (CONTINUED)**

Behavior	Reset Actions
Disconnect and Go to Sleep	<ol style="list-style-type: none"> <li>1. Reset the Total Accumulated Charge registers.</li> <li>2. Clear the RATION status bit.</li> <li>3. Check the M1, M2, EM_EN, S0, and PWR_EN controls and enter the indicated power state if the controls changed (<a href="#">Note 1</a>).</li> </ol>
Ignore	<ol style="list-style-type: none"> <li>1. Reset the Total Accumulated Charge registers.</li> <li>2. Clear the RATION status bit.</li> </ol>

**Note 1:** Any time the charge rationing circuitry checks the pin conditions when changing rationing behavior or resetting charge rationing, if the external pin conditions changed, then charger emulation is restarted (provided emulation is enabled via the pin states). If the pin conditions did not change, the UCS81003 returns to the previous power state as if the rationing threshold is not reached (for example, it does not discharge  $V_{BUS}$  or restart emulation).

## 7.4.1 CHARGE RATIONING INTERACTIONS

When charge rationing is active, regardless of the specified behavior, the UCS81003 normally functions until the charge rationing threshold is reached. Note that charge rationing is only active when the UCS81003 is in the Active state, and it does not automatically resets when a Removal or Attach Detection event occurs. Charger emulation starts over if a Removal Detection event and Attach Detection event occur while charge rationing is active and the charge rationing threshold is not reached. This enables charging of sequential portable devices while charge is being rationed, which means that the accumulated power given to several portable devices is still held to the stated rationing limit.

Changing the charge rationing behavior has no effect on the charge rationing data registers. If the behavior is changed prior to reaching the charge rationing threshold, this change occurs and become transparent to the user. When the charge rationing threshold is reached, the UCS81003 takes action as shown in [Table 7-1](#). If the behavior is changed after the charge rationing threshold is reached, the UCS81003 immediately adopts the newly programmed behavior, clearing the ALERT# pin and restoring switch operation respectively (see [Table 7-3](#)).

**TABLE 7-3: EFFECTS OF CHANGING RATIONING BEHAVIOR AFTER THRESHOLD REACHED**

Previous Behavior	New Behavior	Actions taken
Ignore	Report	Assert ALERT# pin.
	Report and Disconnect	<ol style="list-style-type: none"> <li>1. Assert ALERT# pin.</li> <li>2. Remove charger emulation profile.</li> <li>3. Open port power switch. See the <a href="#">Report and Disconnect (default)</a> in <a href="#">Table 7-1</a>.</li> </ol>
	Disconnect and Go to Sleep	<ol style="list-style-type: none"> <li>1. Remove charger emulation profile.</li> <li>2. Open port power switch.</li> <li>3. Enter the Sleep state. See the <a href="#">Disconnect and Go to Sleep</a> entry in <a href="#">Table 7-1</a>.</li> </ol>

**Note 1:** Any time the charge rationing circuitry checks the pin conditions when changing rationing behavior or resetting charge rationing, if the external pin conditions have changed, then charger emulation is restarted (provided emulation is enabled via the pin states). If the pin conditions did not change, the UCS81003 returns to the previous power state as if the rationing threshold is not reached (for example, it does not discharge  $V_{BUS}$  or restart emulation).

**TABLE 7-3: EFFECTS OF CHANGING RATIONING BEHAVIOR AFTER THRESHOLD REACHED**

Previous Behavior	New Behavior	Actions taken
Report	Ignore	Release ALERT# pin.
	Report and Disconnect	Open port power switch. See the <a href="#">Report and Disconnect (default)</a> entry in <a href="#">Table 7-1</a> .
	Disconnect and Go to Sleep	<ol style="list-style-type: none"> <li>1. Release the ALERT# pin.</li> <li>2. Remove charger emulation profile.</li> <li>3. Open the port power switch.</li> <li>4. Enter the Sleep state. See the <a href="#">Disconnect and Go to Sleep</a> entry in <a href="#">Table 7-1</a>.</li> </ol>
Report and Disconnect	Ignore	<ol style="list-style-type: none"> <li>1. Release the ALERT# pin.</li> <li>2. Check the M1, M2, EM_EN, S0, and PWR_EN controls and enter the indicated power state if the controls changed (see <a href="#">Note 1</a>).</li> </ol>
	Report	Check the M1, M2, EM_EN, S0, and PWR_EN controls and enter the indicated power state if the controls changed (see <a href="#">Note 1</a> ).
	Disconnect and Go to Sleep	<ol style="list-style-type: none"> <li>1. Release the ALERT# pin.</li> <li>2. Enter the Sleep state. See the <a href="#">Disconnect and Go to Sleep</a> entry in <a href="#">Table 7-1</a>.</li> </ol>
Disconnect and Go to Sleep	Ignore	Check the M1, M2, EM_EN, S0, and PWR_EN controls and enter the indicated power state if the controls changed (see <a href="#">Note 1</a> ).
	Report	<ol style="list-style-type: none"> <li>1. Assert the ALERT# pin.</li> <li>2. Check the M1, M2, EM_EN, S0, and PWR_EN controls and enter the indicated power state if the controls changed (see <a href="#">Note 1</a>).</li> </ol>
	Report and Disconnect	<ol style="list-style-type: none"> <li>1. Assert the ALERT# pin.</li> <li>2. Check the M1, M2, EM_EN, S0, and PWR_EN controls to determine the power state, then enter that state except that the port power switch and bypass switch are not closed (see <a href="#">Note 1</a>).</li> </ol>

**Note 1:** Any time the charge rationing circuitry checks the pin conditions when changing rationing behavior or resetting charge rationing, if the external pin conditions have changed, then charger emulation is restarted (provided emulation is enabled via the pin states). If the pin conditions did not change, the UCS81003 returns to the previous power state as if the rationing threshold is not reached (for example, it does not discharge  $V_{BUS}$  or restart emulation).

If the RTN\_EN control is set to '0' prior to reaching the charge rationing threshold, rationing is disabled and the Total Accumulated Charge registers are cleared. If the RTN\_EN control is set to '0' after the charge rationing threshold is reached, the following are done:

1. RATION status bit is cleared.
2. The ALERT# pin is released if asserted by the rationing circuitry and no other conditions are present.
3. The M1, M2, EM\_EN, S0 and PWR\_EN controls are checked to determine the power state. See [Note 1](#) in [Table 7-3](#).

**Note:** If the rationing behavior is set to "Report and Disconnect" when the charge rationing threshold is reached, and then the RTN\_EN bit is cleared, the portable device may start charging sub-optimally because the charger emulation profile is removed. Toggle the PWR\_EN control to restart charger emulation.

Setting the RTN\_RST control to '1' automatically resets the Total Accumulated Charge registers to 00\_00h. If this is done prior to reaching the charge rationing threshold, the data continues to be accumulated restarting from 00\_00h. If this is done after the charge rationing threshold is reached, the UCS81003 takes action as shown in [Table 7-2](#).

# UCS81003

## 7.5 Fault Handling Mechanism

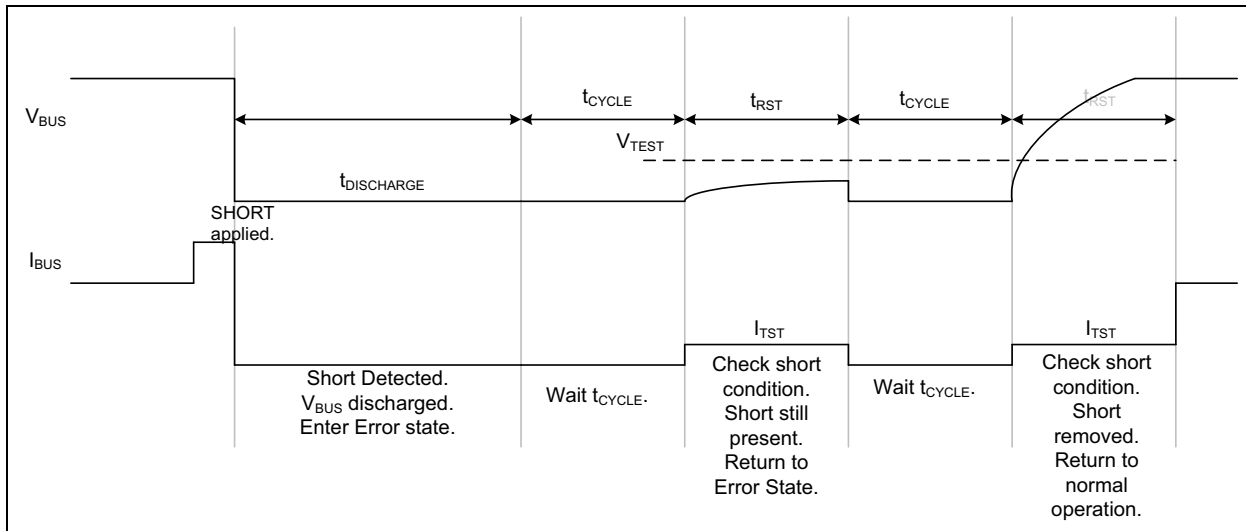
The UCS81003 has two modes for handling faults:

- Latch (latch-upon-fault)
- Auto-Recovery (automatically attempts to restore the Active power state after a fault occurs).

If the SMBus is actively utilized, Auto-Recovery Fault Handling is the default error handler as determined by the LATCHS bit (see [Section 10.4.3 “Switch Configuration Register”](#)). Otherwise, the fault handling mechanism used depends on the state of the LATCH pin. Faults include overcurrent, overvoltage (on  $V_S$ ), undervoltage (on  $V_{BUS}$ ), back-voltage ( $V_{BUS}$  to  $V_S$ , or  $V_{BUS}$  to  $V_{DD}$ ), discharge error, and maximum allowable internal die temperature ( $T_{TSD}$ ) exceeded (see [Section 5.1.5 “Error State Operation”](#)).

### 7.5.1 AUTO-RECOVERY FAULT HANDLING

When the LATCH control is low, Auto-Recovery Fault Handling is used. When an error condition is detected, the UCS81003 immediately enters the Error state and assert the ALERT# pin (see [Section 5.1.5 “Error State Operation”](#)). Independently from the host controller, the UCS81003 waits for a preset time ( $t_{CYCLE}$ ), checks error conditions ( $t_{TST}$ ) and restores Active operation if the error condition(s) no longer exist. If all other conditions that may cause the ALERT# pin to be asserted are removed, the ALERT# pin is released.



**FIGURE 7-1:** Error Recovery Timing (Short Circuit Example).

### 7.5.2 LATCHED FAULT HANDLING

When the LATCH control is high, Latch Fault Handling is used. When an error condition is detected, the UCS81003 enters the Error power state and assert the ALERT# pin. Upon command from the host controller (by toggling the PWR\_EN control from enabled to disabled or by clearing the ERR bit via SMBus), the UCS81003 checks error conditions once and restore Active operation if error conditions no longer exist. If an error condition still exists, the host controller is required to issue the command again to check error conditions.



## 8.0 DETECT STATE

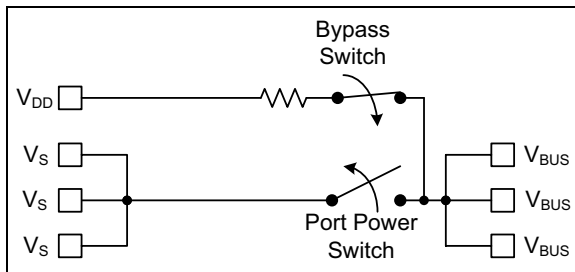
### 8.1 Device Attach/Removal Detection

The UCS81003 can detect the attachment and removal of a portable device on the USB port. Attach and Removal Detection does not perform any charger emulation or qualification of the device. The high-speed switch is OFF (by default) during the Detect power state.

### 8.2 $V_{BUS}$ Bypass Switch

The UCS81003 contains circuitry to provide  $V_{BUS}$  current as shown in Figure 8-1. In the Detect state,  $V_{DD}$  is the voltage source, whereas in the Active state,  $V_S$  is the voltage source. The bypass switch and the port power switch are both never ON at the same time.

While the  $V_{BUS}$  bypass switch is active, the current available to a portable device is limited to  $I_{BUS\_BYP}$ , and the Attach Detection feature is active.



**FIGURE 8-1:** Detect State  $V_{BUS}$  Biasing.

### 8.3 Attach Detection

The primary Attach Detection feature is only active in the Detect power state. When active, this feature constantly monitors the current load on the  $V_{BUS}$  pin. If the current drawn by a portable device is greater than  $I_{DET\_QUAL}$  for longer than  $t_{DET\_QUAL}$ , an Attach Detection event occurs. This causes the  $A\_DET\#$  pin to assert low and the  $ADET\_PIN$  and  $ATT$  status bits to be set.

Until the port power switch is enabled, the current available to a portable device is limited to that used to detect device attachment ( $I_{DET\_QUAL}$ ). Once an Attach Detection event occurs, the UCS81003 waits for the  $PWR\_EN$  control to be enabled. When  $PWR\_EN$  is enabled and  $V_S$  is above the threshold, the UCS81003 activates the USB port power switch and operates in the selected Active mode (see Section 9.0 “Active State”).

### 8.4 Removal Detection

The Removal Detection feature is active in the Active and Detect power states if  $S0 = '1'$ . This feature monitors the current load on the  $V_{BUS}$  pin. If this load drops to less than  $I_{REM\_QUAL\_DET}$  for longer than  $t_{REM\_QUAL}$ , a Removal Detection event is flagged. When this event occurs, the following are performed:

1. Disable the port power switch and the bypass switch.
2. Deassert the  $A\_DET\#$  pin and set the  $REM$  status register bit.
3. Enable an internal discharging device that discharges the  $V_{BUS}$  line within  $t_{DISCHARGE}$ .
4. Once the  $V_{BUS}$  pin is discharged, the device returns to the Detect state regardless of the  $PWR\_EN$  control state.

## 9.0 ACTIVE STATE

### 9.1 Active State Overview

The UCS81003 has the following modes of operation in the Active state: Data Pass-Through, BC1.2 DCP, BC1.2 SDP, BC1.2 CDP, and Dedicated Charger Emulation Cycle. The current limiting mode depends on the Active mode behavior (see [Table 9-2](#)).

### 9.2 Active Mode Selection

The Active mode selection is controlled by three controls: EM\_EN, M1, and M2 as shown in [Table 9-1](#).

**TABLE 9-1: ACTIVE MODE SELECTION**

M1	M2	EM_EN	Active mode
0	0	1	Dedicated Charger Emulation Cycle
0	1	0	Data Pass-Through
0	1	1	BC1.2 DCP
1	0	0	BC1.2 SDP – <a href="#">Note 1</a>
1	0	1	Dedicated Charger Emulation Cycle
1	1	0	Data Pass-Through
1	1	1	BC1.2 CDP

**Note 1:** BC1.2 SDP behaves the same as the Data Pass-Through mode with the exception that it is preceded by a  $V_{BUS}$  discharge when the mode is entered per the BC1.2 specification.

### 9.3 BC1.2 Detection Renegotiation

The BC1.2 specification enables a charger to act as an SDP, CDP or DCP and to change between these roles. To force an attached portable device to repeat the charging detection procedure,  $V_{BUS}$  must be cycled. In compliance with this specification, the UCS81003 automatically cycles  $V_{BUS}$  when switching between the BC1.2 SDP, BC1.2 DCP, and BC1.2 CDP modes.

### 9.4 Data Pass-Through (No Charger Emulation)

When commanded to Data Pass-Through mode, UCS81003 closes its USB high-speed data switch to enable USB communications between a portable device and host controller and operates using Trip Current Limiting. No charger emulation profiles are applied in this mode. Data Pass-Through mode persists until commanded otherwise by the M1, M2, and EM\_EN controls.

**Note 1:** If it is desired that the Data Pass-Through mode operates as a traditional/standard port power switch, the S0 control must be set to '0' to enable the port power switch to be closed without requiring an Attach Detection event. When entering this mode, there is no automatic  $V_{BUS}$  discharge.

**2:** When the M1, M2, and EM\_EN controls are set to '0', '1', '0' or to '1', '1', '0' respectively, Data Pass-Through mode persists if the PWR\_EN control is disabled; however, the UCS81003 draws more current. To leave the Data Pass-Through mode, the PWR\_EN control must be enabled before the M1, M2 and EM\_EN controls are changed to the desired mode.

### 9.5 BC1.2 SDP (No Charger Emulation)

When commanded to BC1.2 SDP mode, UCS81003 discharges  $V_{BUS}$ , closes its USB high-speed data switch to enable USB communications between a portable device and host controller, and operates using Trip Current Limiting. No charger emulation profiles are applied in this mode. BC1.2 SDP mode persists until commanded otherwise by the M1, M2, EM\_EN, and PWR\_EN controls.

**Note:** If it is desired that the BC1.2 SDP mode operates as a traditional/standard port power switch, the S0 control must be set to '0' to enable the port power switch to be closed without requiring an Attach Detection event.

### 9.6 BC1.2 CDP

When BC1.2 CDP is selected as the Active mode, UCS81003 discharges  $V_{BUS}$ , closes its USB high-speed data switch (by default), and applies the BC1.2 CDP charger emulation profile which performs handshaking per the specification. The combination of the UCS81003 CDP handshake along with a standard USB host comprises a Charging Downstream Port. In BC1.2 CDP mode, there is no emulation timeout.

If the handshake is successful, the UCS81003 operates using Constant Current Limiting (variable slope). If the handshake is not successful, the UCS81003 leaves the applied CDP profile in place, leaves the high-speed switch closed, enables Constant Current Limiting, and persists in this condition until commanded otherwise by the M1, M2, EM\_EN, and PWR\_EN controls.



The UCS81003 responds per the BC1.2 specification to the portable device initiated charger renegotiation requests.

**Note 1:** BC1.2 compliance testing may require the S0 control to be set to '0' (Attach and Removal Detection feature disabled) while testing is in progress.

**2:** When the UCS81003 is in BC1.2 CDP mode and the Attach and Removal Detection feature is enabled, if a power thief (such as a USB light or fan) attaches but does not assert  $D_P$  pin, a Removal event does not occur when the portable device is removed. However, if a standard USB device is subsequently attached, Removal Detection is fully functional again. Additionally, if PWR\_EN is cycled or M1, M2 and/or EM\_EN change state, a Removal event occurs and Attach Detection is reactivated.

## 9.6.1 BC1.2 CDP CHARGER EMULATION PROFILE

The BC1.2 CDP charger emulation profile acts in a reactionary manner based on stimulus from the portable device as described below and shown in [Figure 2-1](#).

**Note:** All CDP handshaking is performed with the high-speed switch closed.

1.  $V_{BUS}$  voltage is applied.
2. Primary Detection – when the portable device drives a voltage between 0.4V and 0.8V onto the  $D_{POUT}$  pin, the UCS81003 drives 0.6V onto the  $D_{MOUT}$  pin within 20 ms.
3. When the portable device drives the  $D_{POUT}$  pin back to '0', the UCS81003 then drives the  $D_{MOUT}$  pin back to '0' within 20 ms.
4. Optional Secondary Detection – If the portable device then drives a voltage of 0.6V (nominal) onto the  $D_{MOUT}$  pin, the UCS81003 takes no other action. This causes the portable device to observe a '0' on the  $D_{POUT}$  pin and detects the connection to a CDP.

## 9.7 BC1.2 DCP

When BC1.2 DCP is selected as the Active mode, UCS81003 discharges  $V_{BUS}$  and applies the BC1.2 DCP charger emulation profile per the specification. In BC1.2 DCP mode, the emulation timeout and requirement for portable device current draw are automatically disabled. When the BC1.2 DCP charger emulation profile is applied within the Dedicated Charger Emulation Cycle (see [Section 9.11.3 “Legacy 3 Charger Emulation Profile”](#)), the timeout and current draw requirement are enabled.

If the portable device is charging after the DCP charger emulation profile is applied, the UCS81003 leaves the resistive short in place, leaves the high-speed switch open and enables Constant Current Limiting (variable slope).

**Note:** BC1.2 compliance testing may require the S0 control to be set to '0' (Attach and Removal Detection feature disabled) while testing is in progress.

## 9.7.1 BC1.2 DCP CHARGER EMULATION PROFILE

The BC1.2 DCP charger emulation profile is described as follows:

1.  $V_{BUS}$  voltage is applied. A resistor ( $R_{DCP\_RES}$ ) is connected between the  $D_{POUT}$  and  $D_{MOUT}$  pins.
2. Primary Detection – if the portable device drives 0.6V (nominal) onto the  $D_{POUT}$  pin, the UCS81003 takes no other action than to leave the resistor connected between  $D_{POUT}$  and  $D_{MOUT}$ . This causes the portable device to see 0.6V (nominal) on the  $D_{MOUT}$  pin and know that it is connected to a DCP.
3. Optional Secondary Detection – If the portable device drives 0.6V (nominal) onto the  $D_{MOUT}$  pin, the UCS81003 takes no other action than to leave the resistor connected between  $D_{POUT}$  and  $D_{MOUT}$ . This causes the portable device to see 0.6V (nominal) on the  $D_{POUT}$  pin and know that it is connected to a DCP.

## 9.8 Dedicated Charger

When commanded to Dedicated Charger Emulation cycle mode, the UCS81003 enables an attached portable device to enter its charging mode by applying specific charger emulation profiles in a predefined sequence. Using these profiles, the UCS81003 is capable of generating and recognizing several signal levels on the  $D_{POUT}$  and  $D_{MOUT}$  pins. The preloaded charger emulation profiles include ones compatible with YD/T-1591 (2009), 12W charging, Samsung and many RIM portable devices. Other levels, sequences and protocols are configurable via the SMBus/I<sup>2</sup>C.

When a charger emulation profile is applied, a programmable timer for the emulation profile is started. When emulation timeout occurs, the UCS81003 checks the  $I_{BUS}$  current against a programmable threshold. If the current is above the threshold, the charger emulation profile is accepted and the associated current limiting mode is applied. No active USB data communication is possible when charging in this mode (by default – see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)).

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## 9.8.1 EMULATION RESET

Prior to applying any of the charger emulation profiles, the UCS81003 performs an Emulation Reset. This means that the UCS81003 resets the  $V_{BUS}$  line by disconnecting the port power switch and connecting  $V_{BUS}$  to ground via an internal  $100\Omega$  resistor for  $t_{DISCHARGE}$  time. The port power switch is held open for a time equal to  $t_{EM\_RESET}$  at which point the port power switch is closed and the  $V_{BUS}$  voltage is applied. The  $D_{P\_OUT}$  and  $D_{M\_OUT}$  pins are pulled low using internal  $15\text{ k}\Omega$  pull-down resistors.

**Note:** To help prevent possible damage to a portable device, the  $D_{P\_OUT}$  and  $D_{M\_OUT}$  pins have current limiting in place when the emulation profiles are applied.

## 9.8.2 EMULATION CYCLING

In Dedicated Charger Emulation Cycle mode, the charger emulation profiles, if enabled, are applied in the following order:

1. Legacy 1
2. Legacy 2
3. Legacy 3
4. Legacy 4
5. Legacy 5
6. Legacy 6
7. Legacy 7
8. Custom (disabled by default). If the  $CS\_FRST$  configuration bit is set, then the Custom charger emulation profile is tested first and the order proceeds as given.

If  $S0 = '0'$  and a portable device is not attached in DCE Cycle mode, the UCS81003 is cycling through charger emulation profiles (by default). There is no guarantee which charger emulation profile is applied first when a portable device is attached.

The UCS81003 applies a charger emulation profile until one of the following exit conditions occurs:

- Current greater than  $I_{BUS\_CHG}$  is detected flowing out of  $V_{BUS}$  at the respective emulation timeout time. In this case, the profile is assumed to be accepted and no other profiles is applied.
- The respective emulation timeout ( $t_{EM\_TIMEOUT}$ ) time is reached without current that exceeds the  $I_{BUS\_CHG}$  limit flowing out of  $V_{BUS}$  (the emulation timeout is enabled by default, see [Section 10.4.2 “Emulation Configuration Register”](#) and [Register 10-35](#)). The profile is assumed to be rejected, and the UCS81003 performs the Emulation Reset and applies the next profile, if any.

Emulation timeouts can be programmed for each charger emulation profile (see [Section 10.11 “Preloaded Emulation Timeout Configuration Registers”](#) and [Register 10-35](#)).

## 9.8.3 DCE CYCLE RETRY

If none of the charger emulation profiles cause a charge current to be drawn, the UCS81003 performs the Emulation Reset and cycles through the profiles again if the  $EM\_RETRY$  bit is set (default – see [Section 10.4.2 “Emulation Configuration Register”](#)). The UCS81003 continues to cycle through the profiles as long as charging current is not drawn and the  $PWR\_EN$  control is enabled. If the Emulation Retry is not enabled, the UCS81003 flags “No Handshake” and end the DCE Cycle using Trip Current Limiting.

## 9.9 Current Limit Mode Associations

The UCS81003 closes the port power switch and use the Current Limiting mode as shown in [Table 9-2](#).

**TABLE 9-2: CURRENT LIMIT MODE OPTIONS**

Active Mode	Current Limit Mode (See <a href="#">Section 10.14 “Current Limiting Behavior Configuration Registers”</a> )
Data Pass-Through	Trip mode
BC1.2 SDP	Trip mode
BC1.2 CDP	CC mode if $I_{LIM} < 1.68A$ , otherwise, Trip mode
BC1.2 DCP	CC mode if $I_{LIM} < 1.68A$ , otherwise, Trip mode
<b>DCE Cycle</b>	
During DCE Cycle when a charger emulation profile is being applied and the emulation timeout is active	CC mode if $I_{LIM} < 1.68A$ , otherwise, Trip mode

**Note 1:** As noted in the last three rows in [Table 9-2](#), under those specific conditions with  $I_{LIM} < 1.68A$ , it is the relationship of  $I_{LIM}$  and  $I_{BUS\_R2MIN}$  that determines the current limiting mode. In these cases, the value of  $I_{BUS\_R2MIN}$  is determined by  $CS\_R2\_IMIN<2:0>$  bits 4-2 in the Custom Current Limiting Behavior Configuration register – 51h ([Register 10-49](#)).

**TABLE 9-2: CURRENT LIMIT MODE OPTIONS (CONTINUED)**

Active Mode	Current Limit Mode (See Section 10.14 “Current Limiting Behavior Configuration Registers”)
Legacy 3 charger emulation profile accepted or the emulation timeout is disabled	CC mode if $I_{LIM} < 1.68A$ , otherwise, Trip mode
Legacy 1, Legacy 2 or Legacy 4 – Legacy 7 charger emulation profile accepted or the emulation timeout is disabled	Trip mode if $I_{BUS\_R2MIN} < I_{LIM}$ or $I_{LIM} > 1.68A$ (normal operation), otherwise, CC mode (see Register 10-49)
Custom charger emulation profile accepted or the emulation timeout is disabled	Trip mode if $I_{BUS\_R2MIN} < I_{LIM}$ or $I_{LIM} > 1.68A$ (normal operation), otherwise, CC mode (see Register 10-49)
No handshake (DCE Cycle with Emulation Retry not enabled)	Trip mode if $I_{BUS\_R2MIN} < I_{LIM}$ or $I_{LIM} > 1.68A$ (normal operation), otherwise, CC mode (see Register 10-49)

**Note 1:** As noted in the last three rows in Table 9-2, under those specific conditions with  $I_{LIM} < 1.68A$ , it is the relationship of  $I_{LIM}$  and  $I_{BUS\_R2MIN}$  that determines the current limiting mode. In these cases, the value of  $I_{BUS\_R2MIN}$  is determined by CS\_R2\_IMIN<2:0> bits 4-2 in the Custom Current Limiting Behavior Configuration register – 51h (Register 10-49).

## 9.10 No Handshake

In DCE Cycle mode with emulation retry disabled, a “No Handshake” condition is flagged. The NO\_HS status bit stays set (see Register 10-5) when the end of the DCE Cycle is reached without a handshake and without drawing current.

All signatures/handshaking placed on the  $D_{POUT}$  and  $D_{MOUT}$  pins are removed. The UCS81003 operates with the high-speed switch opened or closed as determined by the high-speed switch configuration, and uses Trip or Constant Current Limiting as determined by the  $I_{BUS\_R2MIN}$  setting (CS\_R2\_IMIN<2:0> bits 4-2 in the Custom Current Limiting Behavior Configuration register 51h).

The portable devices that can cause this are generally the ones that pull up  $D_{POUT}$  to some voltage and leave it there, or apply the wrong voltage.

## 9.11 Preloaded Charger Emulation Profiles

The following charger emulation profiles are resident to the UCS81003:

- [Legacy 1 Charger Emulation Profile](#)
- [Legacy 2, 4, 5, and 7 Charger Emulation Profiles](#)
- [Legacy 3 Charger Emulation Profile](#)
- [Legacy 6 Charger Emulation Profile](#)
- [BC1.2 CDP Charger Emulation Profile](#)
- [BC1.2 DCP Charger Emulation Profile](#)

### 9.11.1 LEGACY 1 CHARGER EMULATION PROFILE

Legacy 1 Charger Emulation Profile does the following:

1. The UCS81003 applies 900 mV to both the  $D_{POUT}$  and the  $D_{MOUT}$  pins.
2.  $V_{BUS}$  voltage is applied.

3. If the portable device draws more than  $I_{BUS\_CHG}$  current when the  $t_{EM\_TIMEOUT}$  timer expires, the UCS81003 accepts that the currently applied profile is the correct charger emulation profile for the attached portable device. Charging commences. The voltages applied to the  $D_{POUT}$  and  $D_{MOUT}$  pins remains in place (unless EM\_RESP is set to 0b). The UCS81003 begins to operate in Trip mode or CC mode as determined by the  $I_{BUS\_R2MIN}$  setting (see Section 10.14 “Current Limiting Behavior Configuration Registers”).
4. If the portable device does not draw more than  $I_{BUS\_CHG}$  current when  $t_{EM\_TIMEOUT}$  timer expires, the UCS81003 stops the currently applied charger emulation profile. This causes all voltages put onto the  $D_{POUT}$  and  $D_{MOUT}$  pins to be removed. Emulation Reset occurs, and the UCS81003 initiates the next charger emulation profile.

### 9.11.2 LEGACY 2, 4, 5, AND 7 CHARGER EMULATION PROFILES

Legacy 2, 4, 5, and 7 Charger Emulation Profiles follow the same pattern of operation, although the voltage that is applied on the  $D_{POUT}$  and  $D_{MOUT}$  pins varies. The profiles do the following:

1. The UCS81003 applies a voltage on the  $D_{POUT}$  pin using either a current-limited voltage source or a voltage divider between  $V_{BUS}$  and ground with the center tap on the  $D_{POUT}$  pin.
2. The UCS81003 applies a possibly different voltage on the  $D_{MOUT}$  pin, using either a current-limited voltage source or a voltage divider between  $V_{BUS}$  and ground, with the center tap on the  $D_{MOUT}$  pin.
3.  $V_{BUS}$  voltage is applied.

4. If the portable device draws more than  $I_{BUS\_CHG}$  current when the  $t_{EM\_TIMEOUT}$  timer expires, the UCS81003 accepts that the currently applied profile is the correct charger emulation profile for the attached portable device. Charging commences. The voltages applied to the  $D_{POUT}$  and  $D_{MOUT}$  pins remain in place (unless  $EM\_RESP$  is set to 0b). The UCS81003 begins operating in Trip mode or CC mode as determined by the  $I_{BUS\_R2MIN}$  setting (see [Section 10.14 “Current Limiting Behavior Configuration Registers”](#)).
5. If the portable device does not draw more than  $I_{BUS\_CHG}$  current when  $t_{EM\_TIMEOUT}$  timer expires, the UCS81003 stops the currently applied charger emulation profile. This causes all voltages put onto the  $D_{POUT}$  and  $D_{MOUT}$  pins to be removed. Emulation Reset occurs, and the UCS81003 initiates the next charger emulation profile.

Additionally, the user may build a charger emulation profile by determining the voltage and resistance characteristics that are placed on each of the  $D_{POUT}$  and  $D_{MOUT}$  pins. See [Section 9.12 “Custom Charger Emulation Profile”](#).

### 9.11.3 LEGACY 3 CHARGER EMULATION PROFILE

The Legacy 3 Charger Emulation Profile does the following:

1. The UCS81003 connects a resistor ( $R_{DCP\_RES}$ ) between  $D_{POUT}$  and  $D_{MOUT}$ .
2.  $V_{BUS}$  is applied.
3. If the portable device draws more than  $I_{BUS\_CHG}$  current when the  $t_{EM\_TIMEOUT}$  timer expires (enabled by default), the UCS81003 accepts that this is the correct charger emulation profile for the attached portable device. Charging commences. The resistive short between the  $D_{POUT}$  and  $D_{MOUT}$  pins is left in place.
4. If the portable device does not draw more than  $I_{BUS\_CHG}$  current when  $t_{EM\_TIMEOUT}$  timer expires, the UCS81003 stops the Legacy 3 Charger Emulation. This causes resistive short between the  $D_{POUT}$  and  $D_{MOUT}$  pins to be removed. Emulation Reset occurs, and the UCS81003 initiates the next charger emulation profile.

### 9.11.4 LEGACY 6 CHARGER EMULATION PROFILE

The Legacy 6 Charger Emulation Profile does the following:

1. The UCS81003 applies a voltage on the  $D_{POUT}$  pin using a voltage divider between  $V_{BUS}$  and ground with the center tap on the  $D_{POUT}$  pin.
2.  $V_{BUS}$  voltage is applied.
3. If the portable device draws more than  $I_{BUS\_CHG}$  current when the  $t_{EM\_TIMEOUT}$  timer expires, the UCS81003 accepts that Legacy 6 is the correct charger emulation profile for the attached portable device. Charging commences. The voltage applied to the  $D_{POUT}$  pin remains in place (unless  $EM\_RESP$  is set to 0b). The UCS81003 begins operating in Trip mode or CC mode as determined by the  $I_{BUS\_R2MIN}$  setting (see [Section 10.14 “Current Limiting Behavior Configuration Registers”](#)).
4. If the portable device does not draw more than  $I_{BUS\_CHG}$  current when  $t_{EM\_TIMEOUT}$  timer expires, the UCS81003 stops the Legacy 6 Charger Emulation Profile. This causes the voltage put onto the  $D_{POUT}$  pin to be removed. Emulation Reset occurs, and the UCS81003 initiates the next charger emulation profile.

## 9.12 Custom Charger Emulation Profile

The UCS81003 enables the user to create a Custom Charger emulation profile to handshake as any type of charger. This profile can be included in the DCE Cycle. In addition, it can be placed first or last in the profile sequence in the DCE Cycle. See [Register 10-35](#).

The Custom charger emulation profile uses a number of registers to define stimuli and behaviors. The Custom Charger emulation profile uses three separate stimulus/response pairs that are detected and applied in sequence, enabling flexibility to build any of the preloaded emulation profiles, or tailor the profile to match a specific charger application.

For details, see Application Note 24.14 – “*UCS1002 Fundamentals of Custom Charger Emulation*”.

## 10.0 REGISTER DESCRIPTION

The registers shown in [Table 10-1](#) are accessible through the SMBus or I<sup>2</sup>C. While in the Sleep state, the UCS81003 retains configuration and charge rationing data as indicated in the text. If a register does not indicate that data is retained in the Sleep power state, this information is lost when the UCS81003 enters the Sleep power state.

**TABLE 10-1: REGISTER SET IN HEXADECIMAL ORDER**

Register Address	Register Name	R/W	Function	Default Value	Page No.
00h	Current Measurement	R	Stores the current measurement	00h	<a href="#">47</a>
01h	Total Accumulated Charge High Byte	R	Stores the total accumulated charge delivered high byte	00h	<a href="#">48</a>
02h	Total Accumulated Charge Middle High Byte	R	Stores the total accumulated charge delivered middle high byte	00h	<a href="#">48</a>
03h	Total Accumulated Charge Middle Low Byte	R	Stores the total accumulated charge delivered middle low byte	00h	<a href="#">48</a>
04h	Total Accumulated Charge Low Byte	R	Stores the total accumulated charge delivered low byte	00h	<a href="#">48</a>
0Fh	Other Status	R	Indicates emulation status as well as the ALERT# and A_DET# pin status	00h	<a href="#">49</a>
10h	Interrupt Status	See <a href="#">Register 10-3</a>	Indicates why ALERT# pin asserted	00h	<a href="#">50</a>
11h	General Status	R/R-C	Indicates general status	00h	<a href="#">51</a>
12h	Profile Status 1	R	Indicates which charger emulation profile is accepted	00h	<a href="#">52</a>
13h	Profile Status 2	R		00h	<a href="#">53</a>
14h	Pin Status	R	Indicates the pin states of the internal control pins	00h	<a href="#">54</a>
15h	General Configuration	R/W	Controls basic functionality	01h	<a href="#">55</a>
16h	Emulation Configuration	R/W	Controls emulation functionality	8Ch	<a href="#">56</a>
17h	Switch Configuration	R/W	Controls advanced switch functions	04h	<a href="#">57</a>
18h	Attach Detect Configuration	R/W	Controls Attach Detect functionality	46h	<a href="#">58</a>
19h	Current Limit	R/W	Controls the maximum current limit	00h	<a href="#">60</a>
1Ah	Charge Rationing Threshold High Byte	R/W	Controls the Current Threshold I <sub>THRESH</sub> used by the charge rationing circuitry	FFh	<a href="#">60</a>
1Bh	Charge Rationing Threshold Low Byte	R/W	Controls the Current Threshold I <sub>THRESH</sub> used by the charge rationing circuitry	FFh	<a href="#">60</a>
1Ch	Auto-Recovery Configuration	R/W	Controls the Auto-Recovery functionality	2Ah	<a href="#">61</a>
1Eh	I <sub>BUS_CHG</sub> Configuration	R/W	Stores the limit for I <sub>BUS_CHG</sub> used to determine if emulation is successful	0Fh	<a href="#">62</a>
1Fh	t <sub>DET_CHARGE</sub> Configuration	R/W	Stores bits that define the t <sub>DET_CHARGE</sub> time	03h	<a href="#">63</a>
20h	BCS Emulation Enable	R/W	Enables BCS charger emulation profiles	16h	<a href="#">63</a>
21h	Legacy Emulation Enable	R/W	Enables Legacy charger emulation profiles	00h	<a href="#">64</a>
22h	BCS Emulation Timeout Config	R/W	Controls timeout for each BCS charger emulation profile	10h	<a href="#">65</a>

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**TABLE 10-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)**

Register Address	Register Name	R/W	Function	Default Value	Page No.
23h	Legacy Emulation Timeout Config 1	R/W	Controls timeout for Legacy charger emulation profiles 1 – 4	6Ch	65
24h	Legacy Emulation Timeout Config 2	R/W	Controls timeout for Legacy charger emulation profiles 5 – 7	01h	66
25h	High-Speed Switch Configuration	R/W	Controls when the high-speed switch is enabled	14h	59
30h	Applied Charger Emulation	R	Indicates which charger emulation profile is being applied	00h	67
31h	Preloaded Emulation Stimulus 1 – Config 1	R	Indicates the stimulus and timing for Stimulus 1	00h	67
32h	Preloaded Emulation Stimulus 1 – Config 2	R	Indicates the response and magnitude for Stimulus 1	26h	68
33h	Preloaded Emulation Stimulus 1 – Config 3	R	Indicates the threshold and pull-up/pull-down settings for Stimulus 1	00h	69
34h	Preloaded Emulation Stimulus 1 – Config 4	R	Indicates the resistor ratio for Stimulus 1	02h	70
35h	Preloaded Emulation Stimulus 2 – Config 1	R	Indicates the stimulus and timing for Stimulus 2	00h	71
36h	Preloaded Emulation Stimulus 2 – Config 2	R	Indicates the response and magnitude for Stimulus 2	09h	72
37h	Preloaded Emulation Stimulus 2 – Config 3	R	Indicates the threshold and pull-up/pull-down settings for Stimulus 2	00h	73
38h	Preloaded Emulation Stimulus 2 – Config 4	R	Indicates the resistor ratio for Stimulus 2	04h	74
39h	Preloaded Emulation Stimulus 3 – Config 1	R	Indicates the stimulus and timing for Stimulus 3 ( <b>CDP only</b> )	00h	75
3Ah	Preloaded Emulation Stimulus 3 – Config 2	R	Indicates the response and magnitude for Stimulus 3 ( <b>CDP only</b> )	00h	76
3Bh	Preloaded Emulation Stimulus 3 – Config 3	R	Indicates the threshold and pull-up/pull-down settings for Stimulus 3 ( <b>CDP only</b> )	00h	77
40h	Custom Emulation Config	R/W	Controls general configuration of the Custom charger emulation profile	01h	79
41h	Custom Stimulus/Response Pair 1 – Config 1	R/W	Sets the stimulus and timing for Stimulus 1	00h	80
42h	Custom Stimulus/Response Pair 1 – Config 2	R/W	Sets the response and magnitude for Stimulus 1	00h	81
43h	Custom Stimulus/Response Pair 1 – Config 3	R/W	Sets the threshold and pull-up/pull-down settings for Stimulus 1	00h	82
44h	Custom Stimulus/Response Pair 1 – Config 4	R/W	Sets the resistor ratio for Stimulus 1	00h	83
45h	Custom Stimulus/Response Pair 2 – Config 1	R/W	Sets the stimulus and timing for Stimulus 2	00h	84
46h	Custom Stimulus/Response Pair 2 – Config 2	R/W	Sets the response and magnitude for Stimulus 2	00h	85
47h	Custom Stimulus/Response Pair 2 – Config 3	R/W	Sets the threshold and pull-up/pull-down settings for Stimulus 2	00h	86
48h	Custom Stimulus/Response Pair 2 – Config 4	R/W	Sets the resistor ratio for Stimulus 2	00h	87



**TABLE 10-1: REGISTER SET IN HEXADECIMAL ORDER (CONTINUED)**

Register Address	Register Name	R/W	Function	Default Value	Page No.
49h	Custom Emulation Stimulus 3 – Config 1	R/W	Sets the stimulus and timing for Stimulus 3	00h	88
4Ah	Custom Stimulus/Response Pair 3 – Config 2	R/W	Sets the response and magnitude for Stimulus 3	00h	89
4Bh	Custom Stimulus/Response Pair 3 – Config 3	R/W	Sets the threshold and pull-up/pull-down settings for Stimulus 3	00h	90
4Ch	Custom Stimulus/Response Pair 3 – Config 4	R/W	Sets the resistor ratio for Stimulus 3	00h	91
50h	Applied Current Limiting Behavior	R	Indicates the applied current limiting behavior	82h	92
51h	Custom Current Limiting Behavior Config	R/W	Controls the custom current limiting behavior	82h	93
FDh	Product ID	R	Stores a fixed value that identifies each product	4Eh	94
FEh	Manufacturer ID	R	Stores a fixed value that identifies Microchip	5Dh	94
FFh	Revision	R	Stores a fixed value that represents the revision number	82h	94

During Power-On Reset (POR), the default values are stored in the registers. A POR is initiated when power is first applied to the part and the voltage on the  $V_{DD}$  supply surpasses the  $V_{DD\_TH}$  level as specified in the electrical characteristics. Any reads to undefined registers returns 00h. Writes to undefined registers do not have an effect.

When a bit is set, this means that the user writes a logic '1' to it. When a bit is cleared, this means that the user writes a logic '0' to it.

## 10.1 Current Measurement Register (Address 00h)

Name	Bits	Address	Cof	Default
Current Measurement	8	00h	R	00h

The Current Measurement register stores the measured current value delivered to the portable device ( $I_{BUS}$ ). This value is updated continuously while the device is in the Active power state. The bit weights are in mA and the range is from 0 mA to 2988.6A (the maximum value corresponds to 255 LSB, where 1 LSB = 11.72 mA).

This data is cleared when the device enters the Sleep or Detect states. This data is also cleared whenever the port power switch is turned OFF (including during emulation or any time that  $V_{BUS}$  is discharged).

## 10.2 Total Accumulated Charge Registers

Name	Bits	Address	Cof	Default
Total Accumulated Charge High Byte	8	01h	R	00h
Total Accumulated Charge Middle High	8	02h	R	00h
Total Accumulated Charge Middle Low Byte	8	03h	R	00h
Total Accumulated Charge Low Byte	8	04h	R	00h

The Total Accumulated Charge registers store the total accumulated charge delivered from the  $V_S$  source to a portable device. The bit weighting of the registers is given in mAh. The register value is reset to 00\_00h only when the RTN\_RST bit is set or if the RTN\_EN bit is cleared. This value is retained when the device transitions out of the Active state and resumes accumulation if the device returns to the Active state and charge rationing is still enabled.

These registers are updated every one (1) second while the UCS81003 is in the Active power state. Whenever the value is updated, it is compared against the target value in the Charge Rationing Threshold registers (see [Section 10.6 “Charge Rationing Threshold Registers”](#)).

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## REGISTER 10-1: TOTAL ACCUMULATED CHARGE REGISTER (ADDRESSES 01H – 04H)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC<25>	ACC<24>	ACC<23>	ACC<22>	ACC<21>	ACC<20>	ACC<19>	ACC<18>
bit 31						bit 24	

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC<17>	ACC<16>	ACC<15>	ACC<14>	ACC<13>	ACC<12>	ACC<11>	ACC<10>
bit 23						bit 16	

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ACC<9>	ACC<8>	ACC<7>	ACC<6>	ACC<5>	ACC<4>	ACC<3>	ACC<2>
bit 15						bit 8	

R-0	R-0	R-x	R-x	R-x	R-x	R-x	R-x
ACC<1>	ACC<0>	—	—	—	—	—	—
bit 7						bit 0	

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 31-6      **ACC<25:0>: Total Accumulated Charge**

1 LSB = 0.00325 mAh

bit 5-0      **Unimplemented**

## 10.3 Status Registers

Name	Bits	Address	Cof	Default
Other Status	8	0Fh	R	00h
Interrupt Status	8	10h	R/W	00h
General Status	8	11h	R/R-C	00h
Profile Status 1	8	12h	R	00h
Profile Status 2	8	13h	R	00h
Pin Status	8	14h	R	00h

The Status registers store bits that indicate error conditions as well as Attach Detection and Removal Detection. Unless otherwise noted, these bits operate as described when the UCS81003 is operating in Stand-Alone mode.



## REGISTER 10-2: OTHER STATUS REGISTER (ADDRESS 0FH)

U-x	U-x	R-0	R-0	R-0	R-0	R-0	R-0
—	—	ALERT_PIN	ADET_PIN	CHG_ACT	EM_ACT	EM_STEP<1:0>	
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 7-6      **Unimplemented**
- bit 5      **ALERT\_PIN:** Reflects the status of the ALERT# pin. This bit is set and cleared as the ALERT# pin changes states.  
 1 = ALERT# pin is asserted low  
 0 = ALERT# pin is released
- bit 4      **ADET\_PIN:** Reflects the status of the A\_DET# pin. When set, indicates that the A\_DET# pin is asserted low. This bit is set and cleared as the A\_DET# pin changes states. (**Note 1**)  
 1 = A\_DET# pin is asserted low  
 0 = A\_DET# pin is released
- bit 3      **CHG\_ACT:** This bit is automatically set when  $IBUS > I_{BUS\_CHG}$  and cleared when  $IBUS < I_{BUS\_CHG}$ . (**Note 2**)  
 1 =  $IBUS > I_{BUS\_CHG}$   
 0 =  $IBUS < I_{BUS\_CHG}$
- bit 2      **EM\_ACT:** Indicates that the UCS81003 is in the Active state and emulating. The actual profile that is being applied is identified by PRE\_EM\_SEL<3:0> (see **Section 10.12.1 “Applied Charger Emulation Register”**). This bit is set and automatically cleared. (**Note 3**)  
 1 = Device is in Active state and emulating  
 0 = Device is not emulating
- bit 1-0    **EM\_STEP<1:0>:** Indicates which stimulus/response pair is currently being applied by the charger emulation profile as shown below. These bits are set and automatically cleared. Note that the Legacy charger emulation profiles and the BC1.2 DCP charger emulation profile do not use Stimulus/Response Pair #3.  
 00 = None Applied. Waiting for current.  
 01 = Stimulus/Response #1  
 10 = Stimulus/Response #2  
 00 = Stimulus/Response #3 if applicable

- Note 1:** If S0 is '1', PWR\_EN is enabled, and  $V_S$  is not present, the ADET\_PIN bit cycles if the current draw exceeds the current capacity of the bypass switch.
- 2:** The CHG\_ACT bit does not indicate that a portable device has accepted one of the charger emulation profiles. This bit cycles during the Dedicated Charger Emulation Cycle.
- 3:** The EM\_ACT bit does not indicate that a portable device has accepted one of the emulation profiles. This bit cycles during the Dedicated Charger Emulation Cycle.

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## REGISTER 10-3: INTERRUPT STATUS REGISTER (ADDRESS 10H)

R/W-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
ERR	DISCH_ERR	RESET	KEEP_OUT	TSD	OV_VOLT	BACK_V	OV_LIM
bit 7							bit 0

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit  
'0' = Bit is cleared

x = Bit is unknown

- bit 7 **ERR:** Indicates that an error is detected and the device has entered the Error state. Writing this bit to a '0' clears the Error state and enables the device to return to the Active state. When written to '0', all error conditions are checked. If all error conditions are removed, the UCS81003 returns to the Active state. This bit is automatically set by the UCS81003 when the Error state is entered. Regardless of the fault handling mechanism used, if any other bit is set in the Interrupt Status register (10h), the device does not leave the Error state. ([Note 1](#) and [Note 2](#))  
This bit is automatically cleared by the UCS81003 if the Auto-Recovery Fault Handling functionality is active and no error conditions are detected. Likewise, this bit is cleared when the PWR\_EN control is disabled.  
1 = One or more errors are detected, and the UCS81003 has entered the Error state.  
0 = There are no errors detected.
- bit 6 **DISCH\_ERR:** Indicates that the UCS81003 is unable to discharge the  $V_{BUS}$  node. This bit is cleared when read if the error condition is removed or if the ERR bit is cleared. This bit causes the ALERT# pin to be asserted and the device to enter the Error state.  
1 = UCS81003 is unable to discharge the  $V_{BUS}$  node.  
0 = No  $V_{BUS}$  discharge error.
- bit 5 **RESET:** Indicates that the UCS81003 is on reset and must be reprogrammed. This bit is set at power-up. This bit is cleared when read or when the PWR\_EN control is toggled. The ALERT# pin is not asserted when this bit is set. This data is retained in the Sleep state.  
1 = UCS81003 is on reset.  
0 = Reset did not occur.
- bit 4 **KEEP\_OUT:** Indicates that the V-I output on the  $V_{BUS}$  pins has dropped below  $V_{BUS\_MIN}$ . This bit is cleared when read if the error condition is removed or if the ERR bit is cleared. This bit causes the ALERT# pin to be asserted and the device to enter the Error state.  
1 =  $V_{BUS} < V_{BUS\_MIN}$   
0 =  $V_{BUS} > V_{BUS\_MIN}$
- bit 3 **TSD:** Indicates that the internal temperature has exceeded  $T_{TSD}$  threshold and the device has entered the Error state. This bit is cleared when read if the error condition is removed or if the ERR bit is cleared. This bit causes the ALERT# pin to be asserted and the device to enter the Error state.  
1 = Internal temperature  $> T_{TSD}$   
0 = Internal temperature  $< T_{TSD}$
- bit 2 **OV\_VOLT:** Indicates that the  $V_S$  voltage has exceeded the  $V_{S\_OV}$  threshold and the device has entered the Error state. This bit is cleared when read, if the error condition is removed or if the ERR bit is cleared. This bit causes the ALERT# pin to be asserted and the device to enter the Error state.  
1 =  $V_S > V_{S\_OV}$   
0 =  $V_S < V_{S\_OV}$
- bit 1 **BACK\_V:** Indicates that the  $V_{BUS}$  voltage has exceeded the  $V_S$  or  $V_{DD}$  voltages by more than 150 mV. This bit is cleared when read if the error condition is removed or if the ERR bit is cleared. This bit causes the ALERT# pin to be asserted and the device to enter the Error state.  
1 =  $V_{BUS} > V_S$ , or  $V_{BUS} > V_{DD}$  by more than 150 mV  
0 =  $V_{BUS}$  voltage did not exceed the  $V_S$  and  $V_{DD}$  voltages by more than 150 mV

## REGISTER 10-3: INTERRUPT STATUS REGISTER (ADDRESS 10H) (CONTINUED)

bit 0 **OV\_LIM:** Indicates that the  $I_{BUS}$  current has exceeded both the  $I_{LIM}$  threshold and the  $I_{BUS\_R2MIN}$  threshold settings. This bit is cleared when read if the error condition is removed or if the ERR bit is cleared. This bit causes the ALERT# pin to be asserted and the device to enter the Error state.

1 =  $I_{BUS} > I_{LIM}$  and  $I_{BUS\_R2MIN}$

0 =  $I_{BUS}$  did not exceed both  $I_{LIM}$  threshold and the  $I_{BUS\_R2MIN}$  threshold settings

**Note 1:** If the Auto-Recovery Fault Handling is not used, the ERR bit must be written to a logic '0' to be cleared. It is also cleared when the PWR\_EN control is disabled.

**2:** Note that the ERR bit does not necessarily reflect the ALERT# pin status. The ALERT# pin may be cleared or asserted without the ERR bit changing states.

## REGISTER 10-4: GENERAL STATUS REGISTER (ADDRESS 11H)

R-0	U-x	U-x	R-0	R-0	R-C	R-C	R-C
RATION	—	—	CC_MODE	TREG	LOW_CUR	REM	ATT
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

C = Clear on Read

bit 7 **RATION:** Indicates that the UCS81003 has delivered the programmed amount of power to a portable device. If the RATION\_BEH bits are set to interrupt the host, this bit causes the ALERT# pin to be asserted. This bit is cleared when read. This bit is also automatically cleared when the RTN\_RST bit is set or the RTN\_EN bit is cleared (see [Section 10.4.1 "General Configuration Register"](#)).

1 = UCS81003 delivered the programmed amount of power to a portable device

0 = UCS81003 did not deliver the programmed amount of power to a portable device

bit 6-5 **Unimplemented**

bit 4 **CC\_MODE:** Indicates that the  $I_{BUS}$  current has exceeded  $I_{LIM}$ . Current is in Region 2 ( $I_{BUS\_R2MIN}$ ).

1 =  $I_{BUS} > I_{LIM}$

0 =  $I_{BUS} < I_{LIM}$

bit 3 **TREG:** Indicates that the internal temperature has exceeded  $T_{REG}$  and that the current limit is reduced. This bit is cleared when read and does not cause the ALERT# pin to be asserted, unless the ALERT\_LINK bit is set.

1 = Internal temperature  $> T_{REG}$

0 = Internal temperature  $< T_{REG}$

bit 2 **LOW\_CUR:** Indicates that a portable device has reduced its charge current to below ~6.4 mA and may be finished charging. This bit is cleared when read and does not cause the ALERT# pin to be asserted, unless the ALERT\_LINK bit is set.

1 =  $I_{BUS} < 6.4$  mA

0 =  $I_{BUS} > 6.4$  mA

bit 1 **REM:** Indicates that a Removal Detection event has occurred and there is no longer a portable device present. This bit is cleared when read and does not cause the ALERT# pin to be asserted. It causes the A\_DET# pin to be released.

1 = Removal Detected

0 = No Removal Detected

bit 0 **ATT:** Indicates that an Attach Detection event has occurred and there is a new portable device present. This bit is cleared when read and does not cause the ALERT# pin to be asserted. It causes the A\_DET# pin to be asserted.

1 = Attach Detected

0 = No Attach Detected

# UCS81003

## 10.3.1 PROFILE STATUS 1 REGISTER

These bits are indicators only and do not cause the ALERT# pin or A\_DET# pin to change states.

The CUST, DCP, CDP and PT bits are cleared under the following circumstances:

- the PWR\_EN control is disabled
- a new Active mode is selected
- a Removal Detection event occurs.

### REGISTER 10-5: PROFILE STATUS 1 REGISTER (ADDRESS 12H)

R-0	U-x	U-x	R-0	R-0	R-0	R-0	R-0
NO_HS	—	—	VS_LOW	CUST	DCP	CDP	PT
bit 7							bit 0

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 7     **NO\_HS:** The NO\_HS bit is only set during the Dedicated Charger Emulation Cycle (see [Section 9.10 “No Handshake”](#)). This bit is automatically cleared whenever a new charger emulation profile is applied. (**Note 1**)  
 1 = No handshake at the end of the DCE Cycle.  
 0 = A new charger emulation profile is applied
- bit 6-5   **Unimplemented**
- bit 4     **VS\_LOW:** Indicates that the  $V_S$  voltage is below the  $V_{S\_UVLO}$  threshold and the port power switch is held OFF. This bit is automatically cleared when the  $V_S$  voltage is above the  $V_{S\_UVLO}$  threshold.  
 1 =  $V_S < V_{S\_UVLO}$   
 0 =  $V_S > V_{S\_UVLO}$
- bit 3     **CUST:** Indicates that the portable device successfully performed a handshake with the user-defined Custom Charger Emulation Profile during the DCE Cycle and is charging. Based on the Custom Charger Emulation Profile configuration, the high-speed switch may either be open or closed (see [Section 10.13 “Custom Emulation Configuration Registers”](#)). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see [Section 10.14.2 “Custom Current Limiting Behavior Configuration Register”](#)).  
 1 = Custom Profile handshake complete  
 0 = No Custom Profile handshake
- bit 2     **DCP:** Indicates that the portable device accepted the BC1.2 DCP charger emulation profile and is charging. The high-speed switch is controlled via the HSW\_DCE bit (see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)), and the port power switch uses Constant Current Limiting.  
 1 = DCP handshake complete  
 0 = No DCP handshake
- bit 1     **CDP:** Indicates that the portable device successfully performed a handshake with the BC1.2 CDP charger emulation profile and is charging. The high-speed switch is closed, and the port power switch uses Trip Current Limiting.  
 1 = CDP handshake complete  
 0 = No CDP handshake
- bit 0     **PT:** Indicates that the UCS81003 is in the Data Pass-Through or BC1.2 SDP Active mode. The high-speed switch is closed, and the port power switch uses Trip Current Limiting. (**Note 2**)  
 1 = UCS81003 is in the Data Pass-Through or BC1.2 SDP Active mode.  
 0 = UCS81003 is not in the Data Pass-Through or BC1.2 SDP Active mode.

**Note 1:** The NO\_HS bit does not indicate that a portable device is drawing current and it may be cleared to '0' (indicating a handshake) and a portable device not charge. This bit is set at the end of each charger emulation profile if a portable device does not handshake with it. This bit is not set at the same time that any other Profile Status register bits are set.

**2:** When the UCS81003 is configured as a Data Pass-Through and a Removal event and then an Attach event occur without changing the Active mode, the PT bit is not set again even though the UCS81003 is still operating as a Data Pass-Through as configured. Toggling the M1 control re-enables the PT status bit.

## 10.3.2 PROFILE STATUS 2 REGISTER

These bits indicate which profile is accepted. These bits are indicators only and do not cause the ALERT# pin or A\_DET# pin to change states.

These bits are cleared under the following circumstances:

- the PWR\_EN control is disabled
- a new Active mode is selected
- a Removal Detection event occurs.

### REGISTER 10-6: PROFILE STATUS 2 REGISTER (ADDRESS 13H)

U-x	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	LG7	LG6	LG5	LG4	LG3	LG2	LG1
bit 7							bit 0

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **LG7:** Indicates that the portable device successfully performed a handshake with the Legacy 7 charger emulation profile and is charging. The high-speed switch is controlled via the HSW\_DCE bit (see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see [Section 10.14.2 “Custom Current Limiting Behavior Configuration Register”](#)).

- 1 = Handshake successful with the Legacy 7 charger emulation profile and charging.
- 0 = Not charging with Legacy 7 charger emulation profile.

bit 5 **LG6:** Indicates that the portable device successfully performed a handshake with the Legacy 6 charger emulation profile and is charging. The high-speed switch is controlled via the HSW\_DCE bit (see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see [Section 10.14.2 “Custom Current Limiting Behavior Configuration Register”](#)).

- 1 = Handshake successful with the Legacy 6 charger emulation profile and charging.
- 0 = Not charging with Legacy 6 charger emulation profile.

bit 4 **LG5:** Indicates that the portable device successfully performed a handshake with the Legacy 5 charger emulation profile and is charging. The high-speed switch is controlled via the HSW\_DCE bit (see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see [Section 10.14.2 “Custom Current Limiting Behavior Configuration Register”](#)).

- 1 = Handshake successful with the Legacy 5 charger emulation profile and charging.
- 0 = Not charging with Legacy 5 charger emulation profile.

bit 3 **LG4:** Indicates that the portable device successfully performed a handshake with the Legacy 4 charger emulation profile and is charging. The high-speed switch is controlled via the HSW\_DCE bit (see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see [Section 10.14.2 “Custom Current Limiting Behavior Configuration Register”](#)).

- 1 = Handshake successful with the Legacy 4 charger emulation profile and charging.
- 0 = Not charging with Legacy 4 charger emulation profile.

bit 2 **LG3:** Indicates that the portable device successfully performed a handshake with the Legacy 3 charger emulation profile and is charging. The high-speed switch is controlled via the HSW\_DCE bit (see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see [Section 10.14.2 “Custom Current Limiting Behavior Configuration Register”](#)).

- 1 = Handshake successful with the Legacy 3 charger emulation profile and charging.
- 0 = Not charging with Legacy 3 charger emulation profile.

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## REGISTER 10-6: PROFILE STATUS 2 REGISTER (ADDRESS 13H) (CONTINUED)

- bit 1 **LG2:** Indicates that the portable device successfully performed a handshake with the Legacy 2 charger emulation profile and is charging. The high-speed switch is controlled via the HSW\_DCE bit (see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see [Section 10.14.2 “Custom Current Limiting Behavior Configuration Register”](#)).
- 1 = Handshake successful with the Legacy 2 charger emulation profile and charging.
  - 0 = Not charging with Legacy 2 charger emulation profile.
- bit 0 **LG1:** Indicates that the portable device successfully performed a handshake with the Legacy 1 charger emulation profile and is charging. The high-speed switch is controlled via the HSW\_DCE bit (see [Section 10.4.5 “High-Speed Switch Configuration Register”](#)). The port power switch current limiting mode is determined by the Custom current limiting behavior settings (see [Section 10.14.2 “Custom Current Limiting Behavior Configuration Register”](#)).
- 1 = Handshake successful with the Legacy 1 charger emulation profile and charging.
  - 0 = Not charging with Legacy 1 charger emulation profile.

### 10.3.3 PIN STATUS REGISTER

The Pin Status register reflects the current pin state of the external control pins and identifies the power state. These bits are linked to the X\_SET bits (see [Section 10.4.3 “Switch Configuration Register”](#)).

## REGISTER 10-7: PIN STATUS REGISTER (ADDRESS 14H)

U-x	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	PWR_EN_PIN	M2_PIN	M1_PIN	EM_EN_PIN	SEL_PIN	PWR_STATE<1:0>	
bit 7							bit 0

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 7 **Unimplemented**
- bit 6 **PWR\_EN\_PIN:** Reflects the PWR\_EN control state. This bit is set and automatically cleared as the PWR\_EN pin/PWR\_ENS bit state changes.
- 1 = PWR\_EN is Logic 1
  - 0 = PWR\_EN is Logic 0
- bit 5 **M2\_PIN:** Reflects the M2 pin state. This bit is set and automatically cleared as the M2 pin/M2\_SET state changes.
- 1 = M2 is Logic 1
  - 0 = M2 is Logic 0
- bit 4 **M1\_PIN:** Reflects the M1 pin state. This bit is set and automatically cleared as the M1 pin/M1\_SET state changes.
- 1 = M1 is Logic 1
  - 0 = M1 is Logic 0
- bit 3 **EM\_EN\_PIN:** Reflects the EM\_EN pin state. This bit is set and automatically cleared as the EM\_EN pin/EM\_EN\_SET state changes.
- 1 = EM\_EN is Logic 1
  - 0 = EM\_EN Logic 0
- bit 2 **SEL\_PIN:** Reflects the polarity settings determined by the SEL pin decode. This bit is set or automatically cleared upon device power-up as the SEL pin is decoded.
- 1 = The PWR\_EN control is active-high
  - 0 = The PWR\_EN control is active-low

## REGISTER 10-7: PIN STATUS REGISTER (ADDRESS 14H) (CONTINUED)

- bit 1-0 **PWR\_STATE<1:0>**: Indicates the current power state. These bits are set and automatically cleared as the power state changes. ([Note 1](#))
- 00 = Sleep
  - 01 = Detect
  - 10 = Active
  - 11 = Error

**Note 1:** Accessing the SMBus/I<sup>2</sup>C causes the UCS81003 to leave the Sleep state. As a result, the PWR\_STATE<1:0> bits are never read as 00b.

## 10.4 Configuration Registers

Name	Bits	Address	Cof	Default
General Configuration	8	15h	R/W	01h
Emulation Configuration	8	16h	R/W	8Ch
Switch Configuration	8	17h	R/W	04h
Attach Detect Configuration	8	18h	R/W	46h
High-Speed Switch Configuration	8	25h	R/W	14h

The Configuration registers control basic device functionality.

### 10.4.1 GENERAL CONFIGURATION REGISTER

The contents of this register are retained in Sleep.

## REGISTER 10-8: GENERAL CONFIGURATION REGISTER (ADDRESS 15H)

R/W-0	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
ALERT_MASK	—	ALERT_LINK	DSCHG	RTN_EN	RTN_RST	RATION_BEH<1:0>	
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 7 **ALERT\_MASK**: Disables the ALERT# pin from asserting in the case of an error.
- 1 = The ALERT# pin is not asserted in the event of an error condition.
  - 0 = The ALERT# pin is asserted if an error condition or an indicator event is detected.
- bit 6 **Unimplemented**
- bit 5 **ALERT\_LINK**: Links the ALERT# pin to be asserted when the LOW\_CUR and/or TREG bits are set.
- 1 = The ALERT# pin is asserted if the LOW\_CUR or TREG indicator bit is set.
  - 0 = The ALERT# pin is not asserted if the LOW\_CUR or TREG indicator bit is set.
- bit 4 **DSCHG**: Forces the V<sub>BUS</sub> to reset and discharge when the UCS81003 is in the Active state. Writing this bit to a logic '1' causes the port power switch to be opened and the discharge circuitry to activate discharging V<sub>BUS</sub>. The port power switch remains open while this bit is '1'. This bit is not self-clearing.
- bit 3 **RTN\_EN**: Ration Enable – enables charge rationing functionality and power monitoring.
- 1 = Charge rationing is enabled (see [Section 7.4 “Battery Full”](#)).
  - 0 = Charge rationing is disabled. The Total Accumulated Charge registers are cleared to 00\_00h and current data is no longer accumulated. If the Total Accumulated Charge registers have reached the Charge Rationing Threshold (see [Section 10.6 “Charge Rationing Threshold Registers”](#)), the applied response is removed as though the charge rationing is placed on reset. This also clears the RATION status bit (if set).



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## REGISTER 10-8: GENERAL CONFIGURATION REGISTER (ADDRESS 15H) (CONTINUED)

- bit 2      **RTN\_RST:** Ration Reset – resets the charge rationing functionality. When this bit is set to ‘1’, the Total Accumulated Charge registers are reset to 00\_00h. In addition, when this bit is set, the RATION status bit is cleared and, if there are no other errors or active indicators, the ALERT# pin is released.
- 1 = EM\_EN is Logic 1  
0 = EM\_EN is Logic 0
- bit 1-0    **RATION\_BEH<1:0>:** Controls the behavior when the power rationing threshold is reached as shown in [Table 7-1](#).
- 00 = Report  
01 = Report and Disconnect  
10 = Disconnect and Go to Sleep  
11 = Ignore

### 10.4.2 EMULATION CONFIGURATION REGISTER

The contents of this register are retained in Sleep.

## REGISTER 10-9: EMULATION CONFIGURATION REGISTER (ADDRESS 16H)

R/W-1	U-x	U-x	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
DIS_TO	—	—	EM_TO_DIS	EM_RETRY	EM_RESP	EM_RESET_TIME<1:0>	
bit 7							bit 0

#### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit  
-n = Value at POR      ‘1’ = Bit is set      ‘0’ = Bit is cleared      x = Bit is unknown

- bit 7      **DIS\_TO:** Disable Timeout – Disables the Timeout and Idle Reset functionality (see [Section 11.2.1.6 “SMBus Timeout and Idle Reset”](#)).
- 1 = The Timeout and Idle Reset functionality is disabled. This is used for I<sup>2</sup>C compliance.  
0 = The Timeout and Idle Reset functionality is enabled.
- bit 6-5    **Unimplemented**
- bit 4      **EM\_TO\_DIS:** Emulation Timeout Disable – disables the emulation circuitry timeout for all charger emulation profiles in the DCE Cycle. There is a separate bit to enable/disable the emulation timeout for the Custom Charger Emulation profile ([Register 10-35](#)); however, if the EM\_TO\_DIS bit is set, the emulation timeout is also disabled for the Custom charger emulation profile. ([Note 1](#))
- 1 = Emulation timeout is disabled during the DCE Cycle. The applied charger emulation profile does not exit as a result of an emulation timeout event. The I<sub>BUS</sub> current is continuously checked and if it exceeds the I<sub>BUS\_CHG</sub> threshold for any reason, the charger emulation profile is accepted.  
0 = Emulation timeout is enabled during the DCE Cycle. An individual charger emulation profile is applied and maintained for the duration of the t<sub>EM\_TIMEOUT</sub> value. When this timer expires, the UCS81003 determines whether the charger emulation profile is successful and takes appropriate action.
- bit 3      **EM\_RETRY:** Configures whether the DCE Cycle must be reset or restarted if it reaches the final profile without the portable device drawing charging current and accepting one of the profiles. This bit is only used if the UCS81003 is configured to emulate a dedicated charger.
- 1 = Once the DCE Cycle is completed, it performs Emulation Reset and restarts from the first enabled charger emulation profile in the DCE Cycle.  
0 = Once the DCE Cycle is completed, it does not restart. The D<sub>POUT</sub> and D<sub>MOUT</sub> are left as High Z pins and the port power switch is closed. The Current Limiting mode is determined by the Custom Current Limiting Behavior settings (see [Section 10.14.2 “Custom Current Limiting Behavior Configuration Register”](#)).



## REGISTER 10-9: EMULATION CONFIGURATION REGISTER (ADDRESS 16H) (CONTINUED)

- bit 2      **EM\_RESP:** Leave Emulation Response – enables the Dedicated Charger Emulation Cycle mode to hold the  $D_{POUT}$  and  $D_{MOUT}$  stimulus response after the UCS81003 has finished emulation using the Legacy, BC1.2 DCP, or Custom charger emulation profiles (**Note 2**).
- 1 = If a portable device begins drawing charging current while the UCS81003 is applying the BC1.2 DCP, Custom or any of the Legacy charger emulation profiles during the DCE Cycle, the last response applied is kept in place until a Removal Detection event occurs, the internal temperature exceeds the  $T_{REG}$  value, or emulation is restarted. In the case of the BC1.2 DCP or Legacy 3 charger emulation profiles, this is the short ( $R_{DCP\_RES}$ ). In the case of the Legacy 1, Legacy 2 or Legacy 4-7 profiles, this is the  $D_{POUT}$  and  $D_{MOUT}$  pin voltages. If a portable device does not draw charging current, the DCE Cycle behaves normally.
- 0 = The dedicated emulation circuitry behaves normally. It removes the short condition when the  $t_{EM\_TIMEOUT}$  timer has expired, regardless if the portable device has drawn charging current or not.

- bit 1-0    **EM\_RESET\_TIME<1:0>:** Determines the length of the  $t_{EM\_RESET}$  time (see **Section 9.8.1 “Emulation Reset”**) as shown below. The value selected does not include discharge time; however, this value plus discharge result in the actual reset time.
- 00 = 50 ms  
 01 = 75 ms  
 10 = 125 ms  
 11 = 175 ms

- Note 1:** If the EM\_TO\_DIS bit is set and the Legacy 2, Legacy 4 or Custom charger emulation profiles are accepted during the DCE cycle, a removal is not detected. To avoid this issue, re-enable the emulation timeout after applying any test profiles and charging with the final profile.
- 2:** If the HSW\_DCE bit is set, the high-speed switch is closed regardless of the status of the EM\_RESP bit. Leaving the emulation response applied does not enable normal USB traffic. Therefore, prior to setting the HSW\_DCE bit, this bit must be cleared.

### 10.4.3 SWITCH CONFIGURATION REGISTER

The contents of this register are retained in Sleep.

## REGISTER 10-10: SWITCH CONFIGURATION REGISTER (ADDRESS 17H)

R/W-0	U-x	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
PIN_IGN	—	EM_EN_SET	M2_SET	M1_SET	S0_SET	PWR_ENS	LATCHS
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 7      **PIN\_IGN:** Ignores the M1, M2, PWR\_EN, and EM\_EN pin states when determining the Active mode selection and power state.
- 1 = The Active mode selection and power state are set by the individual control bits and not by the M1, M2, PWR\_EN, and EM\_EN pin states. These pin states are ignored.
- 0 = The Active mode selection and power state are set by the OR'd combination of the M1, M2, PWR\_EN, and EM\_EN pin states and the corresponding bit states.
- bit 6      **Unimplemented**
- bit 5      **EM\_EN\_SET:** In conjunction with other controls, determines the Active mode that is selected (see **Section 9.2 “Active Mode Selection”**) and power state (see **Table 5-2**). This bit is OR'd with the EM\_EN pin.
- bit 4      **M2\_SET:** In conjunction with other controls, determines the Active mode that is selected (see **Section 9.2 “Active Mode Selection”**) and power state (see **Table 5-2**). This bit is OR'd with the M2 pin.
- bit 3      **M1\_SET:** In conjunction with other controls, determines the Active mode that is selected (see **Section 9.2 “Active Mode Selection”**) and power state (see **Table 5-2**). This bit is OR'd with the M1 pin.

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## REGISTER 10-10: SWITCH CONFIGURATION REGISTER (ADDRESS 17H) (CONTINUED)

- bit 2      **S0\_SET:** In SMBus mode, enables the Attach and Removal Detection feature and affects the power state (see [Section 9.2 “Active Mode Selection”](#)).
- 1 = Detection is enabled. Also see [Table 5-2](#).  
0 = Detection is not enabled. Also see [Table 5-2](#).
- bit 1      **PWR\_ENS:** Controls whether the port power switch may be turned ON or not and affects the power state (see [Section 5.3.4 “PWR\\_EN Input”](#)). This bit is OR'd with the PWR\_EN pin and the polarity of both are controlled by SEL pin decode. Thus, if the polarity is set to active-high, either the PWR\_EN pin or this bit must be '1' to enable the port power switch.
- bit 0      **LATCHS:** In SMBus mode, controls the fault handling routine that is used in case an error is detected (see [Section 5.3.5 “Latch Input”](#)).
- 1 = The UCS81003 latches its error conditions. In order for the device to return to normal Active state, the ERR bit must be cleared by the user.  
0 = The UCS81003 automatically retries when an error condition is detected.

### 10.4.4 ATTACH DETECTION CONFIGURATION REGISTER

The contents of this register are retained in Sleep.

## REGISTER 10-11: ATTACH DETECTION CONFIGURATION REGISTER (ADDRESS 18H)

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0
RESERVED				DISCHG_TIME_SEL<1:0>		ATT_TH<1:0>	
bit 7							bit 0

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 7-4      **RESERVED:** Do not change.
- bit 3-2      **DISCHG\_TIME\_SEL<1:0>:** Sets the  $t_{DISCHARGE}$  time as follows:
- 00 = 100 ms  
01 = 200 ms  
10 = 300 ms  
11 = 400 ms
- bit 1-0      **ATT\_TH<1:0>:** Determines the Attach Detection threshold ( $I_{DET\_QUAL}$ ) and Removal Detection thresholds ( $I_{REM\_QUAL\_DET}$  and  $I_{REM\_QUAL\_ACT}$ ) as shown below. ([Note 1](#))
- 00 = 200  $\mu$ A Attach, 100  $\mu$ A Removal Threshold  
01 = 400  $\mu$ A Attach, 300  $\mu$ A Removal Threshold  
10 = 800  $\mu$ A Attach, 700  $\mu$ A Removal Threshold  
11 = 1000  $\mu$ A Attach, 900  $\mu$ A Removal Threshold

**Note 1:** The removal threshold is different when operating in the Active power state versus when operating in the Detect power state.

## 10.4.5 HIGH-SPEED SWITCH CONFIGURATION REGISTER

The contents of this register are retained in Sleep.

### REGISTER 10-12: HIGH-SPEED SWITCH CONFIGURATION REGISTER (ADDRESS 25H)

U-x	U-x	U-x	R/W-1	R/W-0	R/W-1	R/W-0	R/W-0
—	—	—	RESERVED	HSW_CUST	HSW_CDP	HSW_DET	HSW_DCE
bit 7							bit 0

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-5 **Unimplemented**

bit 4 **RESERVED:** Do not change.

bit 3 **HSW\_CUST:** Enables the USB high-speed data switch to be active during the Custom handshake. This control is checked at the beginning of charger emulation. Therefore, changing this control during emulation has no immediate effect. Upon restarting charger emulation (as a result of the EM\_RETRY bit being set, a Removal Detection event, or change of emulation controls), the high-speed switch is closed.

1 = The USB high-speed data switch is enabled while the Custom charger emulation profile is applied. Also, if the Custom charger emulation profile is accepted during the Dedicated Charger Emulation Cycle, the high-speed switch stays closed.

0 = The USB high-speed data switch is disabled while the Custom charger emulation profile is applied.

bit 2 **HSW\_CDP:** Enables the USB high-speed data switch to be active during the CDP handshake. This control is checked at the beginning of charger emulation. Therefore, changing this control during emulation has no immediate effect. Upon restarting charger emulation (as a result of a Removal Detection event or change of emulation controls), the high-speed switch is closed.

1 = The USB high-speed data switch is enabled during the CDP handshake.

0 = The USB high-speed data switch is disabled during the CDP handshake.

bit 1 **HSW\_DET:** Enables the USB high-speed data switch to be active during the Detect power state. If the S0 control is set to '0', this bit is ignored.

1 = The USB high-speed data switch is closed during the Detect power state.

0 = The USB high-speed data switch is open during the Detect power state.

bit 0 **HSW\_DCE:** Enables the USB high-speed data switch after the DCP charger emulation profile or one of the Legacy charger emulation profiles is accepted during the DCE Cycle and the portable device is charging. This bit is ignored if the UCS81003 is not in the Active state. This bit does not cause the high-speed switch to be closed during emulation when the DCP and Legacy profiles are applied, only after the DCP or a Legacy charger emulation profile is accepted.

1 = The USB high-speed data switch is closed.

0 = The USB high-speed data switch is open.

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## 10.5 Current Limit Register

Name	Bits	Address	Cof	Default
Current Limit	8	19h	R/W	00h

The Current Limit register controls the ILIM used by the port power switch. The default setting is based on the resistor on the COMM\_SEL/I<sub>LIM</sub> pin and this value cannot be changed to be higher than the hardware set value. The contents of this register are retained in Sleep.

### REGISTER 10-13: CURRENT LIMIT REGISTER (ADDRESS 19H)

U-x	U-x	U-x	U-x	U-x	R/W-0	R/W-0	R/W-0
—	—	—	—	—	ILIM_SW<2:0>		
bit 7					bit 0		

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 7-3 **Unimplemented**
- bit 2-0 **ILIM\_SW<2:0>**: Sets the I<sub>LIM</sub> value as follows:
  - 000 = 0.57A
  - 001 = 1.00A
  - 010 = 1.13A
  - 011 = 1.35A
  - 100 = 1.68A
  - 101 = 2.05A
  - 110 = 2.28A
  - 111 = 2.85A (3.0A maximum)

**Note 1:** Unless otherwise indicated, the values specified above are the typical I<sub>LIM</sub> in the [Table 1-2](#).

## 10.6 Charge Rationing Threshold Registers

Name	Bits	Address	Cof	Default
Charge Rationing Threshold High Byte	8	1Ah	R/W	FFh
Charge Rationing Threshold Low Byte	8	1Bh	R/W	FFh

Charge registers are updated, the value is checked against this limit. If the value meets or exceeds this limit, the RATION bit is set (see [Section 10.4.1 “General Configuration Register”](#)) and action taken according to the RATION\_BEH<1:0> bits (see [Section 10.4.1 “General Configuration Register”](#)).

The units are in mAh, with a range from 0 to ~218429. The contents of this register are retained in Sleep.

The Charge Rationing Threshold registers set the maximum allowed charge that is delivered to a portable device. Whenever the Total Accumulated

### REGISTER 10-14: CHARGE RATIONING THRESHOLD (ADDRESS 1AH - 1BH)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CHTHR<15>	CHTHR<14>	CHTHR<13>	CHTHR<12>	CHTHR<11>	CHTHR<10>	CHTHR<9>	CHTHR<8>
bit 15							bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
CHTHR<7>	CHTHR<6>	CHTHR<5>	CHTHR<4>	CHTHR<3>	CHTHR<2>	CHTHR<1>	CHTHR<0>
bit 7							bit 0

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-0 **CHTHR<15:1>**: Charge Rationing Threshold  
LSB = 3.333 mAh

## 10.7 Auto-Recovery Configuration Register

Name	Bits	Address	Cof	Default
Auto-Recovery Configuration	8	1Ch	R/W	2Ah

The contents of this register are retained in Sleep.

The Auto-Recovery Configuration register sets the parameters used when the Auto-Recovery Fault Handling algorithm is invoked (see [Section 7.5.1 “Auto-Recovery Fault Handling”](#)).

Once the Auto-Recovery Fault Handling algorithm has checked the overtemperature and back-drive conditions, it sets the  $I_{LIM}$  value to  $I_{TEST}$  and then turns ON the port power switch and starts the  $t_{RST}$  timer. If after the timer has expired, the  $V_{BUS}$  voltage is less than  $V_{TEST}$ , then it is assumed that a short-circuit condition is present and the Error state is reset.

### REGISTER 10-15: AUTO-RECOVERY CONFIGURATION REGISTER (ADDRESS 1CH)

U-x	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0	R/W-1	R/W-0
—	TCYCLE<2:0>			TRST_SW<1:0>		VTST_SW<1:0>	
bit 7							bit 0

#### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented**

bit 6-4 **TCYCLE<2:0>**: Defines the delay ( $t_{CYCLE}$ ) after the Error state is entered before the Auto-Recovery Fault Handling algorithm is started as shown below.

000 = 15 ms

001 = 20 ms

010 = 25 ms

011 = 30 ms

101 = 40 ms

110 = 45 ms

111 = 50 ms

bit 3-2 **TRST\_SW<1:0>**: Sets the  $t_{RST}$  time as shown as shown below.

00 = 10 ms

01 = 15 ms

10 = 20 ms

11 = 25 ms

bit 1-0 **VTST\_SW<1:0>**: Sets the  $V_{TEST}$  value as shown below.

00 = 250 mV

01 = 500 mV

10 = 750 mV

11 = 1000 mV

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## 10.8 IBUS\_CHG Configuration Register

Name	Bits	Address	Cof	Default
IBUS_CHG Configuration	8	1Eh	R/W	0Fh

The IBUS\_CHG Configuration register sets the  $I_{BUS\_CHG}$  current value. If current greater than  $I_{BUS\_CHG}$  is detected flowing out of  $V_{BUS}$ , emulation is successful. The bit weights are in mA, and the range is from 11.72 mA to 175.8 mA.

The contents of this register are not retained in Sleep.

### REGISTER 10-16: IBUS\_CHG CONFIGURATION REGISTER (ADDRESS 1EH)

U-x	U-x	U-x	U-x	R/W-1	R/W-1	R/W-1	R/W-1
—	—	—	—	ICHG<3>	ICHG<2>	ICHG<1>	ICHG<0>
bit 7				bit 0			

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4      **Unimplemented**  
bit 3-0      **ICHG<3:0>**  
                 1 LSB = 11.72 mA

## 10.9 TDET\_CHARGE Configuration Register

Name	Bits	Address	Cof	Default
TDET_CHARGE Configuration	8	1Fh	R/W	03h

The TDET\_CHARGE Configuration register controls the  $t_{DC\_TEMP}$  and  $t_{DET\_CHARGE}$  timing. The  $t_{DC\_TEMP}$  timer is started whenever the temperature exceeds  $T_{REG}$ . This timer is meant to give the system time to cool at the lower  $I_{LIM}$  setting before changing  $I_{LIM}$  again. The  $t_{DET\_CHARGE}$  timer is started whenever the  $V_{BUS}$  voltage is discharged and the bypass switch is reactivated. This timer is meant to be a time delay to enable the  $V_{BUS}$  capacitor to charge before detecting an Attach Detection event.

If  $t_{DET\_CHARGE}$  time is increased greater than 800 ms, larger bus capacitors can be accommodated; however, with a portable device present and  $PWR\_EN$  disabled, a Removal Detection event and then another Attach Detection event occurs.

The contents of this register are retained in Sleep.

## REGISTER 10-17: TDET\_CHARGE CONFIGURATION REGISTER (ADDRESS 1FH)

U-x	U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
—	—	—	DC_TEMP_SET<1:0>		DET_CHARGE_SET<2:0>		
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-5 **Unimplemented**

bit 4-3 **DC\_TEMP\_SET<1:0>**: Determines the  $t_{DC\_TEMP}$  time as shown below.

00 = 200 ms
01 = 400 ms
10 = 800 ms
11 = 1600 ms

bit 2-0 **DET\_CHARGE\_SET<2:0>**: Determines the  $t_{DET\_CHARGE}$  time as shown below.

000 = 200 ms
001 = 400 ms
010 = 600 ms
011 = 800 ms
100 = 1000 ms
101 = 1200 ms
110 = 1400 ms
111 = 2000 ms

## 10.10 Preloaded Emulation Enable Registers

Name	Bits	Address	Cof	Default
BCS Emulation Enable	8	20h	R/W	16h
Legacy Emulation Enable	8	21h	R/W	00h

The Preloaded Emulation Enable registers enable the charger emulation profiles used by the emulation circuitry. The contents of these registers are retained in Sleep.

## REGISTER 10-18: BCS EMULATION ENABLE REGISTER (ADDRESS 20H)

U-x	U-x	U-x	R/W-1	U-x	R/W-1	R/W-1	R/W-0
—	—	—	DCP_EM_DIS	—	RESERVED		
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-5 **Unimplemented**

bit 4 **DCP\_EM\_DIS**: Disables the DCP charger emulation profile in the DCE Cycle. This bit is ignored if the M1, M2, and EM\_EN control settings have selected the DCP mode (see [Table 9-1](#)).

1 = The BC1.2 DCP charger emulation profile is not enabled during the DCE Cycle.

0 = The BC1.2 DCP charger emulation profile is enabled during the Dedicated Charger Emulation Cycle.

bit 3 **Unimplemented**

bit 2-0 **RESERVED**: Do not change.

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## REGISTER 10-19: LEGACY EMULATION ENABLE REGISTER (ADDRESS 21H)

U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	L7EM_DIS	L6EM_DIS	L5EM_DIS	L4EM_DIS	L3EM_DIS	L2EM_DIS	L1EM_DIS
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 7            **Unimplemented**
- bit 6            **L7EM\_DIS:** Disables the Legacy 7 charger emulation profile.  
                   1 = The Legacy 7 charger emulation profile is not enabled.  
                   0 = The Legacy 7 charger emulation profile is enabled.
- bit 5            **L6EM\_DIS:** Disables the Legacy 6 charger emulation profile.  
                   1 = The Legacy 6 charger emulation profile is not enabled.  
                   0 = The Legacy 6 charger emulation profile is enabled.
- bit 4            **L5EM\_DIS:** Disables the Legacy 5 charger emulation profile.  
                   1 = The Legacy 5 charger emulation profile is not enabled.  
                   0 = The Legacy 5 charger emulation profile is enabled.
- bit 3            **L4EM\_DIS:** Disables the Legacy 4 charger emulation profile.  
                   1 = The Legacy 4 charger emulation profile is not enabled.  
                   0 = The Legacy 4 charger emulation profile is enabled.
- bit 2            **L3EM\_DIS:** Disables the Legacy 3 charger emulation profile.  
                   1 = The Legacy 3 charger emulation profile is not enabled.  
                   0 = The Legacy 3 charger emulation profile is enabled.
- bit 1            **L2EM\_DIS:** Disables the Legacy 2 charger emulation profile.  
                   1 = The Legacy 2 charger emulation profile is not enabled.  
                   0 = The Legacy 2 charger emulation profile is enabled.
- bit 0            **L1EM\_DIS:** Disables the Legacy 1 charger emulation profile.  
                   1 = The Legacy 1 charger emulation profile is not enabled.  
                   0 = The Legacy 1 charger emulation profile is enabled.

## 10.11 Preloaded Emulation Timeout Configuration Registers

Name	Bits	Address	Cof	Default
BCS Emulation Timeout Config	8	22h	R/W	10h
Legacy Emulation Timeout Config 1	8	23h	R/W	6Ch
Legacy Emulation Timeout Config 2	8	24h	R/W	01h

The Preloaded Emulation Timeout Configuration registers control the  $t_{EM\_TIMEOUT}$  setting that is applied whenever the indicated preloaded charger emulation profile is applied during the DCE Cycle. These settings are not used if the EM\_TO\_DIS bit is set.

The contents of this registers are retained in Sleep.



## REGISTER 10-20: BCS EMULATION TIMEOUT CONFIG REGISTER (ADDRESS 22H)

U-x	U-x	R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCP_EM_TO<1:0>		RESERVED			
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7-6                      **Unimplemented**

bit 5-4                      **DCP\_EM\_TO<1:0>**: Defines the  $t_{EM\_TIMEOUT}$  setting as shown below. This is applied when the BC1.2 DCP charger emulation profile is used during the DCE Cycle.

00 = 0.8s  
 01 = 1.6s  
 10 = 6.4s  
 00 = 12.8s

bit 3-0                      **RESERVED**: Do not change.

## REGISTER 10-21: LEGACY EMULATION TIMEOUT CONFIG 1 REGISTER (ADDRESS 23H)

R/W-0	R/W-1	R/W-1	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
L1EM_TO<1:0>		L2EM_TO<1:0>		L3EM_TO<1:0>		L4EM_TO<1:0>	
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7-6                      **L1EM\_TO<1:0>**: Defines the  $t_{EM\_TIMEOUT}$  setting as shown below. This is applied when the Legacy 1 charger emulation profile is used during the DCE Cycle.

00 = 0.8s  
 01 = 1.6s  
 10 = 6.4s  
 11 = 12.8s

bit 5-4                      **L2EM\_TO<1:0>**: Defines the  $t_{EM\_TIMEOUT}$  setting as shown below. This is applied when the Legacy 2 charger emulation profile is used during the DCE Cycle.

00 = 0.8s  
 01 = 1.6s  
 10 = 6.4s  
 11 = 12.8s

bit 3-2                      **L3EM\_TO<1:0>**: Defines the  $t_{EM\_TIMEOUT}$  setting as shown below. This is applied when the Legacy 3 charger emulation profile is used during the DCE Cycle.

00 = 0.8s  
 01 = 1.6s  
 10 = 6.4s  
 11 = 12.8s

bit 1-0                      **L4EM\_TO<1:0>**: Defines the  $t_{EM\_TIMEOUT}$  setting as shown below. This is applied when the Legacy 4 charger emulation profile is used during the DCE Cycle.

00 = 0.8s  
 01 = 1.6s  
 10 = 6.4s  
 11 = 12.8s

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## REGISTER 10-22: LEGACY EMULATION TIMEOUT CONFIG 2 REGISTER (ADDRESS 24H)

U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
—	—	L5EM_TO<1:0>		L6EM_TO<1:0>		L7EM_TO<1:0>	
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **L5EM\_TO<1:0>**: Defines the  $t_{EM\_TIMEOUT}$  setting as shown below. This is applied when the Legacy 5 charger emulation profile is used during the DCE Cycle.

- 00 = 0.8s
- 01 = 1.6s
- 10 = 6.4s
- 11 = 12.8s

bit 3-2 **L6EM\_TOV<1:0>**: Defines the  $t_{EM\_TIMEOUT}$  setting as shown below. This is applied when the Legacy 6 charger emulation profile is used during the DCE Cycle.

- 00 = 0.8s
- 01 = 1.6s
- 10 = 6.4s
- 11 = 12.8s

bit 1-0 **L7EM\_TO<1:0>**: Defines the  $t_{EM\_TIMEOUT}$  setting as shown below. This is applied when the Legacy 7 charger emulation profile is used during the DCE Cycle.

- 00 = 0.8s
- 01 = 1.6s
- 10 = 6.4s
- 11 = 12.8s

## 10.12 Preloaded Emulation Configuration Registers

Name	Bits	Address	Cof	Default
Applied Charger Emulation	8	30h	R	00h
Preloaded Emulation Stimulus 1 – Config 1	8	31h	R	00h
Preloaded Emulation Stimulus 1 – Config 2	8	32h	R	26h
Preloaded Emulation Stimulus 1 – Config 3	8	33h	R	00h
Preloaded Emulation Stimulus 1 – Config 4	8	34h	R	02h
Preloaded Emulation Stimulus 2 – Config 1	8	35h	R	00h
Preloaded Emulation Stimulus 2 – Config 2	8	36h	R	09h
Preloaded Emulation Stimulus 2 – Config 3	8	37h	R	00h
Preloaded Emulation Stimulus 2 – Config 4	8	38h	R	04h
Preloaded Emulation Stimulus 3 – Config 1	8	39h	R	00h
Preloaded Emulation Stimulus 3 – Config 2	8	3Ah	R	00h
Preloaded Emulation Stimulus 3 – Config 3	8	3Bh	R	00h

The Preloaded Emulation Configuration registers store the settings loaded from internal memory as required for the preloaded charger emulation profile that is actively being applied. These registers are read only.

The Legacy charger emulation profiles, the BC1.2 SDP and the BC1.2 DCP, do not use the Stimulus 3 Configuration registers (39h-3Bh). Whenever these charger emulation profiles are applied, registers 39h-3Bh are not updated and their contents must be ignored.

Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls are not updated and must be ignored. These settings are only used by the BC1.2 CDP and BC1.2 DCP charger emulation profiles.

The contents of registers 31h, 35h, and 39h are not retained in Sleep. These are updated as needed.

The contents of registers 32h, 33h, 34h, 36h, 37h, 38h, 3Ah, 3Bh, and 40h are retained in Sleep.

### 10.12.1 APPLIED CHARGER EMULATION REGISTER

The contents of this register are not retained in Sleep. The contents are updated as the charger emulation profile being applied changes.

## REGISTER 10-23: APPLIED CHARGER EMULATION REGISTER (ADDRESS 30H)

U-x	U-x	U-x	U-x	R-0	R-0	R-0	R-0
—	—	—	—	PRE_EM_SEL<3:0>			
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7-4                      **Unimplemented**

bit 3-0                      **PRE\_EM\_SEL<3:0>**: Indicates which of the charger emulation profiles is being actively applied as shown below.

- 0000 = Data Pass-Through or BC1.2 SDP
- 0001 = BC1.2 CDP
- 0010 = BC1.2 DCP
- 0011 = Legacy 1
- 0100 = Legacy 2
- 0101 = Legacy 3
- 0110 = Legacy 4
- 0111 = Legacy 5
- 1000 = Legacy 6
- 1001 = Legacy 7
- 1010 = Custom Profile
- All others = Not used

## REGISTER 10-24: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 1 REGISTER (ADDRESS 31H)

U-x	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	S1_TD_TYPE	S1_TD<2:0>			STIM1<2:0>		
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7                      **Unimplemented**

bit 6                      **S1\_TD\_TYPE**: Determines the behavior of the stimulus timer.

- 1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is immediately applied and held for the duration of the timer, and then removed if the stimulus is removed.
- 0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.

bit 5-3                      **S1\_TD<2:0>**: Determines the stimulus 1  $t_{STIM\_DEL}$  value as shown below.

- 000 = 0 ms
- 001 = 1 ms
- 010 = 5 ms
- 011 = 10 ms
- 100 = 20 ms
- 101 = 40 ms
- 110 = 80 ms
- 111 = 100 ms

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## REGISTER 10-24: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 1 REGISTER (ADDRESS 31H) (CONTINUED)

- bit 2-0 **STIM1<2:0>**: Determines the Stimulus 1 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV (UCS81003AM), or 470 mV (UCS81003AB), and only applies to the D<sub>POUT</sub> pin. This setting cannot be used for the D<sub>MOUT</sub> port.
- 000 = V<sub>BUS</sub> voltage ready to be applied before port power switch is closed. Next stimulus does not wait for this to be removed.
  - 001 = D<sub>POUT</sub> voltage is higher than the threshold (S1\_TH).
  - 010 = Window comparator. D<sub>POUT</sub> voltage is lower than the threshold (S1\_TH) and D<sub>POUT</sub> voltage higher than the fixed threshold.
  - 011 = D<sub>MOUT</sub> voltage is higher than the threshold (S1\_TH).
  - 100 = Do not use.
  - 101 = Do not use.
  - 110 = D<sub>POUT</sub> voltage is higher than the threshold (S1\_TH).
  - 111 = V<sub>BUS</sub> voltage is present after port power switch is closed. Next stimulus does not wait for this to be removed.

## REGISTER 10-25: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 2 REGISTER (ADDRESS 32H)

R-0	R-0	R-1	R-0	R-0	R-1	R-1	R-0
S1_R1MAG<3:0>				S1_R1<3:0>			
bit 7				bit 0			

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 7-4 **S1\_R1MAG<3:0>**: Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response is selected. Data written to any field that is identified as “Do not use” is not accepted. The data is not updated and the settings remain set at the previous value.
- For **S1\_R1 settings 0000-0011**, the response is a voltage applied on the D<sub>POUT</sub>/D<sub>MOUT</sub> pins. The S1\_R1MAG bits specify the voltage relative to ground:

0000 = Pull Down	0110 = 600 mV	1100 = 1800 mV
0001 = 400 mV	0111 = 700 mV	1101 = 2000 mV
0010 = 400 mV	1000 = 800 mV	1110 = 2200 mV
0011 = 400 mV	1001 = 900 mV	1111 = Do not use
0100 = 400 mV	1010 = 1400 mV	
0101 = 500 mV	1011 = 1600 mV	
  - For **S1\_R1 settings 0100, 0111, 1101-1111**, the response is a resistor connected on the D<sub>POUT</sub>/D<sub>MOUT</sub> to GND or V<sub>BUS</sub>. The S1\_R1MAG bits specify the resistor value:

0000 = 1.8 kΩ	0110 = 40 kΩ	1100 = 100 kΩ
0001 = 10 kΩ	0111 = 43 kΩ	1101 = 120 kΩ
0010 = 15 kΩ	1000 = 50 kΩ	1110 = 150 kΩ
0011 = 20 kΩ	1001 = 60 kΩ	1111 = Do not use
0100 = 25 kΩ	1010 = 75 kΩ	
0101 = 30 kΩ	1011 = 80 kΩ	
  - For **S1\_R1 settings 0110, 1001, 1100**, the response is a voltage divider applied from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub>/D<sub>MOUT</sub>. The S1\_R1MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2):

0000 = 93 kΩ	0110 = 200 kΩ	1100 = 200 kΩ
0001 = 100 kΩ	0111 = 200 kΩ	1101 = 200 kΩ
0010 = 125 kΩ	1000 = 93 kΩ	1110 = 200 kΩ
0011 = 150 kΩ	1001 = 100 kΩ	1111 = Do not use
0100 = 200 kΩ	1010 = 125 kΩ	
0101 = 200 kΩ	1011 = 150 kΩ	

## REGISTER 10-25: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 2 REGISTER (ADDRESS 32H) (CONTINUED)

- bit 3-0     **S1\_R1<3:0>**: Defines the stimulus response as shown below.
- 0000 = Remove previous response on D<sub>POUT</sub> and D<sub>MOU</sub>T
  - 0001 = Apply voltage on D<sub>POUT</sub> (Note 1).
  - 0010 = Apply voltage on D<sub>MOU</sub>T (Note 2).
  - 0011 = Apply voltage on D<sub>POUT</sub> and D<sub>MOU</sub>T.
  - 0100 = Connect resistor from D<sub>POUT</sub> to GND (Note 1).
  - 0101 = Do not use.
  - 0110 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> (Note 1).
  - 0111 = Connect resistor from D<sub>MOU</sub>T to GND (Note 2).
  - 1000 = Do not use.
  - 1001 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>MOU</sub>T (Note 2).
  - 1010 = Connect ≤ 200Ω resistor from D<sub>POUT</sub> to D<sub>MOU</sub>T.
  - 1011 = Do not use.
  - 1100 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> and D<sub>MOU</sub>T.
  - 1101 = Connect resistor from D<sub>POUT</sub> to GND and D<sub>MOU</sub>T to GND.
  - 1110 = If STIM1 = 000, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOU</sub>T during Emulation Reset are not removed. If STIM1 = 111, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOU</sub>T during Emulation Reset are removed. For all other STIM1 settings, whatever is applied is not changed.
  - 1111 = Same as 1110 case above.

- Note 1:** If STIM1<2:0> = 000<sub>b</sub> and no other response is applied to the D<sub>POUT</sub> pin, the 15 kΩ pull-down resistor applied to the D<sub>POUT</sub> pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>POUT</sub> pin (if applicable) or the 15 kΩ pull-down resistor is removed.
- 2:** If STIM1<2:0> = 000<sub>b</sub> and no other response is applied to the D<sub>MOU</sub>T pin, the 15 kΩ pull-down resistor applied to the D<sub>MOU</sub>T pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>MOU</sub>T pin (if applicable) or the 15 kΩ pull-down resistor is removed.

## REGISTER 10-26: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 3 REGISTER (ADDRESS 33H)(Note 1)

U-x	U-x	R-0	R-0	R-0	R-0	R-0	R-0
—	—	S1_PUPD<1:0>		S1_TH<3:0>			
bit 7							bit 0

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6     **Unimplemented**

- bit 5-4     **S1\_PUPD<1:0>**: Determines the magnitude of the pull-down current applied on the D<sub>POUT</sub> and D<sub>MOU</sub>T pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000<sub>b</sub>). The bit decode is given below.
- 00 = 10 μA
  - 01 = 50 μA
  - 10 = 100 μA
  - 11 = 150 μA

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## REGISTER 10-26: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 3 REGISTER (ADDRESS 33H)(Note 1) (CONTINUED)

bit 3-0      **S1\_TH<3:0>**: Defines the threshold value as shown below for the specified stimulus. If the stimulus is  $V_{BUS}$  voltage is ready to be applied or applied (that is,  $STIM1<2:0> = 000b$  or  $111b$ ), the threshold value is ignored.

0000 = 400 mV  
 0001 = 400 mV  
 0010 = 400 mV  
 0011 = 300 mV  
 0100 = 400 mV  
 0101 = 500 mV  
 0110 = 600 mV  
 0111 = 700 mV  
 1000 = 800 mV  
 1001 = 900 mV  
 1010 = 1400 mV  
 1011 = 1600 mV  
 1100 = 1800 mV  
 1101 = 2000 mV  
 1110 = 2200 mV  
 1111 = Do not use.

**Note 1:** The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls are not updated and must be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

## REGISTER 10-27: PRELOADED EMULATION STIMULUS 1 CONFIGURATION 4 REGISTER (ADDRESS 34H)(Note 1)

U-x	U-x	U-x	U-x	U-x	R-0	R-1	R-0
—	—	—	—	—	S1_RATIO<2:0>		
bit 7						bit 0	

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7-3      **Unimplemented**

bit 2-0      **S1\_RATIO<2:0>**: Determines the voltage divider ratio as shown below when the stimulus response is set to connect a voltage divider (that is,  $S1\_R1<3:0> = 0110b$ ,  $1001b$ , or  $1100b$ ).

000 = 0.25  
 001 = 0.33  
 010 = 0.4  
 011 = 0.5  
 100 = 0.54  
 101 = 0.6  
 110 = 0.66  
 111 = Do not use.

**Note 1:** The BC1.2 DCP and CDP charger emulation profiles do not use this control. Whenever the BC1.2 CDP or DCP charger emulation profile is applied, these controls are not updated and must be ignored. These settings are only used by the Legacy charger emulation profiles.

## REGISTER 10-28: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 1 REGISTER (ADDRESS 35H)

U-x	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	S2_TD_TYPE	S2_TD<2:0>			STIM2<2:0>		
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7 **Unimplemented**

bit 6 **S2\_TD\_TYPE:** Determines the behavior of the stimulus timer.

1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is immediately applied and held for the duration of the timer, and then removed if the stimulus is removed.

0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.

bit 5-3 **S2\_TD<2:0>:** Determines the Stimulus 2  $t_{\text{STIM\_DEL}}$  value as shown below.

000 = 0 ms

001 = 1 ms

010 = 5 ms

011 = 10 ms

100 = 20 ms

101 = 40 ms

110 = 80 ms

111 = 100 ms

bit 2-0 **STIM2<2:0>:** Determines the Stimulus 2 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV (UCS81003AM), or 470 mV (UCS81003AB), and only applies to the  $D_{\text{P\_OUT}}$  pin. This setting cannot be used for the  $DM_{\text{OUT}}$  port.

000 =  $V_{\text{BUS}}$  voltage ready to be applied before port power switch is closed. Next stimulus does not wait for this to be removed.

001 =  $D_{\text{P\_OUT}}$  voltage is greater than the threshold ( $S2\_TH$ ).

010 = Window comparator.  $D_{\text{P\_OUT}}$  voltage is lower than the threshold ( $S2\_TH$ ) and  $D_{\text{P\_OUT}}$  voltage greater than the fixed threshold.

011 =  $DM_{\text{OUT}}$  voltage is greater than the threshold ( $S2\_TH$ ).

100 = Do not use.

101 = Do not use.

110 =  $D_{\text{P\_OUT}}$  voltage is greater than the threshold ( $S2\_TH$ ).

111 = Voltage is present after the port power switch is closed. Next stimulus does not wait for this to be removed.

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## REGISTER 10-29: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 2 REGISTER (ADDRESS 36H)

R-0	R-0	R-0	R-0	R-1	R-0	R-0	R-1
S2_R2MAG<3:0>				S2_R2<3:0>			
bit 7				bit 0			

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **S2\_R2MAG<3:0>**: Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response is selected. Data written to any field that is identified as “Do not use” is not accepted. The data is not updated and the settings remain set at the previous value.

- For **S2\_R2 settings 0000-0011**, the response is a voltage applied on the D<sub>POUT</sub>/D<sub>MOUT</sub> pins. The S2\_R2MAG bits specify the voltage relative to ground:

0000 = Pull Down	0110 = 600 mV	1100 = 1800 mV
0001 = 400 mV	0111 = 700 mV	1101 = 2000 mV
0010 = 400 mV	1000 = 800 mV	1110 = 2200 mV
0011 = 400 mV	1001 = 900 mV	1111 = Do not use
0100 = 400 mV	1010 = 1400 mV	
0101 = 500 mV	1011 = 1600 mV	

- For **S2\_R2 settings 0100, 0111, 1101-1111**, the response is a resistor connected on the D<sub>POUT</sub>/D<sub>MOUT</sub> to GND or V<sub>BUS</sub>. The S2\_R2MAG bits specify the resistor value:

0000 = 1.8 kΩ	0110 = 40 kΩ	1100 = 100 kΩ
0001 = 10 kΩ	0111 = 43 kΩ	1101 = 120 kΩ
0010 = 15 kΩ	1000 = 50 kΩ	1110 = 150 kΩ
0011 = 20 kΩ	1001 = 60 kΩ	1111 = Do not use
0100 = 25 kΩ	1010 = 75 kΩ	
0101 = 30 kΩ	1011 = 80 kΩ	

- For **S2\_R2 settings 0110, 1001, 1100**, the response is a voltage divider applied from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub>/D<sub>MOUT</sub>. The S2\_R2MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2):

0000 = 93 kΩ	0110 = 200 kΩ	1100 = 200 kΩ
0001 = 100 kΩ	0111 = 200 kΩ	1101 = 200 kΩ
0010 = 125 kΩ	1000 = 93 kΩ	1110 = 200 kΩ
0011 = 150 kΩ	1001 = 100 kΩ	1111 = Do not use
0100 = 200 kΩ	1010 = 125 kΩ	
0101 = 200 kΩ	1011 = 150 kΩ	



## REGISTER 10-29: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 2 REGISTER (ADDRESS 36H) (CONTINUED)

- bit 3-0 **S2\_R2<3:0>**: Defines the stimulus response as shown below.
- 0000 = Remove previous response on D<sub>POUT</sub> and D<sub>MOUT</sub>
  - 0001 = Apply voltage on D<sub>POUT</sub> (Note 1).
  - 0010 = Apply voltage on D<sub>MOUT</sub> (Note 2).
  - 0011 = Apply voltage on D<sub>POUT</sub> and D<sub>MOUT</sub>.
  - 0100 = Connect resistor from D<sub>POUT</sub> to GND (Note 1).
  - 0101 = Do not use.
  - 0110 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> (Note 1).
  - 0111 = Connect resistor from D<sub>MOUT</sub> to GND (Note 2).
  - 1000 = Do not use.
  - 1001 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>MOUT</sub> (Note 2).
  - 1010 = Connect ≤ 200Ω resistor from D<sub>POUT</sub> to D<sub>MOUT</sub>.
  - 1011 = Do not use.
  - 1100 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> and D<sub>MOUT</sub>.
  - 1101 = Connect resistor from D<sub>POUT</sub> to GND and D<sub>MOUT</sub> to GND.
  - 1110 = If STIM2 = 000, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOUT</sub> during Emulation Reset are not removed. If STIM2 = 111, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOUT</sub> during Emulation Reset are removed. For all other STIM2 settings, whatever is applied is not changed.
  - 1111 = Same as 1110 case above.

**Note 1:** If STIM2<2:0> = 000b and no other response is applied to the D<sub>POUT</sub> pin, the 15 kΩ pull-down resistor applied to the D<sub>POUT</sub> pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>POUT</sub> pin (if applicable) or the 15 kΩ pull-down resistor is removed.

**2:** If STIM2<2:0> = 000b and no other response is applied to the D<sub>MOUT</sub> pin, the 15 kΩ pull-down resistor applied to the D<sub>MOUT</sub> pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>MOUT</sub> pin (if applicable) or the 15 kΩ pull-down resistor is removed.

## REGISTER 10-30: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 3 REGISTER (ADDRESS 37H)(Note 1)

U-x	U-x	R-0	R-0	R-0	R-0	R-0	R-0
—	—	S2_PUPD<1:0>		S2_TH<3:0>			
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **S2\_PUPD<1:0>**: Determines the magnitude of the pull-down current applied on the D<sub>POUT</sub> and D<sub>MOUT</sub> pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000b). The bit decode is as follows:

- 00 = 10 μA
- 01 = 50 μA
- 10 = 100 μA
- 11 = 150 μA

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## REGISTER 10-30: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 3 REGISTER (ADDRESS 37H)(Note 1) (CONTINUED)

bit 3-0 **S2\_TH<3:0>**: Defines the threshold value as shown below for the specified stimulus. If the stimulus  $V_{BUS}$  voltage is ready to be applied or applied (that is,  $STIM2<2:0> = 000b$  or  $111b$ ), the threshold value is ignored.

0000 = 400 mV  
 0001 = 400 mV  
 0010 = 400 mV  
 0011 = 300 mV  
 0100 = 400 mV  
 0101 = 500 mV  
 0110 = 600 mV  
 0111 = 700 mV  
 1000 = 800 mV  
 1001 = 900 mV  
 1010 = 1400 mV  
 1011 = 1600 mV  
 1100 = 1800 mV  
 1101 = 2000 mV  
 1110 = 2200 mV  
 1111 = Do not use.

**Note 1:** The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls are not updated and must be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

## REGISTER 10-31: PRELOADED EMULATION STIMULUS 2 CONFIGURATION 4 REGISTER (ADDRESS 38H)(Note 1)

U-x	U-x	U-x	U-x	U-x	R-1	R-0	R-0
—	—	—	—	—	S2_RATIO<2:0>		
bit 7					bit 0		

**Legend:**

R = Readable bit      W = Writable bit      U = Unimplemented bit  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 7-3 **Unimplemented**

bit 2-0 **S2\_RATIO<2:0>**: Determines the voltage divider ratio as shown below when the stimulus response is set to connect a voltage divider (that is,  $S2\_R2<3:0> = 0110b$ ,  $1001b$ , or  $1100b$ ).

000 = 0.25  
 001 = 0.33  
 010 = 0.4  
 011 = 0.5  
 100 = 0.54  
 101 = 0.6  
 110 = 0.66  
 111 = Do not use.

**Note 1:** The BC1.2 DCP and CDP charger emulation profiles do not use this control. Whenever the BC1.2 CDP or DCP charger emulation profile is applied, these controls are not updated and must be ignored. These settings are only used by the Legacy charger emulation profiles.

## REGISTER 10-32: PRELOADED EMULATION STIMULUS 3 CONFIGURATION 1 REGISTER (ADDRESS 39H)

U-x	R-0	R-0	R-0	R-0	R-0	R-0	R-0
—	S3_TD_TYPE	S3_TD<2:0>			STIM3<2:0>		
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7      **Unimplemented**

bit 6      **S3\_TD\_TYPE:** Determines the behavior of the stimulus timer.

1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is immediately applied and held for the duration of the timer, and then removed if the stimulus is removed.

0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.

bit 5-3    **S3\_TD<2:0>:** Determines the Stimulus 3  $t_{\text{STIM\_DEL}}$  value as shown below.

000 = 0 ms

001 = 1 ms

010 = 5 ms

011 = 10 ms

100 = 20 ms

101 = 40 ms

110 = 80 ms

111 = 100 ms

bit 2-0    **STIM3<2:0>:** Determines the Stimulus 3 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV (UCS81003AM), or 470 mV (UCS81003AB), and only applies to the  $D_{\text{POUT}}$  pin. This setting cannot be used for the  $DM_{\text{OUT}}$  port.

000 =  $V_{\text{BUS}}$  voltage ready to be applied before port power switch is closed. Next stimulus does not wait for this to be removed.

001 =  $D_{\text{POUT}}$  voltage is greater than the threshold (S3\_TH).

010 = Window comparator.  $D_{\text{POUT}}$  voltage is less than the threshold (S3\_TH) and  $D_{\text{POUT}}$  voltage greater than the fixed threshold.

011 =  $DM_{\text{OUT}}$  voltage is greater than the threshold (S3\_TH).

100 = Do not use.

101 = Do not use.

110 =  $D_{\text{POUT}}$  voltage is greater than the threshold (S3\_TH).

111 = Voltage is present after the port power switch is closed. Next stimulus does not wait for this to be removed.

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## REGISTER 10-33: PRELOADED EMULATION STIMULUS 3 CONFIGURATION 2 REGISTER (ADDRESS 3AH)

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
S3_R3MAG<3:0>				S3_R3<3:0>			
bit 7				bit 0			

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **S3\_R3MAG<3:0>**: Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response is selected. Data written to any field that is identified as “Do not use” is not accepted. The data is not updated and the settings remain set at the previous value.

- For **S3\_R3 settings 0000-0011**, the response is a voltage applied on the D<sub>POUT</sub>/D<sub>MOUT</sub> pins. The S3\_R3MAG bits specify the voltage relative to ground.

0000 = Pull Down	0110 = 600 mV	1100 = 1800 mV
0001 = 400 mV	0111 = 700 mV	1101 = 2000 mV
0010 = 400 mV	1000 = 800 mV	1110 = 2200 mV
0011 = 400 mV	1001 = 900 mV	1111 = Do not use
0100 = 400 mV	1010 = 1400 mV	
0101 = 500 mV	1011 = 1600 mV	

- For **S3\_R3 settings 0100, 0111, 1101-1111**, the response is a resistor connected on the D<sub>POUT</sub>/D<sub>MOUT</sub> to GND or V<sub>BUS</sub>. The S3\_R3MAG bits specify the resistor value.

0000 = 1.8 kΩ	0110 = 40 kΩ	1100 = 100 kΩ
0001 = 10 kΩ	0111 = 43 kΩ	1101 = 120 kΩ
0010 = 15 kΩ	1000 = 50 kΩ	1110 = 150 kΩ
0011 = 20 kΩ	1001 = 60 kΩ	1111 = Do not use
0100 = 25 kΩ	1010 = 75 kΩ	
0101 = 30 kΩ	1011 = 80 kΩ	

- For **S3\_R3 settings 0110, 1001, 1100**, the response is a voltage divider applied from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub>/D<sub>MOUT</sub>. The S3\_R3MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2).

0000 = 93 kΩ	0110 = 200 kΩ	1100 = 200 kΩ
0001 = 100 kΩ	0111 = 200 kΩ	1101 = 200 kΩ
0010 = 125 kΩ	1000 = 93 kΩ	1110 = 200 kΩ
0011 = 150 kΩ	1001 = 100 kΩ	1111 = Do not use
0100 = 200 kΩ	1010 = 125 kΩ	
0101 = 200 kΩ	1011 = 150 kΩ	

## REGISTER 10-33: PRELOADED EMULATION STIMULUS 3 CONFIGURATION 2 REGISTER (ADDRESS 3AH) (CONTINUED)

- bit 3-0 **S3\_R3<3:0>**: Defines the stimulus response as shown below.
- 0000 = Remove previous response on D<sub>POUT</sub> and D<sub>MOUT</sub>
  - 0001 = Apply voltage on D<sub>POUT</sub> (Note 1).
  - 0010 = Apply voltage on D<sub>MOUT</sub> (Note 2).
  - 0011 = Apply voltage on D<sub>POUT</sub> and D<sub>MOUT</sub>.
  - 0100 = Connect resistor from D<sub>POUT</sub> to GND (Note 1).
  - 0101 = Do not use.
  - 0110 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> (Note 1).
  - 0111 = Connect resistor from D<sub>MOUT</sub> to GND (Note 2).
  - 1000 = Do not use.
  - 1001 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>MOUT</sub> (Note 2).
  - 1010 = Connect ≤ 200Ω resistor from D<sub>POUT</sub> to D<sub>MOUT</sub>.
  - 1011 = Do not use.
  - 1100 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> and D<sub>MOUT</sub>.
  - 1101 = Connect resistor from D<sub>POUT</sub> to GND and D<sub>MOUT</sub> to GND.
  - 1110 = If STIM3 = 000, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOUT</sub> during Emulation Reset are not removed. If STIM3 = 111, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOUT</sub> during Emulation Reset are removed. For all other STIM3 settings, whatever is applied is not changed.
  - 1111 = Same as 1110 case above.

**Note 1:** If STIM3<2:0> = 000b and no other response is applied to the D<sub>POUT</sub> pin, the 15 kΩ pull-down resistor applied to the D<sub>POUT</sub> pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>POUT</sub> pin (if applicable) or the 15 kΩ pull-down resistor is removed.

**2:** If STIM3<2:0> = 000b and no other response is applied to the D<sub>MOUT</sub> pin, the 15 kΩ pull-down resistor applied to the D<sub>MOUT</sub> pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>MOUT</sub> pin (if applicable) or the 15 kΩ pull-down resistor is removed.

## REGISTER 10-34: PRELOADED EMULATION STIMULUS 3 CONFIGURATION 3 REGISTER (ADDRESS 3BH)(Note 1)

U-x	U-x	R-0	R-0	R-0	R-0	R-0	R-0
—	—	S3_PUPD<1:0>		S3_TH<3:0>			
bit 7							bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **S3\_PUPD<1:0>**: Determines the magnitude of the pull-down current applied on the D<sub>POUT</sub> and D<sub>MOUT</sub> pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000b). The bit decode is as follows:

- 00 = 10 μA
- 01 = 50 μA
- 10 = 100 μA
- 11 = 150 μA

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## REGISTER 10-34: PRELOADED EMULATION STIMULUS 3 CONFIGURATION 3 REGISTER (ADDRESS 3BH)(Note 1) (CONTINUED)

bit 3-0 **S3\_TH<3:0>**: Defines the threshold value as shown below for the specified stimulus. If the stimulus is  $V_{BUS}$  voltage is ready to be applied or applied (that is,  $STIM3<2:0> = 000b$  or  $111b$ ), the threshold value is ignored.

0000 = 400 mV

0001 = 400 mV

0010 = 400 mV

0011 = 300 mV

0100 = 400 mV

0101 = 500 mV

0110 = 600 mV

0111 = 700 mV

1000 = 800 mV

1001 = 900 mV

1010 = 1400 mV

1011 = 1600 mV

1100 = 1800 mV

1101 = 2000 mV

1110 = 2200 mV

1111 = Do not use.

**Note 1:** The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls are not updated and must be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

### 10.13 Custom Emulation Configuration Registers

Name	Bits	Address	Cof	Default
Custom Emulation Config	8	40h	R/W	01h
Custom Emulation Stimulus 1 – Config 1	8	41h	R/W	00h
Custom Emulation Stimulus 1 – Config 2	8	42h	R/W	00h
Custom Emulation Stimulus 1 – Config 3	8	43h	R/W	00h
Custom Emulation Stimulus 1 – Config 4	8	44h	R/W	00h
Custom Emulation Stimulus 2 – Config 1	8	45h	R/W	00h
Custom Emulation Stimulus 2 – Config 2	8	46h	R/W	00h
Custom Emulation Stimulus 2 – Config 3	8	47h	R/W	00h
Custom Emulation Stimulus 2 – Config 4	8	48h	R/W	00h
Custom Emulation Stimulus 3 – Config 1	8	49h	R/W	00h
Custom Emulation Stimulus 3 – Config 2	8	4Ah	R/W	00h
Custom Emulation Stimulus 3 – Config 3	8	4Bh	R/W	00h
Custom Emulation Stimulus 3 – Config 3	8	4Ch	R/W	00h

The Custom Emulation Configuration registers store the values used by the Custom Charger Emulation circuitry. The Custom Charger Emulation profile is set up as three stimuli and the respective responses.

The contents of registers 40h to 4Ch are retained in Sleep.

## REGISTER 10-35: CUSTOM EMULATION CONFIGURATION REGISTER (ADDRESS 40H)

U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-1
—	—	CS_TO_DIS	CS_EM_TO<1:0>	CS_FRST	RESERVED	CSEM_DIS	
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5 **CS\_TO\_DIS**: Disables the Emulation Timeout timer when the Custom Charger Emulation profile is applied during the DCE Cycle. If the EM\_TO\_DIS is set, this bit has no effect (**Note 1**).

1 = The Emulation Timeout timer is disabled when the Custom charger emulation profile is applied during the DCE Cycle. When the Custom charger emulation profile is applied, the UCS81003 constantly monitors the  $I_{BUS}$  current. When the  $I_{BUS}$  current is greater than  $I_{BUS\_CHG}$ , regardless of the reason, then the Custom Charger Emulation profile is accepted. If the portable device does not draw more than  $I_{BUS\_CHG}$  current, then the UCS81003 continues to wait until this bit is cleared.

0 = The Emulation Timeout timer is enabled when the Custom charger emulation profile is applied during the DCE Cycle and the EM\_TO\_DIS bit is not set.

bit 4-3 **CS\_EM\_TO<1:0>**: Determines the  $t_{EM\_TIMEOUT}$  value as shown below. This is used when the Custom charger emulation profile is used during the DCE Cycle.

00 = 0.8s

01 = 1.6s

10 = 6.4s

11 = 12.8s

bit 2 **CS\_FRST**: Disables the Custom charger emulation profile.

1 = The Custom charger emulation profile is the first of the profiles applied during the DCE Cycle.

0 = The Custom charger emulation profile is the last of the profiles applied during the DCE Cycle.

bit 1 **RESERVED**: Do not change. This bit reads as '0' and must not be written to a logic '1'.

bit 0 **CSEM\_DIS**: Determines whether the Custom charger emulation profile is placed first or last in the DCE Cycle.

1 = The Custom charger emulation profile is not enabled.

0 = The Custom charger emulation profile is enabled.

**Note 1:** If the CS\_TO\_DIS bit is set and the Custom charger emulation profile is accepted during the DCE cycle, a removal is not detected. To avoid this issue, re-enable the emulation timeout after applying any test profiles and charging with the final profile.

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## REGISTER 10-36: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 1 REGISTER (ADDRESS 41H)

U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W--0	R/W--0	R/W--0
—	CS_S1TYPE	CS_S1_TD<2:0>			CS_STIM1<2:0>		
bit 7							bit 0

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 7      **Unimplemented**
- bit 6      **CS\_S1TYPE:** Determines the behavior of the stimulus timer.
  - 1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is immediately applied and held for the duration of the timer, and then removed if the stimulus is removed.
  - 0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.
- bit 5-3    **CS\_S1\_TD<2:0>:** Determines the stimulus 1  $t_{STIM\_DEL}$  value as shown below.
  - 000 = 0 ms
  - 001 = 1 ms
  - 010 = 5 ms
  - 011 = 10 ms
  - 100 = 20 ms
  - 101 = 40 ms
  - 110 = 80 ms
  - 111 = 100 ms
- bit 2-0    **CS\_STIM1<2:0>:** Determines the Stimulus 1 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV (UCS81003AM), or 470 mV (UCS81003AB), and only applies to the D<sub>POUT</sub> pin. This setting cannot be used for the D<sub>MOU</sub>T port.
  - 000 = V<sub>BUS</sub> voltage ready to be applied before port power switch is closed. Next stimulus does not wait for this to be removed.
  - 001 = D<sub>POUT</sub> voltage is greater than the threshold (CS\_S1\_TH).
  - 010 = Window comparator. D<sub>POUT</sub> voltage is lower than the threshold (CS\_S1\_TH) and D<sub>POUT</sub> voltage greater than the fixed threshold.
  - 011 = D<sub>MOU</sub>T voltage is greater than the threshold (CS\_S1\_TH).
  - 100 = Do not use.
  - 101 = Do not use.
  - 110 = D<sub>POUT</sub> voltage is greater than the threshold (CS\_S1\_TH).
  - 111 = V<sub>BUS</sub> voltage is present after port power switch is closed. Next stimulus does not wait for this to be removed.



## REGISTER 10-37: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 2 REGISTER (ADDRESS 42H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CS_S1_R1MAG<3:0>				CS_S1_R1<3:0>			
bit 7				bit 0			

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit  
'0' = Bit is cleared

x = Bit is unknown

bit 7-4

**CS\_S1\_R1MAG<3:0>**: Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response is selected. Data written to any field that is identified as 'Do not use' is not accepted. The data is not updated and the settings remain set at the previous value.

- For **CS\_S1\_R1 settings 0000-0011**, the response is a voltage applied on the D<sub>POUT</sub>/D<sub>MOU</sub>T pins. The CS\_S1\_R1MAG bits specify the voltage relative to ground:

0000 = Pull Down	0110 = 600 mV	1100 = 1800 mV
0001 = 400 mV	0111 = 700 mV	1101 = 2000 mV
0010 = 400 mV	1000 = 800 mV	1110 = 2200 mV
0011 = 400 mV	1001 = 900 mV	1111 = Do not use
0100 = 400 mV	1010 = 1400 mV	
0101 = 500 mV	1011 = 1600 mV	

- For **CS\_S1\_R1 settings 0100, 0111, 1101-1111**, the response is a resistor connected on the D<sub>POUT</sub>/D<sub>MOU</sub>T to GND or V<sub>BUS</sub>. The CS\_S1\_R1MAG bits specify the resistor value:

0000 = 1.8 kΩ	0110 = 40 kΩ	1100 = 100 kΩ
0001 = 10 kΩ	0111 = 43 kΩ	1101 = 120 kΩ
0010 = 15 kΩ	1000 = 50 kΩ	1110 = 150 kΩ
0011 = 20 kΩ	1001 = 60 kΩ	1111 = Do not use
0100 = 25 kΩ	1010 = 75 kΩ	
0101 = 30 kΩ	1011 = 80 kΩ	

- For **CS\_S1\_R1 settings 0110, 1001, 1100**, the response is a voltage divider applied from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub>/D<sub>MOU</sub>T. The CS\_S1\_R1MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2):

0000 = 93 kΩ	0110 = 200 kΩ	1100 = 200 kΩ
0001 = 100 kΩ	0111 = 200 kΩ	1101 = 200 kΩ
0010 = 125 kΩ	1000 = 93 kΩ	1110 = 200 kΩ
0011 = 150 kΩ	1001 = 100 kΩ	1111 = Do not use
0100 = 200 kΩ	1010 = 125 kΩ	
0101 = 200 kΩ	1011 = 150 kΩ	

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## REGISTER 10-37: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 2 REGISTER (ADDRESS 42H) (CONTINUED)

- bit 3-0      **CS\_S1\_R1<3:0>**: Defines the stimulus response as shown below.
- 0000 = Remove previous response on D<sub>POUT</sub> and D<sub>MOUT</sub>.
  - 0001 = Apply voltage on D<sub>POUT</sub> (Note 1).
  - 0010 = Apply voltage on D<sub>MOUT</sub> (Note 2).
  - 0011 = Apply voltage on D<sub>POUT</sub> and D<sub>MOUT</sub>.
  - 0100 = Connect resistor from D<sub>POUT</sub> to GND (Note 1).
  - 0101 = Do not use.
  - 0110 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> (Note 1).
  - 0111 = Connect resistor from D<sub>MOUT</sub> to GND (Note 2).
  - 1000 = Do not use.
  - 1001 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>MOUT</sub> (Note 2).
  - 1010 = Connect ≤ 200Ω resistor from D<sub>POUT</sub> to D<sub>MOUT</sub>.
  - 1011 = Do not use.
  - 1100 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> and D<sub>MOUT</sub>.
  - 1101 = Connect resistor from D<sub>POUT</sub> to GND and D<sub>MOUT</sub> to GND.
  - 1110 = If CS\_STIM1 = 000, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOUT</sub> during Emulation Reset are not removed. If CS\_STIM1 = 111, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOUT</sub> during Emulation Reset are removed. For all other CS\_STIM1 settings, whatever is applied is not changed.
  - 1111 = Same as 1110 case above.

**Note 1:** If CS\_STIM1<2:0> = 000b and no other response is applied to the D<sub>POUT</sub> pin, the 15 kΩ pull-down resistor applied to the D<sub>POUT</sub> pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>POUT</sub> pin (if applicable) or the 15 kΩ pull-down resistor is removed.

**2:** If CS\_STIM1<2:0> = 000b and no other response is applied to the D<sub>MOUT</sub> pin, the 15 kΩ pull-down resistor applied to the D<sub>MOUT</sub> pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>MOUT</sub> pin (if applicable) or the 15 kΩ pull-down resistor is removed.

## REGISTER 10-38: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 3 REGISTER (ADDRESS 43H)(Note 1)

U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CS_S1_PUPD<1:0>		CS_S1_TH<3:0>			
bit 7							bit 0

### Legend:

R = Readable bit      W = Writable bit      U = Unimplemented bit  
 -n = Value at POR      '1' = Bit is set      '0' = Bit is cleared      x = Bit is unknown

bit 7-6      **Unimplemented**

bit 5-4      **CS\_S1\_PUPD<1:0>**: Determines the magnitude of the pull-down current applied on the D<sub>POUT</sub> and D<sub>MOUT</sub> pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000b). The bit decode is given below.

- 00 = 10 μA
- 01 = 50 μA
- 10 = 100 μA
- 11 = 150 μA

## REGISTER 10-38: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 3 REGISTER (ADDRESS 43H)(Note 1) (CONTINUED)

bit 3-0 **CS\_S1\_TH<3:0>**: Defines the threshold value as shown below for the specified stimulus. If the stimulus is  $V_{BUS}$  voltage is ready to be applied or applied (that is,  $CS\_STIM1<2:0> = 000b$  or  $111b$ ), the threshold value is ignored.

0000 = 400 mV  
 0001 = 400 mV  
 0010 = 400 mV  
 0011 = 300 mV  
 0100 = 400 mV  
 0101 = 500 mV  
 0110 = 600 mV  
 0111 = 700 mV  
 1000 = 800 mV  
 1001 = 900 mV  
 1010 = 1400 mV  
 1011 = 1600 mV  
 1100 = 1800 mV  
 1101 = 2000 mV  
 1110 = 2200 mV  
 1111 = Do not use.

**Note 1:** The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls are not updated and must be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

## REGISTER 10-39: CUSTOM EMULATION STIMULUS 1 CONFIGURATION 4 REGISTER (ADDRESS 44H)(Note 1)

U-x	U-x	U-x	U-x	U-x	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CS_S1_RATIO<2:0>		
bit 7					bit 0		

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7-3 **Unimplemented**

bit 2-0 **CS\_S1\_RATIO<2:0>**: Determines the voltage divider ratio as shown below when the stimulus response is set to connect a voltage divider (that is,  $CS\_S1\_R1<3:0> = 0110b$ ,  $1001b$ , or  $1100b$ ).

000 = 0.25  
 001 = 0.33  
 010 = 0.4  
 011 = 0.5  
 100 = 0.54  
 101 = 0.6  
 110 = 0.66  
 111 = Do not use.

**Note 1:** The BC1.2 DCP and CDP charger emulation profiles do not use this control. Whenever the BC1.2 CDP or DCP charger emulation profile is applied, these controls are not updated and must be ignored. These settings are only used by the Legacy charger emulation profiles.

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## REGISTER 10-40: CUSTOM EMULATION STIMULUS 2 CONFIGURATION 1 REGISTER (ADDRESS 45H)

U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CS_S2TYPE	CS_S2_TD<2:0>			CS_STIM2<2:0>		
bit 7							bit 0

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 7      **Unimplemented**
- bit 6      **CS\_S2TYPE:** Determines the behavior of the stimulus timer.
  - 1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is immediately applied and held for the duration of the timer, and then removed if the stimulus is removed.
  - 0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.
- bit 5-3    **CS\_S2\_TD<2:0>:** Determines the Stimulus 2  $t_{\text{STIM\_DEL}}$  value as shown below.
  - 000 = 0 ms
  - 001 = 1 ms
  - 010 = 5 ms
  - 011 = 10 ms
  - 100 = 20 ms
  - 101 = 40 ms
  - 110 = 80 ms
  - 111 = 100 ms
- bit 2-0    **CS\_STIM2<2:0>:** Determines the Stimulus 2 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV (UCS81003AM), or 470 mV (UCS81003AB), and only applies to the D<sub>POUT</sub> pin. This setting cannot be used for the DM<sub>OUT</sub> port.
  - 000 = V<sub>BUS</sub> voltage ready to be applied before port power switch is closed. Next stimulus does not wait for this to be removed.
  - 001 = D<sub>POUT</sub> voltage is greater than the threshold (CS\_S2\_TH).
  - 010 = Window comparator. D<sub>POUT</sub> voltage is less than the threshold (S1\_TH) and D<sub>POUT</sub> voltage greater than the fixed threshold.
  - 011 = DM<sub>OUT</sub> voltage is greater than the threshold (CS\_S2\_TH).
  - 100 = Do not use.
  - 101 = Do not use.
  - 110 = D<sub>POUT</sub> voltage is greater than the threshold (CS\_S2\_TH).
  - 111 = Voltage is present after the port power switch is closed. Next stimulus does not wait for this to be removed.

## REGISTER 10-41: CUSTOM EMULATION STIMULUS 2 CONFIGURATION 2 REGISTER (ADDRESS 46H)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CS_S2_R2MAG<3:0>				CS_S2_R2<3:0>			
bit 7				bit 0			

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit  
'0' = Bit is cleared

x = Bit is unknown

bit 7-4

**CS\_S2\_R2MAG<3:0>**: Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response is selected. Data written to any field that is identified as "Do not use" is not accepted. The data is not updated and the settings remain set at the previous value.

- For **CS\_S2\_R2 settings** 0000-0011, the response is a voltage applied on the D<sub>POUT</sub>/D<sub>MOUT</sub> pins. The CS\_S2\_R2MAG bits specify the voltage relative to ground.

0000 = Pull Down	0110 = 600 mV	1100 = 1800 mV
0001 = 400 mV	0111 = 700 mV	1101 = 2000 mV
0010 = 400 mV	1000 = 800 mV	1110 = 2200 mV
0011 = 400 mV	1001 = 900 mV	1111 = Do not use
0100 = 400 mV	1010 = 1400 mV	
0101 = 500 mV	1011 = 1600 mV	

- For **CS\_S2\_R2 settings** 0100, 0111, 1101-1111, the response is a resistor connected on the D<sub>POUT</sub>/D<sub>MOUT</sub> to GND or V<sub>BUS</sub>. The CS\_S2\_R2MAG bits specify the resistor value.

0000 = 1.8 kΩ	0110 = 40 kΩ	1100 = 100 kΩ
0001 = 10 kΩ	0111 = 43 kΩ	1101 = 120 kΩ
0010 = 15 kΩ	1000 = 50 kΩ	1110 = 150 kΩ
0011 = 20 kΩ	1001 = 60 kΩ	1111 = Do not use
0100 = 25 kΩ	1010 = 75 kΩ	
0101 = 30 kΩ	1011 = 80 kΩ	

- For **CS\_S2\_R2 settings** 0110, 1001, 1100, the response is a voltage divider applied from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub>/D<sub>MOUT</sub>. The CS\_S2\_R2MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2).

0000 = 93 kΩ	0110 = 200 kΩ	1100 = 200 kΩ
0001 = 100 kΩ	0111 = 200 kΩ	1101 = 200 kΩ
0010 = 125 kΩ	1000 = 93 kΩ	1110 = 200 kΩ
0011 = 150 kΩ	1001 = 100 kΩ	1111 = Do not use
0100 = 200 kΩ	1010 = 125 kΩ	
0101 = 200 kΩ	1011 = 150 kΩ	

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## REGISTER 10-41: CUSTOM EMULATION STIMULUS 2 CONFIGURATION 2 REGISTER (ADDRESS 46H) (CONTINUED)

- bit 3-0 **CS\_S2\_R2<3:0>**: Defines the stimulus response as shown below.
- 0000 = Remove previous response on D<sub>POUT</sub> and D<sub>MOU</sub>T
  - 0001 = Apply voltage on D<sub>POUT</sub> (Note 1).
  - 0010 = Apply voltage on D<sub>MOU</sub>T (Note 2).
  - 0011 = Apply voltage on D<sub>POUT</sub> and D<sub>MOU</sub>T.
  - 0100 = Connect resistor from D<sub>POUT</sub> to GND (Note 1).
  - 0101 = Do not use.
  - 0110 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> (Note 1).
  - 0111 = Connect resistor from D<sub>MOU</sub>T to GND (Note 2).
  - 1000 = Do not use.
  - 1001 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>MOU</sub>T (Note 2).
  - 1010 = Connect ≤ 200Ω resistor from D<sub>POUT</sub> to D<sub>MOU</sub>T.
  - 1011 = Do not use.
  - 1100 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> and D<sub>MOU</sub>T.
  - 1101 = Connect resistor from D<sub>POUT</sub> to GND and D<sub>MOU</sub>T to GND.
  - 1110 = If CS\_STIM2 = 000, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOU</sub>T during Emulation Reset are not removed. If CS\_STIM2 = 111, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOU</sub>T during Emulation Reset are removed. For all other CS\_STIM2 settings, whatever is applied is not changed.
  - 1111 = Same as 1110 case above.

**Note 1:** If CS\_STIM2<2:0> = 000b and no other response is applied to the D<sub>POUT</sub> pin, the 15 kΩ pull-down resistor applied to the D<sub>POUT</sub> pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>POUT</sub> pin (if applicable) or the 15 kΩ pull-down resistor is removed.

**2:** If CS\_STIM2<2:0> = 000b and no other response is applied to the D<sub>MOU</sub>T pin, the 15 kΩ pull-down resistor applied to the D<sub>MOU</sub>T pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>MOU</sub>T pin (if applicable) or the 15 kΩ pull-down resistor is removed.

## REGISTER 10-42: CUSTOM EMULATION STIMULUS 2 CONFIGURATION 3 REGISTER (ADDRESS 47H)(Note 1)

U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	CS_S2_PUPD<1:0>		CS_S2_TH<3:0>				
bit 7								bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **CS\_S2\_PUPD<1:0>**: Determines the magnitude of the pull-down current applied on the D<sub>POUT</sub> and D<sub>MOU</sub>T pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000b). The bit decode is as follows.

- 00 = 10 μA
- 01 = 50 μA
- 10 = 100 μA
- 11 = 150 μA

## REGISTER 10-42: CUSTOM EMULATION STIMULUS 2 CONFIGURATION 3 REGISTER (ADDRESS 47H)(Note 1) (CONTINUED)

bit 3-0 **CS\_S2\_TH<3:0>**: Defines the threshold value as shown below for the specified stimulus. If the stimulus is  $V_{BUS}$  voltage is ready to be applied or applied (that is,  $CS\_STIM2<2:0> = 000b$  or  $111b$ ), the threshold value is ignored.

0000 = 400 mV  
 0001 = 400 mV  
 0010 = 400 mV  
 0011 = 300 mV  
 0100 = 400 mV  
 0101 = 500 mV  
 0110 = 600 mV  
 0111 = 700 mV  
 1000 = 800 mV  
 1001 = 900 mV  
 1010 = 1400 mV  
 1011 = 1600 mV  
 1100 = 1800 mV  
 1101 = 2000 mV  
 1110 = 2200 mV  
 1111 = Do not use.

**Note 1:** The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls are not updated and must be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

## REGISTER 10-43: CUSTOM EMULATION STIMULUS 2 CONFIGURATION 4 REGISTER (ADDRESS 48H)(Note 1)

U-x	U-x	U-x	U-x	U-x	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CS_S2_RATIO<2:0>		
bit 7					bit 0		

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-3 **Unimplemented**

bit 2-0 **CS\_S2\_RATIO<2:0>**: Determines the voltage divider ratio as shown below when the stimulus response is set to connect a voltage divider (that is,  $CS\_S2\_R2<3:0> = 0110b$ ,  $1001b$ , or  $1100b$ ).

000 = 0.25  
 001 = 0.33  
 010 = 0.4  
 011 = 0.5  
 100 = 0.54  
 101 = 0.6  
 110 = 0.66  
 111 = Do not use.

**Note 1:** The BC1.2 DCP and CDP charger emulation profiles do not use this control. Whenever the BC1.2 CDP or DCP charger emulation profile is applied, these controls are not updated and must be ignored. These settings are only used by the Legacy charger emulation profiles.

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## REGISTER 10-44: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 1 REGISTER (ADDRESS 49H)

U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CS_S3TYPE	CS_S3_TD<2:0>			CS_STIM3<2:0>		
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit  
 -n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

bit 7                      **Unimplemented**

bit 6                      **CS\_S3TYPE:** Determines the behavior of the stimulus timer.

1 = The stimulus timer controls how long the response is applied after the stimulus is detected. The response is immediately applied and held for the duration of the timer, and then removed if the stimulus is removed.

0 = The stimulus timer is a delay from when the stimulus is detected until the response is performed.

bit 5-3                      **CS\_S3\_TD<2:0>:** Determines the Stimulus 3  $t_{\text{STIM\_DEL}}$  value as shown below.

000 = 0 ms

001 = 1 ms

010 = 5 ms

011 = 10 ms

100 = 20 ms

101 = 40 ms

110 = 80 ms

111 = 100 ms

bit 2-0                      **CS\_STIM3<2:0>:** Determines the Stimulus 3 that is used as shown below. Note that the lower threshold for the window comparator option is fixed at 400 mV (UCS81003AM), or 470 mV (UCS81003AB), and only applies to the  $D_{\text{POUT}}$  pin. This setting cannot be used for the  $DM_{\text{OUT}}$  port.

000 =  $V_{\text{BUS}}$  voltage ready to be applied before port power switch is closed. Next stimulus does not wait for this to be removed.

001 =  $D_{\text{POUT}}$  voltage is greater than the threshold (CS\_S3\_TH).

010 = Window comparator.  $D_{\text{POUT}}$  voltage is lower than the threshold (CS\_S3\_TH) and  $D_{\text{POUT}}$  voltage greater than the fixed threshold.

011 =  $DM_{\text{OUT}}$  voltage is greater than the threshold (CS\_S3\_TH).

100 = Do not use.

101 = Do not use.

110 =  $D_{\text{POUT}}$  voltage is greater than the threshold (CS\_S3\_TH).

111 = Voltage is present after the port power switch is closed. Next stimulus does not wait for this to be removed.



## REGISTER 10-45: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 2 REGISTER (ADDRESS 4AH)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CS_S3_R3MAG<3:0>				CS_S3_R3<3:0>			
bit 7				bit 0			

### Legend:

R = Readable bit  
-n = Value at POR

W = Writable bit  
'1' = Bit is set

U = Unimplemented bit  
'0' = Bit is cleared

x = Bit is unknown

bit 7-4

**CS\_S3\_R3MAG<3:0>**: Determines the magnitude of the response to the stimulus. The bit decode changes meaning based on which response is selected. Data written to any field that is identified as "Do not use" is not accepted. The data is not updated and the settings remain set at the previous value.

- For **CS\_S3\_R3 settings** 0000-0011, the response is a voltage applied on the D<sub>POUT</sub>/D<sub>MOU</sub>T pins. The CS\_S3\_R3MAG bits specify the voltage relative to ground.

0000 = Pull Down	0110 = 600 mV	1100 = 1800 mV
0001 = 400 mV	0111 = 700 mV	1101 = 2000 mV
0010 = 400 mV	1000 = 800 mV	1110 = 2200 mV
0011 = 400 mV	1001 = 900 mV	1111 = Do not use
0100 = 400 mV	1010 = 1400 mV	
0101 = 500 mV	1011 = 1600 mV	

- For **CS\_S3\_R3 settings** 0100, 0111, 1101-1111, the response is a resistor connected on the D<sub>POUT</sub>/D<sub>MOU</sub>T to GND or V<sub>BUS</sub>. The CS\_S3\_R3MAG bits specify the resistor value.

0000 = 1.8 kΩ	0110 = 40 kΩ	1100 = 100 kΩ
0001 = 10 kΩ	0111 = 43 kΩ	1101 = 120 kΩ
0010 = 15 kΩ	1000 = 50 kΩ	1110 = 150 kΩ
0011 = 20 kΩ	1001 = 60 kΩ	1111 = Do not use
0100 = 25 kΩ	1010 = 75 kΩ	
0101 = 30 kΩ	1011 = 80 kΩ	

- For **CS\_S3\_R3 settings** 0110, 1001, 1100, the response is a voltage divider applied from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub>/D<sub>MOU</sub>T. The CS\_S3\_R3MAG bits specify the minimum resistance of the voltage divider (Sum of R1 + R2).

0000 = 93 kΩ	0110 = 200 kΩ	1100 = 200 kΩ
0001 = 100 kΩ	0111 = 200 kΩ	1101 = 200 kΩ
0010 = 125 kΩ	1000 = 93 kΩ	1110 = 200 kΩ
0011 = 150 kΩ	1001 = 100 kΩ	1111 = Do not use
0100 = 200 kΩ	1010 = 125 kΩ	
0101 = 200 kΩ	1011 = 150 kΩ	

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## REGISTER 10-45: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 2 REGISTER (ADDRESS 4AH) (CONTINUED)

- bit 3-0 **CS\_S3\_R3<3:0>**: Defines the stimulus response as shown below.
- 0000 = Remove previous response on D<sub>POUT</sub> and D<sub>MOUT</sub>
  - 0001 = Apply voltage on D<sub>POUT</sub> (Note 1).
  - 0010 = Apply voltage on D<sub>MOUT</sub> (Note 2).
  - 0011 = Apply voltage on D<sub>POUT</sub> and D<sub>MOUT</sub>.
  - 0100 = Connect resistor from D<sub>POUT</sub> to GND (Note 1).
  - 0101 = Do not use.
  - 0110 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> (Note 1).
  - 0111 = Connect resistor from D<sub>MOUT</sub> to GND (Note 2).
  - 1000 = Do not use.
  - 1001 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>MOUT</sub> (Note 2).
  - 1010 = Connect ≤ 200Ω resistor from D<sub>POUT</sub> to D<sub>MOUT</sub>.
  - 1011 = Do not use.
  - 1100 = Connect voltage divider from V<sub>BUS</sub> to GND with the center tap at D<sub>POUT</sub> and D<sub>MOUT</sub>.
  - 1101 = Connect resistor from D<sub>POUT</sub> to GND and D<sub>MOUT</sub> to GND.
  - 1110 = If CS\_STIM3 = 000, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOUT</sub> during Emulation Reset are not removed. If CS\_STIM3 = 111, the 15 kΩ pull-down resistors applied to D<sub>POUT</sub> and D<sub>MOUT</sub> during Emulation Reset are removed. For all other CS\_STIM3 settings, whatever is applied is not changed.
  - 1111 = Same as 1110 case above.

**Note 1:** If CS\_STIM3<2:0> = 000b and no other response is applied to the D<sub>POUT</sub> pin, the 15 kΩ pull-down resistor applied to the D<sub>POUT</sub> pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>POUT</sub> pin (if applicable) or the 15 kΩ pull-down resistor is removed.

**2:** If CS\_STIM3<2:0> = 000b and no other response is applied to the D<sub>MOUT</sub> pin, the 15 kΩ pull-down resistor applied to the D<sub>MOUT</sub> pin during Emulation Reset is not removed. Otherwise, the previous response is left on the D<sub>MOUT</sub> pin (if applicable) or the 15 kΩ pull-down resistor is removed.

## REGISTER 10-46: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 3 REGISTER (ADDRESS 4BH)(Note 1)

U-x	U-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	CS_S3_PUPD<1:0>		CS_S3_TH<3:0>				
bit 7								bit 0

### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-6 **Unimplemented**

bit 5-4 **CS\_S3\_PUPD<1:0>**: Determines the magnitude of the pull-down current applied on the D<sub>POUT</sub> and D<sub>MOUT</sub> pins when the stimulus response is to apply a voltage and the voltage magnitude is set at pull-down (0000b). The bit decode is as follows.

- 00 = 10 μA
- 01 = 50 μA
- 10 = 100 μA
- 11 = 150 μA

## REGISTER 10-46: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 3 REGISTER (ADDRESS 4BH)(Note 1) (CONTINUED)

bit 3-0     **CS\_S3\_TH<3:0>**: Defines the threshold value as shown below for the specified stimulus. If the stimulus is  $V_{BUS}$  voltage is ready to be applied or applied (that is,  $CS\_STIM3<2:0> = 000b$  or  $111b$ ), the threshold value is ignored.

0000 = 400 mV  
 0001 = 400 mV  
 0010 = 400 mV  
 0011 = 300 mV  
 0100 = 400 mV  
 0101 = 500 mV  
 0110 = 600 mV  
 0111 = 700 mV  
 1000 = 800 mV  
 1001 = 900 mV  
 1010 = 1400 mV  
 1011 = 1600 mV  
 1100 = 1800 mV  
 1101 = 2000 mV  
 1110 = 2200 mV  
 1111 = Do not use.

**Note 1:** The Legacy charger emulation profiles do not use these settings. Whenever a Legacy charger emulation profile is applied within the DCE Cycle, these controls are not updated and must be ignored. These settings are only used by the BC1.2 CDP and DCP charger emulation profiles.

## REGISTER 10-47: CUSTOM EMULATION STIMULUS 3 CONFIGURATION 4 REGISTER (ADDRESS 4CH)(Note 1)

U-x	U-x	U-x	U-x	U-x	R/W-0	R/W-0	R/W-0
—	—	—	—	—	CS_S3_RATIO<2:0>		
bit 7					bit 0		

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 7-3     **Unimplemented**

bit 2-0     **CS\_S3\_RATIO<2:0>**: Determines the voltage divider ratio as shown below when the stimulus response is set to connect a voltage divider (that is,  $CS\_S3\_R3<2:0> = 0110b$ ,  $1001b$ , or  $1100b$ ).

000 = 0.25  
 001 = 0.33  
 010 = 0.4  
 011 = 0.5  
 100 = 0.54  
 101 = 0.6  
 110 = 0.66  
 111 = Do not use

**Note 1:** The BC1.2 DCP and CDP charger emulation profiles do not use this control. Whenever the BC1.2 CDP or DCP charger emulation profile is applied, these controls are not updated and must be ignored. These settings are only used by the Legacy charger emulation profiles.

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## 10.14 Current Limiting Behavior Configuration Registers

Name	Bits	Address	Cof	Default
Applied Current Limiting Behavior	8	50h	R	82h
Custom Current Limiting Behavior Config	8	51h	R/W	82h

### 10.14.1 APPLIED CURRENT LIMITING BEHAVIOR REGISTER

The Applied Current Limiting Behavior Register stores the values used by the applied current limiting mode (Trip or CC) when the custom settings are not used. The contents of this register are automatically updated when charger emulation is completed.

#### REGISTER 10-48: APPLIED CURRENT LIMITING BEHAVIOR REGISTER (ADDRESS 50H)

R-1	R-0	U-x	R-0	R-0	R-0	R-1	R-0
SEL_VBUS_MIN<1:0>		—	SEL_R2_IMIN<2:0>			RESERVED	
bit 7						bit 0	

<b>Legend:</b>			
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **SEL\_VBUS\_MIN<1:0>**: Define the  $V_{BUS\_MIN}$  voltage as follows:

- 00 = 1.5V
- 01 = 1.75V
- 10 = 2.0V
- 11 = 2.25V

bit 5 **Unimplemented**

bit 4-2 **SEL\_R2\_IMIN<2:0>**: Define the  $I_{BUS\_R2MIN}$  current as follows:

- 000 = 120 mA
- 001 = 570 mA
- 010 = 1000 mA
- 011 = 1350 mA
- 100 = 1680 mA
- 101 = 2050 mA

bit 1-0 **RESERVED**: Do not change.

**Note 1:** The values specified above are the typical ones.

## 10.14.2 CUSTOM CURRENT LIMITING BEHAVIOR CONFIGURATION REGISTER

The Custom Current Limiting Behavior Configuration Register enables programming of current limit parameters. These controls are used when a portable device handshakes using the Legacy charger emulation profiles (except Legacy 3), the Custom charger emulation profile, or does not handshake as a dedicated charger (that is, a power thief).

The contents of this register are retained in Sleep.

### REGISTER 10-49: CUSTOM CURRENT LIMITING BEHAVIOR CONFIG REGISTER (ADDRESS 51H)

R/W-1	R/W-0	U-x	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
CS_VBUS_MIN<1:0>		—	CS_R2_IMIN<2:0>			RESERVED	
bit 7						bit 0	

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **CS\_VBUS\_MIN<1:0>**: Defines the Custom  $V_{BUS\_MIN}$  voltage as shown below. Note that  $V_{BUS\_MIN}$  is checked even when operating with Trip Current Limiting.

00 =	1.5V
01 =	1.75V
10 =	2.0V
11 =	2.25V

bit 5 **Unimplemented**

bit 4-2 **CS\_R2\_IMIN<2:0>**: Define the Custom  $I_{BUS\_R2MIN}$  threshold as shown below. The default is 120 mA. This value is used under the following conditions: when a portable device handshakes using the Legacy charger emulation profiles (except Legacy 3) the Custom charger emulation profile, or when it does not handshake in DCE Cycle (that is, a power thief). Under these conditions, the current limiting mode is determined by the relative value of  $I_{BUS\_R2MIN}$  and  $I_{LIM}$ . When  $I_{BUS\_R2MIN} \leq I_{LIM}$  or  $I_{LIM} > 1.68$  A, Trip Current Limiting used; otherwise, CC mode is used.

Define the  $I_{BUS\_R2MIN}$  current as follows.

000 =	120 mA
001 =	570 mA
010 =	1000 mA
011 =	1350 mA
100 =	1680 mA
101 =	2050 mA

bit 1-0 **RESERVED**: Do not change.

**Note 1:** The values specified above are the typical ones.

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## 10.15 Product ID Register

Name	Bits	Address	Cof	Default
Product ID	8	FDh	R	4Eh

The Product ID register stores a unique 8-bit value that identifies the UCS device family.

## 10.16 Manufacturer ID Register

Name	Bits	Address	Cof	Default
Manufacturer ID	8	FEh	R	5Dh

The Manufacturer ID register stores a unique 8-bit value that identifies Microchip Technology Inc.

## 10.17 Revision Register

Name	Bits	Address	Cof	Default
Revision	8	FFh	R	82h

The Revision register stores an 8-bit value that represents the part revision.

## 11.0 COMMUNICATIONS

### 11.1 Operating Mode

The UCS81003 can operate in SMBus mode (see [Section 11.2 “SMBus Operating Mode”](#)) or Stand-Alone mode (see [Section 11.3 “Stand-Alone Operating Mode”](#)). The resistor on the COMM\_SEL/I<sub>LIM</sub> pin determines the operating mode and the hardware-set I<sub>LIM</sub> setting as shown in [Table 11-1](#). Unless connected to GND or V<sub>DD</sub>, the resistors in [Table 11-1](#) are pull-down resistors.

**Note:** If it is necessary to connect the COMM\_SEL/I<sub>LIM</sub> pin to V<sub>DD</sub> via a pull-up resistor, it is recommended that this resistor value does not exceed 100 kΩ.

**TABLE 11-1: UCS81003 COMMUNICATION MODE AND I<sub>LIM</sub> SELECTION (Note 1)**

SELECTION Resistor ±5%	I <sub>LIM</sub> Setting	Communications Mode
GND	570 mA	SMBus – see <a href="#">Section 11.2.1.2</a>
10 kΩ pull-down resistor	1000 mA	SMBus – see <a href="#">Section 11.2.1.2</a>
12 kΩ pull-down resistor	1130 mA	SMBus – see <a href="#">Section 11.2.1.2</a>
15 kΩ pull-down resistor	1350 mA	SMBus – see <a href="#">Section 11.2.1.2</a>
18 kΩ pull-down resistor	1680 mA	SMBus – see <a href="#">Section 11.2.1.2</a>
22 kΩ pull-down resistor	2050 mA	SMBus – see <a href="#">Section 11.2.1.2</a>
27 kΩ pull-down resistor	2280 mA	SMBus – see <a href="#">Section 11.2.1.2</a>
33 kΩ pull-down resistor	2850 mA (3000 mA maximum)	SMBus – see <a href="#">Section 11.2.1.2</a>
47 kΩ pull-down resistor	570 mA	Stand-Alone mode
56 kΩ pull-down resistor	1000 mA	Stand-Alone mode
68 kΩ pull-down resistor	1130 mA	Stand-Alone mode
82 kΩ pull-down resistor	1350 mA	Stand-Alone mode
100 kΩ pull-down resistor	1680 mA	Stand-Alone mode
120 kΩ pull-down resistor	2050 mA	Stand-Alone mode
150 kΩ pull-down resistor	2280 mA	Stand-Alone mode
V <sub>DD</sub> (If a pull-up resistor is used, its value must not exceed 100 kΩ.)	2850 mA (3000 mA maximum)	Stand-Alone mode

**Note 1:** Unless otherwise indicated, the values specified in this table are the typical I<sub>LIM</sub> in [Table 1-2](#).

### 11.2 SMBus Operating Mode

When the COMM\_SEL/I<sub>LIM</sub> pin is directly connected to ground or through a pull-down resistor with a value of 33 kΩ or below as listed in [Table 11-1](#), the UCS81003 communicates via the SMBus or I<sup>2</sup>C communications protocols.

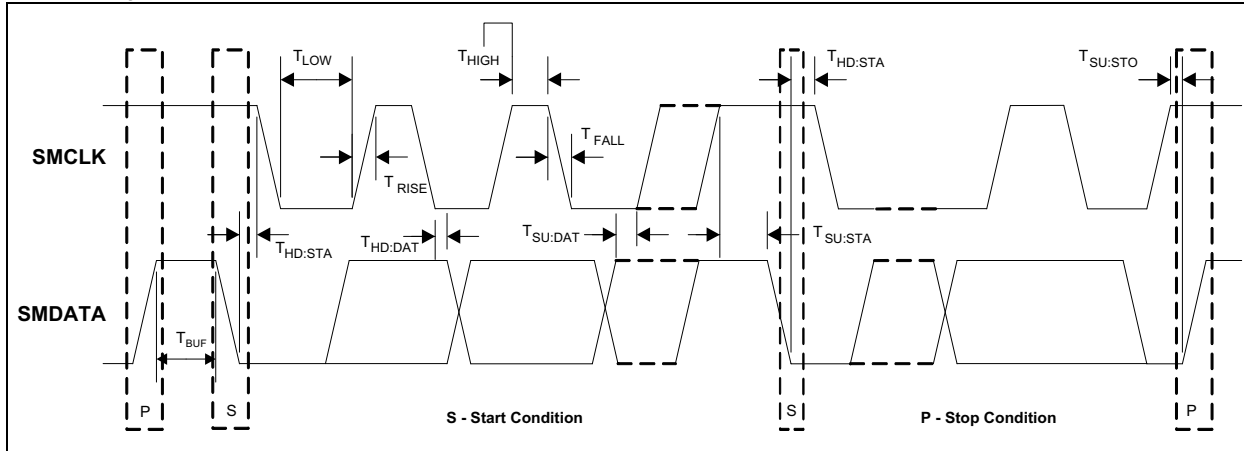
**Note 1:** Upon power-up, the UCS81003 does not respond to any SMBus communications for 5.5 ms. After this time, full functionality is available.

**2:** When in the Sleep state, the first SMBus read command sent to the UCS81003 device address wakes it. Any data sent to the UCS81003 is ignored and any data read from the UCS81003 must be considered invalid. The UCS81003 is fully functional 3 ms after this first read command is sent. See [Section 5.1.2 “Sleep State Operation”](#).

# UCS81003

## 11.2.1 SYSTEM MANAGEMENT BUS

In SMBus mode, the UCS81003 communicates with a host controller. The SMBus is a 2-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 11-1. Stretching of the SMCLK signal is supported; however, the UCS81003 does not stretch the clock signal.



**FIGURE 11-1:** SMBus Timing Diagram.

### 11.2.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus data line from a logic '1' state to a logic '0' state while the SMBus clock line is in a logic '1' state.

The SMBus address is determined based on the resistor connected on the SEL pin as shown in Table 11-2.

**Note:** If it is necessary to connect the SEL pin to  $V_{DD}$  via a resistor, the pull-up resistor may be any value up to 100 k $\Omega$ .

### 11.2.1.2 SMBus Address and RD/WR Bit

The SMBus Address Byte consists of the 7-bit client address followed by the RD/WR indicator bit. If this RD/WR bit is a logic '0', the SMBus host is writing data to the client device. If this RD/WR bit is a logic '1', the SMBus host is reading data from the client device.

**TABLE 11-2: SEL PIN DECODE**

Resistor ( $\pm 5\%$ )	PWR_EN Polarity	SMBus Address
GND	Active-Low	1010_111 (r/ $\bar{w}$ )
10 k $\Omega$ pull-down resistor	Active-Low	1010_110 (r/ $\bar{w}$ )
12 k $\Omega$ pull-down resistor	Active-Low	1010_101 (r/ $\bar{w}$ )
15 k $\Omega$ pull-down resistor	Active-Low	1010_100 (r/ $\bar{w}$ )
18 k $\Omega$ pull-down resistor	Active-Low	0110_000 (r/ $\bar{w}$ )
22 k $\Omega$ pull-down resistor	Active-Low	0110_001 (r/ $\bar{w}$ )
27 k $\Omega$ pull-down resistor	Active-Low	0110_010 (r/ $\bar{w}$ )
33 k $\Omega$ pull-down resistor	Active-Low	0110_011 (r/ $\bar{w}$ )
47 k $\Omega$ pull-down resistor	Active-High	0110_011 (r/ $\bar{w}$ )
56 k $\Omega$ pull-down resistor	Active-High	0110_010 (r/ $\bar{w}$ )
68 k $\Omega$ pull-down resistor	Active-High	0110_001 (r/ $\bar{w}$ )
82 k $\Omega$ pull-down resistor	Active-High	0110_000 (r/ $\bar{w}$ )
100 k $\Omega$ pull-down resistor	Active-High	1010_100 (r/ $\bar{w}$ )
120 k $\Omega$ pull-down resistor	Active-High	1010_101 (r/ $\bar{w}$ )
150 k $\Omega$ pull-down resistor	Active-High	1010_110 (r/ $\bar{w}$ )
$V_{DD}$ (If a pull-up resistor is used, its value must not exceed 100 k $\Omega$ )	Active-High	1010_111 (r/ $\bar{w}$ )



## 11.2.1.3 SMBus Data Bytes

All SMBus data bytes are sent most significant bit first and composed of eight bits of information.

## 11.2.1.4 SMBus ACK and NACK Bits

The SMBus client acknowledges all data bytes that it receives. This is done by the client device pulling the SMBus data line low after the 8<sup>th</sup> bit of each byte that is transmitted. This applies to both the Write Byte and Block Write protocols.

By holding the SMBus data line high after the 8<sup>th</sup> data bit is sent, the host NACK (not acknowledge) the last data byte received from the client. For the Block Read protocol, the host ACK each data byte that it receives except the last data byte.

## 11.2.1.5 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus data line from a logic '0' state to a logic '1' state while the SMBus clock line is in a logic '1' state. When the UCS81003 detects an SMBus Stop bit, and communicates with the SMBus protocol, it resets its client interface and prepares to receive further communications.

## 11.2.1.6 SMBus Timeout and Idle Reset

The UCS81003 includes an SMBus timeout feature. If the clock is held at logic '0' for  $t_{\text{TIMEOUT}}$ , the device can timeout and reset the SMBus interface. The SMBus interface can also reset if both the clock and data lines are held at a logic '1' for  $t_{\text{IDLE\_RESET}}$ . Communication is restored with a Start condition. This functionality defaults to disabled and can be enabled by clearing the DIS\_TO bit in the Emulation Configuration register ([Register 10-9](#)).

## 11.2.2 SMBUS AND I<sup>2</sup>C COMPATIBILITY

The major differences between SMBus and I<sup>2</sup>C devices are highlighted in this section. For more information, refer to the SMBus 2.0 and I<sup>2</sup>C specifications.

- UCS81003 supports I<sup>2</sup>C fast mode at 400 kHz. This covers the SMBus maximum time of 100 kHz.
- Minimum frequency for SMBus communications is 10 kHz.
- The SMBus client protocol resets if the clock is held at a logic '0' for longer than 30 ms. This time-out functionality is disabled by default in the UCS81003 and can be enabled by clearing the DIS\_TO bit. I<sup>2</sup>C does not have a timeout.
- Except when operating in Sleep mode, the SMBus client protocol resets if both the clock and data lines are held at a logic '1' for longer than 200  $\mu$ s (idle condition). This function is disabled by default in the UCS81003 device and can be enabled by clearing the DIS\_TO bit. I<sup>2</sup>C does not have an idle condition.
- I<sup>2</sup>C devices do not support the Alert Response Address functionality (optional for SMBus).
- I<sup>2</sup>C devices support block read and write differently. I<sup>2</sup>C protocol enables for unlimited number of bytes to be sent in either direction. The SMBus protocol requires that an additional data byte indicating number of bytes to read/write is transmitted. The UCS81003 only supports I<sup>2</sup>C formatting.

# UCS81003

## 11.2.3 SMBUS PROTOCOLS

The UCS81003 is SMBus 2.0-compatible and supports Write Byte, Read Byte, Send Byte, and Receive Byte as valid protocols as shown in the following sections.

All protocols in these sections use the convention in [Table 11-3](#).

**TABLE 11-3: PROTOCOL FORMAT**

Data Sent to Device	Data Sent to the Host
Data sent	Data sent

### 11.2.3.1 SMBus Write Byte

The Write Byte is used to write one byte of data to a specific register as shown in [Table 11-4](#).

**TABLE 11-4: WRITE BYTE PROTOCOL**

START	Client Address	WR	ACK	Register Address	ACK	Register Data	ACK	STOP
1->0	YYYY_YYY	0	0	XXh	0	XXh	0	0->1

### 11.2.3.2 SMBus Read Byte

The Read Byte protocol is used to read one byte of data from the registers as shown in [Table 11-5](#).

**TABLE 11-5: READ BYTE PROTOCOL**

START	Client Address	WR	ACK	Register Address	ACK	START	Client Address	RD	ACK	Register Data	NACK	STOP
1->0	YYYY_YYY	0	0	XXh	0	1->0	YYYY_YYY	1	0	XXh	1	0->1

### 11.2.3.3 SMBus Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol as shown in [Table 11-6](#).

**TABLE 11-6: SEND BYTE PROTOCOL**

START	Client Address	WR	ACK	Register Address	ACK	STOP
1->0	YYYY_YYY	0	0	XXh	0	0->1

### 11.2.3.4 SMBus Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (for example, set via Send Byte). This is used for consecutive reads of the same register as shown in [Table 11-7](#).

**TABLE 11-7: RECEIVE BYTE PROTOCOL**

START	CLIENT ADDRESS	RD	ACK	Register Data	NACK	STOP
1->0	YYYY_YYY	1	0	XXh	1	0->1

## 11.2.4 I<sup>2</sup>C PROTOCOLS

The UCS81003 supports I<sup>2</sup>C Block Read and Block Write. The protocols listed below use the convention in [Table 11-3](#).

### 11.2.4.1 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers as shown in [Table 11-8](#).

**Note:** When using the Block Write protocol, the internal address pointer is automatically incremented after every data byte is received. It wraps from FFh to 00h.

**TABLE 11-8: BLOCK WRITE PROTOCOL**

START	Client Address	WR	ACK	Register Address	ACK	Register Data	ACK
1->0	YYYY_YYY	0	0	XXh	0	XXh	0
Register Data	ACK	Register Data	ACK	...	Register Data	ACK	STOP
XXh	0	XXh	0	...	XXh	0	0->1

### 11.2.4.2 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers as shown in [Table 11-9](#).

**Note:** When using the Block Read protocol, the internal address pointer is automatically incremented after every data byte is received. It wraps from FFh to 00h.

**TABLE 11-9: BLOCK READ PROTOCOL**

START	Client Address	WR	ACK	Register Address	ACK	START	Client Address	RD	ACK	Register Data
1->0	YYYY_YYY	0	0	XXh	0	1->0	YYYY_YYY	1	0	XXh
ACK	Register Data	ACK	Register Data	ACK	Register Data	ACK	...	Register Data	NACK	STOP
0	XXh	0	XXh	0	XXh	0	...	XXh	1	0->1

## 11.3 Stand-Alone Operating Mode

Stand-Alone mode enables the UCS81003 to operate without active SMBus/I<sup>2</sup>C communications. Stand-Alone mode can be enabled by connecting a pull-down resistor greater or equal to 47 kΩ on the COMM\_SEL/I<sub>LIM</sub> pin as shown in Table 11-1.

When the device is configured to operate in Stand-Alone mode, the fault handling and Attach Detection controls are determined via the LATCH and S0 pins as shown in Table 11-10.

**Note:** If it is necessary to connect the S0 or LATCH pins to V<sub>DD</sub> via a pull-up resistor, the pull-up resistor value must be 100 kΩ in order to guarantee V<sub>IH</sub> specification. Similarly, if it is necessary to connect the S0 or LATCH pins to GND via a pull-down resistor, the pull-down resistor value must be 100 kΩ in order to guarantee V<sub>IL</sub> specification.

**TABLE 11-10: STAND-ALONE FAULT AND ATTACH DETECTION SELECTION**

Latch Pin	S0 Pin	Command
Low	Low	No Attach Detection. Auto-Recovery upon error detection.
Low	High	Attach Detection in the Detect power state. Auto-Recovery upon error detection.
High	Low	No Attach Detection. Error states are Latched and require host to change PWR_EN control to recover from Error state.
High	High	Attach Detection in the Detect power state. Error states are Latched and require host to change PWR_EN control to recover from Error state.

In the Stand-Alone operating mode, communications from and to the UCS81003 are limited to the PWR\_EN, EM\_EN, M2, M1, ALERT#, and A\_DET# pins.

## 12.0 PACKAGING INFORMATION

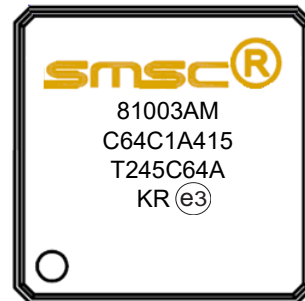
### 12.1 Package Marking Information

28-Lead VQFN (5x5x0.9 mm)

Example



PIN 1  
(MOLDED IN)



PIN 1  
(MOLDED IN)

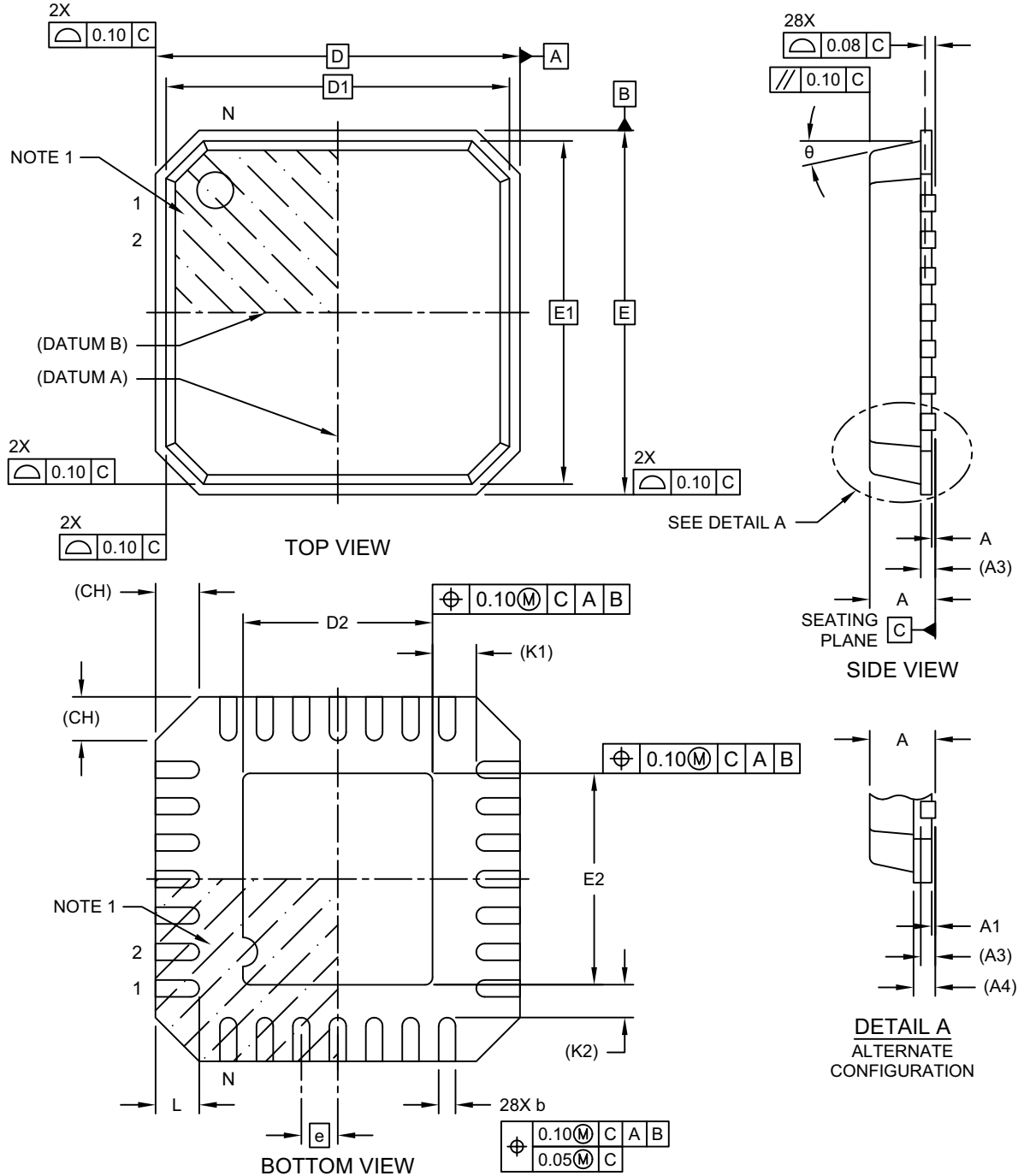
<b>Legend:</b>	Y	Year code (last digit of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	<R>	Package
	<COO>	Country of origin
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# UCS81003

## 28-Lead Very Thin Plastic Quad Flatpack, No Lead Package (PVX) - 5x5x0.9 mm Body [VQFN] With 2.6x2.9 mm Exposed Pad

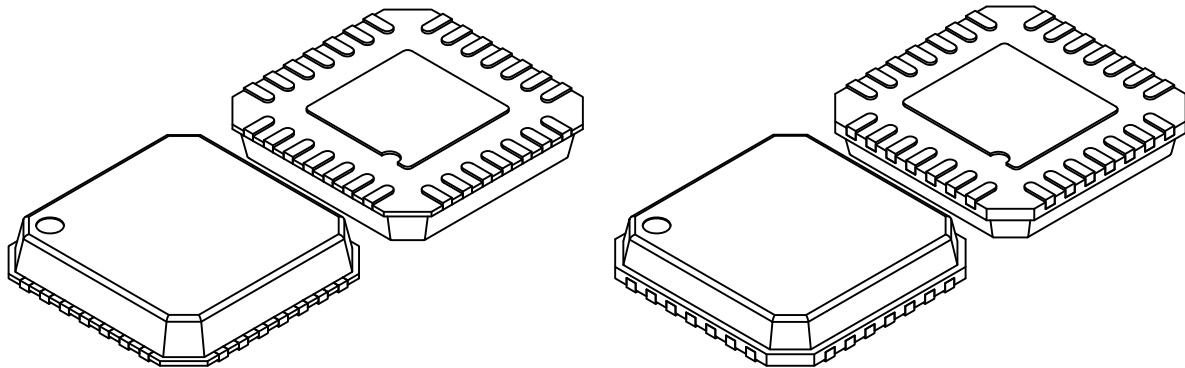
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-334 Rev C Sheet 1 of 2

## 28-Lead Very Thin Plastic Quad Flatpack, No Lead Package (PVX) - 5x5x0.9 mm Body [VQFN] With 2.6x2.9 mm Exposed Pad

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Original Configuration

Alternate Configuration

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	28		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.20 REF		
Overall Length	D	5.00 BSC		
Mold Cap Length	D1	4.75 BSC		
Exposed Pad Length	D2	2.50	2.60	2.70
Overall Width	E	5.00 BSC		
Overall Width	CH	0.60 REF		
Corner Chamfer	E1	4.75 BSC		
Exposed Pad Width	E2	2.80	2.90	3.00
Terminal Width	b	0.18	0.23	0.30
Terminal Length	L	0.50	0.60	0.70
Terminal-to-Exposed-Pad	K1	0.60 REF		
Terminal-to-Exposed-Pad	K2	0.45 REF		
Mold Draft Angle	$\theta$	-	-	12°

### ALTERNATE CONFIGURATION

Overall Height	A	0.80	0.85	0.90
Terminal Thickness	A3	0.20 REF		
Base Thickness	A4	0.30 REF		
Mold Cap Length	D1	4.71 BSC		
Mold Cap Width	E1	4.71 BSC		

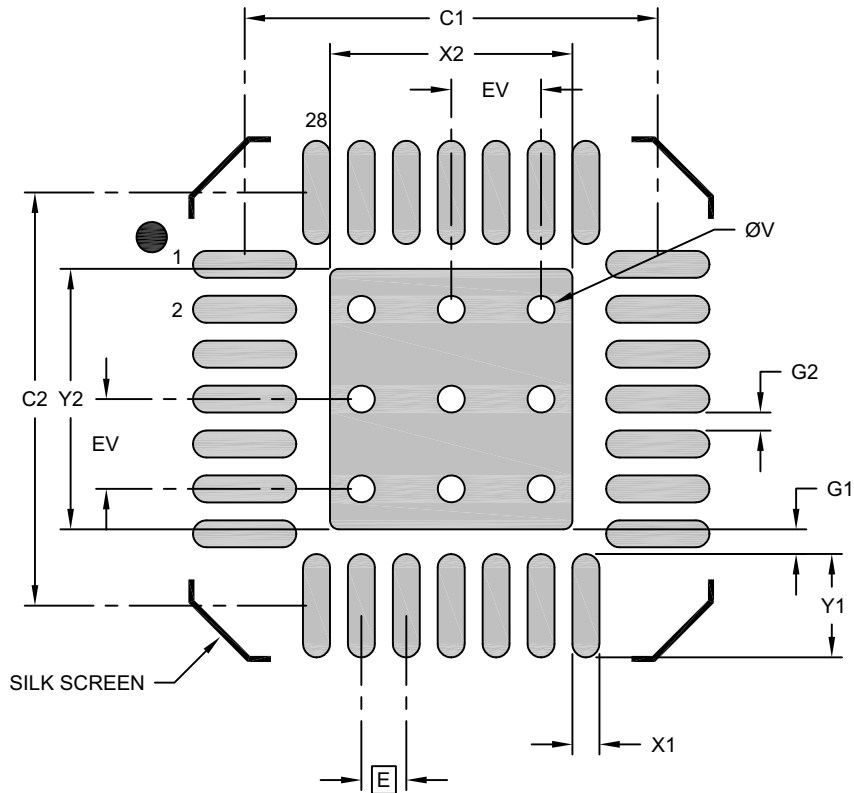
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is punch singulated
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

# UCS81003

## 28-Lead Very Thin Plastic Quad Flatpack, No Lead Package (PVX) - 5x5x0.9 mm Body [VQFN] With 2.6x2.9 mm Exposed Pad

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Center Pad Width	X2			2.70
Center Pad Length	Y2			2.90
Contact Pad Spacing	C1		4.60	
Contact Pad Spacing	C2		4.60	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			1.15
Contact Pad to Center Pad (Xnn)	G1	0.28		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2334 Rev C



## APPENDIX A: REVISION HISTORY

### Revision C (December 2022)

- Added information about the Automotive Qualification status of the device in [Section Features](#).
- Updates package drawings in [Section 12.0 Packaging Information](#).
- Updated [Section Product Identification System](#), with Automotive Qualified devices.

### Revision B (June 2018)

- Added the specifications for UCS81003AB.
- Corrected minor typographical errors and applied formatting changes throughout the document.

### Revision A (September 2014)

- Original release of this document.

# UCS81003

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>[X]<sup>(1)</sup></u>	<u>-XXX</u>	<u>XXX</u>
Device	Tape and Reel	Package	Qualification
<b>Device:</b>	UCS81003AM:	Automotive USB Port Power Controller with Charger Emulation, automatic $V_{BUS}$ discharge at power-up, 400 mV lower threshold for the window comparator on the $D_{POUT}$ pin.	
	UCS81003AB:	Automotive USB Port Power Controller with Charger Emulation, without automatic $V_{BUS}$ discharge at power-up, 470 mV lower threshold for the window comparator on the $D_{POUT}$ pin.	
<b>Tape and Reel Option:</b>	Blank	= Standard packaging (tube or tray)	
	R	= Tape and Reel <sup>(1)</sup>	
<b>Package:</b>	C1A	= Very Thin Plastic Quad Flat, No Lead Package – 5x5 mm Body with Rectangular Exposed Pad, 28-Lead (VQFN)	
<b>Qualification*:</b>	Blank	= Standard part	
	VAO	= Automotive AEC-Q100 Qualified	
	* Contact your local Microchip sales office to request automotive qualified variants for other package types.		

**Examples:**

a) UCS81003AM-C1A: 28-pin, 5x5 VQFN Lead-Free ROHS Compliant Package.

b) UCS81003AMR-C1A: Tape and Reel, 28-pin, 5x5 VQFN Lead-Free ROHS Compliant Package.

c) UCS81003ABR-C1AVAO: Tape and Reel, 28-pin, 5x5 VQFN Lead-Free ROHS Compliant Package, Automotive Qualified

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

# UCS81003

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NOTES:

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