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Making Use of Gate Charge Information in MOSFET and IGBT Data Sheets

Ralph McArthur
Senior Applications Engineer
Advanced Power Technology
405 S.W. Columbia Street
Bend, Oregon 97702

Power MOSFETs and IGBTs have established themselves as premier power semiconductors in a wide range of applications involving switching or amplification. In order to use these devices effectively it is necessary to understand and make use of the gate charge information on the data sheet. This information appears in two locations: in the "Dynamic Characteristics" section of listed parameters and in the figure showing gate-source voltage *versus* total gate charge. Hereafter the figure showing gate-source voltage *versus* total gate charge will be referred to simply as "the gate charge curve." This application note is written with MOSFETs in view, but everything said here applies to IGBTs as well. Just exchange "collector" for "drain" and "emitter" for "source."

The discussion is based on a common MOSFET model, shown in Figure 1. The figure shows the MOSFET model, the total gate resistance, and block elements for the load impedance and the gate drive circuit.

Figure 2 shows a gate charge curve taken from a data sheet. It displays the gate-source voltage as a function of charge injected into the gate. Charge is built up in the gate as long as gate drive current flows into the gate. Note that the main power supply, V_{DD} in the gate charge measurement, serves as a parameter in the figure. Figure 1 shows where V_{DD} is applied. The charge required to reach a certain gate voltage is different for different values of V_{DD}. For a given V_{DD}, if a certain number of nanocoulombs are injected into the gate, the voltage will rise to a certain level. Use of Figure 2 in gate drive design has already been described.[1]

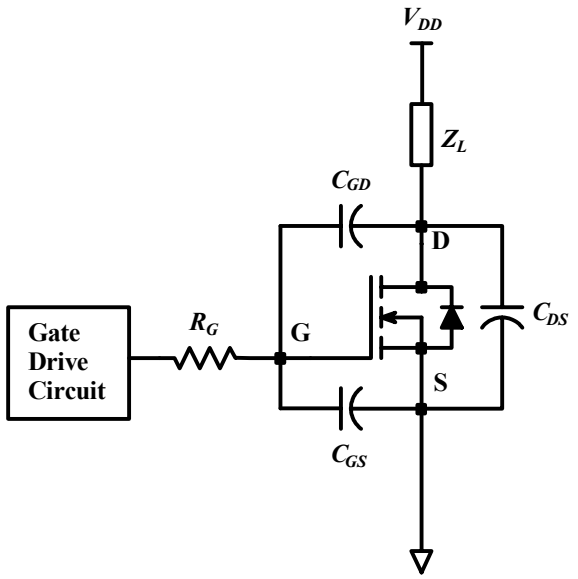

Figure 1. Lumped element model for a power MOSFET

The gate charge parameters called out in the "Dynamic Characteristics" section of the data sheet are as follows: Q_g, the total gate charge, Q_{gs}, the gate-source charge, and Q_{gd}, the gate-drain ("Miller") charge. Figure 3 shows the parts of the gate charge curve from which these charge values are taken.

Q_{gs} is the charge from the origin to the first inflection in the curve, Q_{gd} is the charge from the first inflection in the curve to the second inflection in the curve, and Q_g is the charge from the origin to the point on the curve at which v_{GS} equals the peak drive voltage. In Figure 3, v_{GS} equals the peak drive voltage at the right end of the curve. In Figure 2, *Qgs* equals about 12.5 nC, *Qgd* equals about 100 nC, using the "V_{DD} = 500 V" line, and, assuming a peak gate drive voltage of 10 V, Qg equals about 205 nC, again using the "V_{DD} = 500 V" line. The plateau between the two inflections in Figure 2 is flat, whereas the plateau in Figure 3 is not. This reflects the way it is in general. The plateau is flat in some curves and not in others. More will be said about this later.

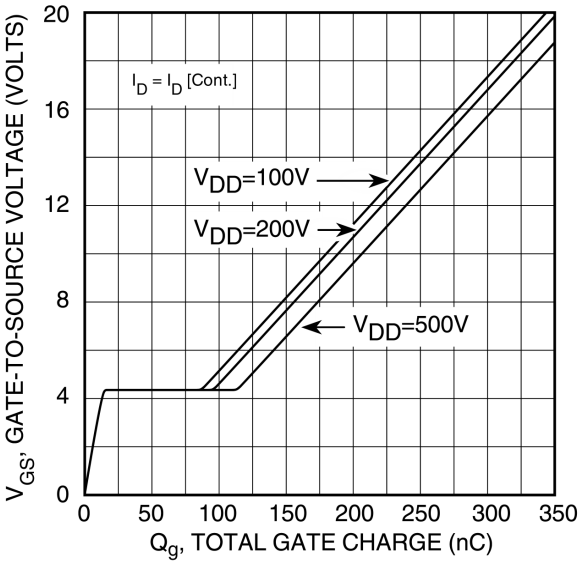

Figure 2. v_{GS} as a function of gate charge

This note will consider again the process of charging the gate in order to clarify important issues and provide a basis for discussion of various topics that depend on them: adjusting the switching speed of the MOSFET, designing gate drive circuits, selecting commercial gate drive circuits, and testing the MOSFET to determine its gate charge properties. These topics will not be covered in the note; rather the note will serve as a basis for discussing them in the future. The process of discharging the gate at turn-off will not be treated, since in principle it is the reverse of charging. Nevertheless it should be noted that there are circuits in which separate drives are used for charging and discharging when the particular application imposes discharging requirements that differ from the charging requirements. Even so, although the drives in that case are different, the physical principles involved are the same.

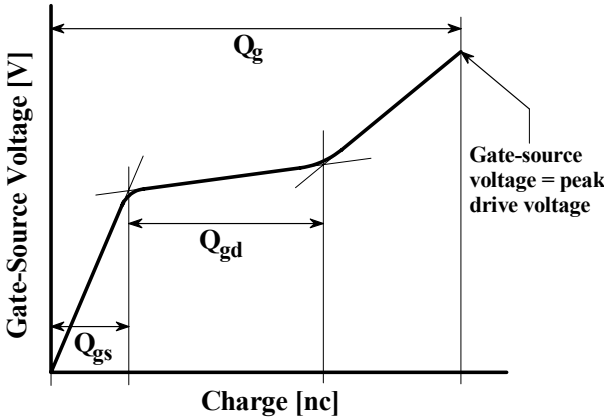

Figure 3. v_{GS} as a function of gate charge

Figure 4 shows the MOSFET capacitances reported in the data sheets as a function of v_{DS}: C_{iss}, the input capacitance, C_{oss}, the output capacitance, and C_{rss}, the reverse transfer capacitance. In terms of the interterminal capacitances in the model of Figure 1, $C_{iss} = C_{GS} + C_{GD}$, $C_{oss} = C_{DS} + C_{GD}$, and $C_{rss} = C_{GD}$.

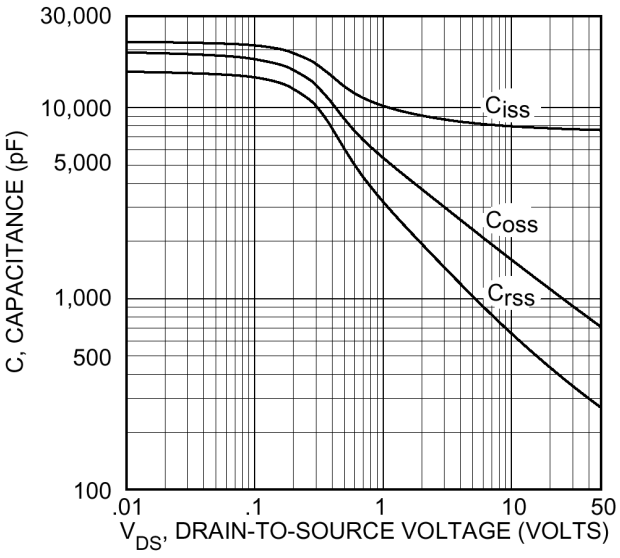

Figure 4. Typical capacitance as a function of v_{DS}

C_{iss}, C_{oss}, and C_{rss} vary as a function of v_{DS}, because C_{GD} and C_{DS} vary as a function of v_{DS}. C_{GS} on the

other hand is constant. This is seen in Figure 5. The current through C_{GD} and C_{DS} depends on the time derivative of the product of the capacitance and its voltage. This will be discussed later.

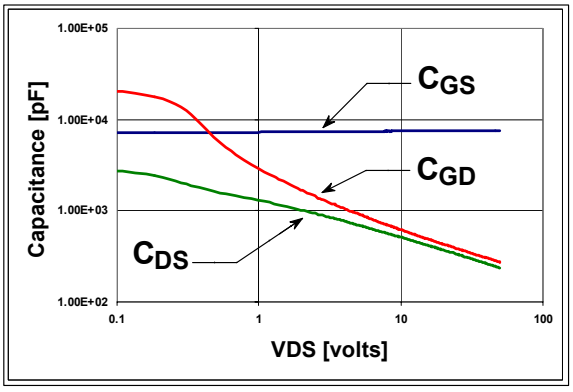

Figure 5. The interterminal capacitances as a function of v_{DS}

Figure 2 plots v_{GS} against gate charge. When the measurements are actually done, v_{GS} is plotted against time, as in Figure 6, and the way they are done makes it possible to treat time as the equivalent of charge. A constant-current gate drive is employed in the gate charge measurement. In order to determine how much charge has been injected into the gate, the current into the gate must be integrated. For any given time period, integrating the gate current from the beginning of the period to its end determines the amount of charge injected into the gate during that time. If we use i_G to represent the gate current, Q to represent the charge going into the gate, and t_b (beginning time) and t_e (ending time) to represent the time period, the equation is as follows:

$$Q = \int_{t_b}^{t_e} i_G dt \ .$$

When a constant gate current is employed, this equation reduces simply to:

$$Q = i_G \Delta t \ ,$$

where Δt is the time period over which the charge is to be integrated, that is, t_e - t_b. Therefore, in Figure 6, $Q_{gs} = i_G \cdot (t_2 - t_0)$, $Q_{gd} = i_G \cdot (t_3 - t_2)$, and $Q_g = i_G \cdot (t_4 - t_0)$. In this way, constant current in the gate makes it possible to treat the voltage *versus* time curve as a voltage *versus* charge curve. Additionally, constant current in the drain eliminates the effect of lead inductance from the measurement.

The four time periods in Figure 6 are delineated by certain levels of v_{GS} and certain changes in v_{GD}. The endpoints of these time periods are the origin at $t = t_0$, V_T, the threshold voltage, V_{PL}, the left end of the plateau in v_{GS}, V_{PR}, the right end of the same plateau, and V_{DR}, the peak value of the drive voltage. When the drive circuit is a voltage source, this peak value is the nominal potential at the output of the driver. However, when, as in Figure 6, constant gate current is employed, the driver is a current source, and the peak value of the gate voltage is chosen to be 10 V, as stated in the data sheets. It is at the peak value of the gate voltage that the total gate charge is determined.

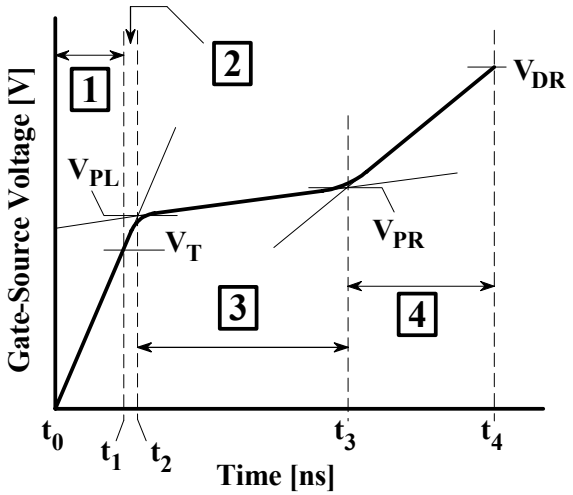

Figure 6. Four time periods in the v_{GS} versus time characteristic curve

Four Time Periods in the Rise of v_{GS}

The four time periods in Figure 6 are described next. Although it is helpful to break the charging time into four periods to explain the events taking place, nevertheless data sheets characterize this

process with the use of the three charge quantities already mentioned. Figure 7 shows the switching waveforms of the MOSFET at turn-on for reference, as well. As the description unfolds, the events can be observed in the figure as they are called out. The times in Figure 7 are in µs, instead of ns, because they were generated using a low magnitude (1 mA) constant-current drive, a standard way of measuring gate charge. The load for the gate charge measurement in Figure 7 is a constant current source (not an inductor).

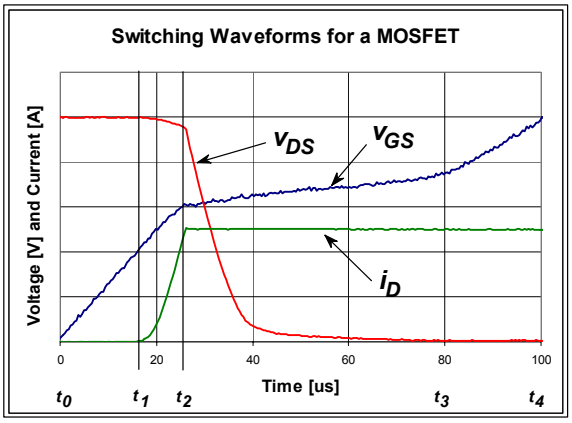

Figure 7. Switching waveforms showing events at times t_0 through t_4.

From Zero to V_T

v_{GS} rises from zero to V_T;
i_D does not flow;
v_{DS} remains unchanged.

When v_{GS} is in this range of values, $0 < v_{GS} < V_T$, the MOSFET is off and v_{DS} is constant at the level of the supply voltage, V_{DD}. At time $t = t_0$, when the constant gate current is applied, v_{GS} begins to rise. This rise in v_{GS} is brought about by the charging of C_{GS} and C_{GD}. It is a misconception to think that only C_{GS} is being charged in this regime, for if the gate node is rising in potential, then the voltage across C_{GD} is changing, and that requires the flow of charge into C_{GD}. At this unchanging value of v_{DS}, C_{GS} is much larger than C_{GD} and, therefore, much more drive current is flowing into C_{GS} than into C_{GD}. The rise of v_{GS} in this time period is brought to an end when $v_{GS} = V_T$ at $t = t_1$. To this point, the drain current has not yet begun to flow.

It should be noted that C_{GS} is not a function of voltage, whereas C_{GD} is. Therefore, in this time period C_{GS} is constant, but C_{GD} is increasing slightly because the magnitude of the potential difference across its terminals is decreasing slightly. Recall that as the voltage decreases the capacitance increases. This can be understood from Figure 5. As v_{DS} decreases, C_{GD} increases. Also, apart from Figure 5, we know that as v_{DS} decreases, v_{GD} increases. Understand that, since $V_{DD} > v_{GS}$, for most of the range of values for v_{DS}, $v_{DS} > v_{GS}$. This means that v_{GD} is negative, since $v_{GD} = v_{GS} - v_{DS}$. Therefore, for v_{GD} to increase is for v_{GD} to become less negative. This means its magnitude is decreasing, and as v_{GD} increases (that is, as v_{DS} is decreasing and v_{GD}'s magnitude is decreasing), C_{GD} increases.

From V_T to V_{PL}

v_{GS} rises from V_T to v_{PL};
i_D begins to flow;
v_{DS} begins to decrease;
Q_{gs} is the charge injected into the gate from time t_0 to time t_2.

Threshold voltage is defined as the gate-source voltage at which i_D begins to flow. To say it this way means that low-level, pre-threshold current is being neglected. Therefore at the beginning of this time period, at $t = t_1$, i_D begins to flow and v_{DS} begins to decrease at some changing rate. The time period ends at $t = t_2$ with the appearance of the first knee.

This appearance of the knee depends on the rate of change of the product $C_{GD} \cdot v_{GD}$ with respect to time. The more general expression for current in a capacitor applies here, since the capacitance, C_{GD}, is varying. Recall that $q = Cv$ and that, in general, the equation for current in a capacitor is

$$i = \frac{dq}{dt} = \frac{d(Cv)}{dt}.$$

This is the expression that must be used when C and v are both varying in time. This is exactly the case with C_{GD} and v_{GD} in the MOSFET. $v_{GD} = v_{GS} - v_{DS}$, and is a function of i_D and Z_L, not i_D only. In other words, it is not correct to say that the left knee occurs when the drain current reaches it maximum, as is often claimed. Any combination of i_D and Z_L that makes v_{DS} decrease fast enough, in turn causing v_{GD} to increase, will bring about the knee. As stated previously, for v_{GD} to increase means that it is becoming less negative. In theory i_D can actually reach its maximum after the left knee occurs, because the current in C_{GD}, $d(C_{GD} \cdot v_{GD})/dt$, determines the occurrence of the knee. A small value of i_D and a large value of Z_L can bring this about.

From V_{PL} to V_{PR}

v_{GS} progresses from v_{PL} to v_{PR};
i_D reaches its maximum at some point;
v_{DS} reaches its minimum at t_3;
Q_{gd} is the charge injected into the gate from time t_2 to time t_3.

As v_{GS} continues to move, rising past V_T and V_{PL}, because of charge delivered by the gate current, the slope of v_{GS} decreases substantially, in some cases decreasing all the way to zero. v_{GS} has hereby moved into the region sometimes referred to as the plateau. This took place at $t = t_2$ in Figure 6. The slope of this plateau region, strictly speaking, depends on the division of drive current between C_{GD} and C_{GS}, and it is the test or circuit conditions that determine this division. If $C_{GD} \cdot v_{GD}$ increases quickly enough, v_{GS} in the plateau region will be constant: $v_{GS} = V_{PL} = V_{PR}$. In this latter case, the slope is zero, which means that none of the drive current is flowing into C_{GS}. Rather, all of the drive current is being used to accommodate the change in voltage across C_{GD} as $C_{GD} \cdot v_{GD}$ continues to increase. If the slope is nonzero, it means that some of the drive current is making its way into C_{GS} with the result that v_{GS} is rising, albeit at a slow rate. Figure 8 shows two gate charge curves for two different MOSFETs tested under the same conditions. One device exhibits low gate charge (the MOS 7 MOSFET from APT's latest generation of low-loss MOSFETS), and the other device exhibits high gate charge (the MOS V MOSFET from an older generation of APT's MOSFETs). Here are two real devices, one with a non-zero slope in the plateau region and one with a nearly zero slope. The time is in µs because a low magnitude (1 mA) constant-current drive was used to drive the gates.

Whereas in the first and second time periods there was no choice (some of the drive current flowed into C_{GD}), here in the third time period, by providing the load with sufficient impedance and providing the input with large enough resistance, it should be possible to divert all (almost all) of the drive current through C_{GD}. That is, the slope of the plateau depends on C_{GS}, C_{GD}, and the drive and load circuit elements. However, regardless of the slope of the plateau, the right end of the plateau occurs when the MOSFET reaches its fully on state.

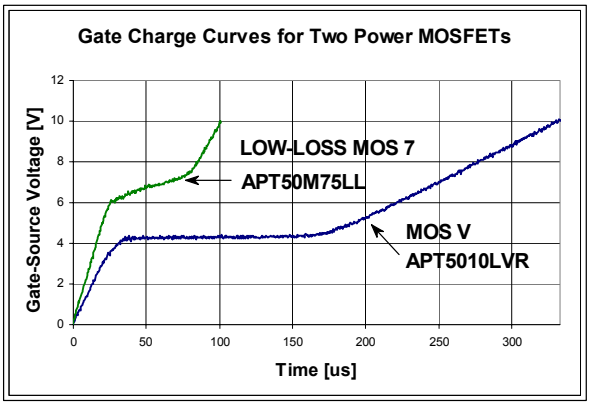

Figure 8. Gate charge curves for two power MOSFETs showing different slopes in the plateau region

For the entire duration of this third time period, v_{DS} is decreasing (which means that v_{GD} is increasing) and C_{GD} is increasing. When v_{DS} reaches the level of I_D X $R_{DS(on)}$, it stops decreasing and C_{GD} stops increasing. Capital "I" in I_D indicates that the peak value of i_D is in view. This phenomemon ends the time period and v_{GS} begins to increase at a new, higher rate. The right end of the plateau has been reached at $v_{GS} = V_{PR}$ and $t = t_3$.

From V_{PR} to V_{DR}

v_{GS} rises from v_{PR} to v_{DR};
i_D stays at its maximum;
v_{DS} stays at its minimum;
Q_g is the charge injected into the gate from time t_0 to time t_4.

Once v_{DS} reaches its minimum, I_D X $R_{DS(on)}$, v_{GS} rises out of the plateau region and increases at a new rate. Now, since v_{DS} is not changing any more, the bulk of the drive current once again flows into C_{GS}. The slope is not as high as it was in the first time period, because C_{GD} is much larger than it was then. It is much closer in value to C_{GS}. Now again both capacitors are being charged, and both capacitors are of constant value or nearly so, C_{GS} because it always is and C_{GD} because $v_{GD} > 0$.[2]

Implications

The foregoing has implications that may also lead to better designs and may improve the way these issues are discussed. Consider the following.

Gate-Source Charge, Q_{gs}

As already stated, Q_{gs} is the charge it takes to bring v_{GS} up from zero to v_{PL} at t_2 in Figure 6. It is best to understand it as such rather than to think, for example, that it is the charge going into C_{GS}, as the name suggests. By the time v_{GS} reaches v_{DR} at t_4 in Figure 6, a great deal more charge has gone into C_{GS} than is represented by Q_{gs}, which again is only the charge needed to raise v_{GS} from zero to v_{PL}. It is also understood that some of the charge represented by Q_{gs} is actually going into C_{GD}.

Gate-Drain Charge, Q_{gd}

Again, as already stated, Q_{gd} is the charge it takes to bring v_{GS} from v_{PL} at time t_2 in Figure 6 to v_{PR} at time t_3 in Figure 6. Therefore, Q_{gd} is taken as the product of the gate current and the duration of the third time period, t_3 - t_2, in the gate charge measurement. It is also best to understand Q_{gd} in this way and not, as the name suggests, as the charge going into C_{GD}. By the time v_{GS} reaches v_{DR} at time t_4 in Figure 6, more charge has gone into C_{GD} than is indicated by Q_{gd}. Additionally, in most cases Q_{gd} also represents some charge that has gone into C_{GS}.

Total Gate Charge, Q_g

Total gate charge depends on V_{DR}, the peak value of the gate drive voltage, on V_{DD}, the voltage supplied to the drain, and on I_D, the peak value of the drain current. These values are stated when the total gate charge number is entered into the data sheet. It is the charge it takes to bring v_{GS} up from zero to V_{DR} at time t_4 in Figure 6, given the chosen values of V_{DD} and V_{DR}.

The two charge quantities discussed previously, when added together, represent an important piece of information. The sum of Q_{gs} and Q_{gd} is the amount of charge that must be injected into the gate to bring the typical MOSFET into full conduction. That is, at the moment Q_{gs} + Q_{gd} has been injected into the gate, $v_{DS} = I_D$ X $R_{DS(on)}$. At this point the MOSFET is in full conduction and any more charge injected into the gate represents overcharge, charge that does not change the output conditions. Manufacturers routinely recommend that the gate be overcharged, because this ensures that enough charge is injected into each gate and it accounts for differences among transistors in their gate charge requirements. For MOSFETs a common gate voltage for overcharge conditions is 10 V. The charge injected into the gate to bring it to the overcharge level is the total gate charge, Q_g.

Switching Times

These ideas have an impact on the switching times for a MOSFET as well. In particular, the time it takes to turn a MOSFET on is the time it takes to

inject the two data sheet charge quantities, Q_{gs} and Q_{gd}, into the gate. For any MOSFET the two charge quantities in question are its own Q_{gs} and Q_{gd}. These numbers may indeed be different for two MOSFETs with the same part number. Once again, overcharge can render the differences unimportant. Instead of designing to the sum of Q_{gs} and Q_{gd}, if one designs to Q_g, the differences should not affect the performance of the circuit. In other words, if one designs the gate drive to have the total gate charge injected into the gate by the time the system needs the MOSFET to be on, the switching time will be correct. This calculation is easier when a constant current gate drive is employed. The current to be delivered to the gate is found as follows:

$$I_G = \frac{Q_g}{t_s}.$$

Capital "I" has been used in I_G to show that the magnitude of the drive current is in view, and t_s represents the switching time required by the system. When a constant voltage drive is used, the peak value of the gate current must be determined from the equation,

$$I_G = \frac{V_{DR}}{R_G},$$

where R_G is the sum of the driver's output impedance, the external gate resistance, and the series resistance of the gate itself. In Figure 1, this total gate resistance has been lumped into R_G. The proper value of R_G must be determined iteratively from the following gate charge equation:

$$Q_g = \int_{t_0}^{t_s} i_G dt.$$

R_G is inherent in the variable i_G. To solve this equation analytically one must cast i_G in the form,

$$i_G = I_G e^{-\frac{t}{R_G C_{eff}}},$$

where I_G is the peak value of the gate current; R_G is the total gate resistance; and C_{eff} is the effective gate input capacitance. How to determine C_{eff} will be treated in a subsequent application note and has been treated by others,[3, 4] but in general it will not be equal to the data sheet value of C_{iss}. The preceding equation may also be written,

$$i_G = \frac{V_{DR}}{R_G} e^{-\frac{t}{R_G C_{eff}}}.$$

Now the gate charge equation becomes

$$Q_g = \int_{t_0}^{t_s} \frac{V_{DR}}{R_G} e^{-\frac{t}{R_G C_{eff}}} dt.$$

The integration can be performed numerically, and it is easier to supply R_G and solve for t_s. If many time points are used, rectangular integration should be adequate to the task. The solution of this equation is iterative, since one must supply a value for R_G and then solve for t_s. These two steps must be repeated until the desired t_s is found. That determines R_G and, in turn, I_G. It remains only to provide a driver that can source the peak current equal to V_{DR}/R_G. Since most designers use constant voltage drive, this is the process they should follow in their designs.

Gate Charge Measurements

How to measure the data sheet Q_{gd} is a question as well. Figure 6 shows the times t_2 and t_3 coincident with their respective ends of the plateau. Straight line intersections define the corners that, projected down onto the time axis, identify t_2 and t_3. This would seem to be the best way to measure Q_{gd}, although there are others.[5] Q_{gd} is simply, then, the constant gate current multiplied by the difference, $t_3 - t_2$.

In like fashion, as suggested earlier, Q_{gs} is the constant gate current times the difference, $t_2 - t_0$, and Q_g is the constant gate current times the difference, $t_4 - t_0$.

Finally, since many designs now anticipate a $V_{DD} = 0.7V_{DSS}$, gate measurements ought to be done at that voltage. V_{DSS} is the rated voltage for the MOSFET. The designer needs to know what the Q_g is going to be under the particular circuit conditions to be used, not the artificial and very common measurement condition of $0.5V_{DSS}$.

Conclusions

Q_{gs} and Q_{gd} do not mean what their names seem to imply. Nevertheless they perform the useful function of identifying together the amount of charge necessary to bring the data-sheet-typical MOSFET into full conduction. Since, however, the data sheet values are for typical devices and do not account for the spread of values from MOSFET to MOSFET, proper gate drive design makes use of Q_g to bring about an overcharge condition in the gate. Proper gate drive design also makes use of the correct current integration equation to determine the current requirements for the gate drive circuit. The principles in this application note, when combined with proper circuit layout[6] and power circuit design and when accounting for the required switching time, will lead to optimal switching performance.

References

[1] "Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and IGBTs." AN-944. International Rectifier.

[2] Grant, Duncan A. and John Gowar. *POWER MOSFETS Theory and Applications*, p. 84. New York: John Wiley & Sons, 1989.

[3] Pressman, Abraham I. *Switching Power Supply Design*, Second Edition, pp. 359-361. New York: McGraw-Hill, 1998.

[4] Erickson, Robert, Bill Behen, R. D. Middlebrook, and Slobodan Ćuk. "Characterization and Implementation of Power MOSFETs in Switching Converters." In *Proceedings of Powercon® 7*, pp. 188-189. The Seventh National Solid-State Power Conversion Conference, March 24-27, 1980, San Diego, California. Power Concepts, Inc., 1980.

[5] *Department of Defense Test Method Standard, Semiconductor Devices*, Mil-Std 750D, February 28, 1995, Method 3471.

[6] Dierberger, Kenneth. "Gate Drive Design for Large Die MOSFETs." Application Note APT9302. Advanced Power Technology.