TC1017

150 mA, Tiny CMOS LDO With Shutdown

Features

- AEC-Q100 Automotive Qualified, See Product Identification System
- Space-saving 5-Pin SC-70 and SOT-23 Packages
- Extremely Low Operating Current for Longer Battery Life: 53 µA (typ.)
- Very Low Dropout Voltage
- Rated 150 mA Output Current
- Requires Only 1 µF Ceramic Output Capacitance
- High Output Voltage Accuracy: ±0.5% (typical)
- 10 µs (typ.) Wake-Up Time from $\overline{\text{SHDN}}$
- Power-Saving Shutdown Mode: 0.05 µA (typ.)
- Overcurrent and Overtemperature Protection
- Pin-Compatible Upgrade for Bipolar Regulators

Applications

- Cellular/GSM/PHS Phones
- Battery-Operated Systems
- Portable Computers
- Medical Instruments
- Electronic Games
- Pagers

General Description

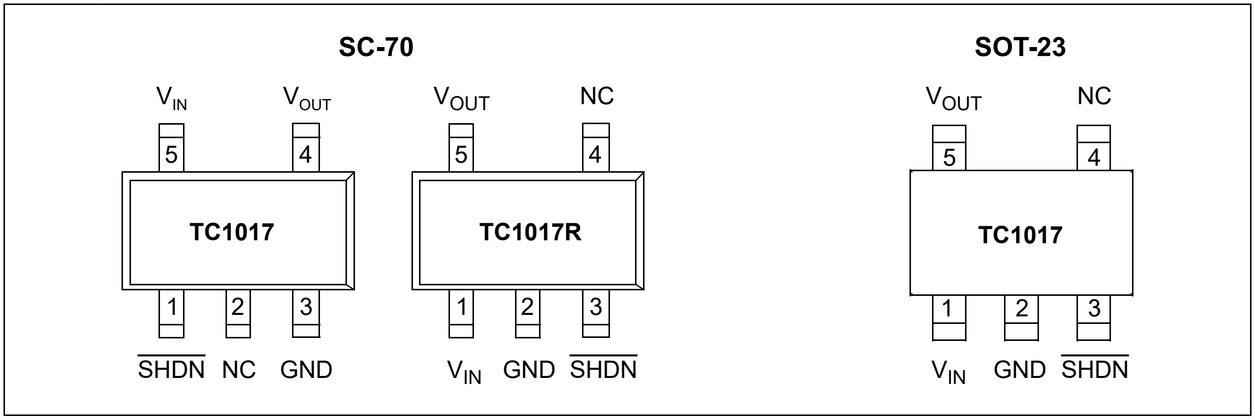
The TC1017 is a high-accuracy (typically ±0.5%) CMOS upgrade for bipolar Low Dropout regulators (LDOs). It is offered in a SC-70 or SOT-23 package. The SC-70 package represents a 50% footprint reduction versus the popular SOT-23 package and is offered in two pinouts to make board layout easier.

Developed specifically for battery-powered systems, the TC1017's CMOS construction consumes only 53 µA typical supply current over the entire 150 mA operating load range. This can be as much as 60 times less than the quiescent operating current consumed by bipolar LDOs.

The TC1017 is designed to be stable, over the entire input voltage and output current range, with low-value (1 µF) ceramic or tantalum capacitors. This helps to reduce board space and save cost. Additional integrated features, such as shutdown, overcurrent and overtemperature protection, further reduce the board space and cost of the entire voltage-regulating application.

Key performance parameters for the TC1017 include low dropout voltage (285 mV typical at 150 mA output current), low supply current while shutdown (0.05 µA typical) and fast stable response to sudden input voltage and load changes.

Package Types



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Input Voltage 6.5V

Power Dissipation .... Internally Limited (Note 7)

Maximum Voltage On Any Pin........ V_{IN} + 0.3V to -0.3V

ESD Protection on All Pins (Note 1)

HBM .... ±2 kV

MM .... ±200V

CDM .... ±1.5 kV

> † **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Testing was performed per AEC-Q100 standard. For additional information contact your local Microchip sales office.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100\ \mu A$, $C_L = 1.0\ \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25°C$
Boldface type specifications apply for junction temperatures of -40°C to +125°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Input Operating Voltage	V_{IN}	**2.7**	—	**6.0**	V	**Note 1**
Maximum Output Current	I_{OUTMAX}	**100**	—	—	mA	**Note 1**
		150	—	—		V_{IN} >= 3V and V_{IN} >= (V_R + 2.5%) + $V_{DROPOUTMAX}$
Output Voltage	V_{OUT}	**V_R – 2.5%**	V_R ±0.5%	**V_R + 2.5%**	V	**Note 2**
V_{OUT} Temperature Coefficient	TCV_{OUT}	—	**40**	—	ppm/°C	**Note 3**
Line Regulation	$\|(\Delta V_{OUT}/\Delta V_{IN})\| / V_R$	—	0.04	**0.2**	%/V	$(V_R + 1V) < V_{IN} < 6V$
Load Regulation (**Note 4**)	$\|\Delta V_{OUT}\| / V_R$	—	0.38	**1.5**	%	I_L = 0.1 mA to I_{OUTMAX}
Dropout Voltage (**Note 5**)	$V_{IN} – V_{OUT}$	— — — —	2 90 180 285	**—** **200** **350** **500**	mV	I_L = 100 µA I_L = 50 mA I_L = 100 mA I_L = 150 mA
Supply Current	I_{IN}	—	53	**90**	µA	$\overline{SHDN} = V_{IH}$, $I_L = 0$
Shutdown Supply Current	I_{INSD}	—	0.05	2	µA	$\overline{SHDN}$ = 0V

Note 1: The minimum V_{IN} has to meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$.

2: V_R is the regulator voltage setting. For example: V_R = 1.8V, 2.7V, 2.8V, 3.0V.

3:

$$TCV_{OUT} = \frac{(V_{OUTMAX} - V_{OUTMIN}) \times 10^6}{V_{OUT} \times \Delta T}$$

4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

5: Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value at a 1V differential.

6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6V for t = 10 msec.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see **Section 5.1 “Thermal Shutdown”**, for more details.

8: Output current is limited to 120 mA (typ) when V_{OUT} is less than 0.5V due to a load fault or short-circuit condition.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100\ \mu A$, $C_L = 1.0\ \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25°C$
Boldface type specifications apply for junction temperatures of -40°C to +125°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Power Supply Rejection Ratio	PSRR	—	58	—	dB	f =1 kHz, I_L = 50 mA
Wake-Up Time (from Shutdown mode)	t_{WK}	—	10	—	µs	V_{IN} = 5V, I_L = 60 mA, $C_{IN} = C_{OUT}$ =1 µF, f = 100 Hz
Settling Time (from Shutdown mode)	t_S	—	32	—	µs	V_{IN} = 5V, I_L = 60 mA, C_{IN} = 1 µF, C_{OUT} = 1 µF, f = 100 Hz
Output Short-Circuit Current	I_{OUTSC}	—	120	—	mA	V_{OUT} = 0V, Average Current **(Note 8)**
Thermal Regulation	V_{OUT}/P_D	—	0.04	—	V/W	**Notes 6, 7**
Thermal Shutdown Die Temperature	T_{SD}	—	160	—	°C	
Thermal Shutdown Hysteresis	ΔT_{SD}	—	10	—	°C	
Output Noise	eN	—	800	—	nV/√Hz	f = 10 kHz
$\overline{SHDN}$ Input High Threshold	V_{IH}	**45**	—	—	$\%V_{IN}$	V_{IN} = 2.7V to 6.0V
$\overline{SHDN}$ Input Low Threshold	V_{IL}	—	—	**15**	$\%V_{IN}$	V_{IN} = 2.7V to 6.0V

Note 1: The minimum V_{IN} has to meet two conditions: $V_{IN} \geq 2.7V$ and $V_{IN} \geq (V_R + 2.5\%) + V_{DROPOUT}$.

2: V_R is the regulator voltage setting. For example: V_R = 1.8V, 2.7V, 2.8V, 3.0V.

3:

$$TCV_{OUT} = \frac{(V_{OUTMAX} - V_{OUTMIN}) \times 10^6}{V_{OUT} \times \Delta T}$$

4: Regulation is measured at a constant junction temperature using low duty-cycle pulse testing. Load regulation is tested over a load range from 0.1 mA to the maximum specified output current. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

5: Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value at a 1V differential.

6: Thermal regulation is defined as the change in output voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a current pulse equal to I_{LMAX} at V_{IN} = 6V for t = 10 msec.

7: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction-to-air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation causes the device to initiate thermal shutdown. Please see **Section 5.1 "Thermal Shutdown"**, for more details.

8: Output current is limited to 120 mA (typ) when V_{OUT} is less than 0.5V due to a load fault or short-circuit condition.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, V_{DD} = +2.7V to +6.0V and V_{SS} = GND.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	Extended Temperature parts
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances3						
Thermal Resistance, 5L-SOT23	θ_{JA}	—	255	—	°C/W	
Thermal Resistance, 5L-SC-70	θ_{JA}	—	450	—	°C/W	

2.0 TYPICAL PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100\ \mu A$, $C_L = 1.0\ \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25°C$.

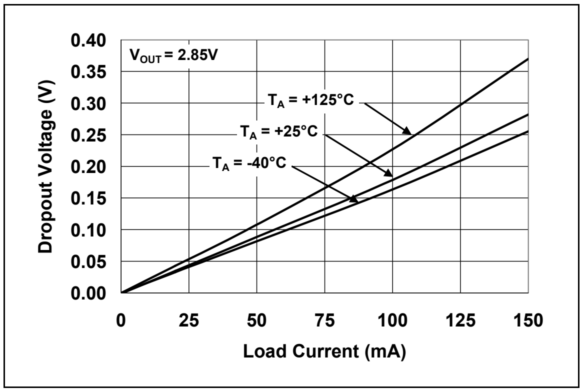


FIGURE 2-1: *Dropout Voltage vs. Output Current.*

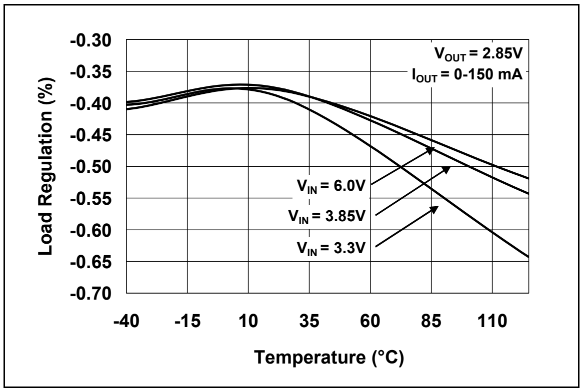


FIGURE 2-2: *Load Regulation vs. Temperature.*

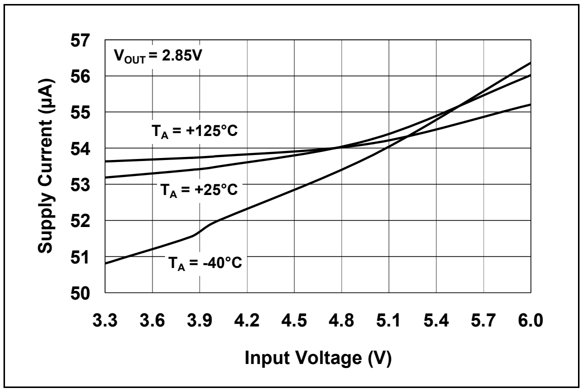


FIGURE 2-3: *Supply Current vs. Input Voltage.*

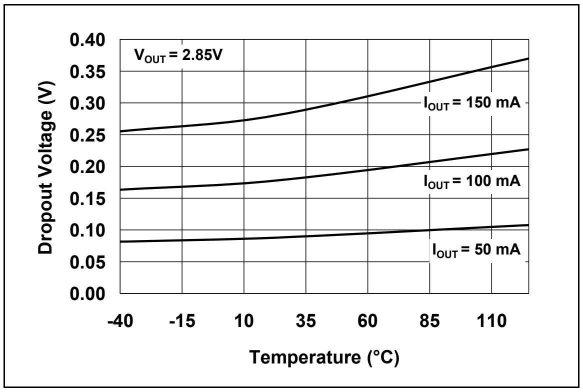


FIGURE 2-4: *Dropout Voltage vs. Temperature.*

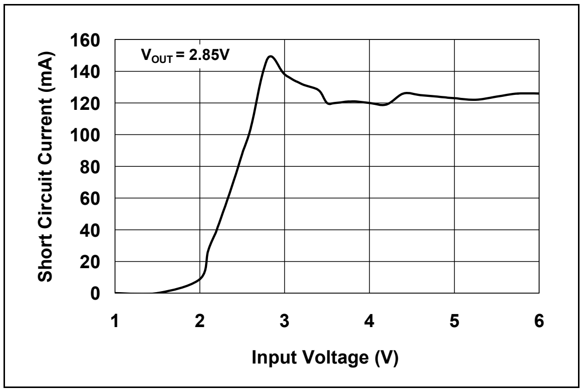


FIGURE 2-5: *Short-Circuit Current vs. Input Voltage.*

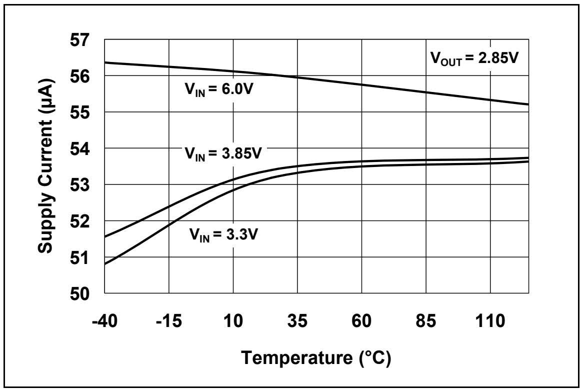


FIGURE 2-6: *Supply Current vs. Temperature.*

Note: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100\ \mu A$, $C_L = 1.0\ \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25°C$.

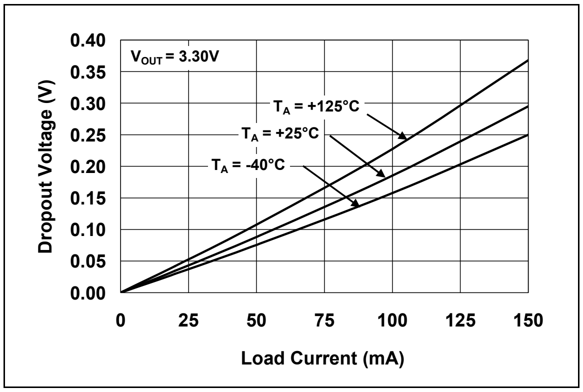


FIGURE 2-7: *Dropout Voltage vs. Output Current.*

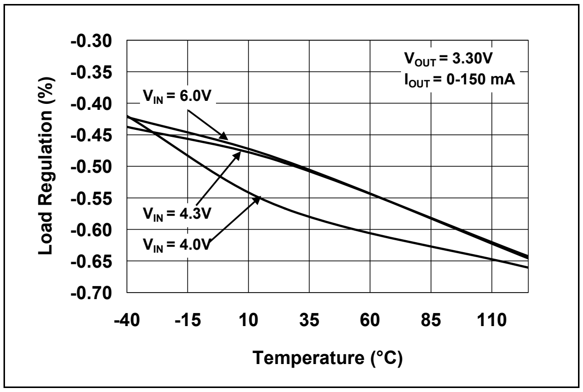


FIGURE 2-8: *Load Regulation vs. Temperature.*

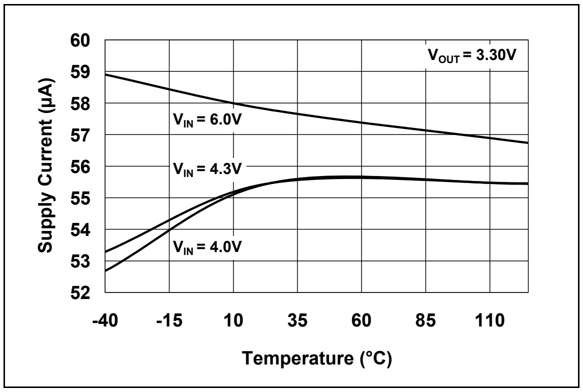


FIGURE 2-9: *Supply Current vs. Temperature.*

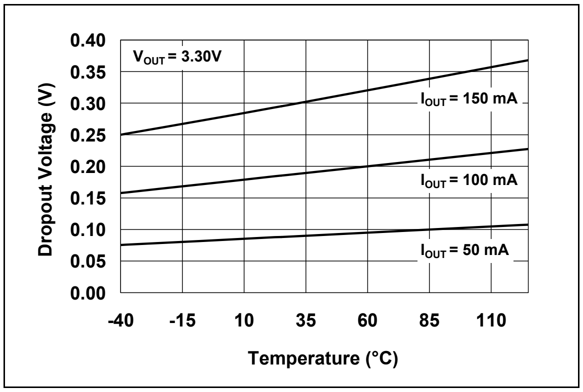


FIGURE 2-10: *Dropout Voltage vs. Temperature.*

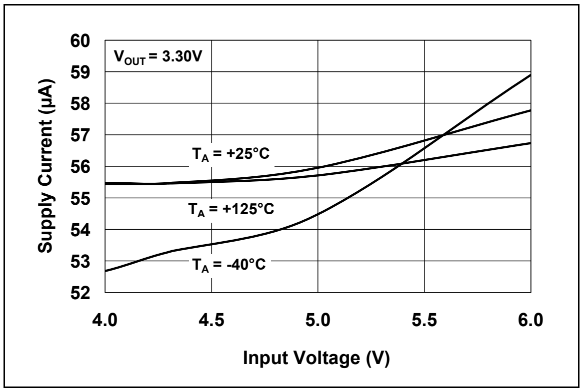


FIGURE 2-11: *Supply Current vs. Input Voltage.*

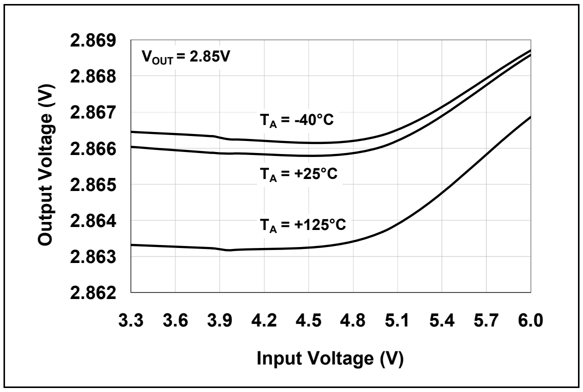


FIGURE 2-12: *Output Voltage vs. Supply Voltage.*

Note: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100\ \mu A$, $C_L = 1.0\ \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25°C$.

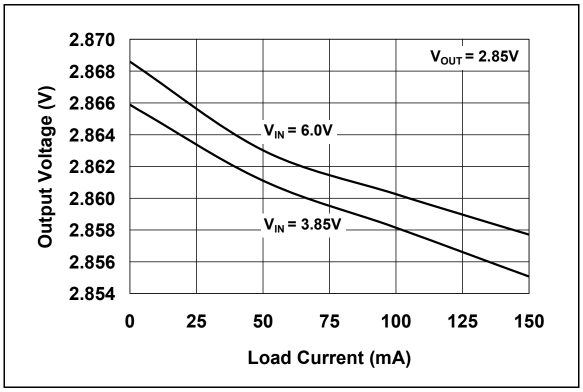


FIGURE 2-13: *Output Voltage vs. Output Current.*

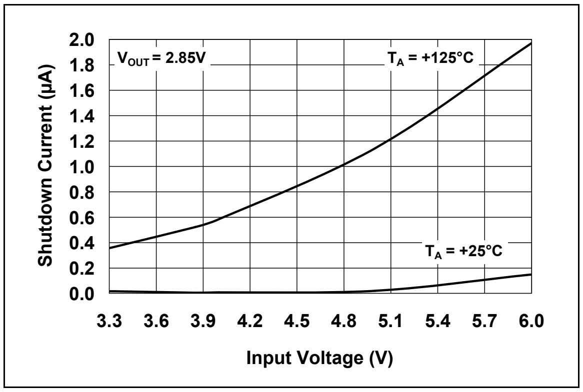


FIGURE 2-14: *Shutdown Current vs. Input Voltage.*

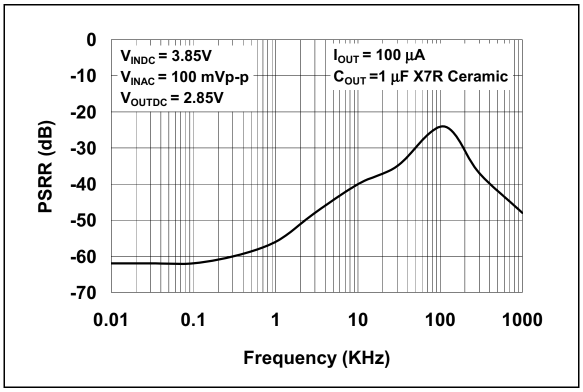


FIGURE 2-15: *Power Supply Rejection Ratio vs. Frequency.*

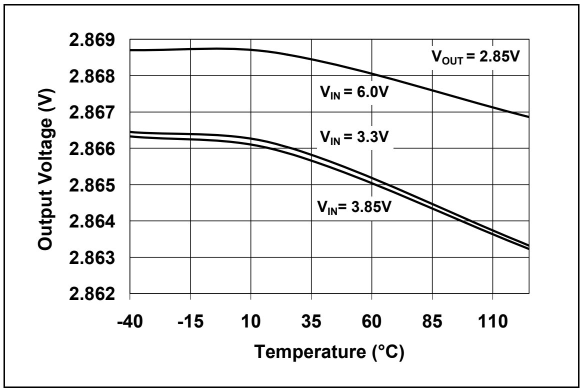


FIGURE 2-16: *Output Voltage vs. Temperature.*

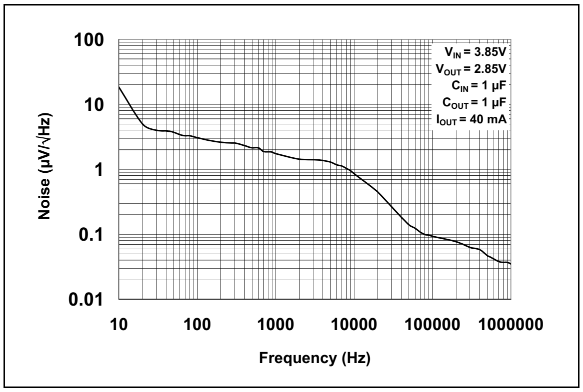


FIGURE 2-17: *Output Noise vs. Frequency.*

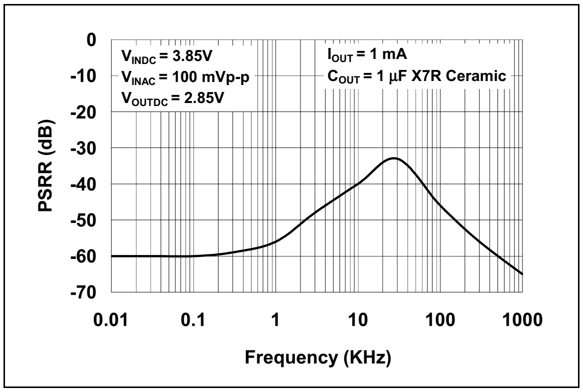


FIGURE 2-18: *Power Supply Rejection Ratio vs. Frequency.*

Note: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100\ \mu A$, $C_L = 1.0\ \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25°C$.

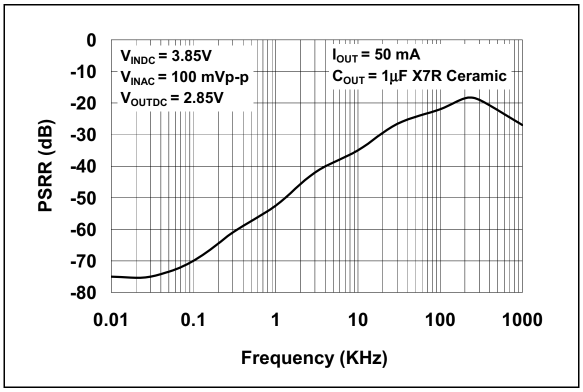


FIGURE 2-19: *Power Supply Rejection Ratio vs. Frequency.*

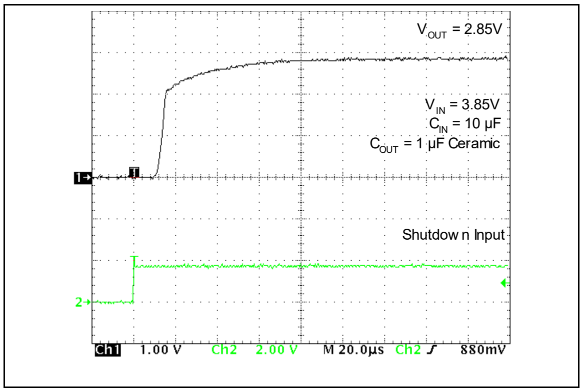


FIGURE 2-20: *Wake-Up Response.*

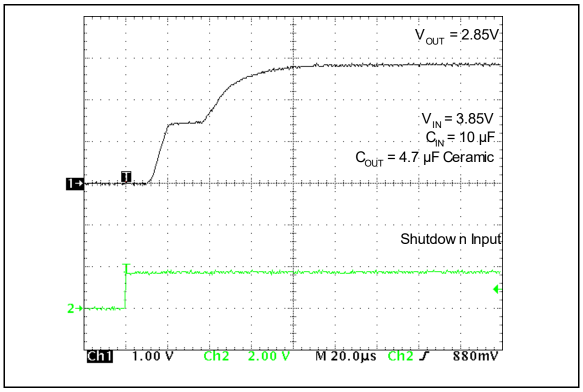


FIGURE 2-21: *Wake-Up Response.*

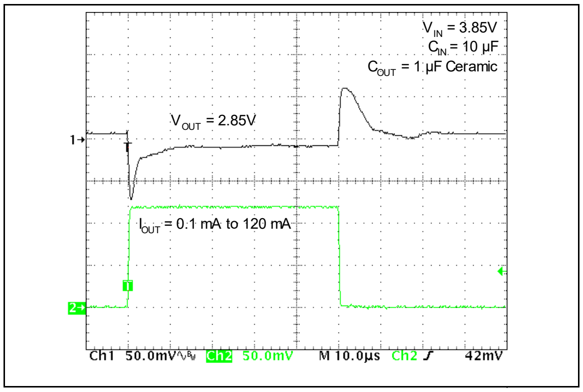


FIGURE 2-22: *Load Transient Response.*

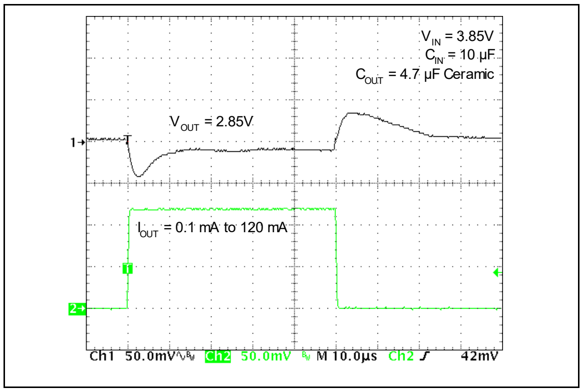


FIGURE 2-23: *Load Transient Response.*

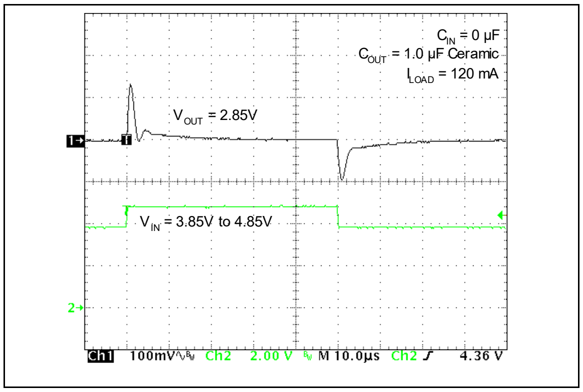


FIGURE 2-24: *Line Transient Response.*

Note: Unless otherwise noted, $V_{IN} = V_R + 1V$, $I_L = 100\ \mu A$, $C_L = 1.0\ \mu F$, $\overline{SHDN} > V_{IH}$, $T_A = +25°C$.

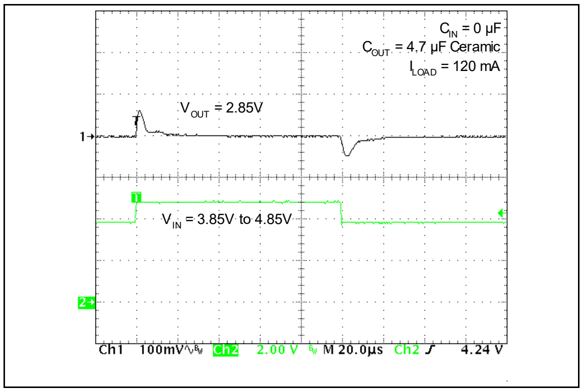


FIGURE 2-25: *Line Transient Response.*

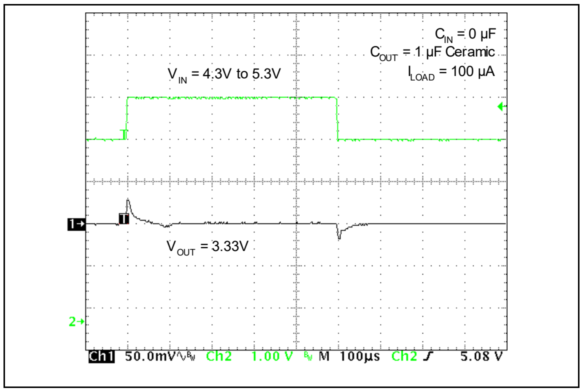


FIGURE 2-26: *Line Transient Response.*

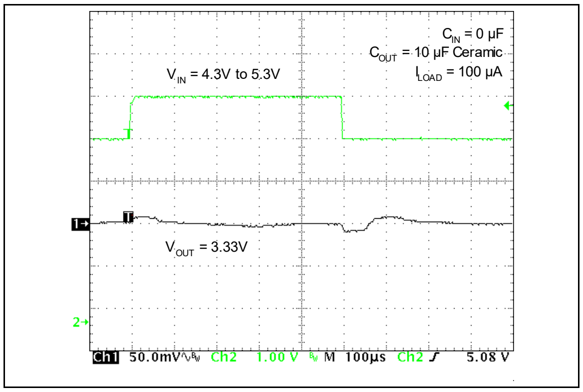


FIGURE 2-27: *Line Transient Response.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. 5-Pin SC-70	Pin No. 5-Pin SOT-23 5-Pin SC-70R	Symbol	Description
1	3	$\overline{\text{SHDN}}$	Shutdown Control Input
2	4	NC	No Connect
3	2	GND	Ground Terminal
4	5	V_{OUT}	Regulated Voltage Output
5	1	V_{IN}	Unregulated Supply Input

3.1 Shutdown Control Input ($\overline{\text{SHDN}}$)

The regulator is fully enabled when a logic-high is applied to $\overline{\text{SHDN}}$. The regulator enters shutdown when a logic-low is applied to this input. During shutdown, the output voltage falls to zero and the supply current is reduced to 0.05 µA (typ.)

3.2 Ground Terminal

For best performance, it is recommended that the ground pin be tied to a ground plane.

3.3 Regulated Voltage Output (V_{OUT})

Bypass the regulated voltage output to GND with a minimum capacitance of 1 µF. A ceramic bypass capacitor is recommended for best performance.

3.4 Unregulated Supply Input (V_{IN})

The minimum V_{IN} has to meet two conditions in order to ensure that the output maintains regulation: $V_{IN} \geq 2.7V$ and $V_{IN} \geq [(V_R + 2.5\%) + V_{DROPOUT}]$. The maximum V_{IN} should be less than or equal to 6V. Power dissipation may limit V_{IN} to a lower potential in order to maintain a junction temperature below 125°C. Refer to **Section 5.0 "Thermal Considerations"**, for determining junction temperature.

It is recommended that V_{IN} be bypassed to GND with a ceramic capacitor.

4.0 DETAILED DESCRIPTION

The TC1017 is a precision, fixed-output, linear voltage regulator. The internal linear pass element is a P-channel MOSFET. As with all P-channel CMOS LDOs, there is a body drain diode with the cathode connected to V_{IN} and the anode connected to V_{OUT} (Figure 4-1).

As is shown in Figure 4-1, the output voltage of the LDO is sensed and divided down internally to reduce external component count. The internal error amplifier has a fixed bandgap reference on the inverting input and the sensed output voltage on the noninverting input. The error amplifier output will pull the gate voltage down until the inputs of the error amplifier are equal to regulate the output voltage.

Output overload protection is implemented by sensing the current in the P-channel MOSFET. During a shorted or faulted load condition in which the output voltage falls to less than 0.5V, the output current is limited to a typical value of 120 mA. The current-limit protection helps prevent excessive current from damaging the Printed Circuit Board (PCB).

An internal thermal sensing device is used to monitor the junction temperature of the LDO. When the sensed temperature is over the set threshold of 160°C (typical), the P-channel MOSFET is turned off. When the P-channel is off, the power dissipation internal to the device is almost zero. The device cools until the junction temperature is approximately 150°C and the P-channel is turned on. If the internal power dissipation is still high enough for the junction to rise to 160°C, it will again shut off and cool. The maximum operating junction temperature of the device is 125°C. Steady-state operation at or near the 160°C overtemperature point can lead to permanent damage of the device.

The output voltage V_{OUT} remains stable over the entire input operating voltage range (2.7V to 6.0V) and the entire load range (0 mA to 150 mA). The output voltage is sensed through an internal resistor divider and compared with a precision internal voltage reference. Several fixed-output voltages are available by changing the value of the internal resistor divider.

Figure 4-2 shows a typical application circuit. The regulator is enabled any time the shutdown input pin is at or above V_{IH}. It is shut down (disabled) any time the shutdown input pin is below V_{IL}. For applications where the $\overline{\text{SHDN}}$ feature is not used, tie the $\overline{\text{SHDN}}$ pin directly to the input supply voltage source. While in shutdown, the supply current decreases to 0.05 µA (typical) and the P-channel MOSFET is turned off.

As shown in Figure 4-2, batteries have internal source impedance. An input capacitor is used to lower the input impedance of the LDO. In some applications, high input impedance can cause the LDO to become unstable. Adding more input capacitance can compensate for this.

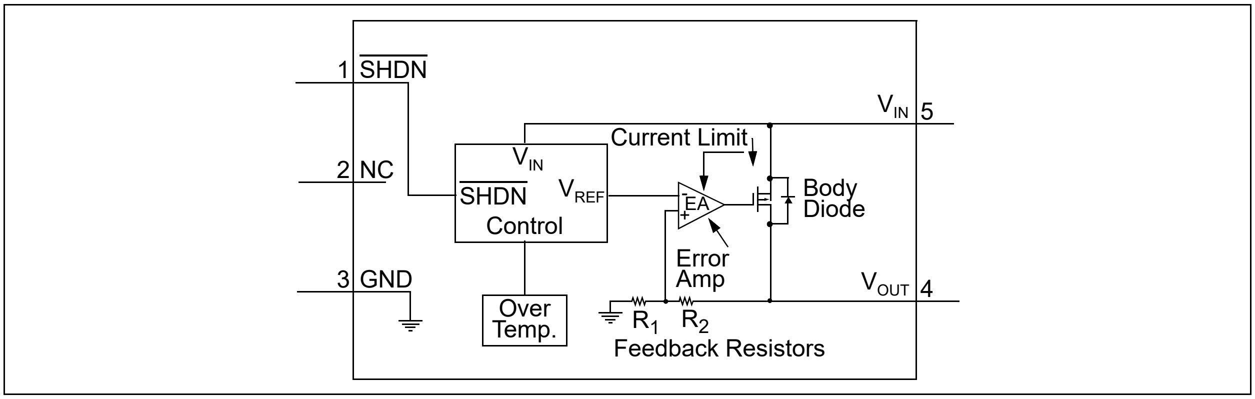


FIGURE 4-1: *TC1017 Block Diagram (5-Pin SC-70 Pinout).*

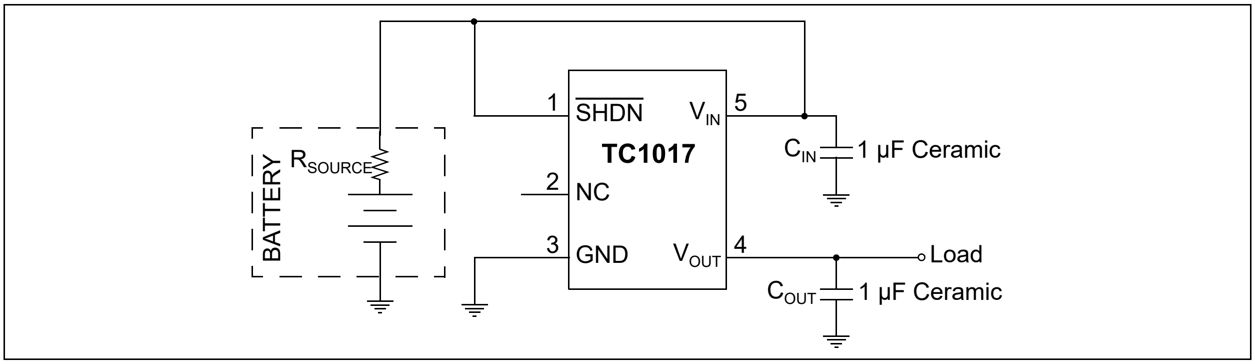


FIGURE 4-2: *Typical Application Circuit (5-Pin SC-70 Pinout).*

4.1 Input Capacitor

Low input source impedance is necessary for the LDO to operate properly. When operating from batteries, or in applications with long lead length (> 10") between the input source and the LDO, some input capacitance is required. A minimum of 0.1 µF is recommended for most applications and the capacitor should be placed as close to the input of the LDO as is practical. Larger input capacitors will help reduce the input impedance and further reduce any high-frequency noise on the input and output of the LDO.

4.2 Output Capacitor

A minimum output capacitance of 1 µF for the TC1017 is required for stability. The Equivalent Series Resistance (ESR) requirements on the output capacitor are between 0 and 2 ohms. The output capacitor should be located as close to the LDO output as is practical. Ceramic materials X7R and X5R have low temperature coefficients and are well within the acceptable ESR range required. A typical 1 µF X5R 0805 capacitor has an ESR of 50 milli-ohms. Larger output capacitors can be used with the TC1017 to improve dynamic behavior and input ripple-rejection performance.

Ceramic, aluminum electrolytic or tantalum capacitor types can be used. Since many aluminum electrolytic capacitors freeze at approximately -30°C, ceramic or solid tantalums are recommended for applications operating below -25°C. When operating from sources other than batteries, supply-noise rejection and transient response can be improved by increasing the value of the input and output capacitors and employing passive filtering techniques.

4.3 Turn-On Response

The turn-on response is defined as two separate response categories, wake-up time (t_{WK}) and settling time (t_S).

The TC1017 has a fast wake-up time (10 µsec, typical) when released from shutdown. See Figure 4-3 for the wake-up time designated as t_{WK}. The wake-up time is defined as the time it takes for the output to rise to 2% of the V_{OUT} value after being released from shutdown.

The total turn-on response is defined as the settling time (t_S) (see Figure 4-3). Settling time (inclusive with t_{WK}) is defined as the condition when the output is within 98% of its fully-enabled value (32 µsec, typical) when released from shutdown. The settling time of the output voltage is dependent on load conditions and output capacitance on V_{OUT} (RC response).

The table below demonstrates the typical turn-on response timing for different input voltage power-up frequencies: V_{OUT} = 2.85V, V_{IN} = 5.0V, I_{OUT} = 60 mA and C_{OUT} = 1 µF.

Frequency	Typical (t_{WK})	Typical (t_S)
1000 Hz	5.3 µsec	14 µsec
500 Hz	5.9 µsec	16 µsec
100 Hz	9.8 µsec	32 µsec
50 Hz	14.5 µsec	52 µsec
10 Hz	17.2 µsec	77 µsec

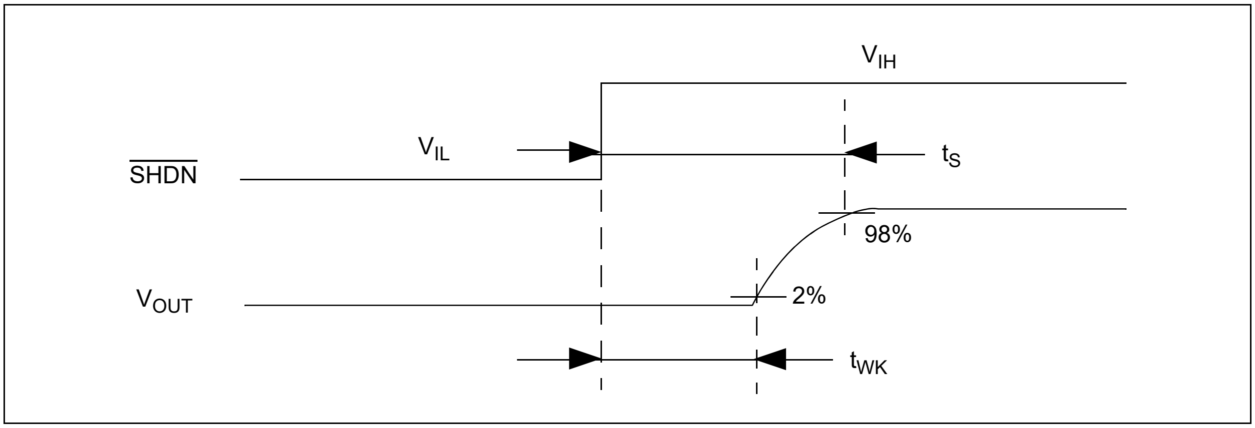


FIGURE 4-3: *Wake-Up Time from Shutdown.*

5.0 THERMAL CONSIDERATIONS

5.1 Thermal Shutdown

Integrated thermal protection circuitry shuts the regulator off when the die temperature exceeds approximately 160°C. The regulator remains off until the die temperature drops to approximately 150°C.

5.2 Power Dissipation: SC-70

The TC1017 is available in the SC-70 package. The thermal resistance for the SC-70 package is approximately 450°C/W when the copper area used in the PCB layout is similar to the JEDEC J51-7 high thermal conductivity standard or semi-G42-88 standard. For applications with a larger or thicker copper area, the thermal resistance can be lowered. See AN792, "*A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application*" (DS00792), for a method to determine the thermal resistance for a particular application.

The TC1017 power dissipation capability is dependant upon several variables: input voltage, output voltage, load current, ambient temperature and maximum junction temperature. The absolute maximum steady-state junction temperature is rated at +125°C. The power dissipation within the device is equal to:

EQUATION 5-1:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD} + V_{IN} \times I_{GND}$$

The V_{IN} x I_{GND} term is typically very small when compared to the (V_{IN}–V_{OUT}) x I_{LOAD} term, simplifying the power dissipation within the LDO to be:

EQUATION 5-2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

To determine the maximum power dissipation capability, the following equation is used:

EQUATION 5-3:

$$P_{DMAX} = \frac{(T_{J\_MAX} - T_{A\_MAX})}{R\theta_{JA}}$$

Where:

T_{J_MAX} = the maximum junction temperature allowed

T_{A_MAX} = the maximum ambient temperature

$R\theta_{JA}$ = the thermal resistance from junction to air

Given the following example:

V_{IN} = 3.0V to 4.1V

V_{OUT} = 2.85V ±2.5%

I_{LOAD} = 120 mA (output current)

T_A = 55°C (max. desired ambient)

Find:

1. Internal power dissipation:

$$\begin{aligned} P_{DMAX} &= (V_{IN\_MAX} - V_{OUT\_MIN}) \times I_{LOAD} \\ &= (4.1V - 2.85 \times (0.975)) \times 120mA \\ &= 158.5mW \end{aligned}$$

2. Maximum allowable ambient temperature:

$$\begin{aligned} T_{A\_MAX} &= T_{J\_MAX} - P_{DMAX} \times R\theta_{JA} \\ &= (125\,°C - 158.5mW \times 450\,°C/W) \\ &= (125\,°C - 71\,°C) \\ &= 54\,°C \end{aligned}$$

3. Maximum allowable power dissipation at desired ambient:

$$\begin{aligned} P_D &= \frac{T_{J\_MAX} - T_A}{R\theta_{JA}} \\ &= \frac{125\,°C - 55\,°C}{450\,°C/W} \\ &= 155mW \end{aligned}$$

In this example, the TC1017 dissipates approximately 158.5 mW and the junction temperature is raised 71°C over the ambient. The absolute maximum power dissipation is 155 mW when given a maximum ambient temperature of 55°C.

Input voltage, output voltage or load current limits can also be determined by substituting known values in the power dissipation equations.

Figure 5-1 and Figure 5-2 depict typical maximum power dissipation versus ambient temperature, as well as typical maximum current versus ambient temperature, with a 1V input voltage to output voltage differential, respectively.

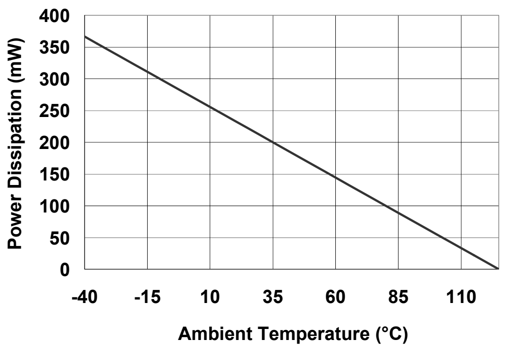


FIGURE 5-1: *Power Dissipation vs. Ambient Temperature (SC-70 package).*

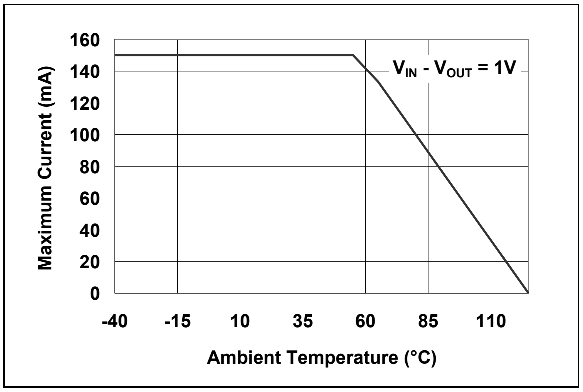


FIGURE 5-2: Maximum Current vs. Ambient Temperature (SC-70 package).

5.3 Power Dissipation: SOT-23

The TC1017 is also available in a SOT-23 package for improved thermal performance. The thermal resistance for the SOT-23 package is approximately 255°C/W when the copper area used in the printed circuit board layout is similar to the JEDEC J51-7 low thermal conductivity standard or semi-G42-88 standard. For applications with a larger or thicker copper area, the thermal resistance can be lowered. See AN792, "*A Method to Determine How Much Power a SOT-23 Can Dissipate in an Application*" (DS00792), for a method to determine the thermal resistance for a particular application.

The TC1017 power dissipation capability is dependant upon several variables: input voltage, output voltage, load current, ambient temperature and maximum junction temperature. The absolute maximum steady-state junction temperature is rated at +125°C. The power dissipation within the device is equal to:

EQUATION 5-4:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD} + V_{IN} \times I_{GND}$$

The V_{IN} x I_{GND} term is typically very small when compared to the (V_{IN}–V_{OUT}) x I_{LOAD} term, simplifying the power dissipation within the LDO to be:

EQUATION 5-5:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

To determine the maximum power dissipation capability, the following equation is used:

EQUATION 5-6:

$$P_{DMAX} = \frac{(T_{J\_MAX} - T_{A\_MAX})}{R\theta_{JA}}$$

Where:

T_{J_MAX} = the maximum junction temperature allowed

T_{A_MAX} = the maximum ambient temperature

$R\theta_{JA}$ = the thermal resistance from junction to air

Given the following example:

V_{IN} = 3.0V to 4.1V
V_{OUT} = 2.85V ±2.5%
I_{LOAD} = 120 mA (output current)
T_A = +85°C (max. desired ambient)

Find:

1. Internal power dissipation:

$$\begin{aligned} P_{DMAX} &= (V_{IN\_MAX} - V_{OUT\_MIN}) \times I_{LOAD} \\ &= (4.1V - 2.85 \times (0.975)) \times 120mA \\ &= 158.5mW \end{aligned}$$

2. Maximum allowable ambient temperature:

$$\begin{aligned} T_{A\_MAX} &= T_{J\_MAX} - P_{DMAX} \times R\theta_{JA} \\ &= (125\,°C - 158.5mW \times 255\,°C/W) \\ &= (125\,°C - 40.5\,°C) \\ &= 84.5\,°C \end{aligned}$$

3. Maximum allowable power dissipation at desired ambient:

$$\begin{aligned} P_D &= \frac{T_{J\_MAX} - T_A}{R\theta_{JA}} \\ &= \frac{125\,°C - 85\,°C}{255\,°C/W} \\ &= 157mW \end{aligned}$$

In this example, the TC1017 dissipates approximately 158.5 mW and the junction temperature is raised 40.5°C over the ambient. The absolute maximum power dissipation is 157 mW when given a maximum ambient temperature of +85°C.

Input voltage, output voltage or load current limits can also be determined by substituting known values in the power dissipation equations.

Figure 5-3 and Figure 5-4 depict typical maximum power dissipation versus ambient temperature, as well as typical maximum current versus ambient temperature with a 1V input voltage to output voltage differential, respectively.

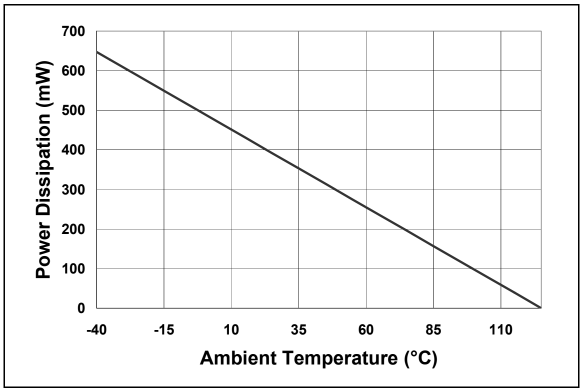


FIGURE 5-3: *Power Dissipation vs. Ambient Temperature (SOT-23 Package).*

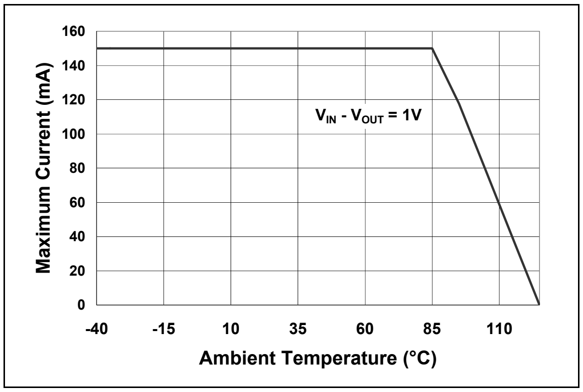


FIGURE 5-4: *Maximum Current vs. Ambient Temperature (SOT-23 Package).*

5.4 Layout Considerations

The primary path for heat conduction out of the SC-70/SOT-23 package is through the package leads. Using heavy, wide traces at the pads of the device will facilitate the removal of the heat within the package, thus lowering the thermal resistance $R\theta_{JA}$. By lowering the thermal resistance, the maximum internal power dissipation capability of the package is increased.

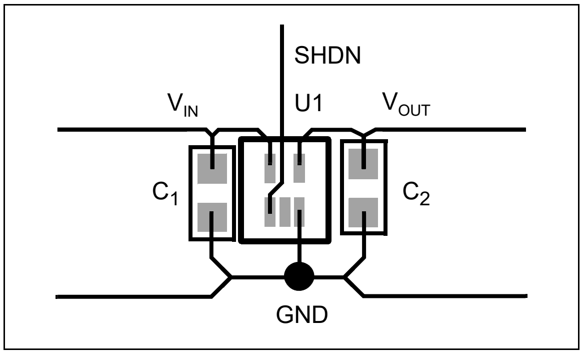
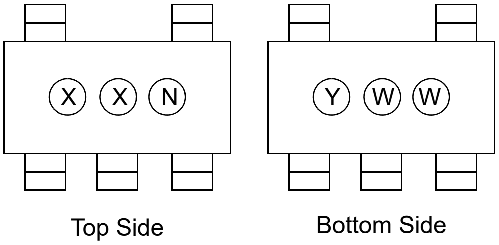


FIGURE 5-5: *SC-70 Package Suggested Layout.*

6.0 PACKAGE INFORMATION

6.1 Package Marking Information

5-Pin SC-70/SC-70R

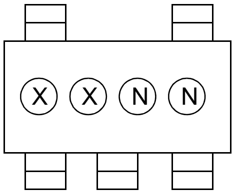


Top Side

Bottom Side

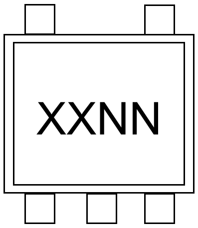
OR

5-Pin SC-70/SC-70R



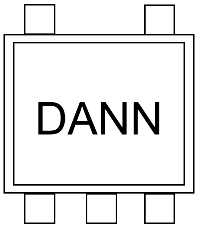
Part Number	TC1017 Pinout Code	TC1017R Pinout Code
TC1017 – 1.8VLT	CE	CU
TC1017 – 1.85VLT	CQ	DF
TC1017 – 1.9VLT	CB	
TC1017 – 2.5VLT	CR	CV
TC1017 – 2.6VLT	CF	CW
TC1017 – 2.7VLT	CG	CX
TC1017 – 2.8VLT	CH	CY
TC1017 – 2.85VLT	CJ	CZ
TC1017 – 2.9VLT	CK	DA
TC1017 – 3.0VLT	CL	DB
TC1017 – 3.2VLT	CC	DC
TC1017 – 3.3VLT	CM	DD
TC1017 – 4.0VLT	CP	DE

5-Lead SOT-23



Part Number	Code
TC1017 – 1.8VCT	DA
TC1017 – 1.85VCT	DK
TC1017 – 2.6VCT	DB
TC1017 – 2.7VCT	DC
TC1017 – 2.8VCT	DD
TC1017 – 2.85VCT	DE
TC1017 – 2.9VCT	DF
TC1017 – 3.0VCT	DG
TC1017 – 3.3VCT	DH
TC1017 – 4.0VCT	DJ

Example:

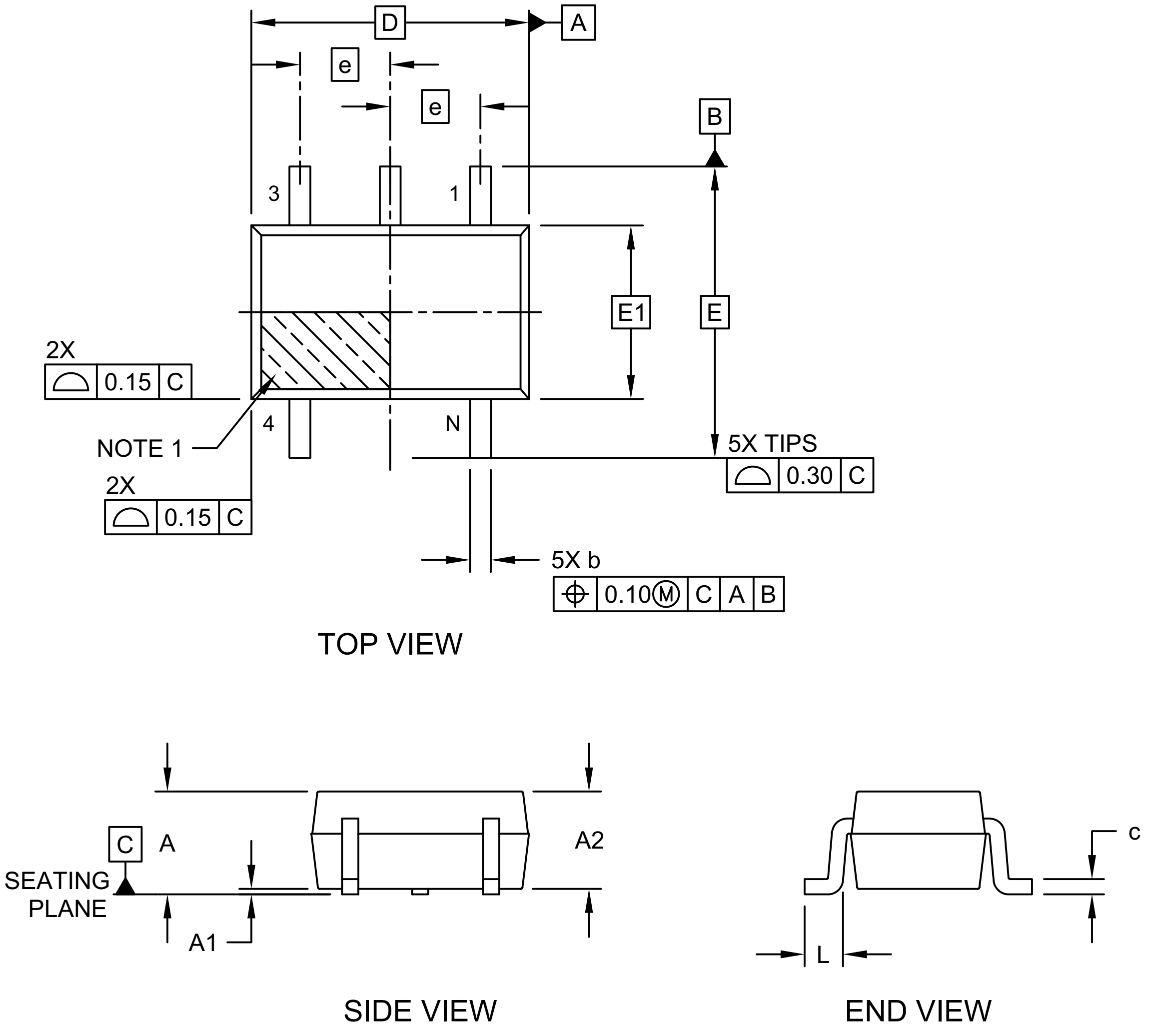


Legend:		
	XX...X	Customer-specific information*
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5-Lead Plastic Small Outline Transistor (LT) [SC70]

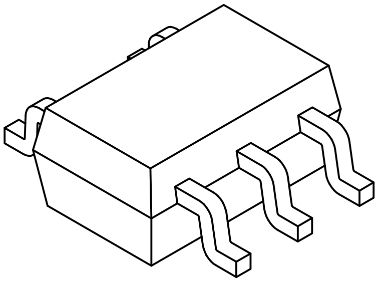
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-061-LT Rev E Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.65 BSC		
Overall Height	A	0.80	-	1.10
Standoff	A1	0.00	-	0.10
Molded Package Thickness	A2	0.80	-	1.00
Overall Length	D	2.00 BSC		
Overall Width	E	2.10 BSC		
Molded Package Width	E1	1.25 BSC		
Terminal Width	b	0.15	-	0.40
Terminal Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	-	0.26

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

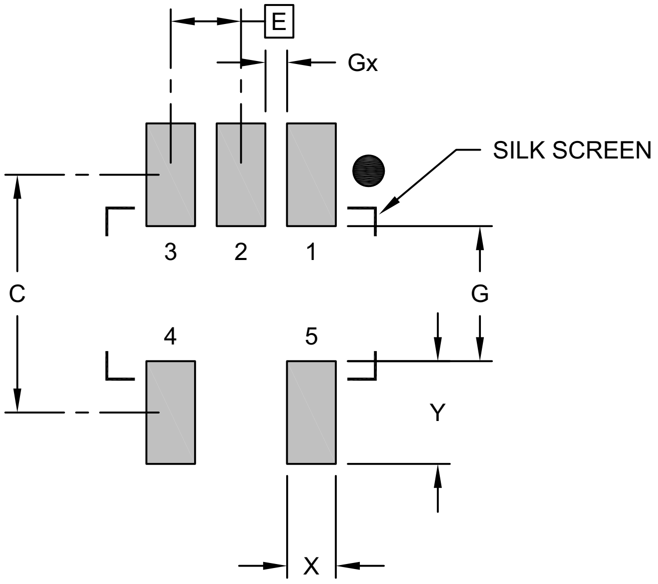
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-061-LT Rev E Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

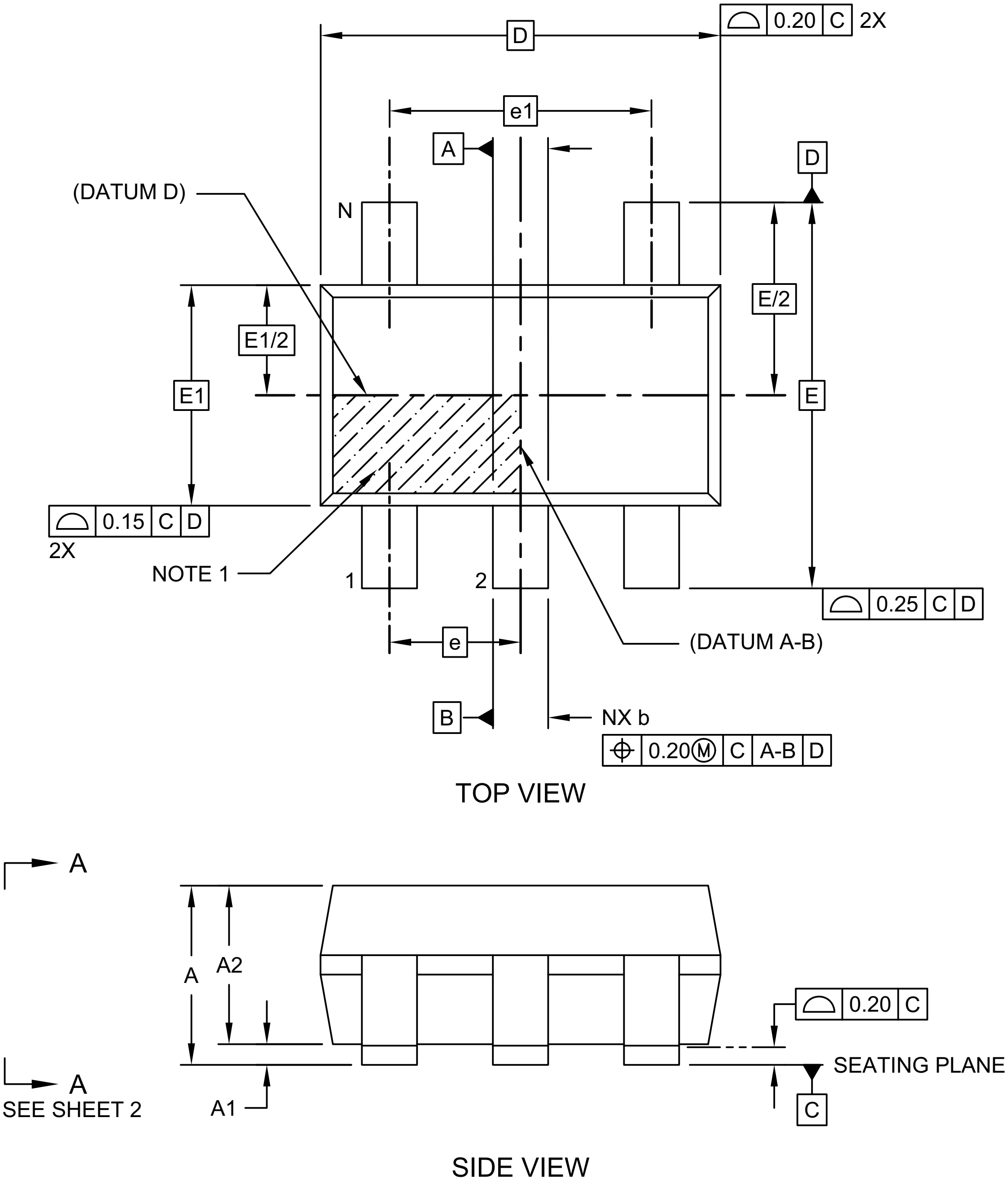
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061-LT Rev E

5-Lead Plastic Small Outline Transistor (C7X) [SOT-23]

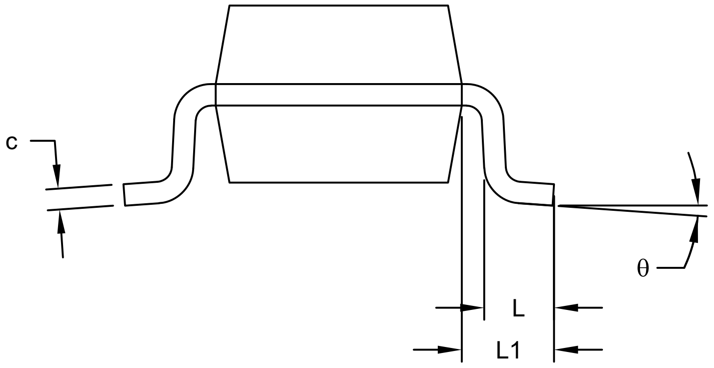
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



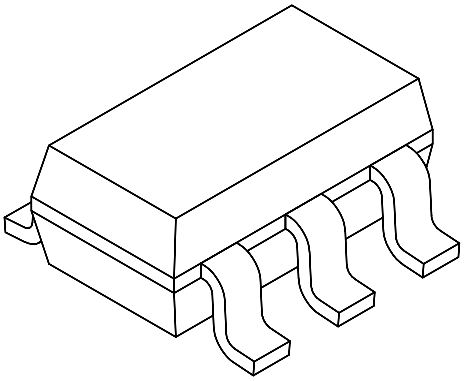
Microchip Technology Drawing C04-091-C7X Rev H Sheet 1 of 2

5-Lead Plastic Small Outline Transistor (C7X) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW A-A
SHEET 1



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	-	0.60
Footprint	L1	0.60 REF		
Foot Angle	θ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

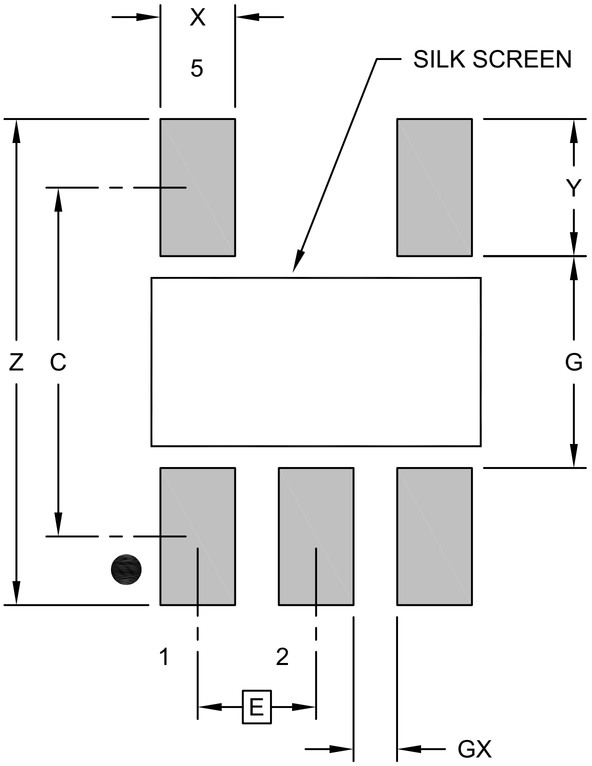
Notes:

1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-C7X Rev H Sheet 2 of 2

5-Lead Plastic Small Outline Transistor (C7X) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-C7X Rev H

NOTES:

APPENDIX A: REVISION HISTORY

Revision G (August 2023)

- Added information about the Automotive Qualification status of the device in Section , Features.
- Added ESD values to Section 1.0, Electrical Characteristics.
- Updated package drawings in Section 6.0, Package Information.
- Updated Section , Product Identification System, with Automotive Qualified devices.

Revision F (April 2013)

The following is the list of modifications:

- Updated the information for the Maximum Output Current parameter in the Electrical Characteristics table.

Revision E (January 2013)

- Added a note to each package outline drawing.

Revision D (February 2005)

- Undocumented changes.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X.XX	X	XXXX	–XXX
Device	**Voltage Options**	**Temperature Range**	**Package**	**Qualification**

Device:	TC1017: 150 mA Tiny CMOS LDO with Shutdown TC1017R:150 mA Tiny CMOS LDO with Shutdown (SC-70 only)
Voltage Options:* (Standard)	1.8V 1.85V 2.5V SC-70 only 2.6V 2.7V 2.8V 2.85V 2.9V 3.0V 3.2V SC-70 only 3.3V 4.0V * Other voltage options available. Please contact your local Microchip sales office for details.
Temperature Range:	V = -40°C to +125°C
Package:	LTTR = 5-pin SC-70 (Tape and Reel) CTTR = 5-pin SOT-23 (Tape and Reel)
Qualification:**	<Blank> = Standard Part VAO = AEC-Q100 Automotive Qualified ** Contact your local Microchip sales office to request automotive qualified part variants.

Examples:

a) TC1017-1.8VLTTR:	150 mA, Tiny CMOS LDO with Shutdown, SC-70 package
b) TC1017R-1.8VLTTR:	150mA, Tiny CMOS LDO with Shutdown, SC-70 package
c) TC1017-2.6VCTTR:	150 mA, Tiny CMOS LDO with Shutdown, SOT-23 package
d) TC1017-2.7VLTTR:	150 mA, Tiny CMOS LDO with Shutdown, SC-70 package
e) TC1017-2.8VCTTR:	150 mA, Tiny CMOS LDO with Shutdown, SOT-23 package
f) TC1017-2.85VLTTR:	150 mA, Tiny CMOS LDO with Shutdown, SC-70 package
g) TC1017-2.9VCTTR:	150 mA, Tiny CMOS LDO with Shutdown, SOT-23 package
h) TC1017-3.0VLTTR:	150 mA, Tiny CMOS LDO with Shutdown, SC-70 package
i) TC1017-3.3VCTTR:	150 mA, Tiny CMOS LDO with Shutdown, SOT-23 package
j) TC1017-3.3VCTTR-VAO**:	150 mA, Tiny CMO LDO with Shutdown, SOT-23 package, AEC-Q100Automotive Qualified
k) TC1017-4.0VLTTR:	150 mA, Tiny CMOS LDO with Shutdown, SC-70 package

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

** Example of automotive part variant that can be set up.

NOTES:

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ISBN: 978-1-6683-2958-0

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