# KSZ8895MQX

## Hardware Design Checklist

## 1.0 INTRODUCTION

This document provides a hardware design checklist for the Microchip KSZ8895MQX. These checklist items should be followed when utilizing the KSZ8895MQX in a new design. A summary of these items is provided in Section 12.0, "Hardware Checklist Summary," on page 17. Detailed information on these subjects can be found in the corresponding sections:



## 2.0 GENERAL CONSIDERATIONS

### 2.1 Required References

The KSZ8895MQX implementor should have the following documents on hand:

- *KSZ8895MQX/RQX/FQX/ML Integrated 5-Port 10/100 Managed Switch Data Sheet*
- *KSZ8895/KSZ8864 Silicon Errata and Data Sheet Clarification*
- KSZ8895MQX_RQX_DP_V1.3.zip for the KSZ8895 Design Package

### 2.2 Pin Check

Check the pinout of the part against the data sheet. Ensure that all pins match the data sheet and are configured as inputs, outputs, or bidirectional for error checking.

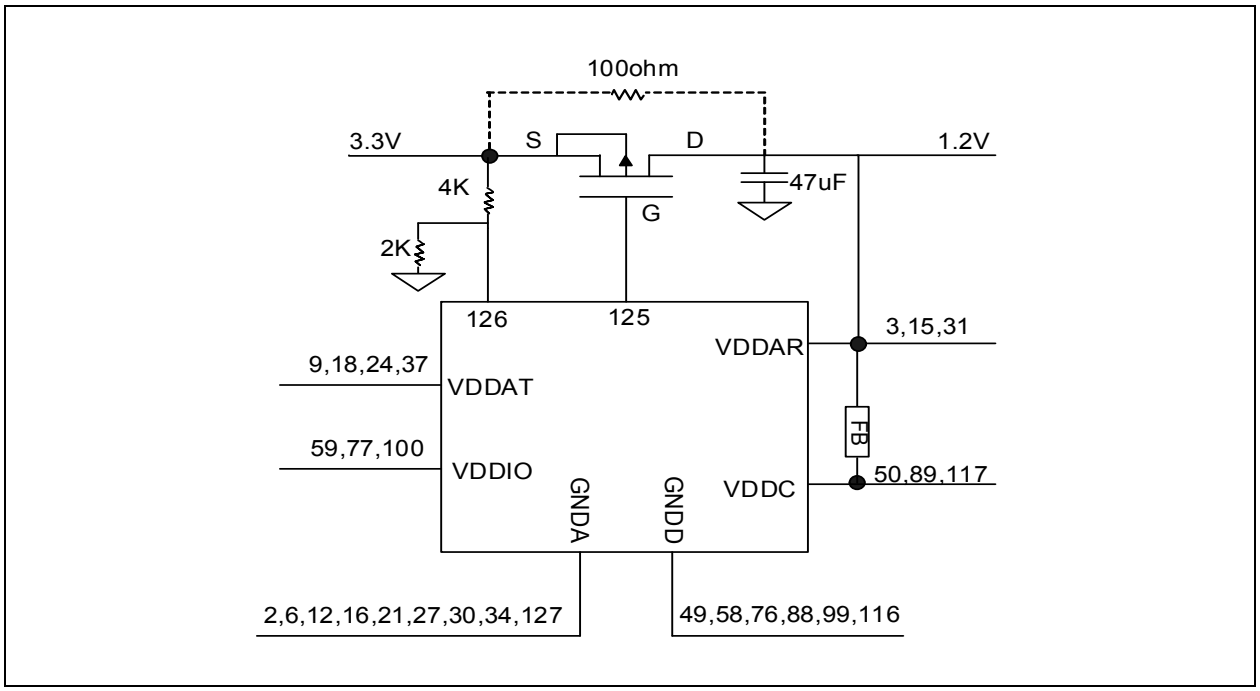
### 2.3 Ground

- The ground pin, **GND**, should be connected to the digital ground, and the analog ground should be connected to the solid contiguous ground plane as system ground on the board. Separate digital ground and analog ground planes are not recommended.
- If using the magnetics and RJ45 connector, a chassis ground should be used for the line side of the magnetics and the metal case of the RJ45 connector. The system ground and the chassis ground should be tied together by a ferrite bead. The ferrite bead should be placed far away from the Ethernet device for better ESD and EMI.

## 3.0 POWER

- The analog supply (**VDDAT**) pins on the KSZ8895MQX are 9, 18, 24, and 37. It requires a connection to **VDDAT** (created from +3.3V through a ferrite bead). Be sure to place bulk capacitance on each side of the ferrite bead.
- **VDDAT** pins should have a 0.1 µF capacitor to decouple the device. The capacitor size should be SMD_0603 or smaller.
- The KSZ8895MQX **VDDIO** supports three VDDIO voltages—1.8V, 2.5V, and 3.3V. Pins 59, 77, and 100 (**VDDIO**) should be connected to one of three VDDIO voltages based on real application.
- For KSZ8895MQX 1.2V core power, there are two solutions. The first is using an internal 1.2V LDO controller with an external MOSFET. The second is using an external 1.2V LDO.

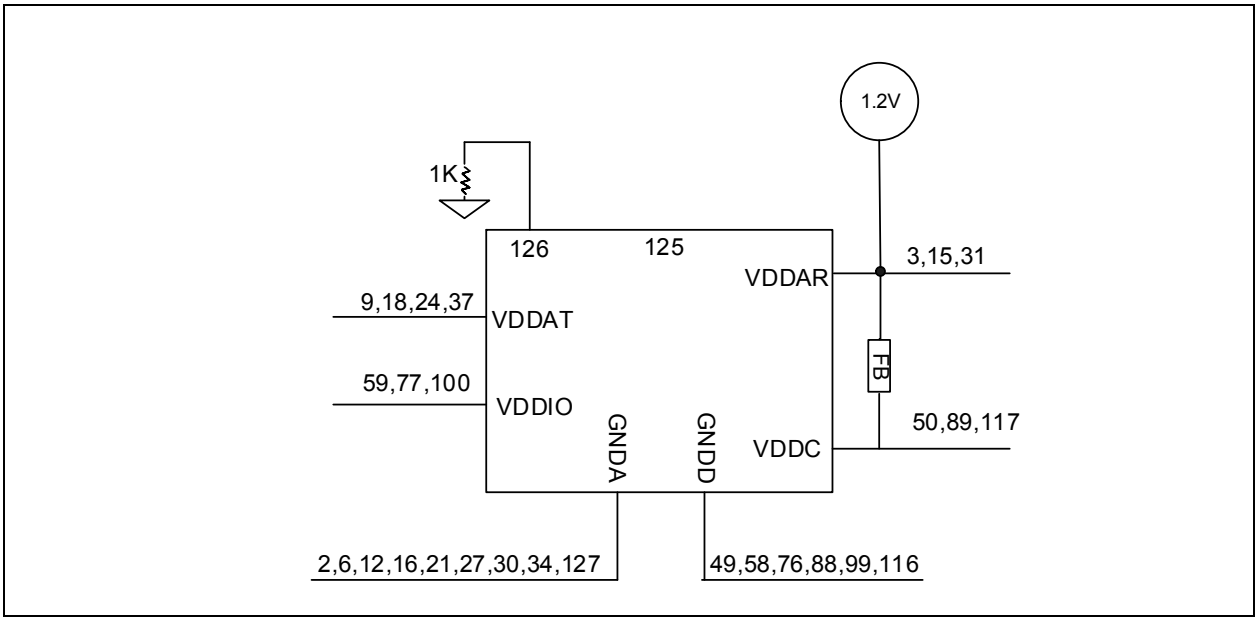
**FIGURE 3-1: USING INTERNAL 1.2V LDO CONTROLLER**




a) The internal 1.2V LDO controller with external MOSFET is shown in Figure 3-1. The MOSFET pin S in Figure 3-1 should use 3.3V as input power. The KSZ8895MQX pin 126 should use a resistor divider with 2:1 (pull-up:pull-down) resistor ratio. To control the internal 1.2V LDO controller correctly, it is recommended that 4 kΩ pull-up and 2 kΩ pull-down resistor dividers be used. The trace from **FET** pin D to **VDDAR** should be as short as possible without a ferrite bead. Use a 47 µF capacitor on FET pin D for a 1.2V power rail. It is highly suggested that a 100Ω resistor be placed between **FET** pin S and pin D. Except the previously mentioned, all power rails and power pins should have 0.1 µF capacitors as the decouple capacitors. A ferrite bead is necessary between analog 1.2V **VDDAR** and digital 1.2V **VDDC**.

b) The external 1.2V solution is shown in Figure 3-2.There is no MOSFET circuit, and an external 1.2V power source is needed.

**FIGURE 3-2: USING EXTERNAL 1.2V LDO**



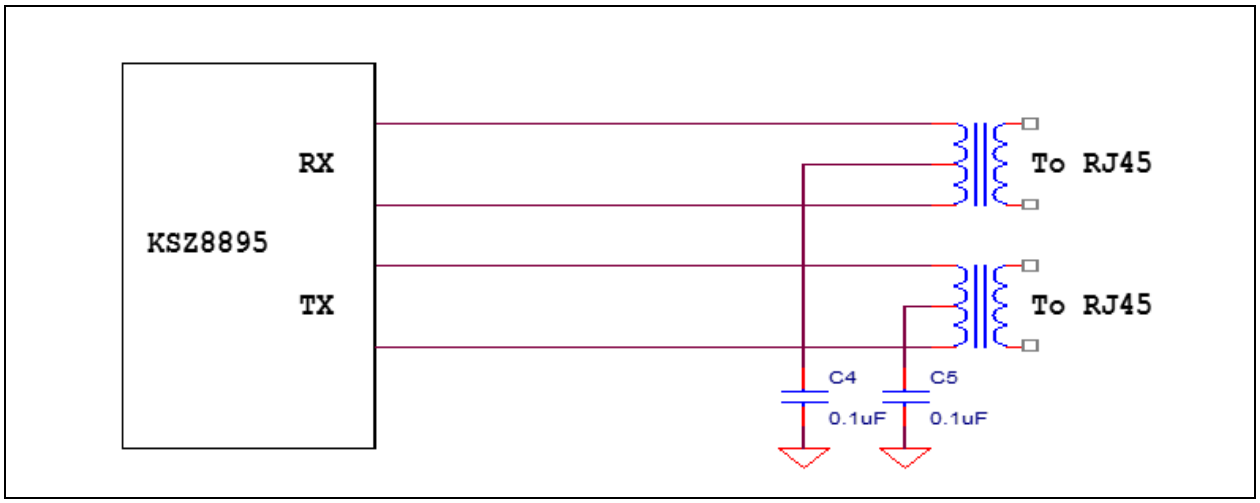
## 4.0 ETHERNET SIGNALS

The KSZ8895MQX has five integrated PHYs that are fully compliant with IEEE 802.3u standard to support 10/100Base-T/TX Ethernet copper port.

### 4.1 KSZ8895MQX Copper Ports Connection

- The KSZ8895MQX has five Ethernet copper ports. All ports are voltage drivers with internal DC biasing and on-chip termination, so there are no external termination resistors and DC biasing power on the magnetics. Each port connection between KSZ8895MQX and magnetics is illustrated in Figure 4-1.

**FIGURE 4-1: ONE ETHERNET PORT CONNECTION WITH MAGNETICS**




- Both center taps, **RX** and **TX**, of the magnetics on the chip side should be separately connected to the ground with two capacitors.
- In the Ethernet switch, the **RX** +/– differential pair should be connected to RJ45 connector pins 1 and 2 through magnetics.
- In the Ethernet switch, **TX** +/–differential pair should be connected to RJ45 connector pins 3 and 6 through magnetics.

### 4.2 Other Ethernet Copper Ports

- Other Ethernet ports on KSZ8895MQX are same with Section 4.1, KSZ8895MQX Copper Ports Connection and have similar schematic connection with Figure 4-1 on the chip side.
- For unused Ethernet copper port, the user may leave the **RX** pair and **TX** pair floating because KSZ8895MQX analog ports have internal termination for this on-chip termination device.

### 4.3 Magnetics Connection at the Chip Side

- The center tap connection on the KSZ8895MQX side for the transmit channel should not be connected to **VDDAT**. The transmit channel center tap of the magnetics should connect to system ground through Common-mode capacitor only. The Common-mode capacitor value can be from 0.1 µF to 10 µF.
- The center tap connection on the KSZ8895MQX side for the receive channel should not be connected to **VDDAT**. The receive channel center tap of the magnetics should connect to system ground through Common-mode capacitor only. The Common mode capacitor value can be from 0.1 µF to 10 µF.
- When using the KSZ8895MQX device in the HP Auto MDIX mode of operation, use a magnetics module with identical TX and RX paths.

## 4.4 Magnetics Connection at Line Side of RJ45 Connector

- In the Switch design, the pin 1 of the RJ45 should be connected to **RX**+ of the KSZ8895MQX. The pin 2 of the RJ45 should be connected to **RX**– of the KSZ8895MQX.
- In the Switch design, the pin 3 of the RJ45 should be connected to **TX**+ of the KSZ8895MQX. The pin 6 of the RJ45 should be connected to **TX**– of the KSZ8895MQX.
- The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 pF, 2 KV capacitor to chassis ground.
- The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 pF, 2 KV capacitor to chassis ground.
- The RJ45 pins 4 and 5 should be shorted and then terminated with a 75Ω resistor through the 1000 pF to the chassis ground.
- The RJ45 pins 7 and 8 should be shorted and then terminated with a 75Ω resistor through the 1000 pF to the chassis ground.
- Only one 1000 pF, 2 KV capacitor to chassis ground is required. It is shared by both **TX** and **RX** center taps.
- The RJ45 connector shield should be tied directly to the chassis ground.

## 4.5 Alternative Termination Selection for RJ45 Connector

- Pins 4 and 5 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 KV capacitor. There are two methods for accomplishing this:
  a) Pins 4 and 5 can be connected with two 49.9Ω resistors. The common connection of these resistors should be linked through a third 49.9Ω resistor to the 1000 pF, 2 KV capacitor.
  b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. An equivalent circuit is created by shorting pins 4 and 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 KV capacitor to chassis ground.
- Pins 7 and 8 of the RJ45 connector interface to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2 KV capacitor. There are two methods for accomplishing this:
  a) Pins 7 and 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be linked through a third 49.9Ω resistor to the 1000 pF, 2 KV capacitor.
  b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel perform like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω resistor causes the entire circuit to function as a 75Ω resistor. An equivalent circuit is created by shorting pins 7 and 8 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2 KV capacitor to chassis ground.
- The RJ45 connector shield should be attached directly to chassis ground.

## 4.6 Using RJ45 with Integrated LED

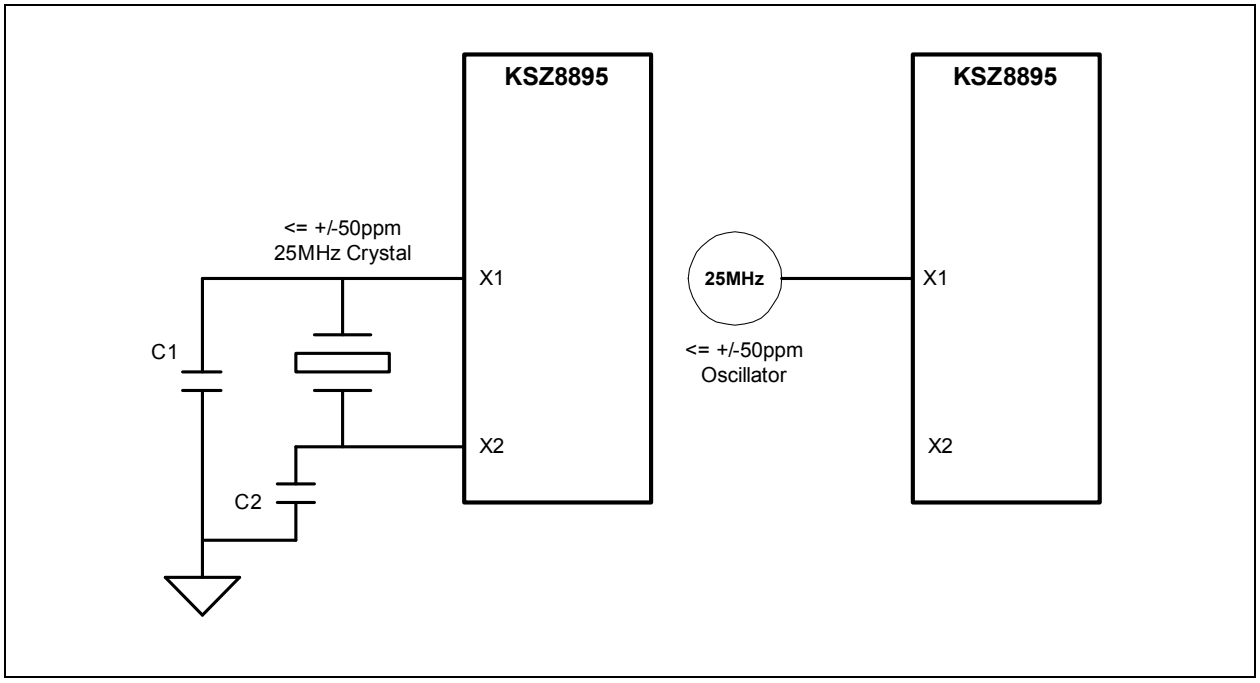
- The user can utilize the RJ45 connector with integrated LED components if the product working environment is not very noisy.
- If the designed product works inside an electrically noisy outside environment, it is not recommended to use RJ45 with integrated LED. This is because the outside interference signal or voltage is coupled to the LED circuit through the line side of RJ45 due to the LED circuit directly connected to chip and system power/ground. It is better to use independent LED components.
- If the user needs to utilize the RJ45 with an integrated LED circuit in a noisy environment, consider adding TVS diodes to protect the chip.

## 5.0 CLOCK CIRCUIT

### 5.1 Crystal and External Oscillator/Clock Connections

- **X1** (pin 121) is the clock circuit input for the KSZ8895MQX device. This pin requires a capacitor to ground when a crystal is used. One side of the crystal connects to this pin.
- **X2** (pin 122) is the clock circuit output for the KSZ8895MQX device. This pin requires a capacitor to ground when a crystal is used. One side of the crystal connects to this pin.
- Since every system design is unique, the capacitor values are system dependent based on the $C_L$ specifications of the crystal and the stray capacitance value. Refer to the crystal data sheet for the $C_L$ required. The PCB design, crystal, and layout all contribute to the characteristics of this circuit.
- Alternatively, a 25.000 MHz clock oscillator may be used to provide the clock source for the KSZ8895MQX. When using a single-ended clock source, **X1** (pin 121) connects to a 3.3V-tolerant oscillator. **X2** (pin 122) should be left floating as No Connect (NC). See Figure 5-1.

**FIGURE 5-1: CRYSTAL OR OSCILLATOR CONNECTIONS FOR KSZ8895MQX**



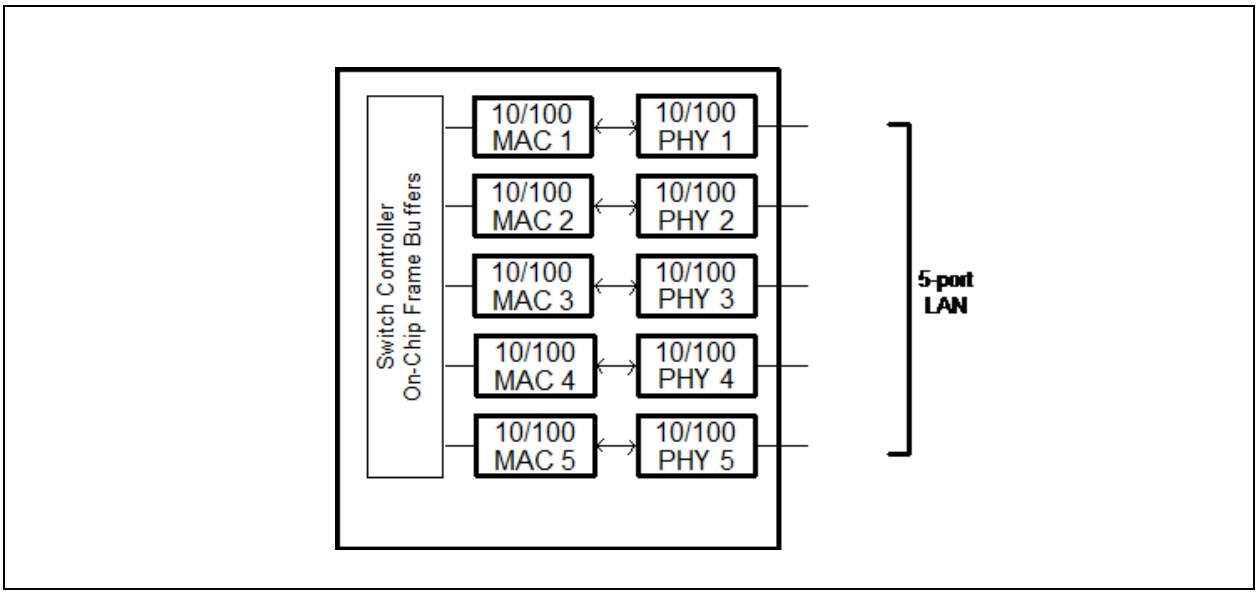
## 6.0 SYSTEM APPLICATION

The KSZ8895MQX applications can be divided into the following three categories:

### 6.1 Design for a Standalone Five-Port Switch

- Set strap-in pin# [91, 86, 87] = '100' to keep their default values for a standalone five-port switch.
- Based on real application, select with or without EEPROM for an unmanaged five-port switch. See Figure 6-1.

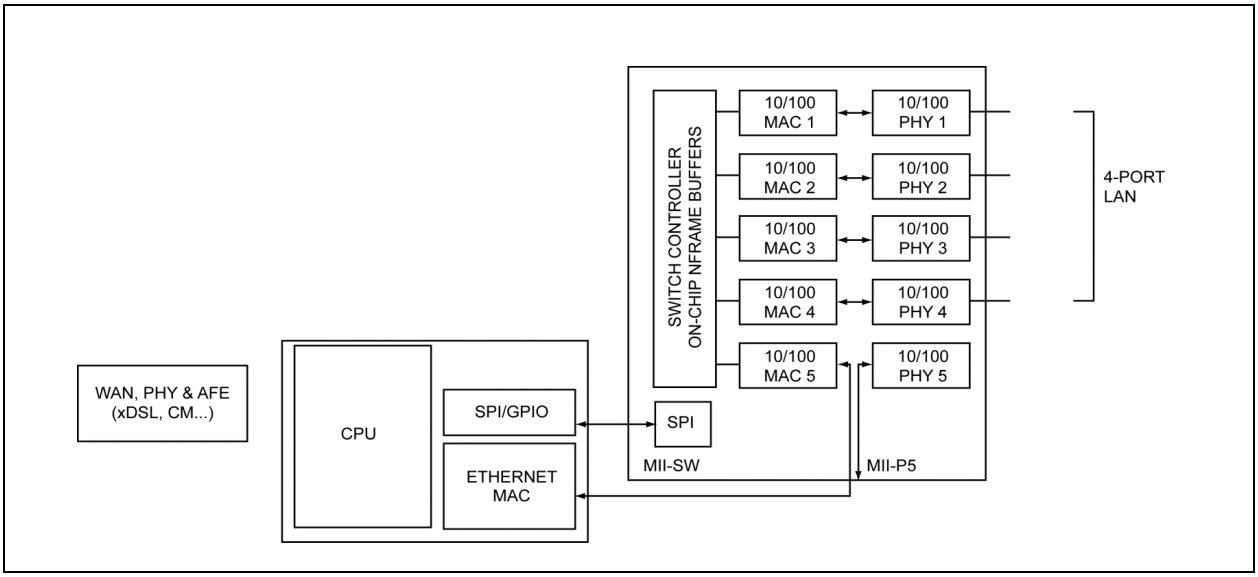
**FIGURE 6-1: UNMANAGED STANDALONE SWITCH**




### 6.2 Design for Managed Switch using only Port 5 MAC 5 MII

- The strap-in pin# [91, 86, 87] should be configured to '001' for MAC 5 MII PHY mode to SoC.
- Use SPI interface that can access all registers for a managed switch. See Figure 6-2.

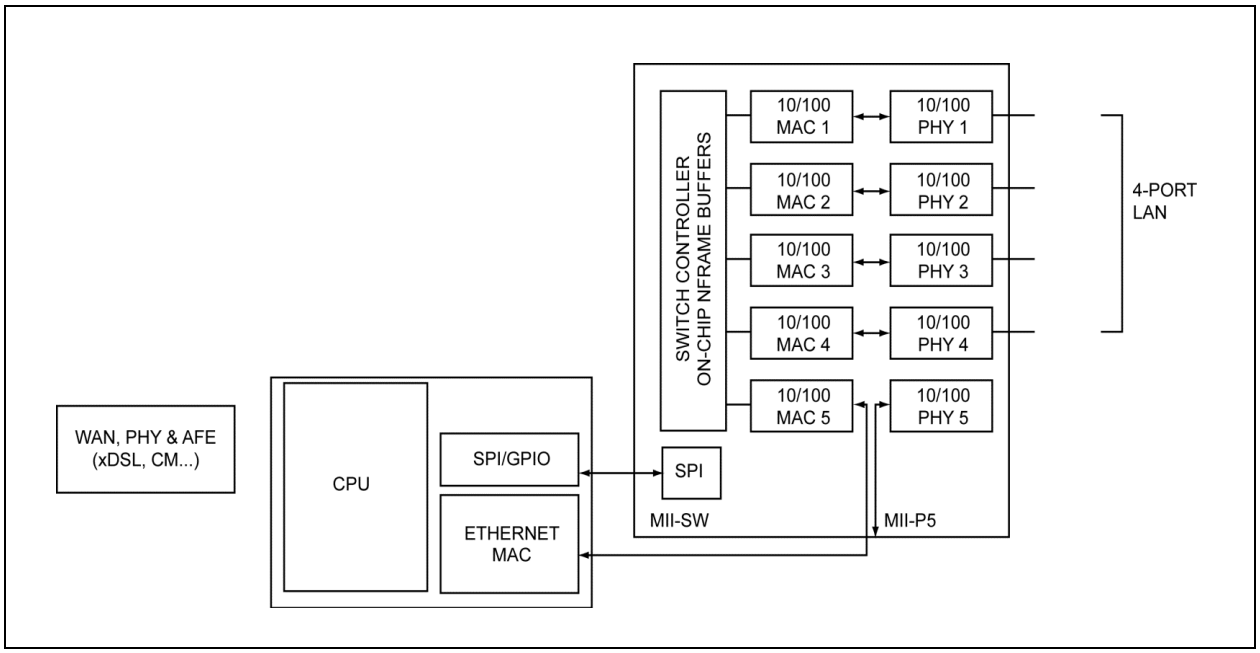
**FIGURE 6-2: DIAGRAM EXAMPLE FOR A ROUTER**



## 6.3 Design for Managed Switch using only Port 5 MAC 5 MII and PHY 5 MII

- The Strap-in pin# [91, 86, 87] should be configured to '101' for MAC 5 MII PHY mode to SoC MAC. In addition, enable PHY 5 MII interface to SoC second MAC.
- Use SPI interface that can access all registers for a managed switch. See Figure 6-3.

**FIGURE 6-3: DIAGRAM EXAMPLE FOR A GATEWAY**



# 7.0 DIGITAL INTERFACE

## 7.1 Port 5 MAC 5/PHY 5 Configuration

- The Port 5 MAC 5/PHY 5 MII configuration is based on the trap-in pins [91, 86, 87] for a real application. See Table 7-1.

**TABLE 7-1: PORT 5 MAC 5/PHY 5 CONFIGURATION**

| Pin Numbers 91, 86, and 87 | Port 5 Switch MAC 5 SW5- MII | Port 5 PHY 5 P5- MII |
|---|---|---|
| 000 | Disable, Otri | Disable, Otri |
| 001 | PHY Mode MII | Disable, Otri |
| 010 | MAC Mode MII | Disable, Otri |
| 100 (Default for standalone 5-port Switch) | Disable (default) | Disable (default) |
| 101 | PHY Mode MII | P5-MII |
| 110 | MAC Mode MII | P5-MII |

## 7.2 Port 5 MAC 5 MII Interface

- The MII provided by the KSZ8895MQX is connected to the device's Port 5 SW-5 MAC 5. It complies with the MII Specification. Table 7-2 describes the signals used by the MII bus.

**TABLE 7-2: PORT 5 MAC 5 MII SIGNALS CONNECTION**

| KSZ8895MQX PHY Mode Connection | | | | KSZ8895MQX MAC Mode Connection | | |
|---|---|---|---|---|---|---|
| External MAC | KSZ8895MQX SW5-MII Signals | Type | Description | External PHY | KSZ8895MQX SW5-MII Signals | Type |
| MTXEN | SMTXEN | Input | Transmit enable | MTXEN | SMRXDV | Output |
| MTXER | SMTXER | Input | Transmit error | MTXER | Not used | Not used |
| MTXD3 | SMTXD [3] | Input | Transmit data bit 3 | MTXD3 | SMRXD [3] | Output |
| MTXD2 | SMTXD [2] | Input | Transmit data bit 2 | MTXD2 | SMRXD [2] | Output |
| MTXD1 | SMTXD [1] | Input | Transmit data bit 1 | MTXD1 | SMRXD [1] | Output |
| MTXD0 | SMTXD [0] | Input | Transmit data bit 0 | MTXD0 | SMRXD [0] | Output |
| MTXC | SMTXC | Output | Transmit clock | MTXC | SMRXC | Input |
| MCOL | SCOL | Output | Collision detection | MCOL | SCOL | Input |
| MCRS | SCRS | Output | Carrier sense | MCRS | SCRS | Input |
| MRXDV | SMRXDV | Output | Receive data valid | MRXDV | SMTXEN | Input |
| MRXER | Not used | Output | Receive error | MRXER | SMTXER | Input |
| MRXD3 | SMRXD [3] | Output | Receive data bit 3 | MRXD3 | SMTXD [3] | Input |
| MRXD2 | SMRXD [2] | Output | Receive data bit 2 | MRXD2 | SMTXD [2] | Input |
| MRXD1 | SMRXD [1] | Output | Receive data bit 1 | MRXD1 | SMTXD [1] | Input |
| MRXD0 | SMRXD [0] | Output | Receive data bit 0 | MRXD0 | SMTXD [0] | Input |
| MRXC | SMRXC | Output | Receive clock | MRXC | SMTXC | Input |

## 7.3 Key Characteristics of MAC 5 MII

MAC 5 MII provides a common interface between two devices with MII interface and has the following key characteristics:

- Sets 10 Mbps and 100 Mbps data rates for KSZ8895MQX MII through register 0x06 bit 4. The default is 100 Mbps.
- Sets Half-Duplex mode and Full-Duplex mode for KSZ8895MQX MII through register 0x06 bit 6. The default is Full-Duplex mode.
- The processor MAC MII should be set to the same speed and the Duplex mode for MII interface consistence in the system configuration.
- Since the MAC 5 MII PHY mode does not produce any error, there is no SMRXER pin from MAC 5 MII. Therefore, the corresponding input pin can be pulled down by a pull-down resistor.
- Contains two distinct groups of signals: one for transmission and one for reception.
- The KSZ8895MQX Port 5 MAC 5 MII PHY mode and MAC 5 MII MAC mode connections are shown in Figure 7-1 and Figure 7-2.

**FIGURE 7-1: CONNECTION BETWEEN KSZ8895MQX PORT 5 MII PHY MODE AND CPU MAC MII**

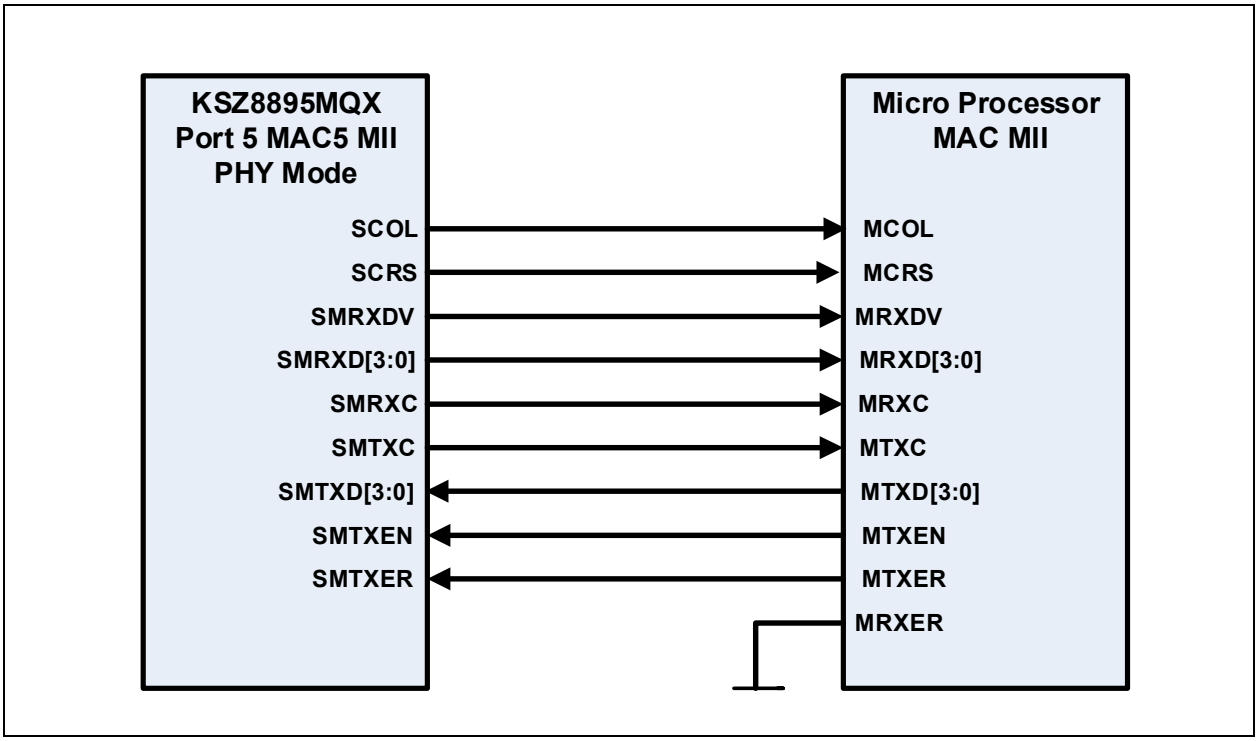
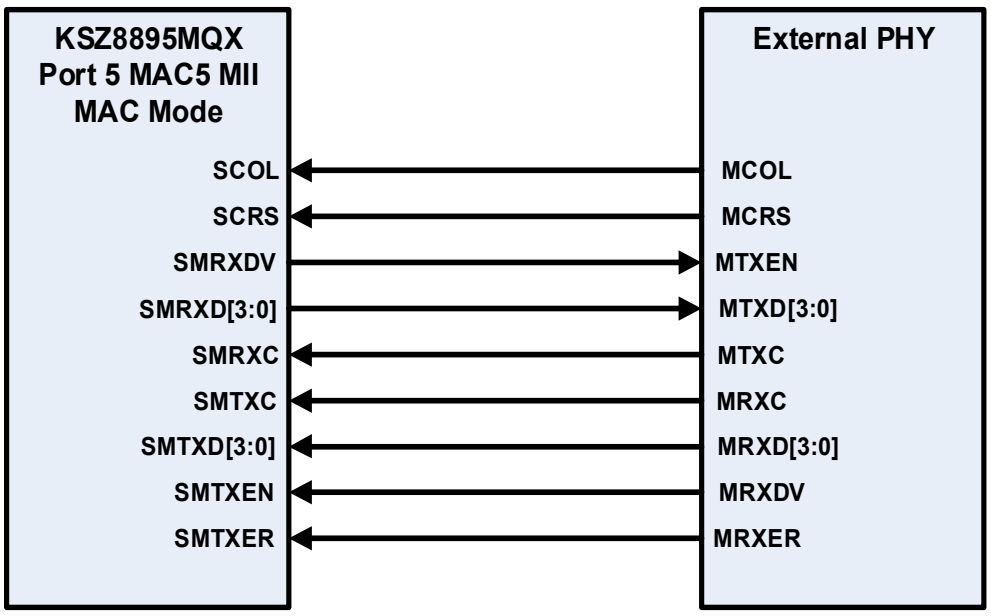


**FIGURE 7-2: CONNECTION BETWEEN KSZ8895MQX PORT 5 MAC 5 MII MAC MODE AND EXTERNAL PHY**



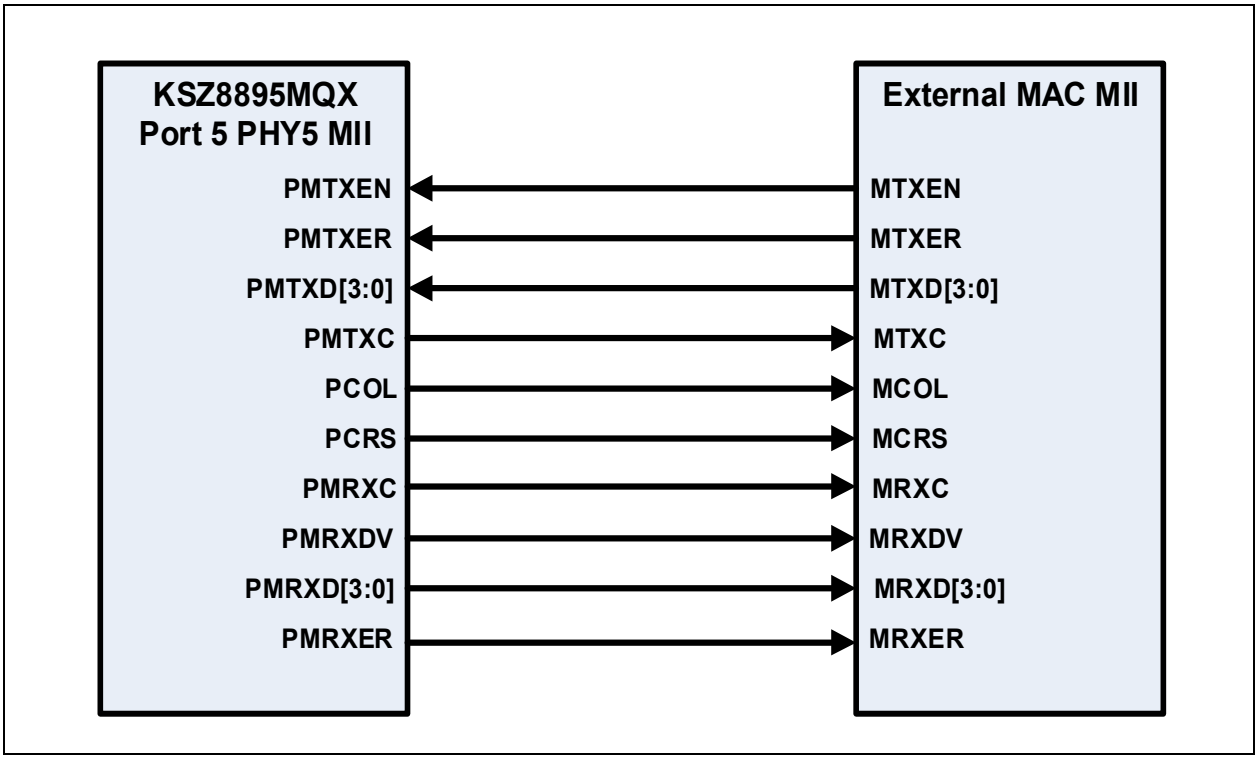

## 7.4 Port 5 PHY 5 MII Interface

- The MII provided by the KSZ8895MQX is connected to the device's Port 5 PHY 5. Table 7-3 describes the signals used by the MII bus illustrated in Figure 7-3.

**TABLE 7-3: PORT 5 PHY 5 MII SIGNALS CONNECTION**

| MAC MII Signal | Description | KSZ8895MQX PHY 5-MII | KSZ8895MQX PHY 5 MII Signal Type |
|---|---|---|---|
| MTXEN | Transmit enable | PMTXEN | Input |
| MTXER | Transmit error | PMTXER | Input |
| MTXD3 | Transmit data bit 3 | PMTXD [3] | Input |
| MTXD2 | Transmit data bit 2 | PMTXD [2] | Input |
| MTXD1 | Transmit data bit 1 | PMTXD [1] | Input |
| MTXD0 | Transmit data bit 0 | PMTXD [0] | Input |
| MTXC | Transmit clock | PMTXC | Output |
| MCOL | Collision detection | PCOL | Output |
| MCRS | Carrier sense | PCRS | Output |
| MRXDV | Receive data valid | PMRXDV | Output |
| MRXER | Receive error | PMRXER | Output |
| MRXD3 | Receive data bit 3 | PMRXD [3] | Output |
| MRXD2 | Receive data bit 2 | PMRXD [2] | Output |
| MRXD1 | Receive data bit 1 | PMRXD [1] | Output |
| MRXD0 | Receive data bit 0 | PMRXD [0] | Output |
| MRXC | Receive clock | PMRXC | Output |

FIGURE 7-3: CONNECTION BETWEEN KSZ8895 PORT 5 PHY 5 MII AND EXTERNAL MAC MII




## 7.5 MII Interface Series Terminations

- Provisions should be made for series terminations for all outputs on the MII interface. Series resistors will enable the designer to closely match the output driver impedance of the KSZ8895MQX and PCB trace impedance to minimize ringing on these signals. Exact resistor values are application dependent and must be analyzed in-system. A suggested starting point for the value of these series resistors would be 22Ω. See Table 7-4.

TABLE 7-4: MII SERIES TERMINATIONS AT THE KSZ8895MQX SIDE

| Signals for Both MAC 5 MII PHY Mode/PHY 5 MII | Series Resistors at KSZ8895MQX MII Drive Pins | Series Resistors at the Other End MII Drive Pins |
|---|---|---|
| SMRXD [3:0]/PMRXD [3:0] | 22Ω | |
| SMRXDV/PMRXDV | 22Ω | |
| SCOL/PCOL | 22Ω | |
| SCRS/PCRS | 22Ω | |
| SMRXC/PMRXC | 22Ω | |
| SMTXC/PMTXC | 22Ω | |
| SMTXEN/PMTXEN | | 22Ω |
| SMTXD [3:0]/PMTXD [3:0] | | 22Ω |

**Note 1:** The series resistors should be placed as close as possible to both KSZ8895MQX MII drive pins and the other end drive pins in the PCB layout.

# 8.0 MANAGEMENT INTERFACE

## 8.1 Configuration for Management Interface Mode

- The strap pin 113 PS1 and pin 114 PS0 are used to configure to the different Management Interface modes. Both pins of PS [1:0] have internal pull-down resistors.
- If the EEPROM is not present, the KSZ8895MQX will start itself with the PS [1:0] = 00 default register values. See Table 8-1.

**TABLE 8-1: REGISTER CONFIGURATION INTERFACE MODE**

| Pin Configuration | Serial Bus Configuration |
|---|---|
| PS [1:0] = 00 (Default) | $I^2C$ Master mode for EEPROM |
| PS [1:0] = 01 | SMI Interface mode |
| PS [1:0] = 10 | SPI Slave mode for CPU Interface |
| PS [1:0] = 11 | Factory Test mode (BIST) |

- KSZ8895MQX has an independent MIIM PHYs register interface MDC/MDIO.
- Select one Interface mode of $I^2C$, SMI, SPI or MDC/MDIO based on real application in the design.

## 8.2 Required External Pull-Ups

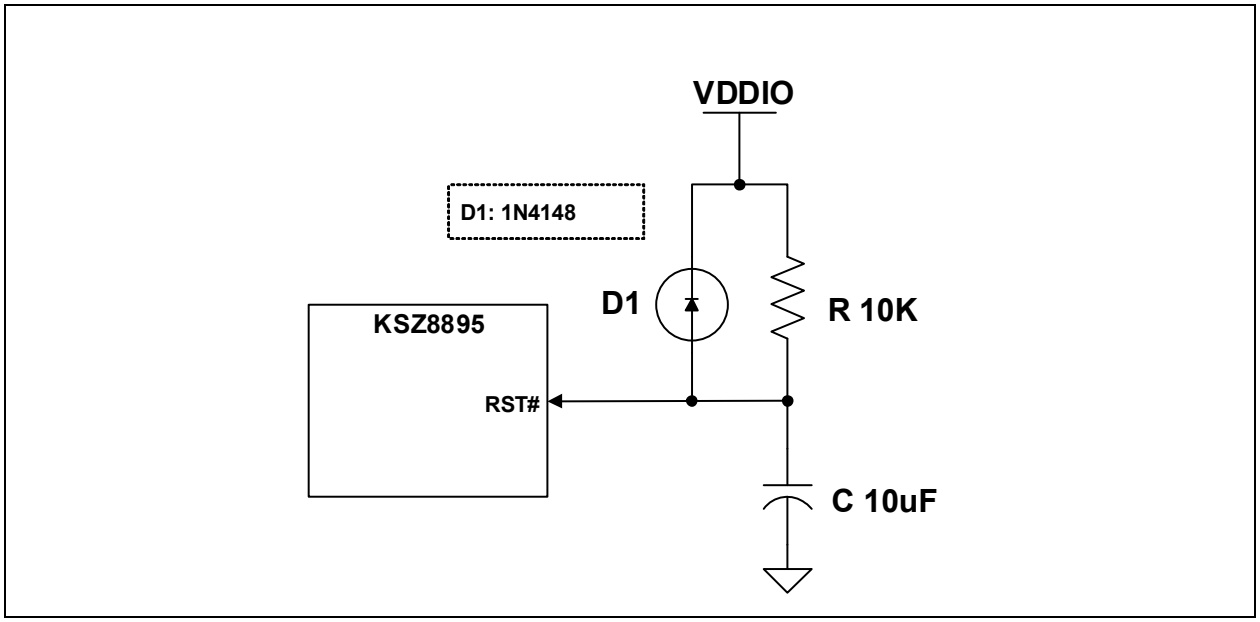
- When using the MDC/MDIO, SMI, $I^2C$, or SPI management interface of the KSZ8895MQX, the pull-up resistors of 4.7 kΩ on the MDIO, SPIQ, and SDA signal pins are required.
- **INTR_N** (pin 48) requires a 4.7 kΩ external pull-up resistor because this output is an open-drain type.

# 9.0 STARTUP

## 9.1 Reset Circuit

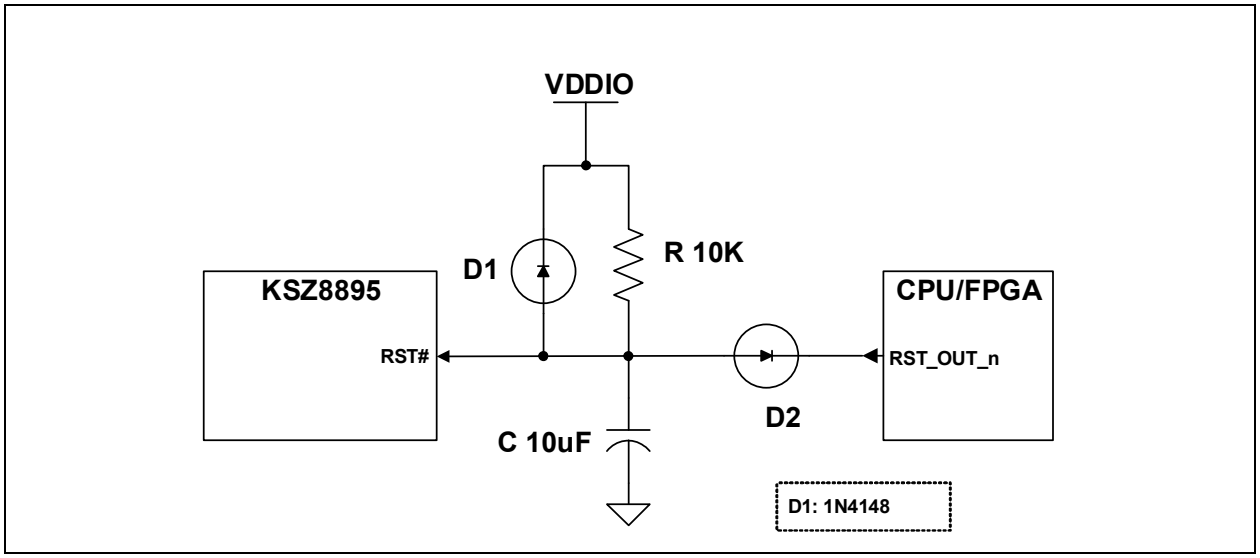
- The **RST_N** (pin 47) is an active-low reset input. This signal resets all logic and registers within the KSZ8895MQX. A hardware reset (**RST_N** assertion) is required following power-up. Please refer to the latest copy of the *KSZ8895MQX Data Sheet* for reset timing requirements. Figure 9-1 shows a recommended reset circuit for powering up the KSZ8895MQX device when reset is triggered by the power supply.

**FIGURE 9-1: R/C RESET CIRCUIT FOR KSZ8895MQX POWER-UP RESET**




- Reset circuit interface with CPU/FPGA reset output pin shows the recommended reset circuit for applications where reset is driven by external CPU or FPGA. The reset-out pin, **RST_OUT_N**, from CPU/FPGA provides warm reset after a power-up reset is done. If the Ethernet device and CPU/FPGA use the same VDDIO voltage, D2 can be removed and both reset pins can be connected directly. See Figure 9-2.

**FIGURE 9-2: RESET CIRCUIT INTERFACE WITH CPU/FPGA RESET OUTPUT**



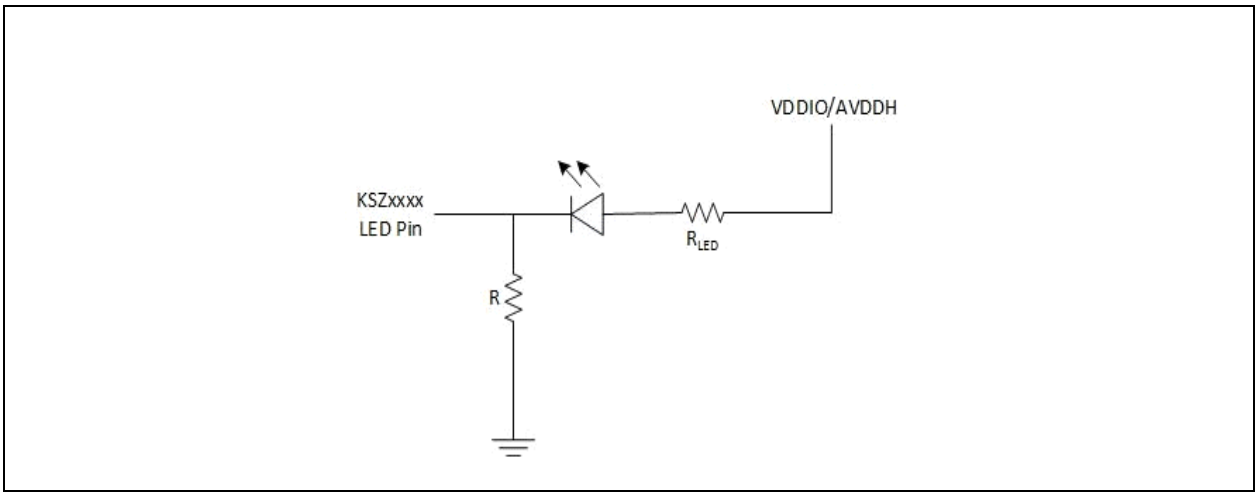
## 10.0 CONFIGURATION PINS (STRAPPING OPTIONS)

There are some strap-in pins to help with the KSZ8895MQX configuration after power-up or hardware reset. The *KSZ8895MQX Data Sheet* has complete details on the operation of strapping pins. The LED strap pin and other requirements are shown in the succeeding sections.

### 10.1 LED Pins as Strap-in Pins

Since LED pins have internal pull-up resistors in KSZ8895MQX, LED pin does not typically need an external pull-up resistor for LED pin to be used for the Strap-high. However, LED Strap-low needs an external pull-down resistor R. See LED pin strap-in circuit in Figure 10-1.

**FIGURE 10-1: LED PIN STRAP-LOW WITH PULL-DOWN RESISTOR R AND LED LIMIT RESISTOR RLED**




Based on the different VDDIO values in the experiment and testing, use the following recommended pull-down resistor R and current limit resistor $R_{LED}$ values:

- When using 3.3V VDDIO power, use 1 kΩ current limit resistor $R_{LED}$ and a 1 kΩ pull-down resistor R to meet $V_{IL}$ specifications.
- When using 2.5V VDDIO power, use 1 kΩ current limit resistor $R_{LED}$ and 0.75 kΩ pull-down resistor R to meet $V_{IL}$ specifications.
- When using 1.8V VDDIO power, use 1 kΩ current limit resistor $R_{LED}$ and 0.5 kΩ pull-down resistor R to meet $V_{IL}$ specifications.

### 10.2 General Strap-In Pins

- Except for LED strap-in pins, the recommended pull-up and pull-down resistors values for strap pins are 4.7 kΩ and 1 kΩ, respectively. Users are highly discouraged from directly executing a pull-up to power and pull-down to ground without pull-up and pull-down resistors.

# 11.0 MISCELLANEOUS

## 11.1 ISET Resistor

- **ISET** (pin 17) on the KSZ8895MQX should connect to the system ground through a 12.4 kΩ resistor with a tolerance of 1%. This **ISET** pin is used to set-up critical bias currents for the embedded 10/100 Ethernet physical devices.

## 11.2 Other Considerations

- Incorporate an SMD ferrite bead footprint to connect the chassis ground to the system ground. This allows some flexibility at EMI testing for different grounding options if leaving the footprint open keeps the two grounds separated. For best performance, short the grounds together with a cap or a ferrite bead. Users are required to place the capacitor/ferrite bead far from KSZ8895MQX device in PCB layout placement for better ESD.
- Make sure that enough bulk capacitors (4.7 µF to 22 µF) are incorporated in each power rail.

# 12.0 HARDWARE CHECKLIST SUMMARY

## TABLE 12-1: HARDWARE DESIGN CHECKLIST

| Section | Check | Explanation | √ | Notes |
|---|---|---|---|---|
| Section 2.0, "General Considerations" | Section 2.1, "Required References" | All necessary documents are on hand. | | |
| | Section 2.2, "Pin Check" | The pins match the data sheet. | | |
| | Section 2.3, "Ground" | Verify if the digital ground and the analog ground are tied together. Check if there is a chassis ground for the line-side ground. | | |
| Section 3.0, "Power" | Section 3.0, "Power" | • Ensure that **VDDA_3.3** and **VDDIO_3.3** are within 3.135V to 3.465V. **VDDIO** is for the strap pull-up and interface. Capacitors in 10 µF to 47 µF values are for each power rail, while 0.1 µF capacitors are attached to each power pin and power rail.<br>• If using 1.2V LDO controller + MOSFET solution, check pin 126 to see if there is a resistor divider with 2:1 ratio. There is a 47 µF capacitor on 1.2V power rail. If using external 1.2V LDO, verify if there is a pull-down resistor on pin 126. | | |
| Section 4.0, "Ethernet Signals" | Section 4.1, "KSZ8895MQX Copper Ports Connection" | Verify if there is no 49.9Ω termination resistors on **TX** and **RX** pairs. | | |
| | Section 4.2, "Other Ethernet Copper Ports" | Verify if there is no 49.9Ω termination resistors on **TX** and **RX** pairs. | | |
| | Section 4.3, "Magnetics Connection at the Chip Side" | Verify if the center taps of the magnetics on the KSZ8895MQX chip side are NOT connected to the VDDAT 3.3V analog power as KSZ8895MQX is an internal biasing device. The center taps of the magnetics on the chip side should also have two 0.1 µF capacitors to ground individually. | | |
| | Section 4.4, "Magnetics Connection at Line Side of RJ45 Connector" | Verify if the line side of the magnetics has two 75Ω resistors through a 1000 pF, 2 KV capacitor connected to chassis ground that is also linked to the metal case of the RJ45 for the line side. | | |
| | Section 4.5, "Alternative Termination Selection for RJ45 Connector" | Verify if pins 4/5 and 7/8 of the RJ45 connect to CAT-5 cable and are terminated to chassis ground through a 1000 pF, 2 KV capacitor. | | |
| | Section 4.6, "Using RJ45 with Integrated LED" | Use RJ45 with integrated LED if the product working environment is not very noisy. Otherwise, use an independent LED solution. | | |
| Section 5.0, "Clock Circuit" | Section 5.1, "Crystal and External Oscillator/Clock Connections" | Verify the usage of 25 MHz max. ±50 ppm crystal. The drive level should be about 100 uW or above (preferably higher). If using 25 MHz oscillator with maximum ±50 ppm, it is better to use 3.3V power for the oscillator power and use 3.3V **VDDAT** for the oscillator. | | |
| Section 6.0, "System Application" | Section 6.1, "Design for a Standalone Five-Port Switch" | Verify if your design is for a standalone 5-port switch. Check the strap pins PS[1:0] ='00 default. Pins 91, 86, and 87 are default, too. | | |
| | Section 6.2, "Design for Managed Switch using only Port 5 MAC 5 MII" | Verify if your design is using Port 5 MAC 5 MII interface only. If yes, check the pin 91,86, and 87 strap pin configurations based on MAC mode or PHY mode that corresponds to the other end. | | |
| | Section 6.3, "Design for Managed Switch using only Port 5 MAC 5 MII and PHY 5 MII" | Verify if your design is using both Port 5 MAC 5 and PHY 5 MII interfaces. If yes, check the pin 91,86, and 87 strap pin configurations based on MAC 5 MII MAC mode or PHY mode that corresponds to the other end. | | |

**TABLE 12-1: HARDWARE DESIGN CHECKLIST (CONTINUED)**

| Section | Check | Explanation | √ | Notes |
|---|---|---|---|---|
| Section 7.0, "Digital Interface" | Section 7.1, "Port 5 MAC 5/PHY 5 Configuration" | Use your system design for setting strap pin [91,86,87] configurations. | | |
| | Section 7.2, "Port 5 MAC 5 MII Interface" and Section 7.3, "Key Characteristics of MAC 5 MII" | Refer to Table 7-2, Figure 7-1 and Figure 7-2 to verify Port 5 MAC 5 MII interface connections for MAC mode or PHY mode. | | |
| | Section 7.4, "Port 5 PHY 5 MII Interface" | Refer to Table 7-3 and Figure 7-3 to check the PHY 5 MII interface connection and see if Port 5 PHY 5 MII is used for an external MAC MII. | | |
| | Section 7.5, "MII Interface Series Terminations" | If the trace routing is more than 1 inch in the PCB layout, verify if 22Ω series termination resistors were added to all driver pins on MII interface and are placed to close all driver pins. | | |
| Section 8.0, "Management Interface" | Section 8.1, "Configuration for Management Interface Mode" | Check the strap pins PS [1:0] to verify if they match with the Series Management Interface mode in the design. | | |
| | Section 8.2, "Required External Pull-Ups" | Check if there is a pull-up resistor for the data line of the management interface and the interrupt pin if they are used.<br>Use 4.7 kΩ as a pull-up resistor. | | |
| Section 9.0, "Startup" | Section 9.1, "Reset Circuit" | Verify if R/C reset circuit is used for a power-up reset. A 10 kΩ resistor and a 10 uF capacitor are recommended.<br>For the cost-down, the D1 Figure 9-1 and Figure 9-2 can be ignored because RST_N pin has an internal protection diode.<br>For a warm reset from CPU/FPGA to KSZ8895MQX, D2 can be removed from Figure 9-1 and Figure 9-2 if KSZ8895MQX and CPU/FPGA are using same VDDIO voltage. | | |
| Section 10.0, "Configuration Pins (Strapping Options)" | Section 10.1, "LED Pins as Strap-in Pins" | If using an LED pin to do a strap-in for the different **VDDIO** design, please follow the specified recommended resistor value for the pull-down resistors and the current limit resistor to meet VIL specifications. If LED strap pin for pull-up is necessary, there is no need for an external pull-up resistor because KSZ8895MQX LED pins have internal pull-up as default. | | |
| | Section 10.2, "General Strap-In Pins" | It is generally recommended to use 4.7 kΩ pull-up and 1 kΩ pull-down resistor. Avoid pulling up/down to power/ground directly. If not specified, NC pin should have no connection. | | |
| Section 11.0, "Miscellaneous" | Section 11.1, "ISET Resistor" | Check ISET resistor (12.4 kΩ, 1%) without any capacitor in parallel. | | |
| | Section 11.2, "Other Considerations" | Incorporate an SMD footprint (SMD_0805-1210) to connect the chassis ground to the system ground. The SMD footprint should be placed far from the devices in PCB layout placement. | | |
| | | Incorporate sufficient power plane bulk capacitors (4.7 µF to 22 µF) for each power rail. It is advisable to use 47 µF bulk capacitor on 1.2V power rail when using the internal 1.2V LDO controller + MOSFET solution. | | |

## APPENDIX A: REVISION HISTORY

**TABLE A-1: REVISION HISTORY**

| Revision Level & Date | Section/Figure/Entry | Correction |
|---|---|---|
| DS00003196B (10-14-19) | Table 8-1 | Changed the table title from “PORT 5 PHY5 MII SIGNALS CONNECTION” to “REGISTER CONFIGURATION INTERFACE MODES.” |
| DS00003196A (08-20-19) | Initial release | |

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