

RELIABILITY REPORT FOR MAX2042AETP+ PLASTIC ENCAPSULATED DEVICES

November 15, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

| Approved by | | | |
|---------------------------------|--|--|--|
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| Quality Assurance | | | |
| Manager, Reliability Operations | | | |



Conclusion

The MAX2042AETP+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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- I. Device Description
 - A. General

The MAX2042A single, high-linearity up/down-conversion mixer provides up to +33dBm input IP3, 7.5dB NF and 7dB conversion loss for 1600MHz to 3900MHz GSM/EDGE, CDMA, TD-SCDMA, WCDMA, LTE, TD-LTE, WiMAX and MMDS wireless infrastructure applications. With an ultra-wide LO frequency range of 1300MHz to 4000MHz, the MAX2042A can be used in either low- or high-side LO injection architectures for virtually all 1.7GHz to 3.5GHz applications. (For a 2.5GHz variant tuned specifically for low-side LO injection, refer to the MAX2042).

In addition to offering excellent linearity and noise performance, the MAX2042A also yields a high level of component integration. This device includes a double-balanced passive mixer core, an LO buffer, and on-chip baluns which allow for single-ended RF and LO inputs. The MAX2042A requires a nominal LO drive of 0dBm, and supply current is typically 138mA at $V_{cc} = +5.0V$ or 120mA at $V_{cc} = +3.3V$.

The MAX2042A is pin compatible with the MAX2042 2000MHz to 3000MHz mixer. The device is also pin similar with the MAX2029/MAX2031 815MHz to 1000MHz mixers and the MAX2039 / MAX2041 1700MHz to 2200MHz mixers, making this entire family of mixers ideal for applications where a common PCB layout is used for multiple frequency bands.

The MAX2042A is available in a compact 20-pin thin QFN package (5mm x 5mm) with an exposed paddle. Electrical performance is guaranteed over the extended temperature range, from $Tc = -40^{\circ}C$ to +85°C.



II. Manufacturing Information

| A. Description/Function: | SiGe, High-Linearity, 1600MHz to 3900MHz Upconversion/Downconversion Mixer with LO Buffer |
|----------------------------------|--|
| B. Process: | G4 |
| C. Number of Device Transistors: | |
| D. Fabrication Location: | USA |
| E. Assembly Location: | China, Taiwan and Thailand |
| F. Date of Initial Production: | June 24, 2011 |
| III. Packaging Information | |

| ŀ | A. Package Type: | 20-pin TQFN 5x5 |
|-----------------------------|---|---|
| E | B. Lead Frame: | Copper |
| (| C. Lead Finish: | 100% matte Tin |
| [| D. Die Attach: | Conductive |
| E | E. Bondwire: | Au (1 mil dia.) |
| F | F. Mold Material: | Epoxy with silica filler |
| (| G. Assembly Diagram: | #05-9000-2904 |
| ŀ | H. Flammability Rating: | Class UL94-V0 |
| | Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| | J. Single Layer Theta Ja: | 48°C/W |
| ł | K. Single Layer Theta Jc: | 2°C/W |
| L | L. Multi Layer Theta Ja: | 32°C/W |
| Ν | M. Multi Layer Theta Jc: | 3°C/W |
| IV. Die Info | ormation | |
| ŀ | A. Dimensions: | 91 X 80 mils |
| E | B. Passivation: | Si ₃ N ₄ |
| (| C. Interconnect: | Au |
| [| D. Backside Metallization: | None |
| E | E. Minimum Metal Width: | Metal1-3 = 1.2 / Metal 4 = 5.6 microns (as drawn) |
| L IV. Die Info E C | L. Multi Layer Theta Ja: M. Multi Layer Theta Jc: ormation A. Dimensions: B. Passivation: C. Interconnect: D. Backside Metallization: | 32°C/W 3°C/W 91 X 80 mils Si ₃ N ₄ Au None |

Metal1-3 = 1.6 / Metal 4 = 4.2 microns (as drawn)

G. Bondpad Dimensions: H. Isolation Dielectric: SiO₂

I. Die Separation Method: Wafer Saw

F. Minimum Metal Spacing:



V. Quality Assurance Information

| A. Quality Assurance Contacts: | Richard Aburano (Manager, Reliability Engineering) | | |
|-----------------------------------|---|--|--|
| | Don Lipps (Manager, Reliability Engineering) | | |
| | Bryan Preeshl (Vice President of QA) | | |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects. | | |
| C. Observed Outgoing Defect Rate: | < 50 ppm | | |
| D. Sampling Plan: | Mil-Std-105D | | |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{192 \text{ x} 4340 \text{ x} 96 \text{ x} 2}_{(\text{where } 4340 \text{ = Temperature Acceleration factor assuming an activation energy of 0.8eV)}$ $\lambda = 11.5 \text{ x} 10^{-9}$ $\lambda = 11.5 \text{ F.I.T. (60\% confidence level @ 25°C)}$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the G4 Process results in a FIT Rate of 0.02 @ 25C and 0.37 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The CR43-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.



Table 1 Reliability Evaluation Test Results

MAX2042AETP+

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|------------------|---------------------------|---------------------------|-------------|-----------------------|----------------------|
| Static Life Test | (Note 1) | | | | |
| | Ta = 135°C | DC Parameters | 48 | 0 | NHVWBQ002C, D/C 0906 |
| | Biased Time = 192 hrs. | & functionality | 48 | 0 | NHVYBQ002B, D/C 0809 |

Note 1: Life Test Data may represent plastic DIP qualification lots.