RELIABILITY REPORT

FOR

MAX5214GUA+T

PLASTIC ENCAPSULATED DEVICES

April 8, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Richard Aburano
Quality Assurance
Manager, Reliability Engineering

Maxim Integrated. All rights reserved.

maxim integrated™

Conclusion

The MAX5214GUA+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. ....Device Description

II. ....Manufacturing Information

III. ....Packaging Information

.....Attachments

IV. ....Die Information

V. ....Quality Assurance Information

VI. ....Reliability Evaluation

I. Device Description

A. General

The MAX5214/MAX5216 are pin-compatible, 14-bit and 16-bit digital-to-analog converters (DACs). The MAX5214/MAX5216 are single-channel, low-power, buffered voltage-output DACs. The devices use a precision external reference applied through the high resistance input for rail-to-rail operation and low system power consumption. The MAX5214/MAX5216 accept a wide 2.7V to 5.25V supply voltage range. Power consumption is extremely low to accommodate most low-power and low-voltage applications. These devices feature a 3-wire SPI-/QSPI(tm)- / MICROWIRE(tm)- / DSP-compatible serial interface to save board space and to reduce the complexity in isolated applications. The MAX5214/MAX5216 minimize the digital noise feedthrough from input to output with SCLK and DIN input buffers powered down after completion of each serial input frame. On power-up, the MAX5214/MAX5216 reset the DAC output to zero, providing additional safety for applications that drive valves or other transducers that need to be off on power-up. The DAC output is buffered resulting in a low supply current of 80µA (max) and a low offset error of ±0.25mV. A zero level applied to the active-low CLR pin asynchronously clears the contents of the input and DAC registers and sets the DAC output to zero independent of the serial interface. The MAX5214/MAX5216 are available in an ultra-small (3mm x 3mm), 8-pin µMAX® package and are specified over the -40°C to +105°C extended industrial temperature range.

Maxim Integrated. All rights reserved.

maxim integrated™

II. Manufacturing Information

A. Description/Function:	14-/16-Bit, Low-Power, High-Performance, Buffered Single DACs
B. Process:	S45
C. Number of Device Transistors:	33014
D. Fabrication Location:	USA
E. Assembly Location:	Philippines and Thailand
F. Date of Initial Production:	November 24, 2010

III. Packaging Information

A. Package Type:	8-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3979
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	221°C/W
K. Single Layer Theta Jc:	42°C/W
L. Multi Layer Theta Ja:	206.3°C/W
M. Multi Layer Theta Jc:	42°C/W

IV. Die Information

A. Dimensions:	66 X 88 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.4 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

Maxim Integrated. All rights reserved.

V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 0.13 @ 25C and 2.3 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TC1ZCQ001L, D/C 1042)

The DB45 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Maxim Integrated. All rights reserved.

Table 1
Reliability Evaluation Test Results

MAX5214GUA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	TC1ZCQ001L, D/C 1042

Note 1: Life Test Data may represent plastic DIP qualification lots.

Maxim Integrated. All rights reserved.