

RELIABILITY REPORT
FOR
MAX17574ATG+T
PLASTIC ENCAPSULATED DEVICES

December 28, 2016

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX17574ATG+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX17574, high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input. The converter can deliver up to 3A current. Output voltage is programmable from 0.9V to 90%VIN. The feedback voltage regulation accuracy over -40°C to +125°C is $\pm 0.9\%$. The MAX17574 features a peak-current-mode control architecture. The device can be operated in the pulse-width modulation (PWM), pulse-frequency modulation (PFM), or discontinuous-conduction mode (DCM) control schemes. A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input voltage level. An open-drain RESET pin provides a delayed power-good signal to the system upon achieving successful regulation of the output voltage. The MAX17574 is available in a 24-pin (4mm x 5mm) TQFN package. Simulation models are available.

II. Manufacturing Information

A. Description/Function:	4.5V to 60V, 3A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Internal Compensation
B. Process:	S18
C. Number of Device Transistors:	24862
D. Fabrication Location:	Japan
E. Assembly Location:	Thailand
F. Date of Initial Production:	September 27, 2016

III. Packaging Information

A. Package Type:	24-pin TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Ab8200t
E. Bondwire:	CuPD (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-100392
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	24°C/W
M. Multi Layer Theta Jc:	1.8°C/W

IV. Die Information

A. Dimensions:	118.8976X100.7874 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Isolation Dielectric:	SiO ₂
G. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 13.7 \times 10^{-9}$$

$$\lambda = 13.7 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PI51-2 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX17574ATG+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.