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FAIRCHILD SEMICONDUCTOR®

March 2012

FSSD07
1-Bit / 4-Bit SD/SDIO and MMC Dual-Host Multiplexer

Features

- On Resistance: 5Ω Typical, V_{DDC}=2.7V
- f_{toggle}: >75MHz
- Low On Capacitance: 6pF Typical
- Low Power Consumption: 2µA Maximum
- Supports Secure Digital (SD), Secure Digital I/O (SDIO), and Multimedia Card (MMC) Specifications
- Supports 1-Bit / 4-Bit Host Controllers ($V_{DDH1/H2}$=1.65V to 3.6V) Communicating with High-Voltage (2.7-3.6V) and Dual-Voltage Cards (1.65-1.95V, 2.7-3.6V)
  - V_{DDC}=1.65 to 3.6V, $V_{DDH1/H2}$=1.65 to 3.6V
- 24-Lead MLP and UMLP Packages

Applications

- Cell Phone, PDA, Digital Camera, Portable GPS, and Notebook Computer
- LCD Monitor, TV, and Set-Top Box

Related Resources

- *FSSD07 Evaluation Board*
- *Evaluation Board Users Guide*
- *For samples, questions, or board requests; please contact analogswitch@fairchildsemi.com*

Description

The FSSD07 is a 2:1 multiplexer that allows dual Secure Digital (SD), Secure Digital I/O (SDIO), and Multimedia Card (MMC) host controllers to share a common peripheral. The host controllers can be equal to, greater than, or less than peripheral card supply with minimal power consumption. This configuration enables dual host CMD, CLK, and D[3:0] signals to be multiplexed to a common peripheral.

The architecture includes the necessary bi-directional data and command transfer capability for single high-voltage cards or dual-voltage supply cards. The clock path is a uni-directional buffer.

Typical applications involve switching in portables and consumer applications: cell phones, digital cameras, home theater monitors, set-top boxes, and notebooks.

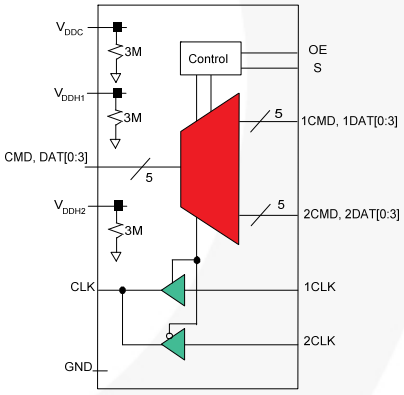

Figure 1. Analog Symbol Diagram

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package Description	Packing Method
FSSD07BQX	FSSD07	-40°C to +85°C	24-Lead Molded Leadless Package (MLP), JEDEC MO-220, 3.5 x 4.5mm	Tape & Reel
FSSD07UMX	JK	-40°C to +85°C	24-Lead Ultra-thin Molded Leadless Package (UMLP), 0.4mm pitch	Tape & Reel

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Pin Configuration

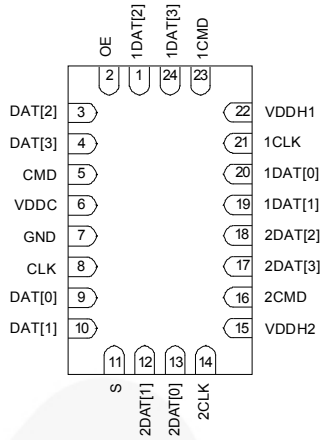

Figure 2. MLP Pin Assignments

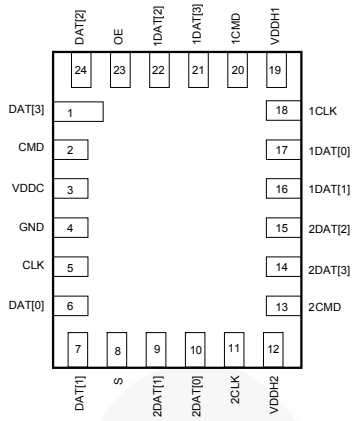

Figure 3. UMLP Pin Assignments

Pin Definitions

Pin# MLP	Pin# UMLP	Name	Description
1	22	1DAT[2]	SDIO Common Port
2	23	OE	Output Enable (Active HIGH)
3	24	DAT[2]	SDIO Common Port
4	1	DAT[3]	
5	2	CMD	
6	3	VDDC	Power Supply (SDIO Peripheral Card Port)
7	4	GND	Ground
8	5	CLK	Clock Path Port
9	6	DAT[0]	SDIO Common Port
10	7	DAT[1]	
11	8	S	Select Pin
12	9	2DAT[1]	Host Common Port
13	10	2DAT[0]	
14	11	2CLK	Clock Path Port
15	12	VDDH2	Power Supply (Host Port)
16	13	2CMD	Host Common Port
17	14	2DAT[3]	
18	15	2DAT[2]	
19	16	1DAT[1]	
20	17	1DAT[0]	
21	18	1CLK	Clock Path Port
22	19	VDDH1	Power Supply (SDIO Host Port)
23	20	1CMD	Host Common Port
24	21	1DAT[3]	

Truth Table

OE	S	Function
HIGH	LOW	1CMD, 1CLK, 1DAT[3:0] connected to CMD, CLK, DAT[3:0]
HIGH	HIGH	2CMD, 2CLK,2DAT[3:0] connected to CMD, CLK, DAT[3:0]
LOW	X	CMD, DAT[3:0] ports high impedance; CLK is function of selected nCLK

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Typical Application

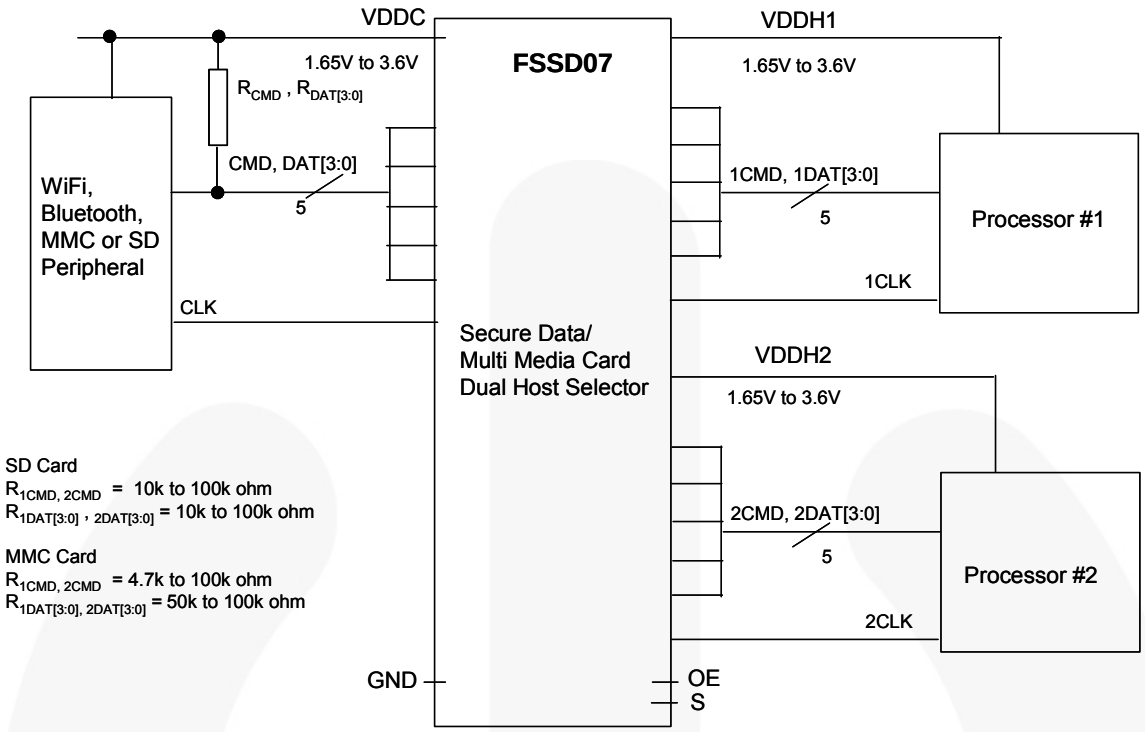

Figure 4. Typical Application Diagram

Functional Description

The FSSD07 enables the multiplexing of dual ASIC / baseband processor hosts to a common peripheral card or module, providing bi-directional support of the dual-voltage SD/SDIO or MMC cards available in the marketplace. Each host SDIO port has its own supply rail, such that hosts with different supplies can be interfaced to a common peripheral module or card. The peripheral card supply must be equal to or greater than the host(s) to minimize power consumption. The independent V_{DDC}, V_{DDH1}, and V_{DDH2} are defined by the supplies connected from the application Power Management ICs (PMICs) to the FSSD07. The clock path is a uni-directional buffered path rather than a bi-directional switch port. The supplies (V_{DDC}, V_{DDH1}, and V_{DDH2}) have an internal termination resistor (typically 3MΩ) to ensure the supply rails internally do not float if the application turns off one or all of these sources.

CMD, DAT Bus Pull-ups

The CMD and DAT[3:0] ports do not have, internally, the system pull-up resistors as defined in the MMC or SD card system bus specifications. The system bus pull-up must be added external to the FSSD07. The value, within the specific specification limits, is a function of the individual application and type of card or peripheral connected. For SD card applications, the R_{CMD} and R_{DAT} pull-ups should be between 10kΩ and 100kΩ. For MMC applications, the R_{CMD} pull-ups should be between 4.7kΩ and 100kΩ, and the R_{DAT} pull-ups between 50kΩ and 100kΩ. The card-side CMD and DAT[3:0] outputs have a circuit that facilitates incident wave switching, so the external pull-up resistors ensure retention of the output high level.

The OE pin can be used to place the CMD and DAT[3:0] into high-impedance mode during power-up sequencing or when the system enters IDLE state (*see IDLE State CMD/DAT Bus "Parking"*).

CLK Bus

The 1CLK and 2CLK inputs are bi-state buffer architectures, rather than a switch I/O, to ensure 52MHz incident wave switching. Since most host controllers also have a clock enable register bit to enable or disable the system clock when in IDLE mode, the CLK output is not disabled by the OE pin. Instead, the CLK output is a function of whichever host controller clock is selected by the S pin.

Consequently, there is always a clock path connected between the selected host and the card. The state of the CLK pin is a function of the selected host controller nCLK output pin, which facilitates retaining clock duty cycle in the system or performing read / wait operations.

IDLE State & Power-Up CMD/DAT Bus "Parking"

The SD and MMC card specifications were written for a direct point-to-point communication between host controller and card. The introduction of the FSSD07 in that path, as an expander, requires that the functional operation and system latency not be impacted by the switch characteristics. Since there are various card formats, protocols, and configurable controllers, an OE pin is available to facilitate a fast IDLE transition for the CMD/DAT[3:0] outputs. Some controllers, rather than placing CMD/DAT into high-impedance mode, pull the outputs HIGH for a clock cycle prior to going into high-impedance mode (referred to as "parking" the output). Some legacy controllers pull their outputs HIGH versus high impedance.

If the OE pin is pulled HIGH and the controller places its command and data outputs into high-impedance (driving nCMD/nDAT[3:0]), the FSSD07 CMD/DAT[3:0] output rise time is a function of the RC time constant through the switch path. Pulling OE LOW puts the switches into high impedance, disabling communication from the host to card, and the CMD/DAT[3:0] outputs are pulled HIGH by the system pull-up resistors chosen for the application. This mechanism facilitates power-up sequencing by holding OE LOW until supplies are stable and communication between the host(s) and card is enabled.

Power Optimization

Since the FSSD07 has multiple supplies (V_{DDC}, V_{DDH1}, and V_{DDH2}), the control signals have been referenced to the card peripheral side (V_{DDC}). To minimize power consumption, current paths between supplies are isolated when one or more supplies are not present. This includes the configuration of the removal of V_{DDC} with host controller supplies remaining present.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DDC}	Card Supply Voltage		-0.5	4.6	V
V_{DDH1},V_{DDH2}	Host Controller Supply Voltage		-0.5	4.6	V
V_{SW}	Switch I/O Voltage(1)	1DAT[3:0], 2DAT[3:0], 1CMD, 2CMD Pins	-0.5	V_{DDx}(2)+ 0.3V (4.6V maximum)	V
		DAT[3:0], CMD Pins	-0.5	V_{DDx}(2)+ 0.3V (4.6V maximum)	V
V_{CNTRL}	Control Input Voltage(1)	S, OE	-0.5	4.6	V
V_{CLKI}	CLK Input Voltage (1)	1CLK, 2CLK	-0.5	4.6	V
V_{CLKO}	CLK Output Voltage(1)	CLK	-0.5	V_{DDx}(2)+ 0.3V (4.6V maximum)	V
I_{INDC}	Input Clamp Diode Current			-50	mA
I_{SW}	Switch I/O Current	SDIO Continuous		50	mA
I_{SWPEAK}	Peak Switch Current	SDIO Pulsed at 1ms Duration, <10% Duty Cycle		100	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature	Soldering, 10 Seconds		+260	°C
ESD	Human Body Model, JEDEC: JESD22-A114	I/O to GND		8	kV
		Supply to GND		10	
		All Other Pins		5	
	Charged Device Model, JEDEC-JESD-C101			2	

Notes:
1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. V_{DDx} references the specific SDIO port V_{DD} rail (i.e. V_{DDH1}, V_{DDH2}, V_{DDC}).

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{DDC}	Supply Voltage - Card Side		1.65	3.60	V
$V_{DDH1,}$ V_{DDH2}	Supply Voltage - Dual Host Controller		1.65	3.60	V
V_{CNTRL}	Control Input Voltage - V_S, V_{OE}		0	V_{DDC}	V
V_{CLKI}	Clock Input Voltage - V_{CLKI}		0	$V_{DDH1/H2}$	V
V_{SW}	Switch I/O Voltage	CMD, DAT[3:0]	0	V_{DDC}	V
		1CMD, 1DAT[3:0]	0	V_{DDH1}	V
		2CMD, 2DAT[3:0]	0	V_{DDH2}	V
T_A	Operating Temperature		-40	+85	°C
θ_{JA}	Thermal Resistance, Free Air	MLP Package		+50	°C/W

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DC Electrical Characteristics at 1.8V V_{DDC}

All typical values are for V_{DDC}=1.8V at 25°C unless otherwise specified.

Symbol	Parameter	V_{DDC} (V)	V_{DDH1} / V_{DDH2} (V)	Conditions	T_A=-40 to +85°C			Unit
					Min.	Typ.	Max.	
Common Pins								
V_{IK}	Clamp Diode Voltage	1.80	1.80	I_{IK}=-18mA			-1.2	V
V_{IH}	Control Input Voltage High	1.80	1.80		1.3			V
V_{IL}	Control Input Voltage Low	1.80	1.80				0.5	V
I_{IN}	S, OE Input High Current	1.95	1.95	V_{CNTRL}=0V to V_{DDC}	-1		1	µA
I_{OZ}	Off Leakage, Current of all ports	1.95	1.95	V_{SW}=0V to V_{DDC}	-1.0	0.5	1.0	µA
V_{OHC}	CLK Output Voltage High(3)	1.95	1.95	I_{OH}=-2mA	1.6			V
V_{OLC}	CLK Output Voltage Low(3)	1.65	1.65	I_{OL}=-2mA			90	mV
R_{ON}	Switch On Resistance(4)	1.65	1.65	$V_{CMD, DAT[3:0]}$=0V, I_{ON}=-2mA Figure 5			10	Ω
ΔR_{ON}	Delta On Resistance(3, 5)	1.65	1.65	$V_{CMD, DAT[3:0]}$=0V, I_{ON}=- 2mA		0.85		Ω
Power Supply								
$I_{CC(VDDC)}$	Quiescent Supply Current (Card)	1.95	0	V_{SW}=0 or V_{DDC}, I_{OUT}=0			2	µA
$I_{CC(VDDH1/H2)}$	Quiescent Supply Current (Hosts)	1.95	1.95	V_{SW}=0 or V_{DDx}, I_{OUT}=0, V_{CLKI}=V_{DDHX}, V_{CLKO}=Open, OE=V_{DDC}			2	µA
ΔI_{HOST}	Delta $I_{CC(VDDH1, VDDH2)}$ for One Host Powered Off	1.95	1.95 / 0 0 / 1.95	V_{SW}=0 or V_{DDx}, I_{OUT}=0, V_{CLKI}=V_{DDHX}, V_{CLKO}=Open, OE=V_{DDC}			2	µA

Notes:

3. Guaranteed by characterization, not production tested.
4. On resistance is determined by the voltage drop between the switch I/O pins at the indicated current through the switch.
5. $\Delta R_{ON}=R_{ON\,max} - R_{ON\,min}$ measured at identical V_{CC}, temperature, and voltage.

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DC Electrical Characteristics at 2.7V V_{DDC}

All typical values are for V_{DDC}=2.7V at 25°C unless otherwise specified.

Symbol	Parameter	V_{DDC} (V)	V_{DDH1} / V_{DDH2} (V)	Conditions	T_A=-40 to +85°C			Unit
					Min.	Typ.	Max.	
Common Pins								
V_{IK}	Clamp Diode Voltage	2.7	2.7	I_{IK}=-18mA			-1.2	V
V_{IH}	Control Input Voltage High	2.7	2.7		1.8			
V_{IL}	Control Input Voltage Low	2.7	2.7				0.8	
I_{IN}	S, OE Input High Current	3.6	3.6	V_{CNTRL}=0V to V_{DDC}	-1		1	µA
I_{OZ}	Off Leakage Current of all Ports	3.6	3.6	V_{SW}=0V to V_{DDC}	-1.0	0.5	1.0	µA
V_{OHC}	CLK Output Voltage High(6)	2.7	2.7	I_{OH}=-2mA	2.4			V
V_{OLC}	CLK Output Voltage Low(6)	3.6	3.6	I_{OL}=-2mA			90	mV
R_{ON}	Switch On Resistance(7)	2.7	2.7	$V_{CMD,\ DAT[3:0]}$=0V, I_{ON}=-2mA Figure 5		5.0	8.0	Ω
ΔR_{ON}	Delta On Resistance(6, 8)	2.7	2.7	$V_{CMD,\ DAT[3:0]}$=0V, I_{ON}=- 2mA		0.8		Ω
Power Supply								
$I_{CC(VDDC)}$	Quiescent Supply Current (Card)	3.6	0	V_{SW}=0 or V_{DDC}, I_{OUT}=0			2	µA
I_{CC} (VDDH1/C2)	Quiescent Supply Current (Hosts)	3.6	3.6	V_{SW}=0 or V_{DDx}, I_{OUT}=0, V_{CLKI}=V_{DDHX}, V_{CLKO}=Open, OE=V_{DDC}			2	µA
ΔI_{HOST}	Delta $I_{CC(VDDH1,\ VDDH2)}$ for One Card Powered Off	3.6	3.6 / 0 0 / 3.6	V_{SW}=0 or V_{DDx}, I_{OUT}=0, V_{CLKI}=V_{DDHX}, V_{CLKO}=Open, OE=V_{DDC}			2	µA

Notes:

6. Guaranteed by characterization, not production tested.
7. On resistance is determined by the voltage drop between the switch I/O pins at the indicated current through the switch.
8. $\Delta R_{ON}=R_{ON\ max} - R_{ON\ min}$ measured at identical V_{CC}, temperature, and voltage.

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AC Electrical Characteristics at 1.8V V_{DDC}

All typical values are for V_{DDC}=1.8V at 25°C unless otherwise specified.

Symbol	Parameter	V_{DDC} (V)	V_{DDH1} / V_{DDH2} (V)	Conditions	T_A=-40 to +85°C			Unit
					Min.	Typ.	Max.	
t_{ON}	Turn-On Time, S, OE to CMD, DAT[3:0]	1.65 to 1.95	1.65 to 3.6	V_{SW}=0V, R_L=1kΩ, C_L=20pF Figure 7, Figure 8		8	18	ns
t_{OFF}	Turn-Off Time, S, OE to CMD, DAT[3:0]	1.65 to 1.95	1.65 to 3.6	V_{SW}=0V, R_L=1kΩ, C_L=20pF Figure 7, Figure 8		6	13	ns
$t_{RISE1/FALL1}$	CMD/DAT Output Edge Rates(9)	1.65 to 1.95	1.65 to 3.6	R_L=1kΩ, C_L=20pF (10-90%) Figure 7, Figure 8		3		ns
t_{PD}	Switch Propagation Delay(9)	1.65 to 1.95	1.65 to 3.6	R_L=1kΩ, C_L=20pF Figure 7, Figure 89		4.5	9	ns
t_{pLH}	LH Propagation Delay 1CLK, 2CLK to CLK	1.65 to 1.95	1.65 to 3.6	C_L=20pF Figure 10, Figure 11		4	6	ns
t_{pHL}	HL Propagation Delay 1CLK, 2CLK to CLK	1.65 to 1.95	1.65 to 3.6	C_L=20pF Figure 10, Figure 11		4	6	ns
$t_{RISE2/FALL2}$	CLK Output Edge Rates(9)	1.65 to 1.95	1.65 to 3.6	C_L=20pF (10-90%) Figure 7, Figure 8		3		ns
O_{IRR}	Off Isolation(9)	1.8	1.65 to 3.6	f=10MHz, R_T=50Ω, C_L=20pF, Figure 12		-60		dB
Xtalk	Non-Adjacent Channel Crosstalk(9)	1.8	1.65 to 3.6	f=10MHz, R_T=50Ω, C_L=20pF, Figure 13		-60		dB
f_{toggle}	Clock Frequency(9)	1.8	1.65 to 3.6	C_L=20pF		75		MHz

Note:

9. Guaranteed by characterization, not production tested.

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AC Electrical Characteristics at 3.3V V_{DDC}

All typical values are for V_{DDC}=3.3V at 25°C unless otherwise specified.

Symbol	Parameter	V_{DDC} (V)	V_{DDH1} / V_{DDH2} (V)	Conditions	T_A=-40 to +85°C			Unit
					Min.	Typ.	Max.	
t_{ON}	Turn-On Time, S, OE to CMD, DAT[3:0]	2.7 to 3.6	1.65 to 3.6	V_{SW}=0V, R_L=1kΩ, C_L=20pF Figure 7, Figure 8		8	18	ns
t_{OFF}	Turn-Off Time, S, OE to CMD, DAT[3:0]	2.7 to 3.6	1.65 to 3.6	V_{SW}=0V, R_L=1kΩ, C_L=20pF Figure 7, Figure 8		6	13	ns
$t_{RISE1/FALL1}$	CMD/DAT Output Edge Rates(10)	2.7 to 3.6	1.65 to 3.6	R_L=1kΩ, C_L=20pF (10-90%) Figure 7, Figure 8		3		ns
t_{PD}	Switch Propagation Delay(10)	2.7 to 3.6	1.65 to 3.6	R_L=1kΩ, C_L=20pF Figure 7, Figure 8		2.5	6	ns
t_{pLH}	LH Propagation Delay 1CLK, 2CLK to CLK	2.7 to 3.6	1.65 to 3.6	C_L=20pF Figure 10, Figure 11		4	6	ns
t_{pHL}	HL Propagation Delay 1CLK, 2CLK to CLK	2.7 to 3.6	1.65 to 3.6	C_L=20pF Figure 10, Figure 11		4	6	ns
$t_{RISE2/FALL2}$	CLK Output Edge Rates(10)	2.7 to 3.6	1.65 to 3.6	C_L=20pF (10-90%) Figure 7, Figure 8		3		ns
O_{IRR}	Off Isolation(10)	2.7	1.65 to 3.6	f=10MHz, R_T=50Ω, C_L=20pF Figure 12		-60		dB
Xtalk	Non-Adjacent Channel Crosstalk(10)	2.7	1.65 to 3.6	f=10MHz, R_T=50Ω, C_L=20pF, Figure 13		-60		dB
f_{toggle}	Clock Frequency(10)	2.7	1.65 to 3.6	C_L=20pF		75		MHz

Note:
10. Guaranteed by characterization, not production tested.

Capacitance

Symbol	Parameter	V_{DDC} (V)	$V_{DDH1/H2}$ (V)	Conditions	T_A=-40 to +85°C			Unit
					Min.	Typ.	Max.	
$C_{IN(S, OE, CLK)}$	Control and nCLK Pin Input Capacitance(11)	0	2.7	V_{DDC}=0V		2.5		pF
C_{ON}	Common Port On Capacitance(11) ($C_{DAT[3:0], CMD}$)	2.7	2.7	V_{OE}=V_{DDC}, V_{bias}=0.5V, f=1MHz Figure 14		7.5		pF
C_{OFF}	Input Source Off Capacitance(11)	2.7	2.7	V_{OE}=0V, V_{bias}=0.5V, f=1MHz Figure 15		4		pF

Note:
11. Guaranteed by characterization, not production tested.

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Test Diagrams

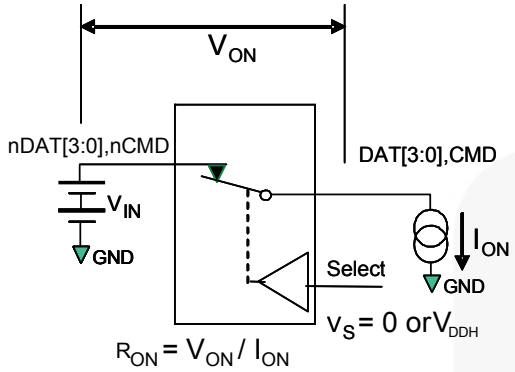


Figure 5. On Resistance

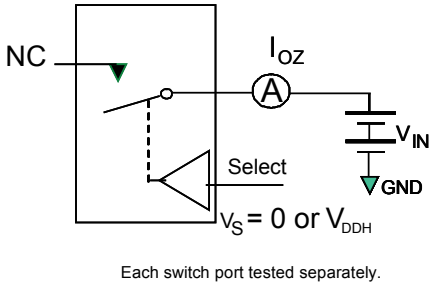
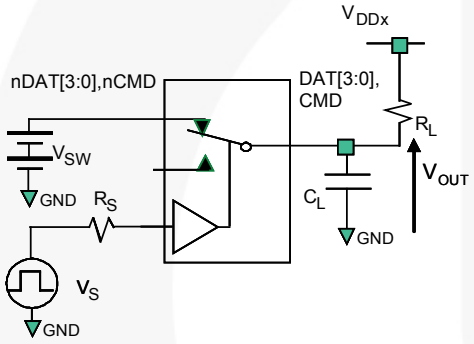


Figure 6. Off Leakage



R_L, R_S, and C_L are functions of the application environment (see AC tables for specific values).
C_L includes test fixture and stray capacitance.

Figure 7. AC Test Circuit Load

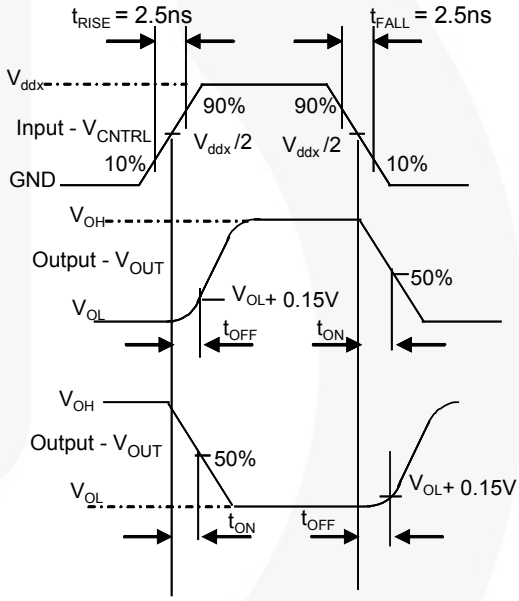


Figure 8. Turn On/Off Time Waveforms

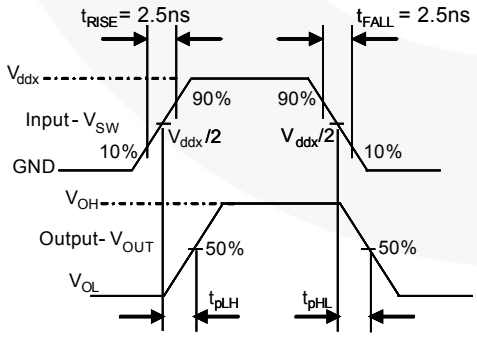
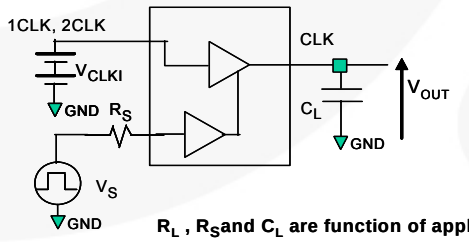


Figure 9. Switch Propagation Delay (t_{PD}) Waveform



R_L , $R_S$and C_L are function of application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance

Figure 10. AC Test Circuit Load (CLK)

Test Diagrams (Continued)

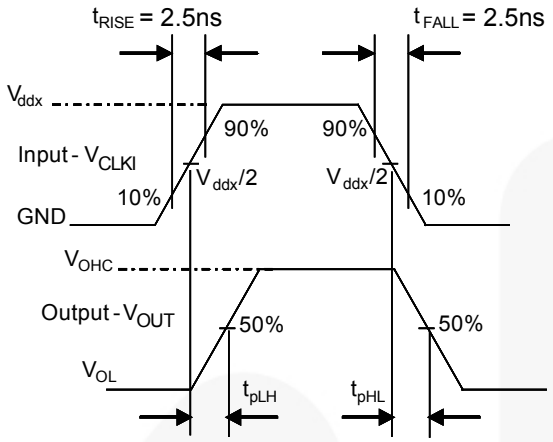


Figure 11. CLK Propagation Delay Waveforms

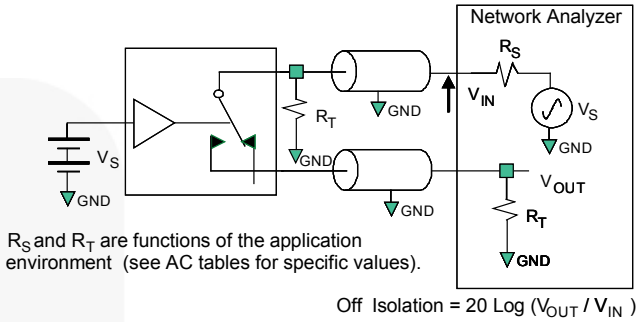


Figure 12. Channel Off Isolation

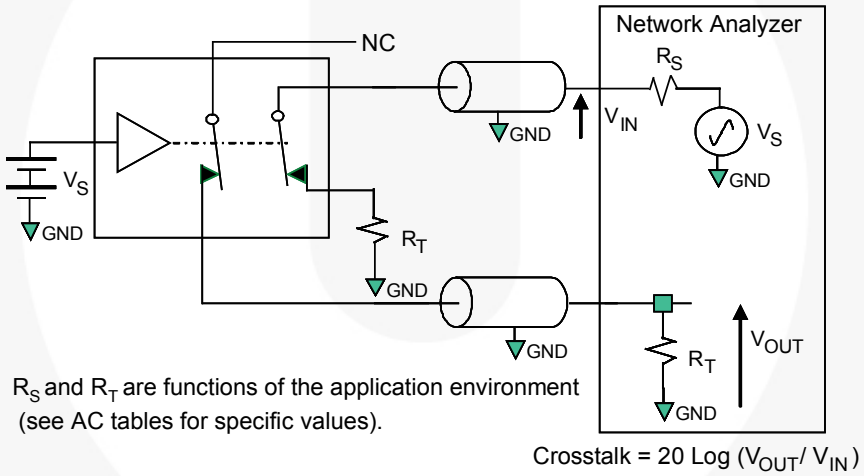


Figure 13. Channel-to-Channel Crosstalk

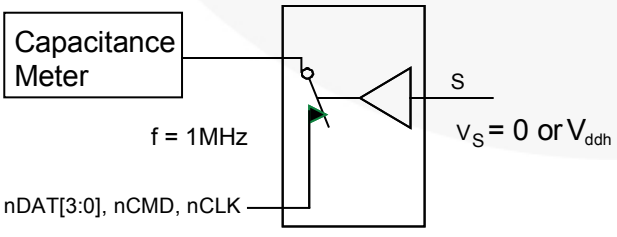


Figure 14. Channel On Capacitance

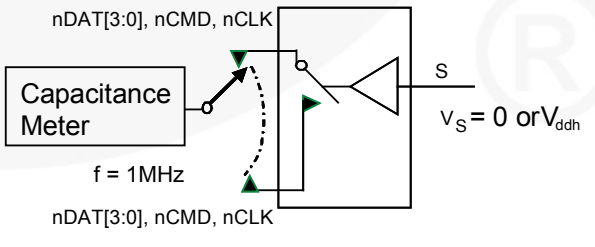


Figure 15. Channel Off Capacitance

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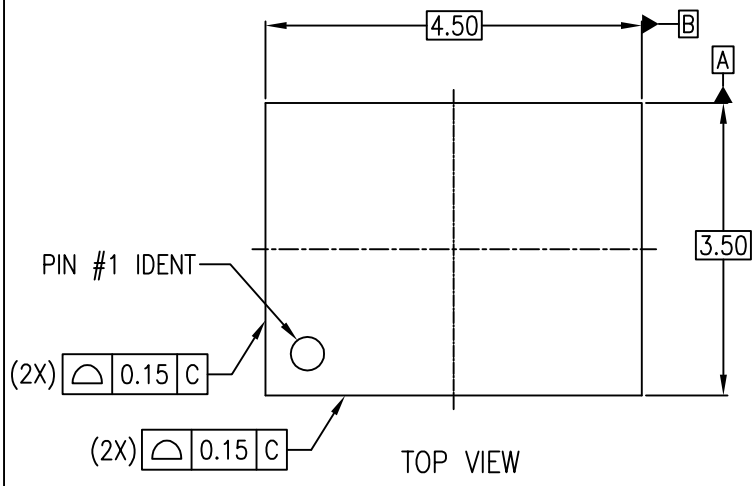
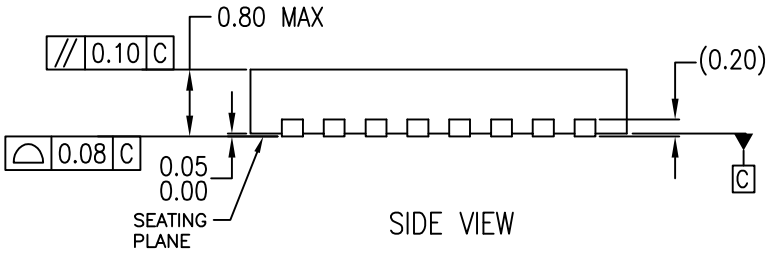
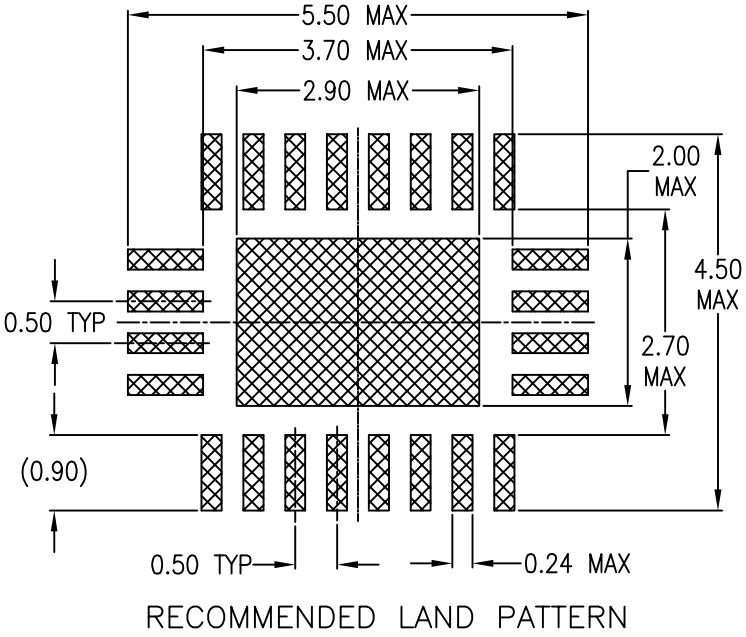
REVISIONS

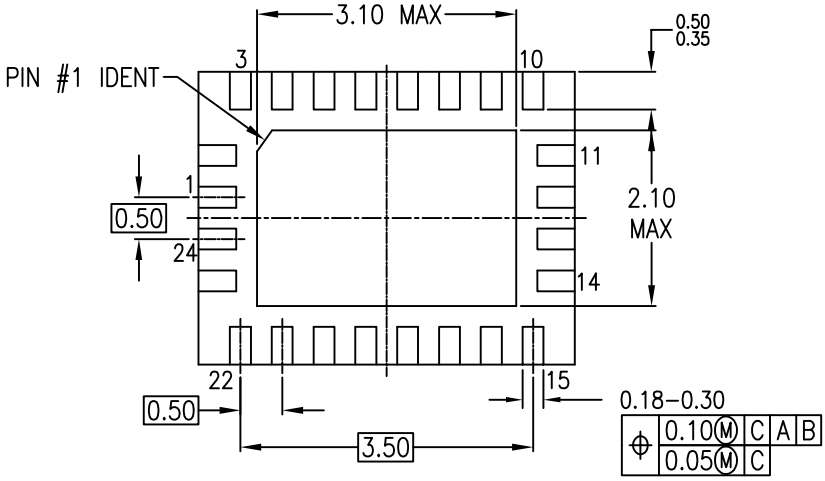
LTR	DESCRIPTION	EDCN	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL		7-4-2003	FEITAN
B	REVISE DWG NAME AND NOTE 1.		12-11-2003	FEITAN
C	CORRECTED PIN NUMBERING AND DAP DIM REMOVED LAND PATTERN NUMBERING. REVISED NOTE 1. TOP VIEW ADDED PIN #1 DOT		17-11-2003	HALLEN
4	CORRECTED THE LEAD LENGTH FROM 0.35~0.75 TO 0.35~0.50		26 JAN 2007	CHIPKING







RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WFSD-2 FOR DIMENSIONS ONLY. PIN NUMBERING DOES NOT COMPLY.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP24Brev4

APPROVALS	DATE
DRAWN FEITAN	31-3-2003
DFTG. CHK.	
ENGR. CHK.	

FAIRCHILD SEMICONDUCTOR® Bayan Lepas, FIZ, 11900, Penang, Malaysia.

24LD, MLP, QUAD, JEDEC MO-220, 3.5x4.5 MM

PROJECTION INCH [MM]

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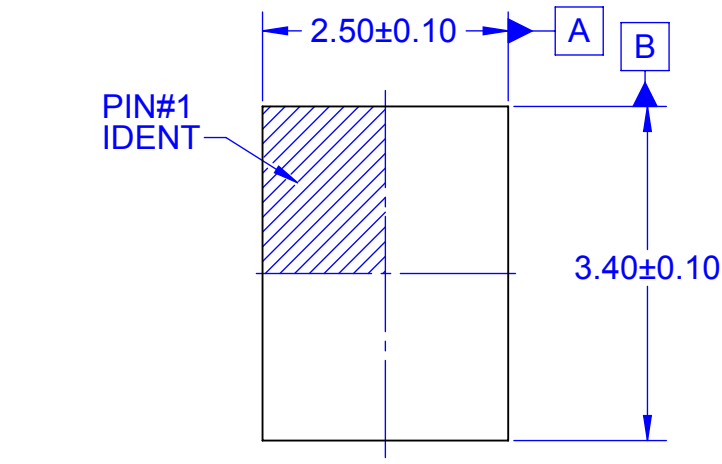
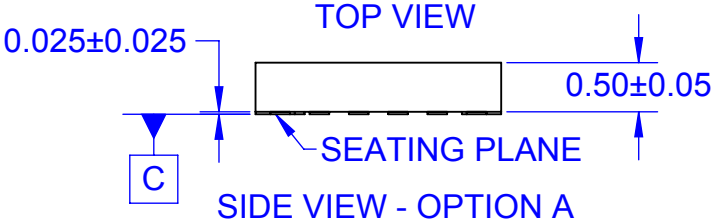
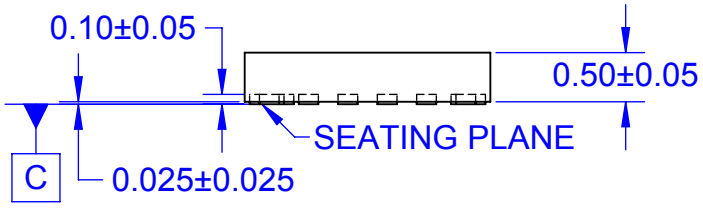
DO NOT SCALE DRAWING | SHEET 1 of 1



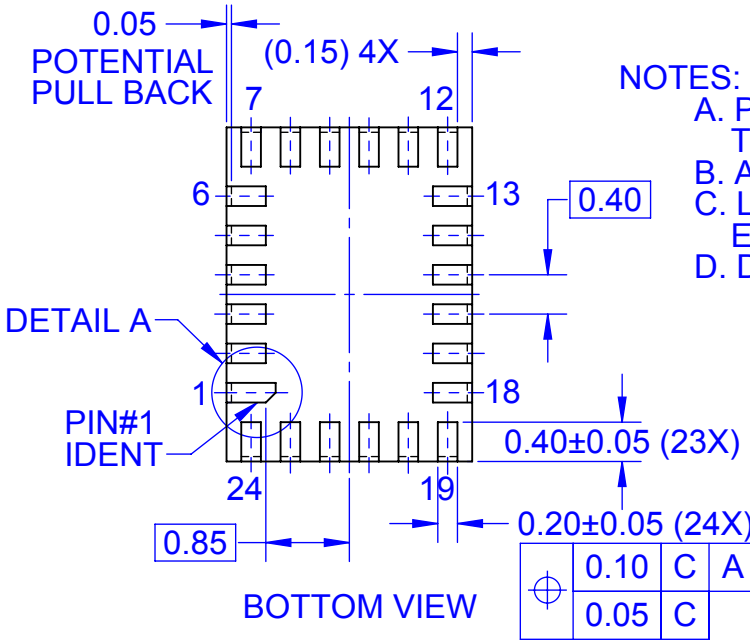
TOP VIEW



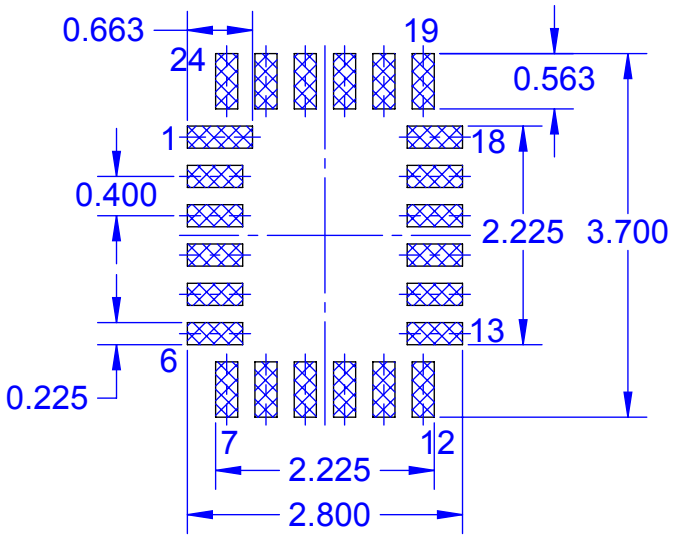
SIDE VIEW - OPTION A



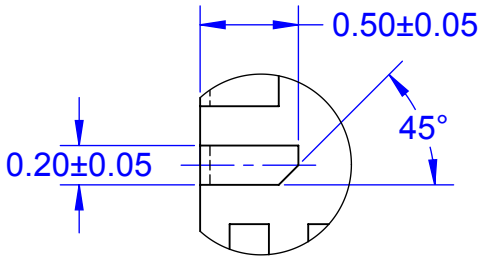
SIDE VIEW - OPTION B



BOTTOM VIEW



LAND PATTERN RECOMMENDATION



DETAIL A
SCALE 2:1

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
D. DRAWING FILENAME: MKT-UMLP24ArevE

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