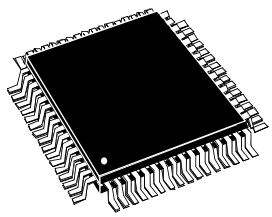
STV2310

Multistandard TV digital video decoder with adaptive comb filter and RGB/YCrCb input

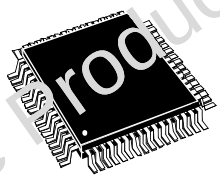
Features

- **Worldwide TV Standards Compatible**
- **Automatic NTSC/PAL/SECAM Digital Chroma Decoder**
- **NTSC/PAL Adaptive 4H/2D Comb Filter**
- **VBI Data Slicer for Teletext, Closed Caption, WSS and other systems**
- **Analog RGB/Fast Blanking Capture and Insertion in YCrCb Output Flow (SCART legacy)**
- **Analog YCrCb inputs with Tint Control**
- **10-bit, 30-MSPS A/D Converter for Y/CVBS input**
- **8-bit, 30-MSPS A/D Converter for C and RGB/CrCb inputs**
- **Hue control and automatic flesh control for NTSC CVBS/YC signals**
- **Programmable Horizontal Scaling (x0.25 to x4 Scaling Factor) and Panorama Vision**
- **Copy-Protection System compatible**
- **H and V Synchronisation Processing that is robust to non-standard sources such as VCR, and to weak and noisy signals**
- **8-bit Pixel Output Interface Line-Locked ITU-R BT_656/601 or square pixel YCrCb outputs**
- **Single System Clock for all Video Input Formats**
- **Two-wire I²C Bus Interface up to 400 kHz**
- **Typical Power Consumption: 550 mW**
- **Power Supply: 1.8 V and 3.3 V**



TQFP64 14x14x1.4 mm
(Thin Quad Flat Package)

ORDER CODE: STV2310D/DT



TQFP64 10x10x1.4 mm
(Thin Quad Flat Package)

ORDER CODE: STV2310SD/SDT

The STV2310 is a high-quality front-end video circuit for processing all analog NTSC/PAL/SECAM standards into a 4:2:2 YCrCb digital video format ,as well as conventional analog RGB or YCrCb signals. The STV2310 is programmable through an I²C interface.

The STV2310 provides a cost-effective solution for digitized TV, LCD TV/monitors, digital TV, STB, video surveillance/security, video conferencing, video capturing devices and PC video card.

It can be used as a stand-alone chip working with third-party products, as a companion chip to the TV processor STV3500, STV3600 for digitized 100-Hz/ ProScan CRT TVs, or as a companion chip to the TV processor STV3550 for LCD-TVs.

Figure 1: STV2310 Block Diagram

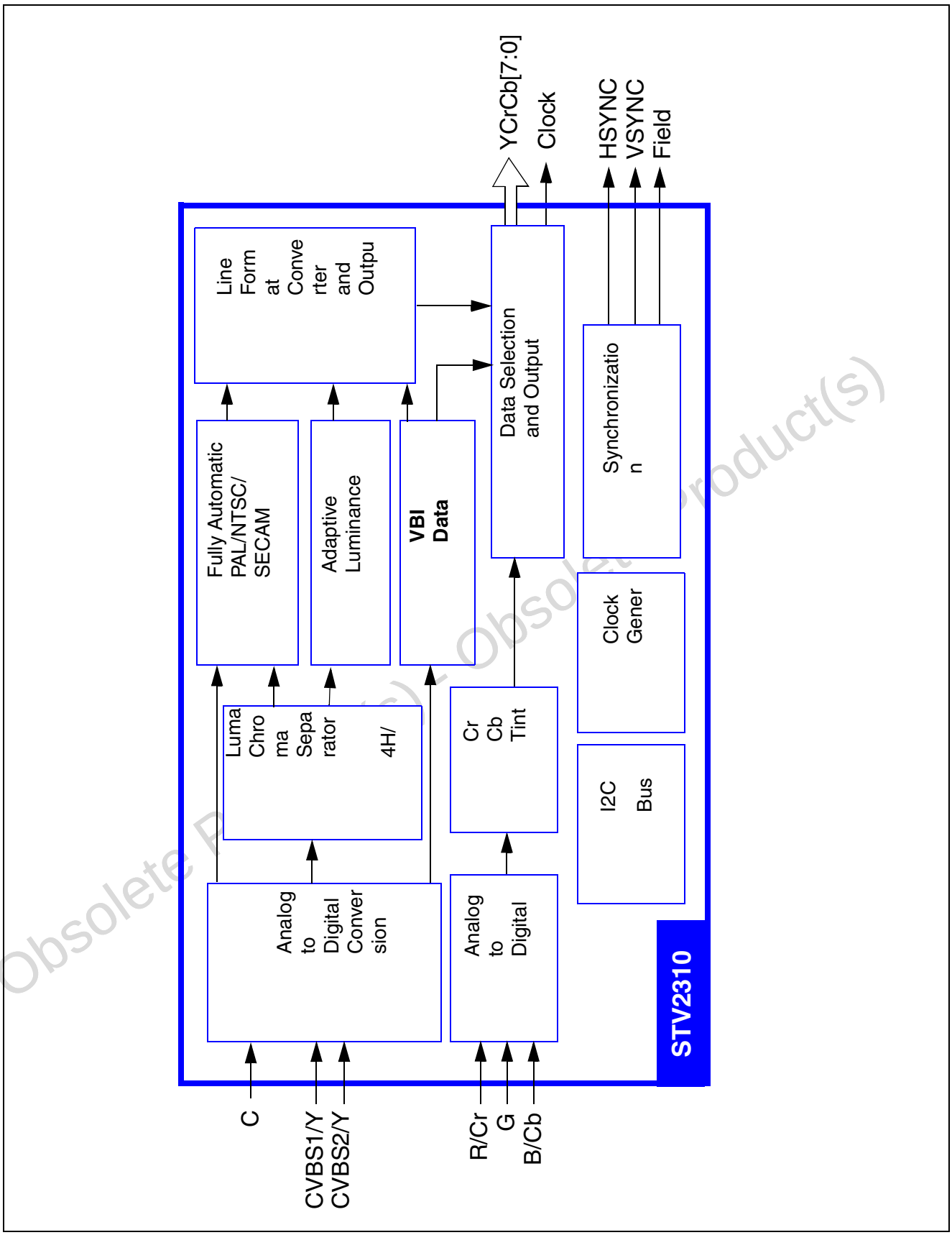


Table of Contents

1 General Description

The STV2310 is a high-quality video front-end circuit for processing all analog standards into a digitalized 4:2:2 YCrCb video format. It processes NTSC/PAL/SECAM CVBS signals, as well as conventional analog RGB or YCrCb signals.

This circuit outputs demodulated chrominance, in-phased luminance and sliced Vertical Blanking Interval (VBI) data for the most common services such as Teletext, Closed Caption, WSS, VPS, Gemstar.

The STV2310 does not need an external synchronization system. It extracts all necessary synchronization signals from CVBS or Y signals, and delivers the horizontal, vertical and frame signals either on dedicated pins or embedded into the digital bit stream.

It features automatic standard recognition and automatic selection of the optimal Y/C separation algorithm according to the standard and has extensive output scaling capabilities. The STV2310 chip includes an analog RGB capture feature and programmable automatic mixing with the main picture digital output.

8-bit ITU-R BT.601/656 and Square Pixel output standards are supported.

The STV2310 provides a cost-effective solution for digitized TV, LCD TV/monitors, digital TV, STB, video surveillance/security, video conferencing, video capturing devices and PC video card.

It can be used as a stand-alone chip working with third-party products, as a companion chip to the TV processor STV3500, STV3600 for digitized 100-Hz/ProScan CRT TVs, or as a companion chip to the TV processor STV3550 for LCD-TVs.

All sub-level blocks operate at the frequency used as a sampling frequency (f_S) for the five embedded A/D converters. This free-running clock is called the system clock (f_S) and is provided

either by an embedded crystal oscillator or an external clock generator (27 MHz).The only exception is the output stage which operates at the line-locked output pixel clock frequency.

Figure 2: Architectural Block Diagram

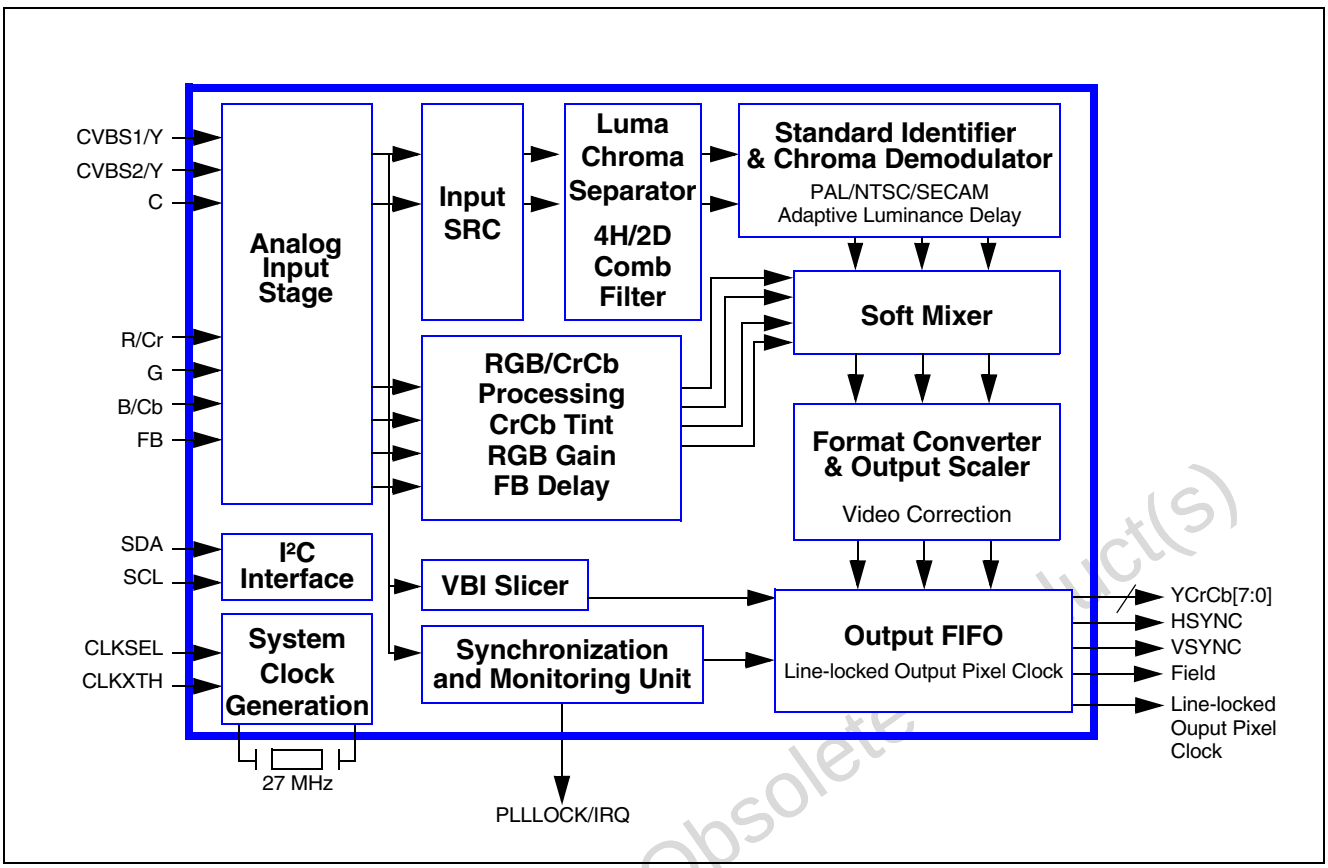
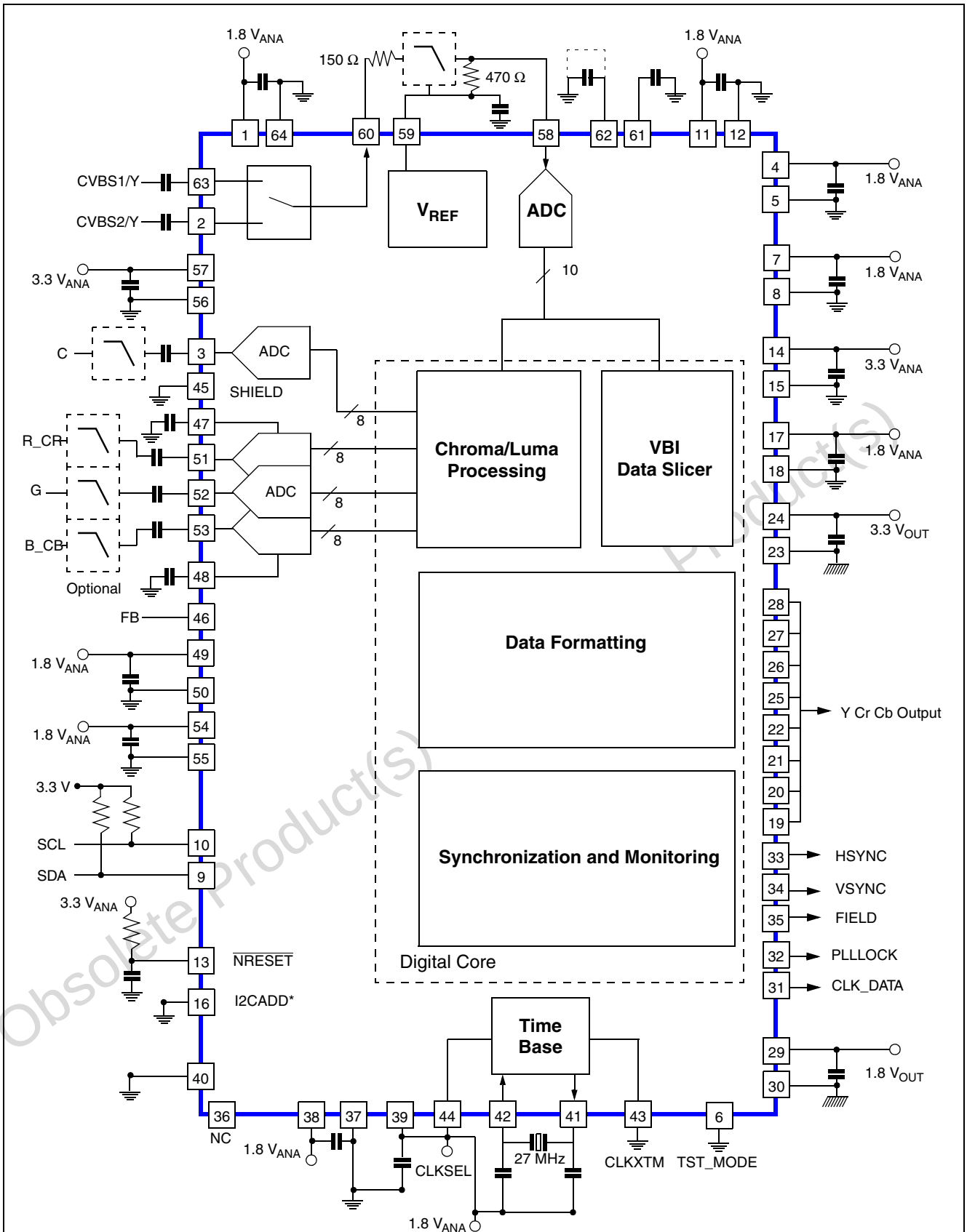


Figure 3: Application Block Diagram

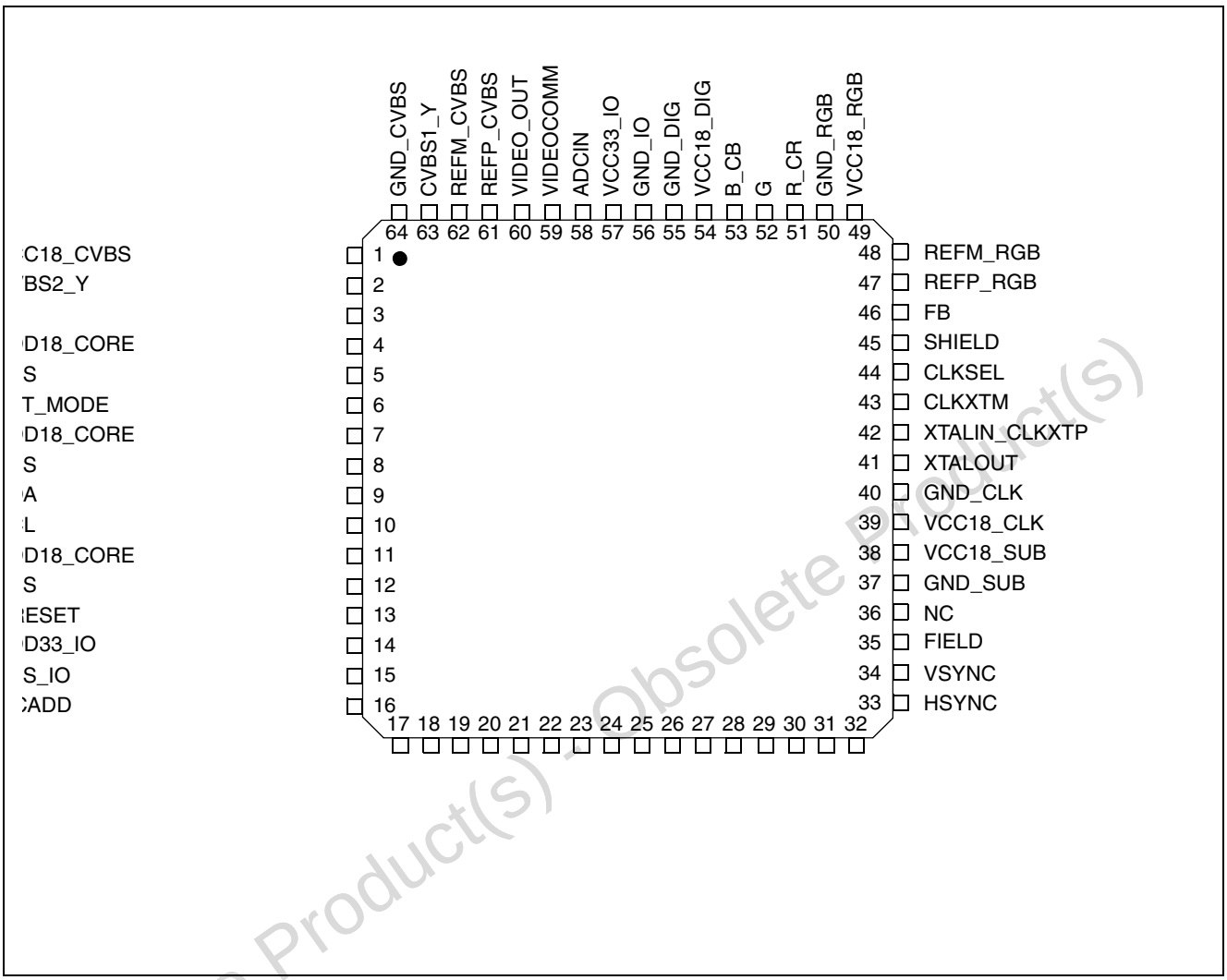


* Possible alternate I²C address. See Section 5.1: Register Map on page 55.

2 Pin Allocation and Description

2.1 Pinout Diagram

Figure 4: 64-Pin 14 x 14 TQFP Package Pinout



2.2 Pin Descriptions

Table 1: Power Supply Pins (page 1 of 2)

Pin	Pin Name	Pin Description
Analog		
1	VCC18_CVBS	1.8 V Analog Voltage Supply for Analog Input Stage
36	NC	Not connected
37	GND_SUB	Analog Ground Supply (Substrate Polarization)
38	VCC18_SUB	1.8 V Analog Voltage Supply (Output and Pin Isolation layer)
39	VCC18_CLK	1.8 V Analog Voltage Supply for Clock Generator

Table 1: Power Supply Pins (page 2 of 2)

Pin	Pin Name	Pin Description
40	GND_CLK	Analog Ground Supply for Clock Generator
45	SHIELD	Guard Ring (Analog Input Stage) To be connected to Analog Ground Supply
49	VCC18_RGB	1.8 V Analog Voltage Supply (RGB)
50	GND_RGB	Analog Ground Supply (RGB)
54	VCC18_DIG	1.8 V Analog Voltage Supply (Analog Input Stage)
55	GND_DIG	Analog Ground Supply (Analog Input Stage)
56	GND_IO	Analog Ground Supply (Analog Input Stage)
57	VCC33_IO	3.3 V Analog Voltage Supply (Analog Input Stage)
64	GND_CVBS	Analog Ground Supply (Analog Input Stage)
Digital		
4	VDD18_CORE	1.8 V Digital Voltage Supply (Digital Core)
5	VSS	Digital Ground Supply (Digital Core)
7	VDD18_CORE	1.8 V Digital Voltage Supply (Digital Core)
8	VSS	Digital Ground Supply (Digital Core)
11	VDD18_CORE	1.8 V Digital Voltage Supply (Digital Core)
12	VSS	Digital Ground Supply (Digital Core)
14	VDD33_IO	3.3 V I/O Voltage Supply (Digital Core)
15	VSS_IO	I/O Ground Supply
17	VDD18_CORE	1.8 V Digital Voltage Supply (Digital Core)
18	VSS	Digital Ground Supply (Digital Core)
23	VSS_IOOUT	Output Ground Supply (Output Stage)
24	VDD33_OUT	3.3 V Output Voltage Supply (Output Stage)
29	VDD18_OUT	1.8 V Digital Voltage Supply (Output Stage)
30	VSS_OUT	Digital Ground Supply (Output Stage)

Table 2: Analog Pins (page 1 of 2)

Pin	Pin Name	Pin Description
2	CVBS2_Y	CVBS or Y Input 2 (Selected by programming)
3	C	Chroma Input (Y/C inputs used for S-Video) (Selected by programming)
46	FB	Fast Blanking Input (To be used only when R_CR, G, and B_CB inputs are connected)
47	REFP_RGB	Positive Reference Voltage for RGB ADCs
48	REFM_RGB	Negative Reference Voltage for RGB ADCs
51	R_CR	R Input for RGB Insertion. Cr Input for Analog YCrCb mode.
52	G	G Input for RGB Insertion.
53	B_CB	B Input for RGB Insertion. Cb Input for Analog YCrCb mode.

Table 2: Analog Pins (page 2 of 2)

Pin	Pin Name	Pin Description
58	ADCIN	CVBS ADC Input (To be connected to Anti-Aliasing Filter output)
59	VIDEOCOMM	CVBS Anti-Aliasing Filter Reference Voltage
60	VIDEO_OUT	Video Analog Front-end Multiplexer Output for external filtering
61	REFP_CVBS	Positive Reference Voltage for CVBS and Chroma ADCs
62	REFM_CVBS	Ground CVBS and Chroma ADCs
63	CVBS1_Y	CVBS or Y Input 1 (Selected by programming)

Table 3: Output Pins

Pin	Pin Name	Type	Pin Description
19	YCRCB7	O	Digital Video Output 7
20	YCRCB6	O	Digital Video Output 6
21	YCRCB5	O	Digital Video Output 5
22	YCRCB4	O	Digital Video Output 4
25	YCRCB3	O	Digital Video Output 3
26	YCRCB2	O	Digital Video Output 2
27	YCRCB1	O	Digital Video Output 1
28	YCRCB0	O	Digital Video Output 0
31	CLK_DATA	O	Output Pixel Clock, active edge is programmable
32	PLLLOCK/IRQ	O	Output PLL Lock Signal Alternate Function 1: OUTBUS[0] Bus extension Alternate Function 2: Interrrupt Request (IRQ)
33	HSYNC	O	Horizontal Synchronization Pulse Output Alternate Function: OUTBUS[1] Bus extension
34	VSYNC	O	Vertical Synchronization Pulse Output Alternate Function: OUTBUS[2] Bus extension
35	FIELD	O	Field (Parity) Output Signal Alternate Function: OUTBUS[3] Bus extension

Table 4: Clock Signal Pins

Pin	Pin Name	Pin Description
41	XTALOUT	Crystal Pad Oscillator Output
42	XTALIN_CLKXTP	Crystal Pad Oscillator Input Alternate Function: Differential Clock input
43	CLKXTM	Differential Clock input (To be used in conjunction with CLKXTP)
44	CLKSEL	OV: Differential Clock input active (CLKXTM, CLKXTP 3.3V: Crystal Pad Oscillator active (XTALOUT, XTALIN)

Table 5: Configuration Pins

Pin	Pin Name	Type	Pin Description
6	TST_MODE	I	To be Connected to Ground
9	SDA	I/O	I²C Bus Data
10	SCL	I/O	I²C Bus Clock
13	NRESET	I	Active Low Reset
16	I2CADD	I	0V: 86h/87h and output pad active at Reset 3.3V: 8Eh/8Fh and output pad high impedance state at Reset

3 Default Setup At Reset

The default configuration at reset is:

- CVBS1_ input active
- Fast Blanking input for RGB insertion enable
- Automatic Standard Recognition of NTSC/PAL/SECAM
- Comb filter enable
- Data slicer enable
- Output ITU_R BT. 656/601
- Output clock CLK_DATA rising edge active
- PLL lock, HSYNC, VSYNC, FIELD primary functions enable
- Output pads active when Pin 16 connected to ground
- Output pads high impedance state when pin 16 connected to 3.3V
- Automatic HPLL time constant selection

For more detailed reset configuration descriptions, refer to Chapter 5: Register List.

3.1 System Clock Generation

The STV2310 clock is either provided by an internal 27-MHz crystal oscillator connected to pins XTALIN_CLKXTP and XTALOUT, or imported in Differential mode from an external device such as the STV3500 and connected to the XTALIN_CLKXTP and CLKXTM pins.

4 Functional Description

4.1 Analog Input Stage

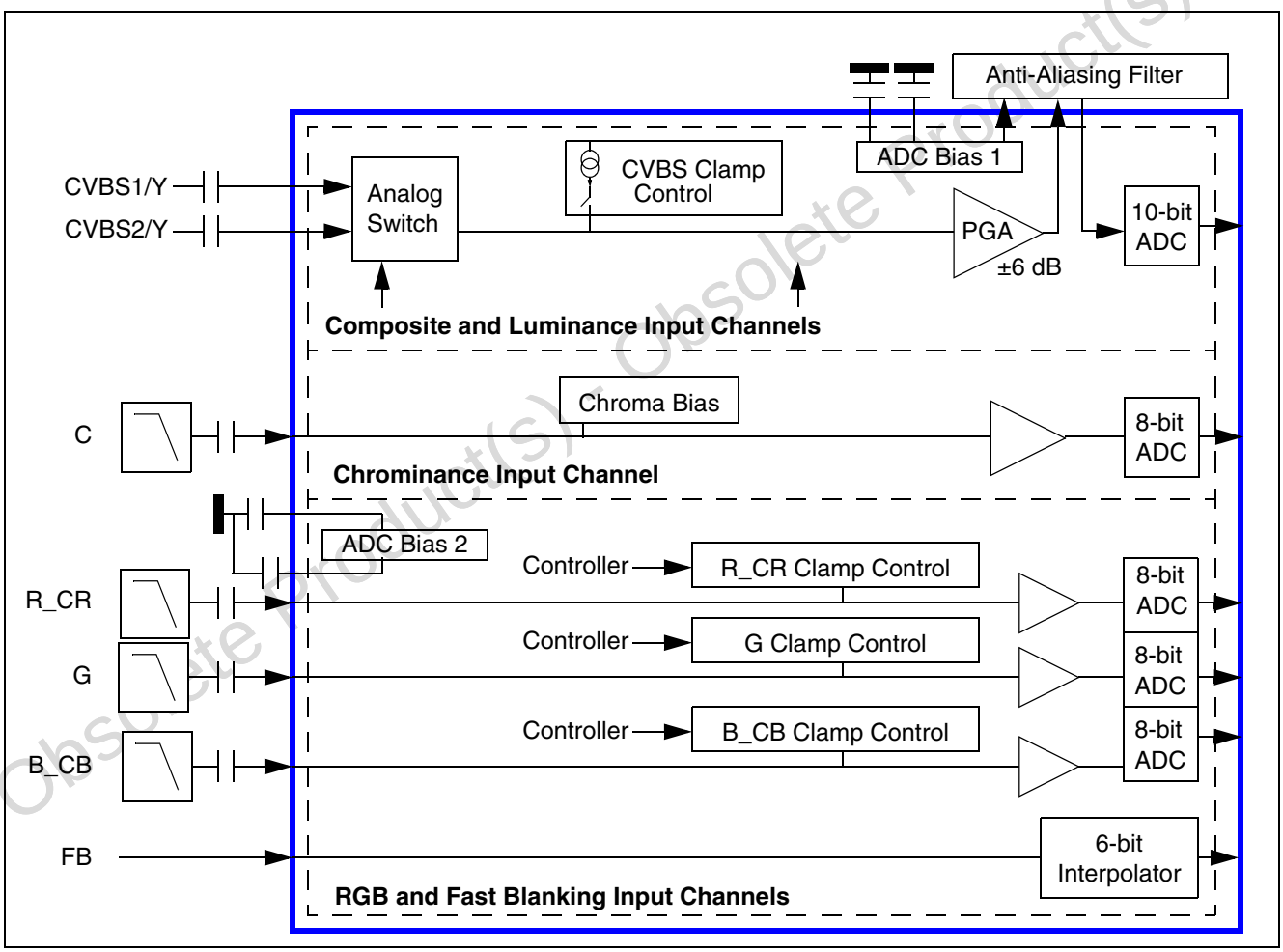
4.1.1 General Description

The Analog Input Stage provides the interface between the incoming video signals and the Analog-to-Digital Converters (ADC) using Clamp and Automatic Gain Control (AGC) stages to fit the analog signals to the ADC range.

Several video sources are processed in this stage:

- CVBS signals from a broadcast signal or the SCART connector.
- S-Video (Y/C) signals coming from an external video source (VCR, DVD, STB).
- RGB signals with Fast Blanking (FB) input coming from the SCART connector.
- Analog YCrCb signals coming from a DVD player (1H interlaced).

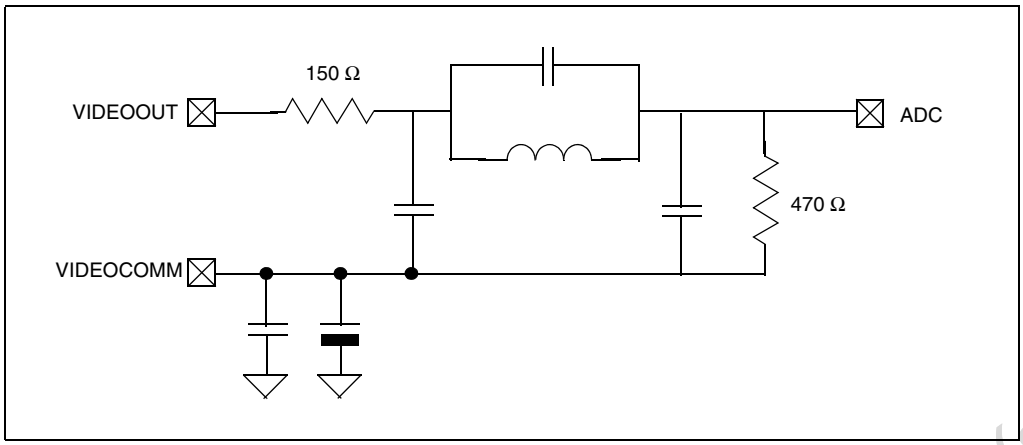
Figure 5: Analog Input Stage Functional Block Diagram



The CVBS/Y signal from the selected input channel goes through an automatic clamp and a Programmable Gain Amplifier (PGA) circuit. The clamping circuit automatically adjusts the black level to a programmable A/D output digital code. The clamp voltage is stored on the input coupling capacitor (22 nF, external to the STV2310). The PGA automatically adjusts the input signal

magnitude by ±6 dB in 63 logarithmic steps to the optimal range of the A/D Converter. The video signal then goes through an external anti-aliasing filter before reaching the A/D Converter. The A/D Converter dedicated to the CVBS/Y channel has a 10-bit resolution. The A/D Converters dedicated to the C, R_Cr, G and B_Cb channels have an 8-bit resolution.

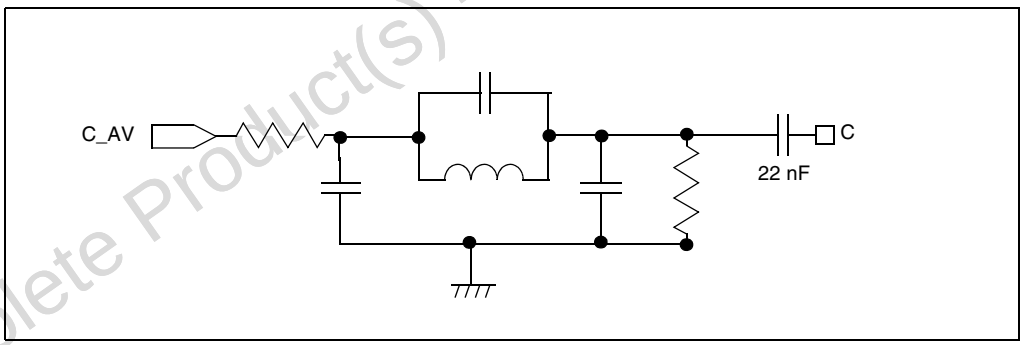
Figure 6: Anti-Aliasing FIlter for CVBS Input Signals



Two independent CVBS sources can be connected to the STV2310. To process S-Video signals, the luma signal is connected to one of the CVBS inputs and the chroma signal is connected to the C input. RGB signals are directly connected to the three separate inputs (R_Cr, G and B_Cb). For Analog YCrCb signals, the luma signal is connected to one of the CVBS inputs, the Cr signal is connected to the R_CR input and the Cb signal is connected to the B_CB input.

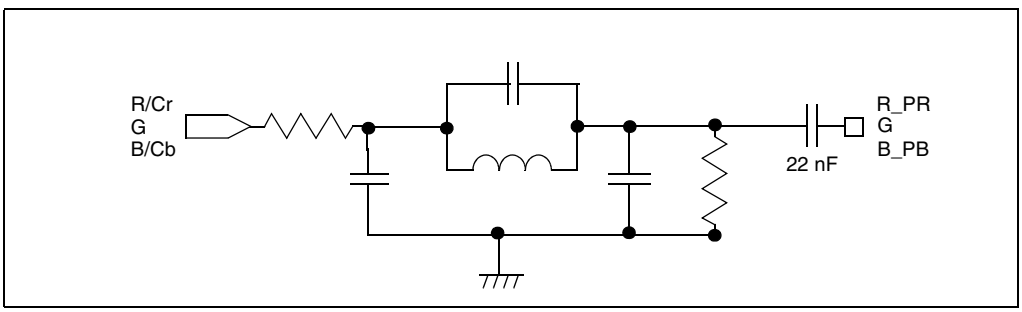
For S-Video signals, the Y (luminance) signal is connected to the selected CVBS input. The analog C (chrominance) input includes a bias and fixed gain circuit. The C signal is digitized by an 8-bit A/D Converter. It is recommended that an external anti-aliasing filter be added before the C input.

Figure 7: Anti-Aliasing FIlter for Chroma Input Signals



Analog R_PR, G and B_PB signals are clamped to the black level during the back porch period. These signals are digitized by a triple 8-bit A/D converter. It is recommended that an external anti-aliasing filter be added before each channel input.

Figure 8: Anti-Aliasing FIlter for R_PR, G and B_PB Input Signals



The analog insertion (Fast Blanking) signal is sliced and sent to a shaper, controlling the soft switching between the analog R, G and B signals and the decoded main picture CVBS stream.

All reference voltages required by the A/D Converter are internally generated. Only two pairs of reference levels, REFP and REFM must be decoupled externally (REFP_CVBS and REFM_CVBS, REFP_RGB and REFM_RGB).

4.1.2 Programming

The channel for the desired CVBS signal source is selected by the CVBSMUX bit in the DDECCONT0 register. The AGC and clamp mechanisms are described in Section 4.2.

4.2 Synchronization and Monitoring Unit

4.2.1 General Description

The STV2310 system clock sampling frequency is provided by a free-running embedded crystal oscillator or an external clock generator. The nominal value of this sampling frequency is 27 MHz and is independent of any input TV standard.

Synchronization data (horizontal and vertical sync signals) is extracted from the video signal. After a low pass stage removing all high frequency information and noise, the video signal is sent to a synchronization slicer. Then the horizontal and vertical pulses are separated to generate the Hsync and Vsync pulses. The extracted Hsync pulses are sent to the horizontal PLL (HPLL) in order to filter the jitter. The HPLL has an adaptive time constant with noise level and other operating conditions. It provides an easy lock even in difficult conditions and performs the skew extraction. Using this data, skew correction on the data stream is performed by the output scaler. This PLL can hold a frequency range of ±8% of the H frequency. A second PLL, associated with the output FIFO, is used to perform the line-locked clock generation from which the output HSYNC and VSYNC pulses are obtained by synchronous division.

A vertical sync processor is used to generate the output Vsync pulse, synchronous to the incoming CVBS signal. This processor is able to automatically detect 50 Hz/60 Hz standards. In the event of missing pulses, the Vsync processor replaces the missing pulse by inserting a V-pulse at the end of the 50 Hz or 60 Hz windows.

If an input video signal (CVBS or S-Video) is not detected, the sync processor operates in Free-running mode.

The Output Sync Pulse (H, V and F) can be embedded in the digital output stream, according to the ITU_R BT_656/601 format, using the EAV and SAV codes. The Output Sync Pulse can also be delivered on dedicated external pins (33, 34, 35). These pins can be used specifically if the output sync pulses are no longer compliant with the ITU_R BT_656/601 format, as non-interlaced pictures or signals from a non-standard source (VCR). See Section 4.12.2.1 and Section for more information.

4.2.2 Programming

The circuit can function in Automatic mode or use a programmable HPLL time constant. Automatic mode is selected by default. In this case the STV2310 automatically adapts the time constant to the reception conditions. In the case of unstable sources (such as VCRs) the circuit uses a special user-programmable VCR time constant. This HPLL time constant's proportional gain is selected in the HSYN_GP[7:0] bits in the DDECCONT26 register. The value for the integral gain is selected in the HSYN_GI[7:0] bits in the DDECCONT27 register. These bits also define the programmable time constant when the HTIMECSTSEL bit is reset in the DDECCONT22 register (Automatic mode disabled).

To be automatically selected, the VCR time constant requires that the noise level be below the noise threshold selected by the NOISE_THRESHOLD[2:0] bits in the DDECCONT25 register.

The Vsync search and initial Free-running modes are selected by the 5060MODE[1:0] bits in the DDECCONT0 register.

The (fluctuating) average sync bottom and blanking level values, based on the Hsync Pulse Bottom Period and Composite Video Burst Period identification data, are necessary in turn to perform the clamp correction on the CVBS signal in the analog domain. (See Figure 9.) The clamp level is programmed by the BLANKMODE[1:0] bits in the DDECCONT1 register.

The Active Input Video Period and small amplitude signals for the Active Input Video Period levels which control the gain level of the AGC are programmed in the ACTITH[1:0] and SMHITH[1:0] bits (respectively) in the DDECCONT16 register.

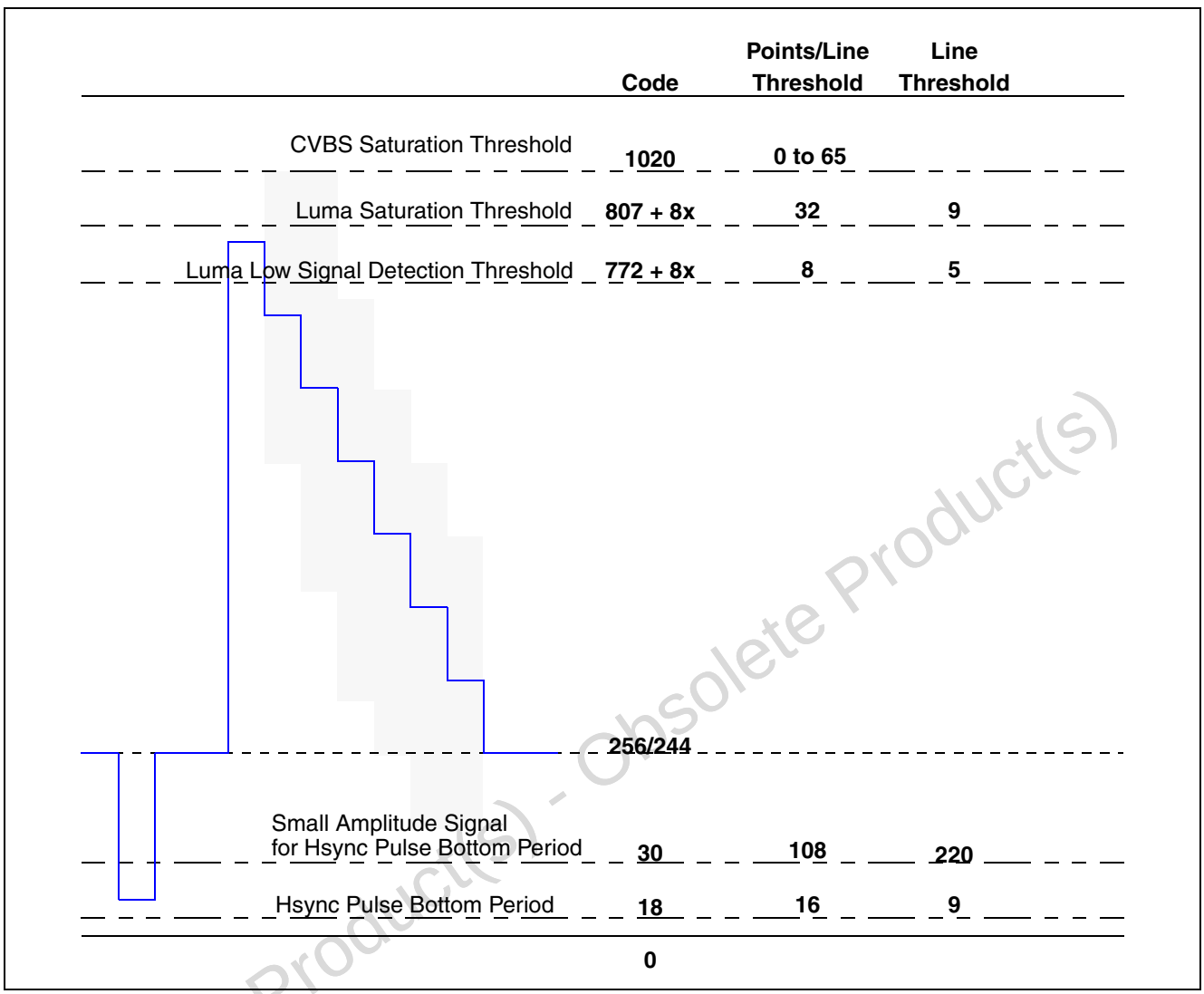
The CVBS saturation threshold is programmed in the SATLMTPT[1:0] and SATLMTLN[1:0] bits of the DDECCONT16 register in the event of a high level of chroma demodulation. It is expressed as a number of samples per field (when, according to the algorithm, the number of samples is reached, the gain is decreased).

Output mode can be forced to 50 Hz or 60 Hz by 5060MODE[1:0] bits in the the DDECCONT00 register.

To output a non-interlaced image, the chip must be set in direct parity mode by the DIRECTPARITY bit in the DDECCONT1F register.

The external HSync pulse can be synchronised to the End of Active Video (EAV) and the Start of Active Video (SAV) pulses, or initialized according to the usual analog H/V pulse using the HSYNC_SAV bit in the DDECCONT25 register.

Figure 9: AGC Flowchart



4.3 Input Sample Rate Conversion

4.3.1 General Description

An Input Sample Rate Converter (ISRC) converts the acquisition pixel rate to a clock domain virtually locked to the color subcarrier. This ISRC is controlled by a subcarrier phased-locked loop (Chroma PLL). This enables comb filtering and chroma demodulation to be carried out on various subcarrier frequencies using the same system clock sampling frequency.

The Input SRC uses the data provided by the front-end ADCs to process both the CVBS and C flows (in the event of separated Y/C inputs, the CVBS flow = Y flow). The same processing is applied to the CVBS and C data.

When the input video standard has been identified, its subcarrier frequency (f_{SC}) is known and the Chroma PLL is locked. The Input SRC transforms the input data captured at the 27-MHz system clock sampling frequency (f_S) to the subcarrier clock domain frequency (4 x f_{SC}).

The practical value of the 4 x f_{SC} frequency depends on the actual input TV standard.

4.4 Luminance and Chrominance Separation

4.4.1 General Description

The Y/C Separator separates the chrominance (C) component from the composite signal which also includes the luminance (Y), synchronization and color burst (subcarrier) components. In normal operation (NTSC and PAL standards), this is done through comb or notch filtering which relies on the correlation of consecutive lines. For SECAM inputs, a Chroma Bandpass/Trap filter system is required. If an S-Video input is selected, Y/C separation is not required and the Y/C Separator operates in Bypass mode. Y/C delay adjustment can be done with both pixel and sub-pixel accuracy.

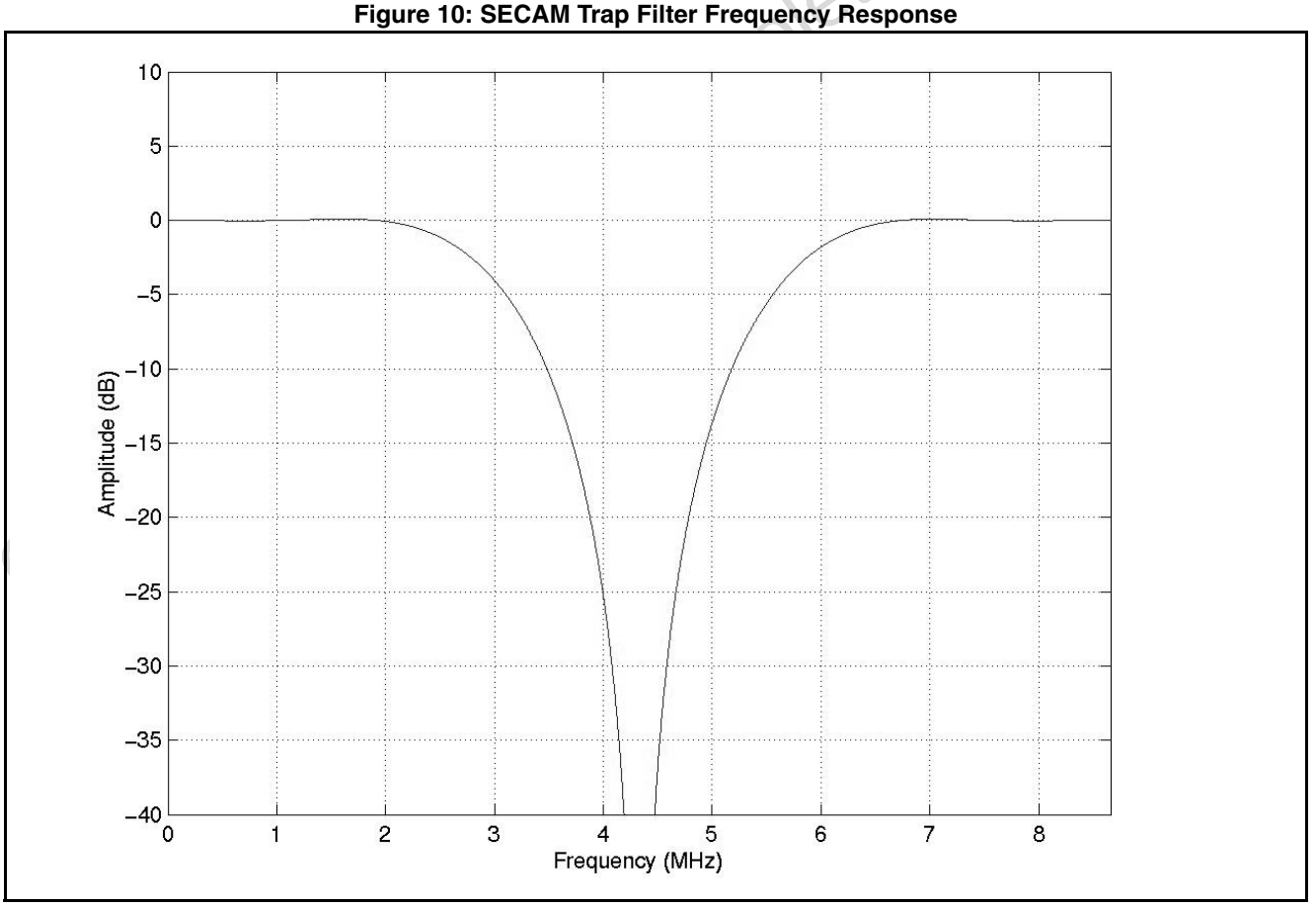
4.4.2 Programming

Once the samples processed by the input SRC have been stored in RAM, the type of input signal (Y/C or CVBS) must be specified before the chroma component can be separated from the CVBS input signal. This is done by setting the SVIDEOSEL bit in the DDECCONT0 register.

The Y/C separator block can either operate in auto-adaptive mode (Default mode) or Forced Separation mode (notch). This operating mode is selected by the COMB_MODE bit in the DDECCONT18 register:

- Chroma Bandpass/Trap filtering is forced
- Adaptative Comb Filtering mode is forced. (This applies to PAL/NTSC signals only. SECAM signals remain processed by Chroma Bandpass/Trap filter)

Figure 10: SECAM Trap Filter Frequency Response



The notch filter width used in the Y/C separation can be adjusted from narrow to wide by the BW_SEL[2:0] bits in the DDECCONT18 register. Luma Chroma delay can be adjusted by the DEM_YC_DELAY[3:0] bits in the DDECCONT15 register and DDECCONT1A register, bit [5:0].

Figure 11: Notch Filter - Narrow Group

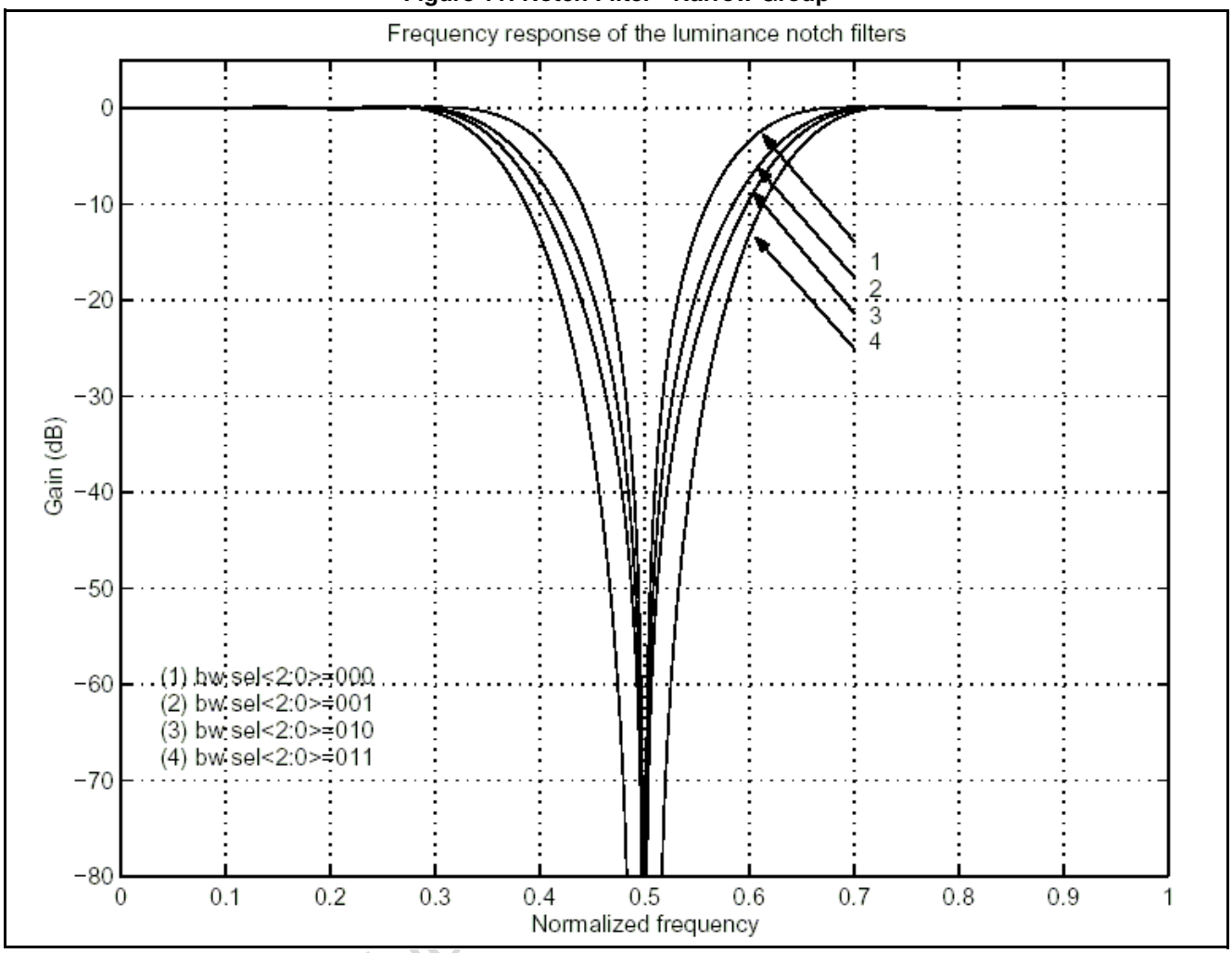
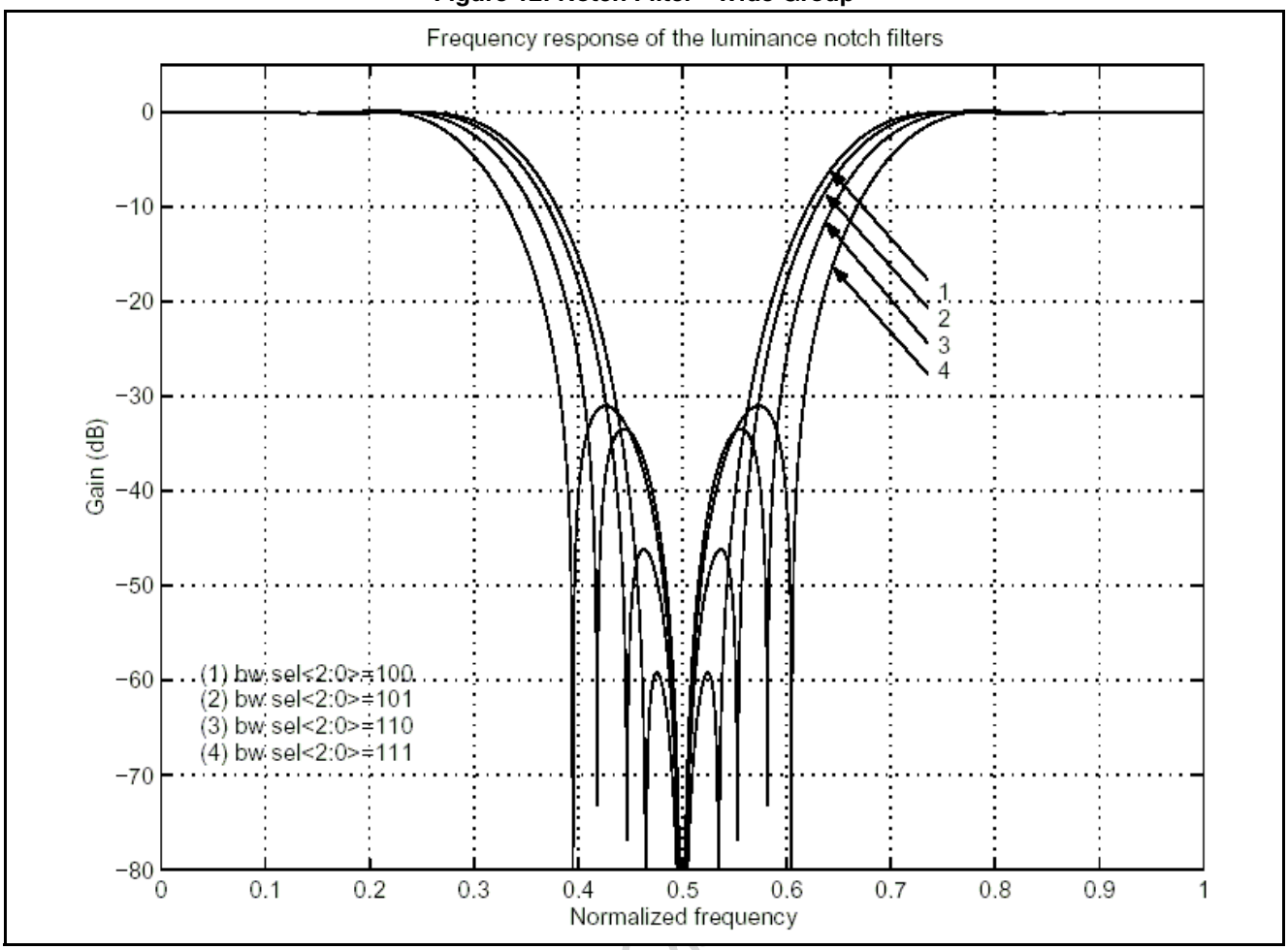


Figure 12: Notch Filter - Wide Group



4.5 Standard Research Sequence Programming

The chroma signal is sent to the Standard Identifier and Chroma Demodulator. The Standard Identifier performs an automatic recognition sequence for one of the following standards.

Table 6: TV Standards

Chroma Standard	Subcarrier Frequency	Standard Code
PAL B,D,G,H,I	4.4336 MHz	000
SECAM	4.406 MHz (foR) 4.250 MHz (foB)	001
NTSC M	3.5795 MHz	010
PAL M	3.5756 MHz	011
PAL N	3.5820 MHz	100
NTSC 4.43	4.4336 MHz	101
No Standard[1]	n/a	110
No Standard[1]	n/a	111

Note 1: Codes 110 and 111 are associated with “No Standard”.

From this list of possible standards, the user must complete the Automatic Standard Recognition table required for the automatic search. Identification will be restricted to the table entries and the first entry will be tried first. Entering code 110 or 111 in the Automatic Standard Recognition table terminates the standard sequence search. It is possible to enter several times the same code. The Automatic Standard Recognition table and its default values are presented in Table 7.

Table 7: Automatic Standard Recognition Table

Standard Entries	Code (Default values)	Register
Standard 1	000	DDECCONT4[5:0]
Standard 2	001	
Standard 3	010	DDECCONT3[5:0]
Standard 4	111	
Standard 5	001	DDECCONT2[5:0]
Standard 6	001	
Standard 7	111	DDECCONT1[5:0]
Standard 8	111	

If the default values are used, code 111 (no standard) is the fourth entry and the standard identification will be restricted to the first three standards (in order PAL BGDHI, SECAM and NTSC M).

Each standard recognition trial period lasts 2 fields. All trials corresponding to table entries are performed. The identification decision is based on the results of the trials and a single table entry should be identified. If two entries are identified by error, the standard recognition sequence will re-start from the beginning of the table and no standard will be identified.

The DDECCONT4[5:0], DDECCONT3[5:0], DDECCONT2[5:0], and DDECCONT1[5:0] registers are used to program the Automatic Standard Recognition table.

After the sequence search, a second step (also called a confirmation step) is performed by the algorithm. It is performed on the single identified Automatic Standard Recognition table entry. It is possible to program the number of fields where the standard identification must be confirmed before the status flags are modified. The confirmation code is described in Table 8.

Table 8: Confirmation Codes

Confirmation Code	Number of Successive Fields with Correct Identification
000	1
001	3 (Default)
010	7
011	10

The confirmation code is programmed in the STI_NB_FIELDS_CONFIRM[2:0] bits of the DDECCONT17 register.

After the confirmation step has been successful, the standard is considered as identified. The TVSTID flag is set in the DDECSTAT2 register and the code of the identified standard is set in the TVSTD[2:0] bits of the DDECSTAT2 register.

4.6 Standard Identification

The input signal standard is automatically recognized using a proprietary ST patented algorithm. It avoids false identification and ensures a good recognition of the color standard, even in bad signal conditions.

4.7 Chroma Demodulation

4.7.1 General Description

The Chroma PLL and the Input SRC are the main hardware blocks involved in chroma demodulation. The Chroma PLL is locked to the input video burst signal in frequency and phase. Demodulation is performed on the chroma samples positioned in the virtual 4 x f_{SC} clock domain.

Dedicated demodulation hardware is used for SECAM demodulation (frequency modulated signals). Demodulated chroma components are low pass filtered and matrixed into Cr and Cb components.

The Chroma Demodulator also includes an Automatic Chroma Control (ACC) which rescales the chroma components from -20 dB to +6 dB. The color is killed (output Cr Cb components to 80h value) until the standard is identified. ACC is disabled (fixed gain) in SECAM standard.

If NTSC M or NTSC 4.43 standards are identified, the Chroma Demodulator also incorporates a Hue Control mechanism and a Flesh Tone Correction mechanism. The Hue Control is a programmable fixed offset in the demodulation angle and is only operational in the active line.

The Flesh Tone Correction mechanism operates with a programmable reference axis. It performs an on-the-fly change of demodulation axis for any color with a phase of approximately ± 39.4° around the reference axis. It is only operational in the active video line.

Flesh Tone Correction (cφ) is up to a maximum of ±10°.

Cr and Cb amplitudes can be adjusted separately. (See Section 4.12.1 .)

4.7.2 Programming

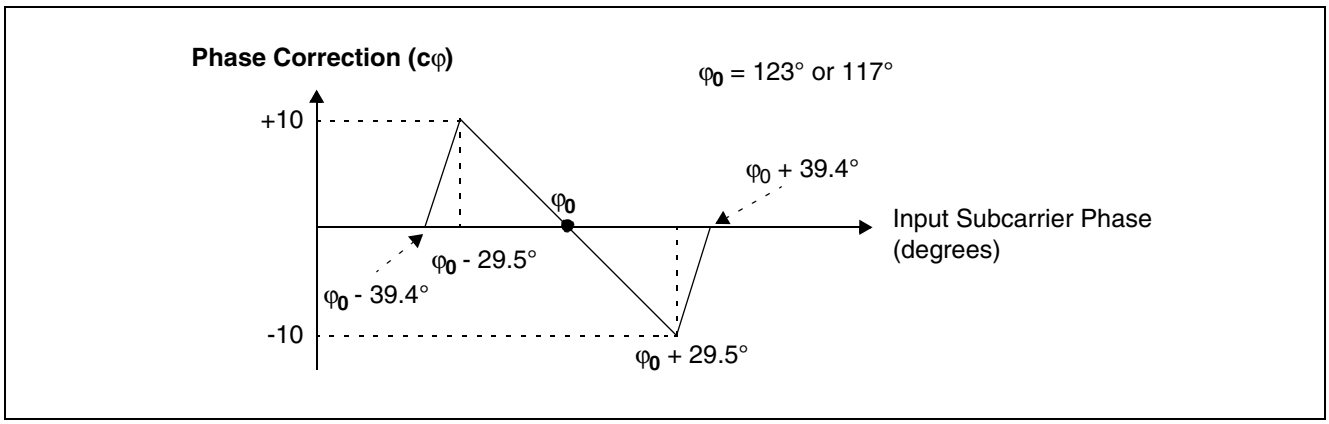
For NTSC standards, there are several ways to improve the video input. The hue value is controlled by the HUECTRL[5:0] bits in the DDECCONT2 register. The hue control value is defined in 63 steps of approximately 1.4 degrees each, which provide an offset between -45.0° and +43.6°. When 00000, the hue angle is 0, otherwise the value of the hue angle is coded in 2's complement.

An Automatic Flesh Control is also available with the STV2310. This mode is enabled by setting the FLESH_EN bit in the DDECCONT10 register. For the Automatic Flesh Control Phase Shift selection, the Flesh Tone Reference Angle in the [B-Y, R-Y] axis system is either 123° or 117°. This value is selected in the FLESHPH_SEL bit of the DDECCONT10 register.

The Color Kil control mode can be automatic, depending on the standard identification, or forced On or Off by the DEM_CKILL_CTRL[1:0] bits in the DDECCONTD register. In PAL/NTSC mode, it can also depend on burst amplitude by setting the in the DDECCONTF register.

A pedestal can be removed from the luminance input signal by the video standard using the PEDESTAL_REMOVE bit in the DDECCONT2 register.

Figure 13: Phase Correction when Automatic Flesh Control Enabled



4.8 Soft Mixer

4.8.1 General Description

The Soft Mixer is used to mix the Y, Cr and Cb data flows (respectively) from the CVBS source and the RGB Insertion block. The mixing of the data flows is controlled by Fast Blanking mode. A forced CVBS or RGB flow mode can also be programmed. In this case, the mixer acts as a multiplexer. A static mixing (also called alpha blending) mode is also programmable.

When the normal mixing mode is programmed, the CVBS and RGB flows are blending according to the Fast Blanking (FB) signal. The FB signal is sampled with subpixel accuracy to ensure correct mixing. The mixing slope between flows is programmable.

4.8.2 Programming

Fast Blanking mode is selected by the FBLANKMODE[2:0] bits in the DDECCONT5 register.

Table 9: Fast Blanking Modes

Bit Value	Mixing Mode	Description
00x	Normal Mixing mode	FB active during active line. Soft Mixing between 0 and 1. (Default mode)
01x	Dynamic Mixer mode	FB active and Soft Mixing from 0 to MIXSLOPE[7:0]
100	Static Mixer or Alpha Blending 1 mode	FB inactive. Y_{OUT} = alpha x Y_{CVBS} + (1-alpha) x Y_{RGB} with alpha = MIXSLOPE[7:0] (same for Cr and Cb signals)
101	Static Mixer or Alpha Blending 2 mode	FB inactive. Y_{OUT} = alpha x Y_{RGB} + (1- alpha) x Y_{CVBS} with alpha = MIXSLOPE[7:0] (same for Cr and Cb signals)
110	Forced CVBS mode	FB inactive. Y_{OUT} = Y_{CVBS} (same for Cr and Cb signals)
111	Forced RGB mode	FB inactive. Y_{OUT} = Y_{RGB} (same for Cr and Cb signals)

Note: The FBLANKMODE value is only applied when the STV2310 is not in Analog YCrCb mode

The soft mixing slope or the Alpha Blending value, depending on the Fast Blanking mode, is set in the MIX_SLOPE[7:0] bits in the DDECCONT6 register. When the blanking mode is in Forced RGB or Forced CVBS mode, this value is ignored.

When one of the Alpha Blending modes is used for mixing, the alpha value is set in the MIX_SLOPE[7:0] bits.

When the STV2310 is in normal RGB and CVBS mixing mode, the MIX_SLOPE[3:0] bits indicate the mixing slope (duration of mixing). The MIX_SLOPE[7:4] bits must be set to 0000. The MIX_SLOPE[3:0] bits code the soft mixing slope from 0000 to 1111, with 0000 corresponding to a slope of 1 clock cycle (virtual 4 x f_{SC} clock domain) and 1111 corresponding to a transition from one signal to the other spanned on 16 clock cycles.

4.9 Output Scaler and Format Converter

4.9.1 General Description

An Output Sample Rate Converter (OSRC) is used to transpose the subcarrier locked virtual clock domain to the output sample rate domain. This converter is used to provide a fixed number of pixels per active line (i.e. 720 for ITU-R BT.601 format) independently of the input video standard and line length.

- Upsampling is required for zoom-in functions.
- Downsampling is required for zoom-out functions.

The Output Sample Rate Converter compensates for line length variations. At this level, a skew correction is applied on each pixel in order to compensate for the shift of the asynchronous acquisition with respect to the current line horizontal sync pulse. New sample rate and skew correction factors are computed at every line, taking into account the line length variation.

The Output Sample Rate Converter is also used to perform an horizontal format conversion to support zoom in/out functions. For linear scaling, the scaling factor can be programmed in linear steps from 0.25 to 4. Non-linear scaling is also available for Panorama mode. Region borders are fully programmable as well as the associated scaling factors (in the 0.25 to 4 range).

At the sample rate converter output, an active line is transposed into a fixed number of skew corrected pixels, according to the selected output format (ITU-R BT.601 or square pixel). This is used for the orthogonal display or field storage for the field-rate up-conversion, using an external up-converter.

4.9.1.1 Square Pixel Mode

When a standard TV screen is used to display computer-generated images, Square Pixel mode is required to ensure the correct aspect ratio in relation to the required sampling frequency of the TV display format.

Table 10: TV Display Formats

Luma Sampling Frequency	Format	Pixels/Line
13.5 MHz	ITU-R BT.601 (NTSC/PAL)	720
12.27 MHz	NTSC Square Pixel	640
14.75 MHz	PAL Square Pixel	768

The output formatting can be performed with Normal or Square Pixel modes. For Square Pixel mode, the number of required samples per line depends on the input standard.

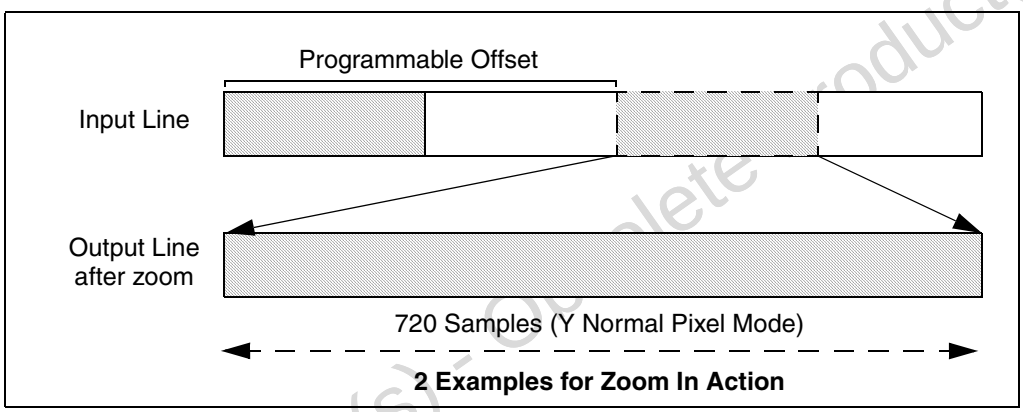
Table 11: Required Samples per Line for Square Pixel Mode

Standard	Samples per Line		
	Y SIgnal	Cr Signal	Cb Signal
625 Lines/50 Hz	768	384	384
525 Lines/60 Hz	640	320	320

4.9.1.2 Zoom-In Mode

In Zoom-In mode, a portion of the TV scan line is expanded to take all the available output samples for that line.The zoom-in factor ranges from 1 (no zoom) to 4 (large zoom). The Zoom-In mode start position is programmable.

Figure 14: Zoom-In Mode

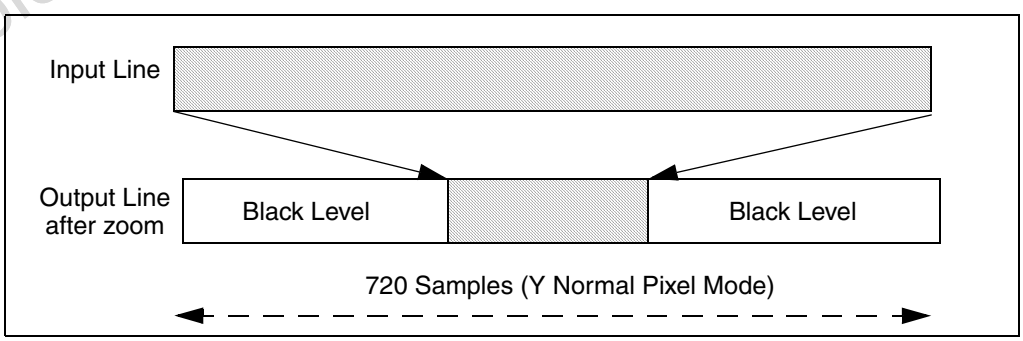


2 Examples for Zoom In Action

4.9.1.3 Zoom-Out Mode

In Zoom-Out mode, the entire input TV scan line is compressed to take only a part of the output line. The active samples are positionned in the center of the output line and the rest of the line is blacked out. The zoom-out factor ranges from 0.25 (large zoom) to 1 (no zoom).

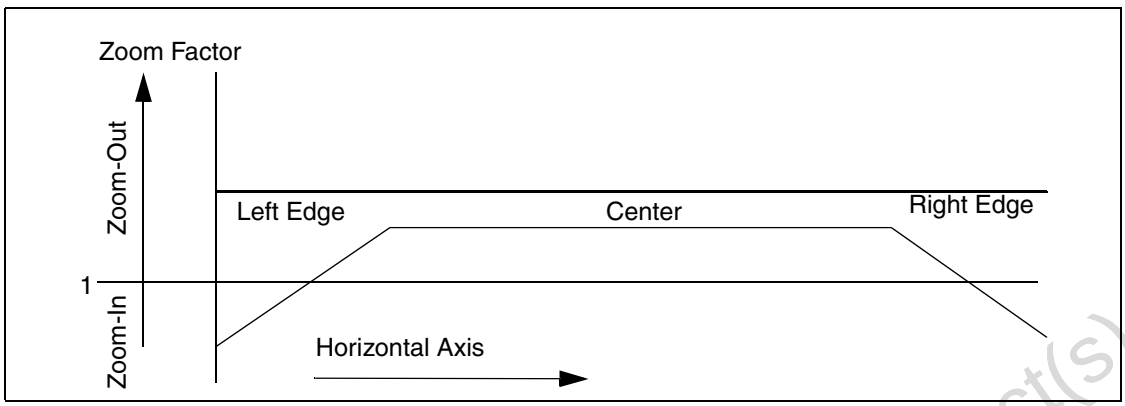
Figure 15: Zoom-Out Mode



4.9.1.4 Panorama Mode (Non-Linear Scaling)

To better display wider TV screen aspect ratios, Panorama mode applies a different zoom factor to the center of the image in relation to the edges; i.e. a Non-Linear Scaling mode must be implemented. This implies that the compression/expansion factor will vary on the edges and remain stable at the center. Note in Figure 16 that the resulting TV image is symetrical (right and left edges are equal).

Figure 16: Non-Linear Scaling



4.9.2 Programming

4.9.2.1 Square Pixel Mode

Square Pixel mode is enabled by setting the PIXMODE bit in the DDECCONT0 register.

4.9.2.2 Zoom-In Mode

To enable Zoom-In mode, the ZOOMIN_EN bit in the DDECCONTB register must be set.

The zoom-in value must be between 256 and 1023. A value of 512 will zoom-in the picture by a factor of 2.0; i.e. pixels are twice as large. The zoom-in factor is programmed in the ZOOMIN_FACT[9:0] bits in the DDECCONT6 and DDECCONTB registers. The default value is 256 (No Zoom).

The position where the zoom-in operation starts is programmed in the ZOOMIN_OFFSET[9:0] bits in the DDECCONTA and DDECCONTB registers. If the value is 0, the zoom-in starts at the beginning of the TV scan line (first left pixel). The number of pixels per line is based on the vertical frequency and the pixel mode. For more information, refer to Table 10. The default value is 0; i.e. the first left pixel of the active line is the first pixel of zoom.

4.9.2.3 Zoom-Out Mode

To enable Zoom-Out mode, the ZOOMOUT_EN bit in the DDECCONTB register must be set.

The zoom-out value must be between 256 and 1023. A value of 512 will zoom-out the picture by a factor of 0.5; i.e. pixels are twice as small. The zoom-out factor is programmed in the ZOOMOUT_FACT[9:0] bits in the DDECCONT9 and DDECCONTB registers.

4.9.2.4 Panorama Mode

Panorama mode is enabled when both the ZOOMIN_EN bit in the DDECCONTB register and the ZOOMOUT_EN bit in the DDECCONTB register are set to 1.

In Panorama mode, the ZOOMIN_FACT, the ZOOMOUT_FACT and the ZOOMIN_OFFSET values are used (see Figure 16).

- The ZOOMIN_FACT bits determine the zoom-in factor at the left and right edges of the picture
- The ZOOMOUT_FACT bits determine the zoom-out factor at the center of the picture
- The ZOOMIN_OFFSET bits determine the border width where the zoom factor increases from the zoom-in factor to the zoom-out factor, starting from the left edge (resp. the border width finishing on the right edge where the zoom factor decreases from the zoom-out factor to the zoom-in factor)

For correct programming the following formula must be checked:

Zt x (Zout - Zin) = N x (Zout -1)

where Zin = ZOOMIN_FACT ; Zout = ZOOMOUT_FACT ; Zt = ZOOMIN_OFFSET ; N number of Y pixels per line (720 in Normal Pixel mode, 640 or 768 in Square Pixel mode).

4.10 RGB Insertion

4.10.1 General Description

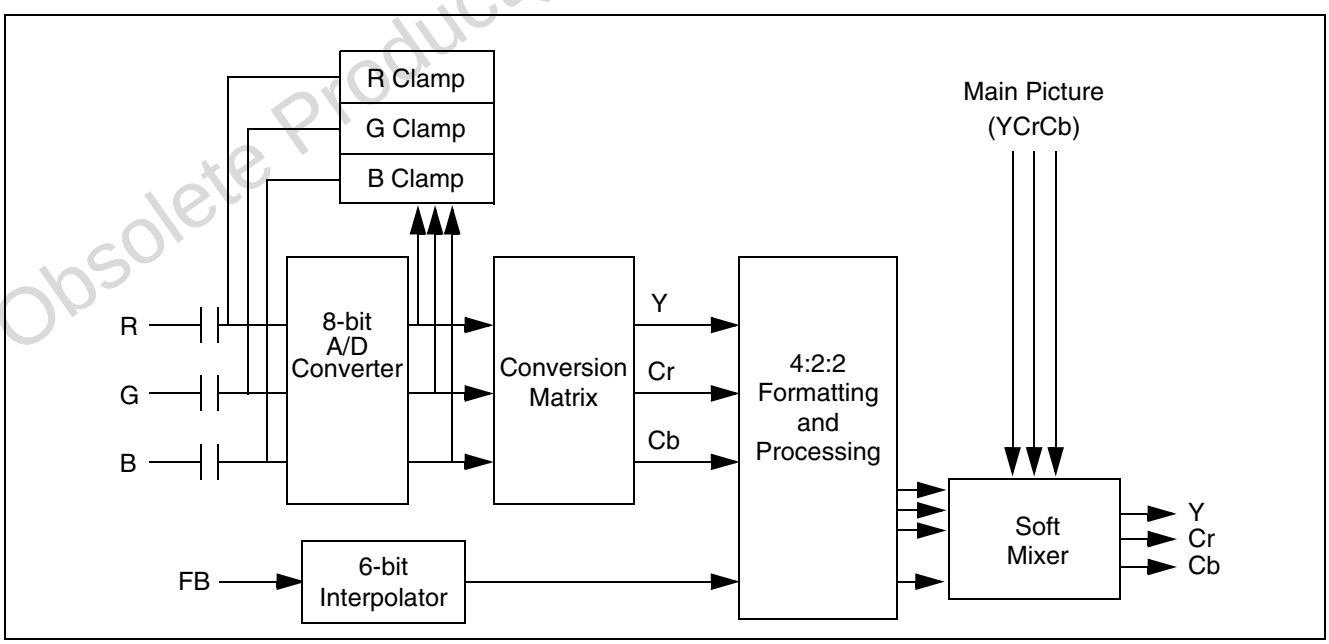
The RGB signals are captured by three 8-bit A/D converters and should be synchronous to the selected CVBS or Y/C sources. The RGB signals are also adjusted in the analog domain by clamp circuits used for sourcing and sinking charges on the front end capacitor.

A digital adjustable gain can be applied to the RGB data flow, in order to adapt to the CVBS dynamic range.

The RGB signals are YCrCb formatted and mixed with the YCrCb signals from the main picture. Soft mixing is driven by the FB signal. The rising and falling edges of the FB signal are measured with subpixel accuracy to perform correct insertion. (For more information, refer to Section 4.8: Soft Mixer on page 24).

The RGB insertion block also provides a Cr Cb overload mechanism. This mechanism is used to avoid clipping YCrCb signals (i.e when the input RGB signals are too large). The Cr Cb overload mechanism measures the chroma signal during the video line in order to compute the correcting scale factor.

Figure 17: RGB Capture and Mixing with Main Picture



4.10.2 Programming

To enable the CrCb overload mechanism, set the CRCBOVER_EN bit in the DDECCONTB register. The automatic gain for the RGB is set in the DDECCONT35 register.

4.11 Analog YCrCb Mode

4.11.1 General Description

The STV2310 can be programmed in Analog YCrCb mode. This mode has specific input connections:

- the Y analog input signal must be connected to the CVBS1_Y (or CVBS2_Y) pin
- the Cr and Cb analog input signals must be connected to the R_CR and B_CB input pins (respectively).

A ±20 degree Tint Control mechanism is available to compensate for incorrect hue levels on the input signals. When the Analog YCrCb mode is programmed, the various clamp circuits are modified accordingly.

Note: The Fast Blanking (FB) signal is not relevant in Analog YCrCb mode. This mode is a full-page display mode.

4.11.2 Programming

The YCrCb Tint Angle Correction values are programmed in the TINTANGLE[4:0] bits in the DDECCONT12 register. The tint angle is coded from -20° to +20° in steps of 1.33°. These bits are coded in 2's complement. The default value is 0 (no correction).

4.12 Output FIFO and Line-locked Ouput Pixel Clock Generator

4.12.1 General Description

The Output FIFO and Line-Locked Output Pixel Clock Generator block has two functions:

1 Handle the active line data received from the Output Scaler and Format Converter and the ancillary data from the VBI slicer.

The active video line data is provided on 3 buses: Y, Cr and Cb. The output flow is on 8 bit and multiplexes the Y, Cr and Cb flows. Before being multiplexed, a programmable attenuation can be applied to the Cr, Cb data. For every output line, digital preambles for synchronization and ancillary data (when available) are inserted in the output flow in compliance with standard ITU-R BT 656.

2 Generate the Output Pixel Clock and associated signals.

A line-locked output pixel clock is generated. This output clock is a multiple of the input line frequency. There are 4 possible multiples:

- 1716 or 1728 in Normal Pixel mode,
- 1560 or 1888 in Square Pixel mode.

When there is no input signal, the output data can be blanked in option.

When required the STV2310 is able to enlarge the vertical blanking area. On the other hand it is possible to disable the blanking mode during the VBI, using the "pass through" mode. (The "pass through" mode must not be selected when the TXT VBI slice is used).

4.12.2 Output Data

There are 4 data output standards which are a combination of 525/625 input standards and Normal/ Square pixel format. There are four possible multiples:

- 1716 or 1728 in Normal Pixel mode,
- 1560 or 1888 in Square Pixel mode.

For each output standard, the blanking code (Cb = 80h, Y = 10h, Cr = 80h, Y = 10h...) is used in the active line section during the Vertical Blanking Interval (VBI). (See Figure 18.)

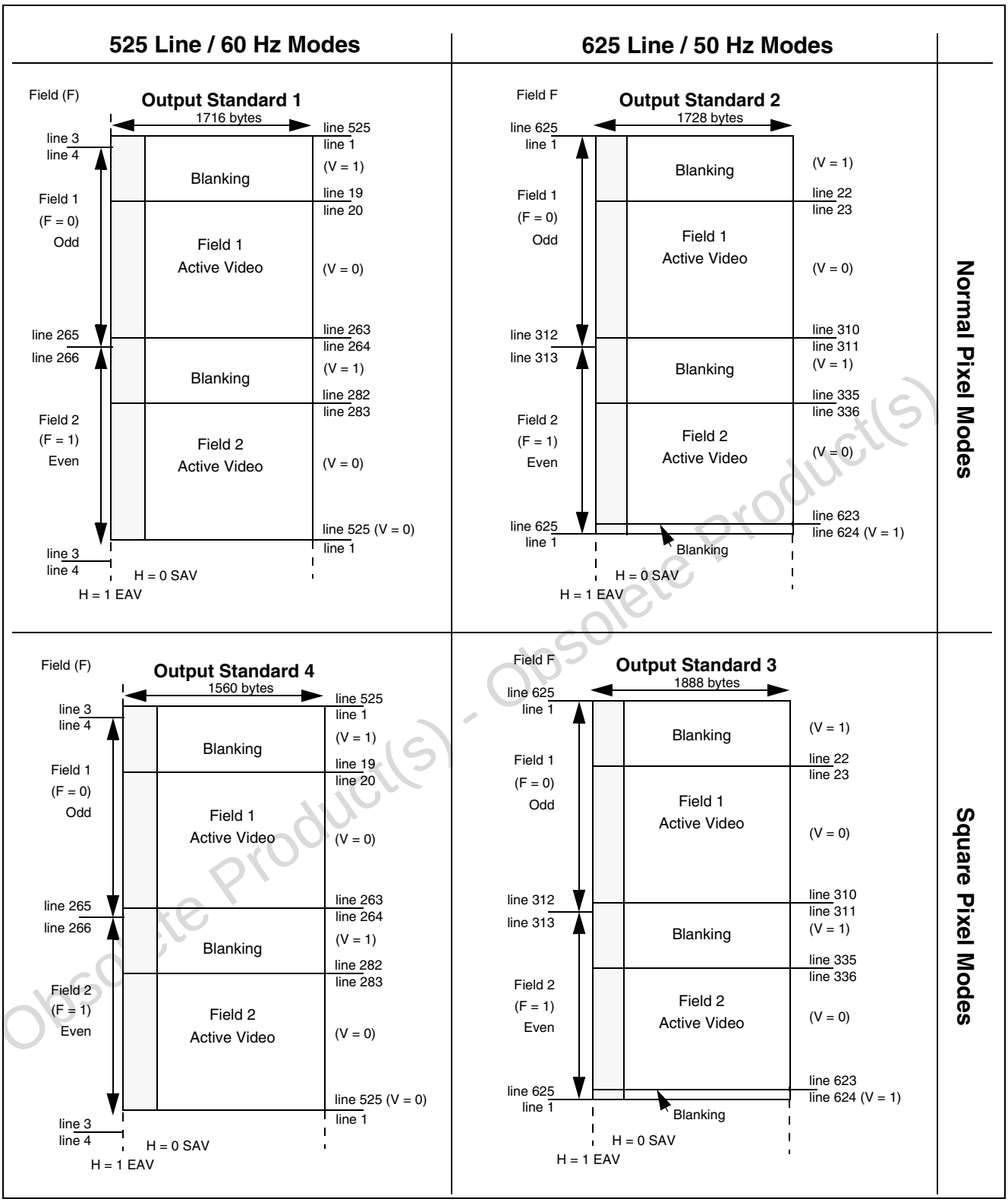
Table 12: Frame Output Standards

	Output Standard 1	Output Standard 2	Output Standard 3	Output Standard 4
Input Standard	525/60 Hz	625/50 Hz	625/50 Hz	525/60 Hz
Pixel Format	Normal	Normal	Square	Square
Blanking (bytes)	268 + 8	280 + 8	344 + 8	272 + 8
Active Video (bytes)	1440	1440	1536	1280
Vertical Blanking Interval[1]	Lines 1 to 19 Lines 264 to 282	Lines 1 to 22 Lines 311 to 335 Lines 624 and 625	Lines 1 to 22 Lines 311 to 335 Lines 624 and 625	Lines 1 to 19 Lines 264 to 282
Vsync SIgnal	Synchronized with the output pixel clock. See below.			
Hsync Signal	Synchronized with the output pixel clock.			
Field Signal	Synchronized with the Hsync signal output pixel clock.			

1. Lines are numbered in compliance with specification ITU-R BT470.

4.12.2.1 Vsync Output Pin Modes

Figure 18: Frame Output Standards



For all output standards, the Vsync output signal changes twice per frame. The Vsync signal (pin 34) can be generated at the output in one of two modes:

1 "Digital" Vsync mode: The VSYNC signal always changes at the beginning of the line, depending on the output standard.

2 "Analog" Vsync mode: The VSYNC signal changes either at the beginning or the middle of the line, depending on the analog input signal.

- ➢ for Output Standard 1: Start of line 4 and middle of line 266
- ➢ for Output Standard 2: Start of line 1 and middle of line 313
- ➢ for Output Standard 3: Start of line 1 and middle of line 313 (same as standard 2)
- ➢ for Output Standard 4: Start of line 4 and middle of line 266

Note that the output standard depends on the input TV standard and the programmable Normal Pixel or Square Pixel mode.

The VSYNC output mode is selected by the VSYNCTYPE bit in the DDECCONT0 register.

The V bit of the output flow always changes at the beginning of the line (in compliance with standard ITU-R BT 656).

Non-Interlaced mode: When required, the STV2310 is able to interlace the output, even if the source is non-interlaced (by default, the output Vsync follows the input Vsync).

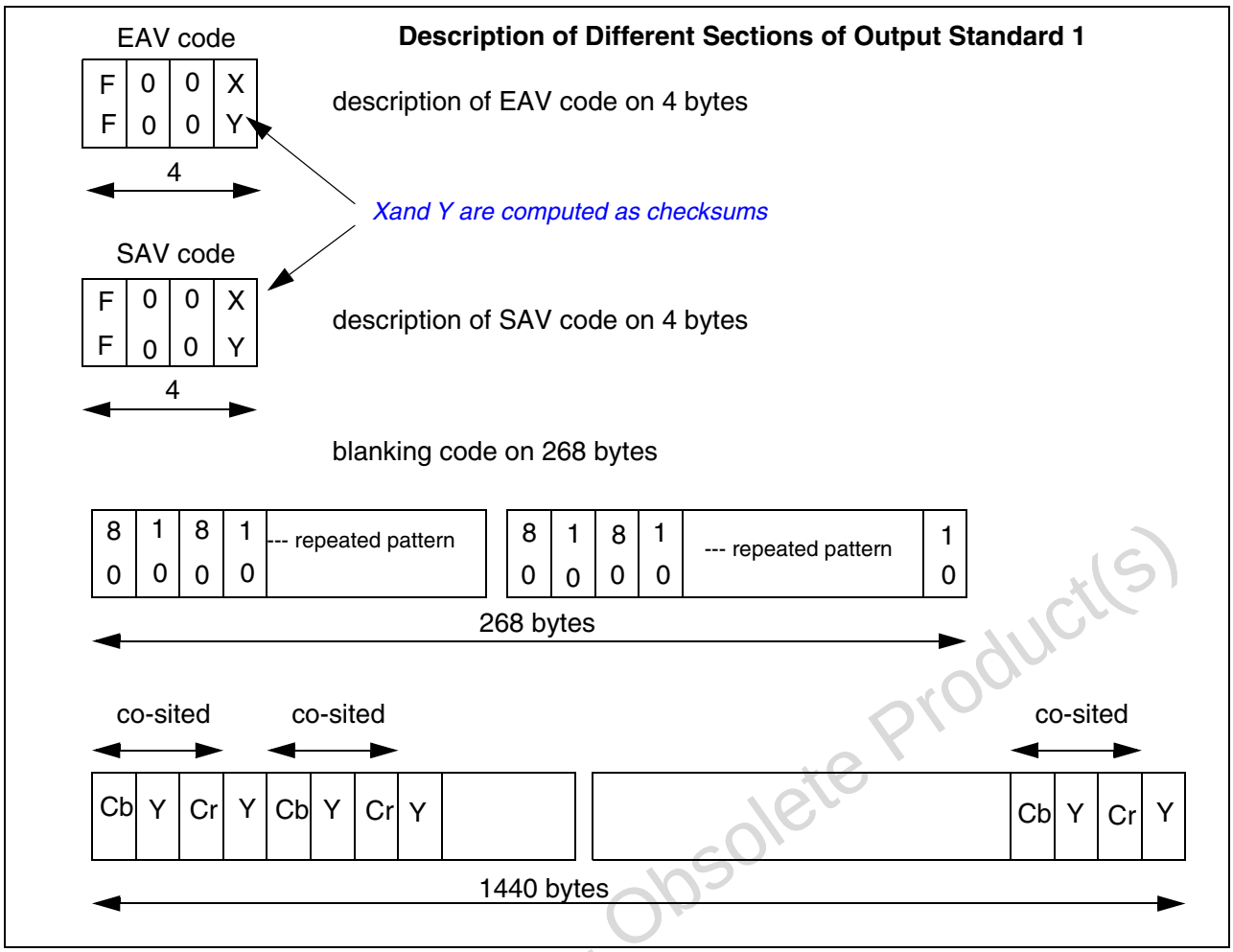
4.12.2.2 Hsync Output Pin Mode

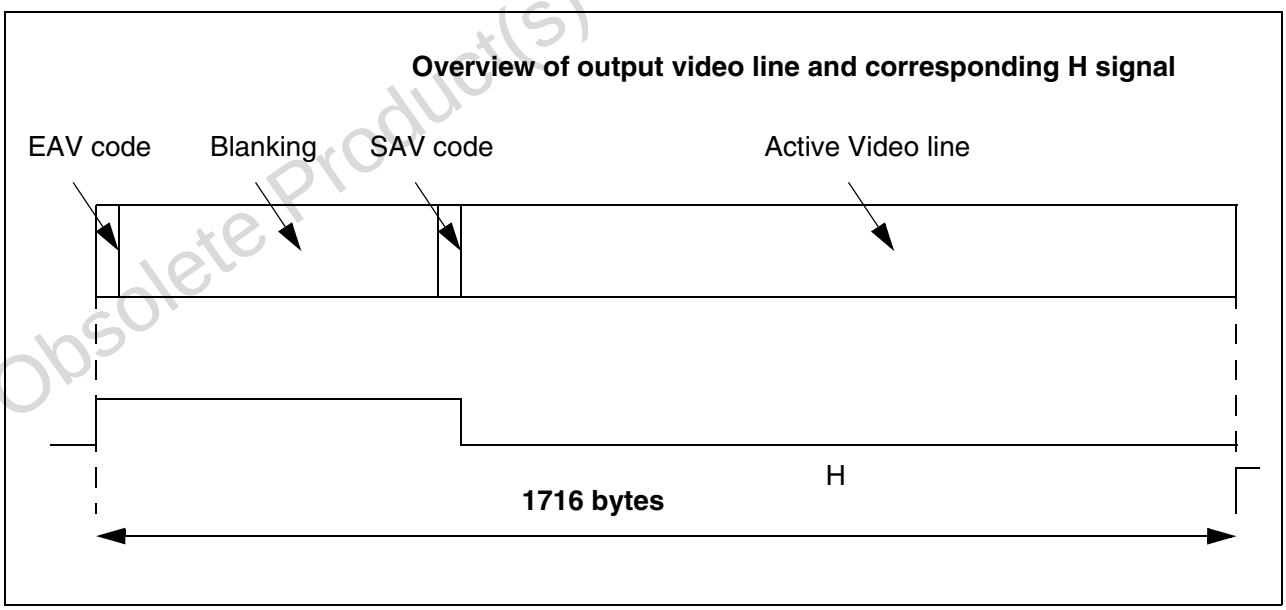
The Hsync output pulse can shifted, this is in comparision with the embedded Hsync pulse.

4.12.2.3 FIELD Output Pin Mode

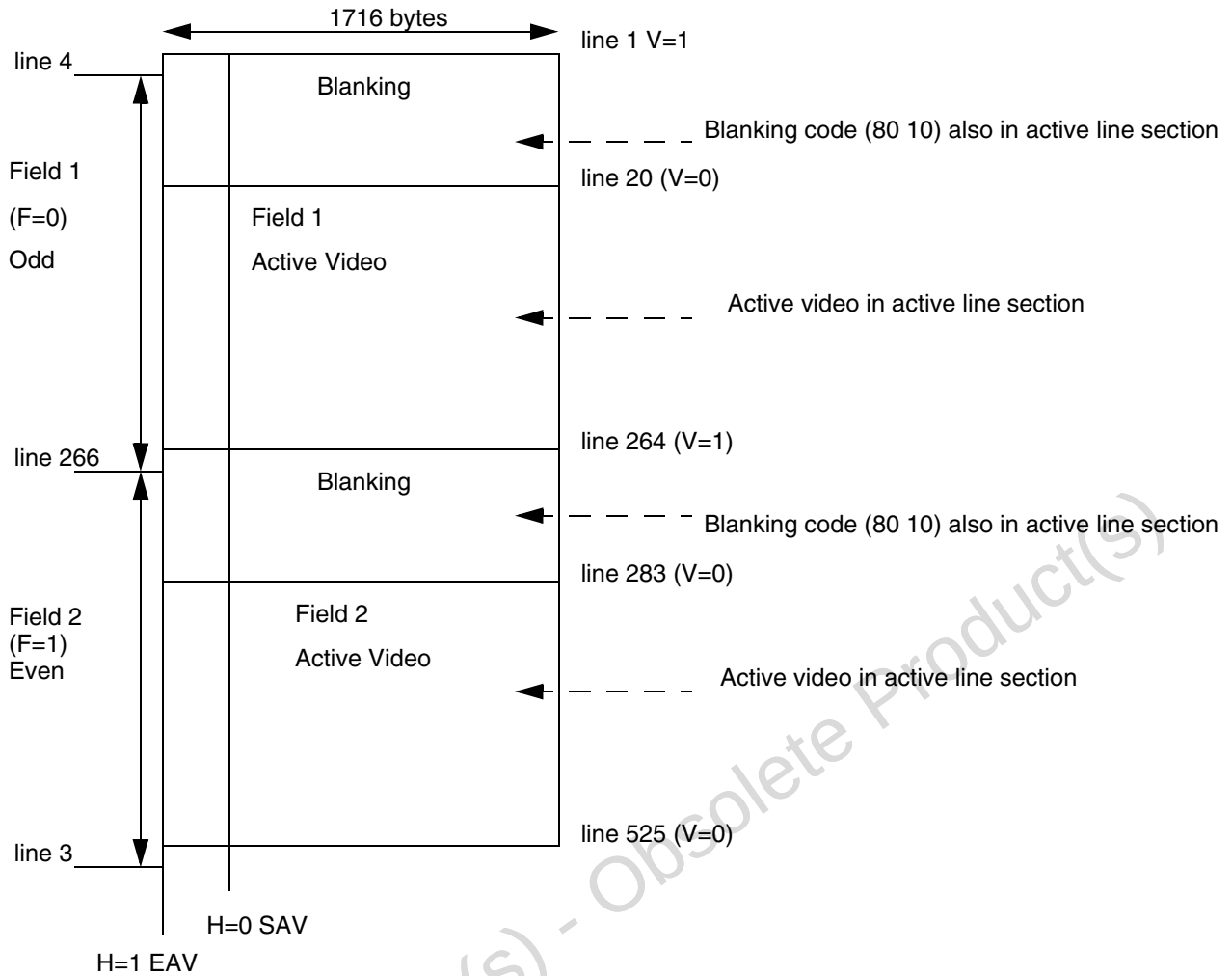
The FIELD output pulse represents the parity of the field and toggles either with the embedded FIELD pulse, or is synchronous with the Vsync pin, when set in analog interlaced mode. To toggle in analog interlaced mode, the direct parity mode must be selected.

4.12.2.4 Output Standard 1 : Normal Pixel mode / 525 lines / 60 Hz (NTSC)





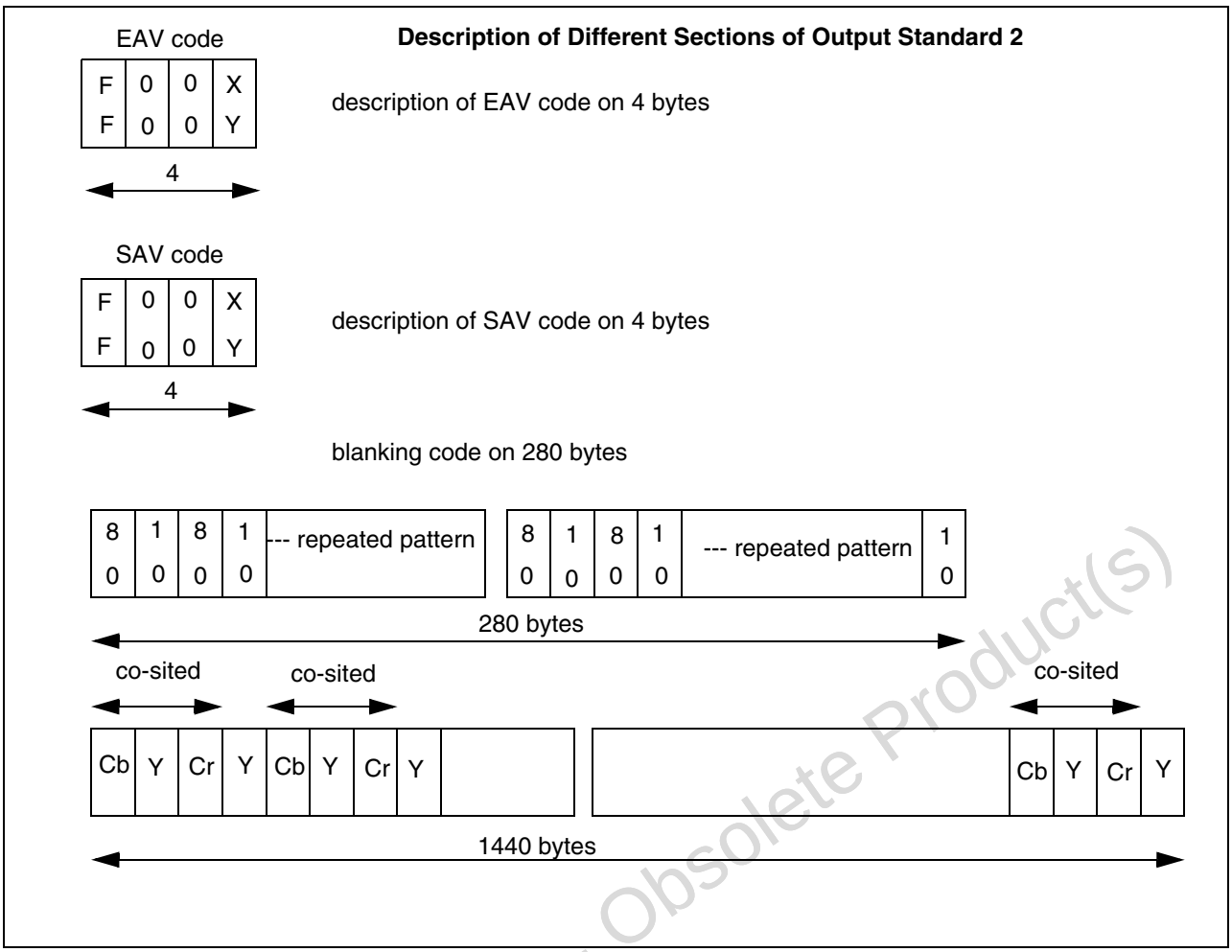
Digital Output Frame Overview for Output Standard 1

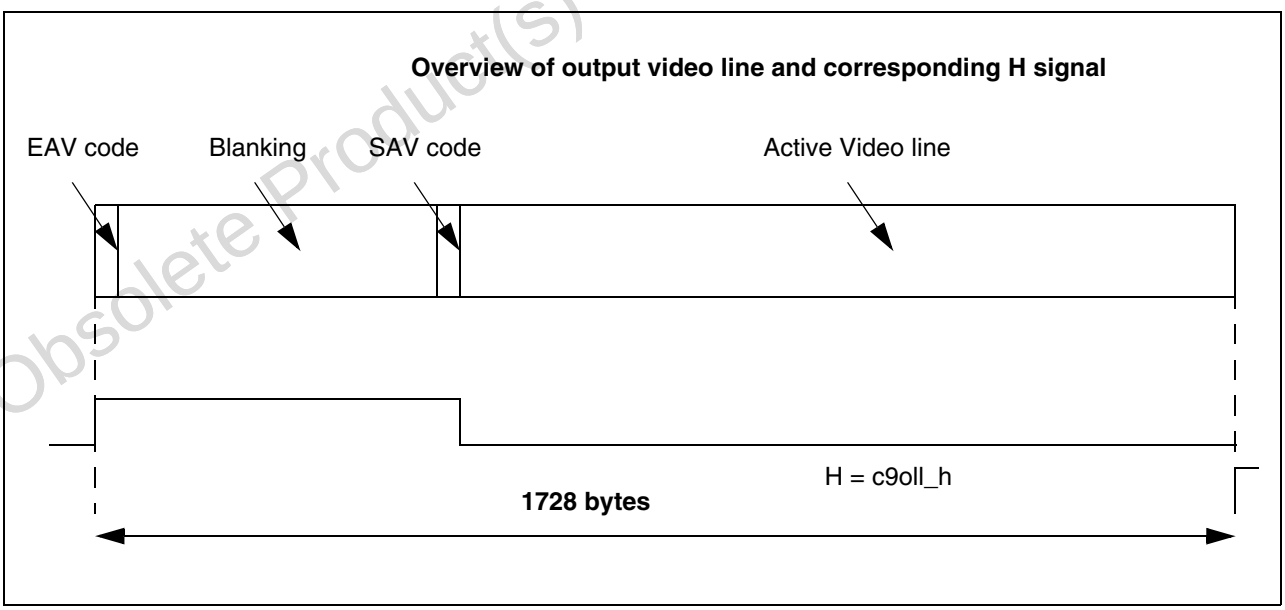


Note that the vertical blanking interval has been extended from line 1 to line 19 included (transition from Field 2 to Field 1 of next Frame) and from line 264 to line 282 included (transition from Field 1 to Field 2)
This encompasses the optional blanking lines described in the standard (lines 11 to 19 included and lines 273 to 282 included respectively)

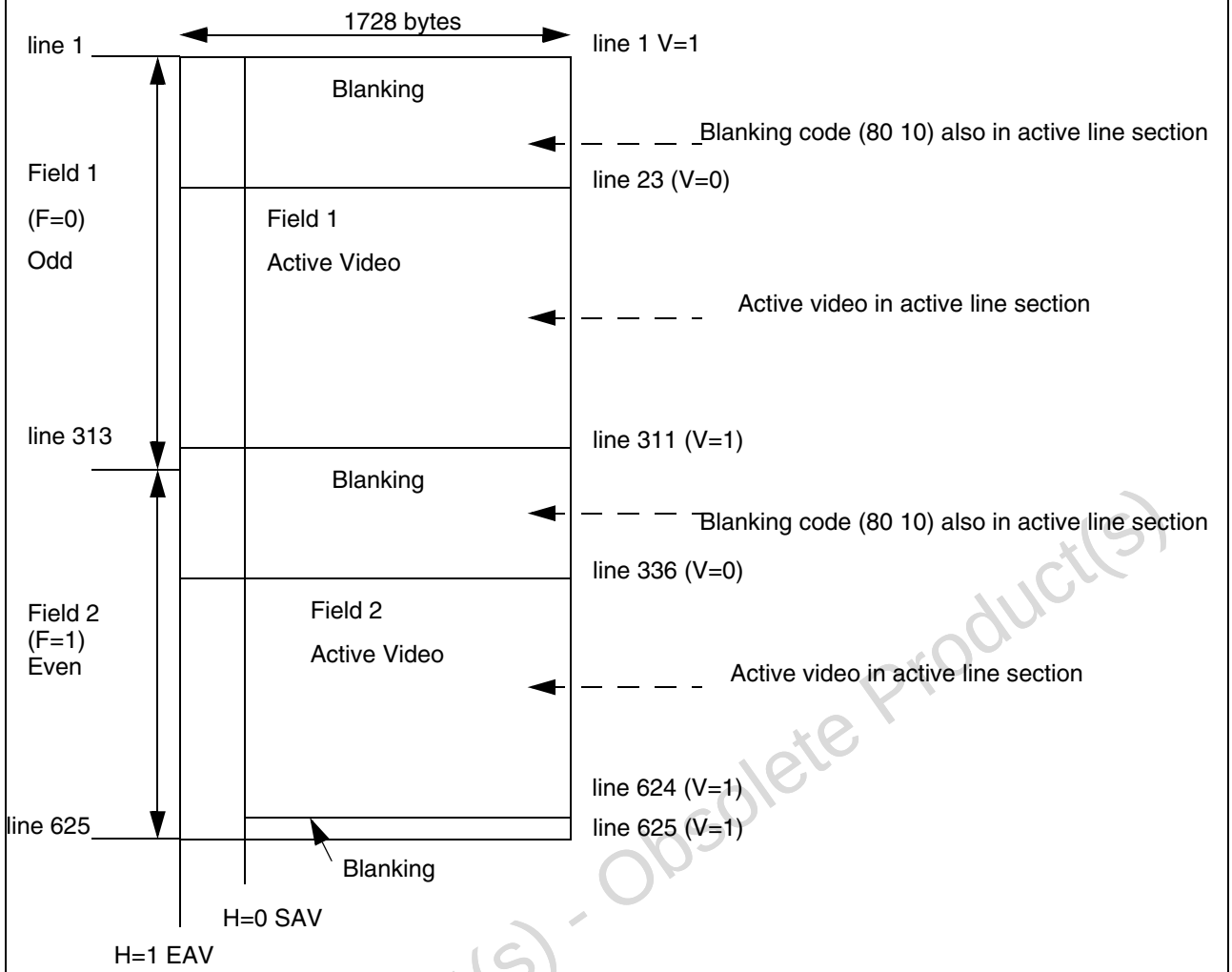
The V and H signals change synchronously with the output pixel clock.
The F signal change synchronously with the H signal and the output pixel clock.
The V signal changes twice during one frame:
- either at the start of line 1 and at the start of line 264 (“digital Vsync mode”)
- or at the start of line 1 and in the middle of line 263 (“analog Vsync mode”)

4.12.2.5 Output Standard 2: Normal Pixel / 625 lines / 50 Hz (PAL & SECAM)





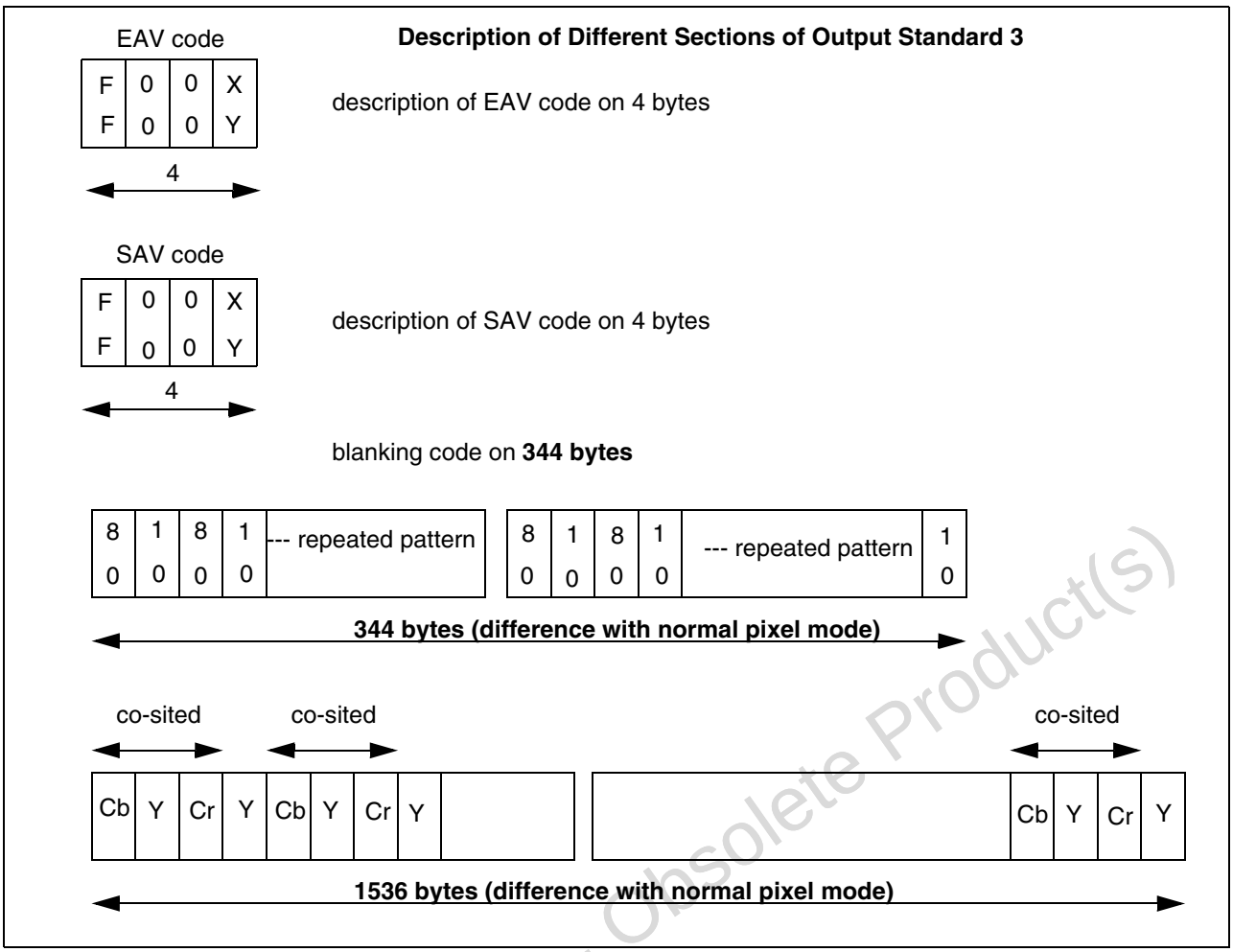
Digital Output Frame Overview for Output Standard 2

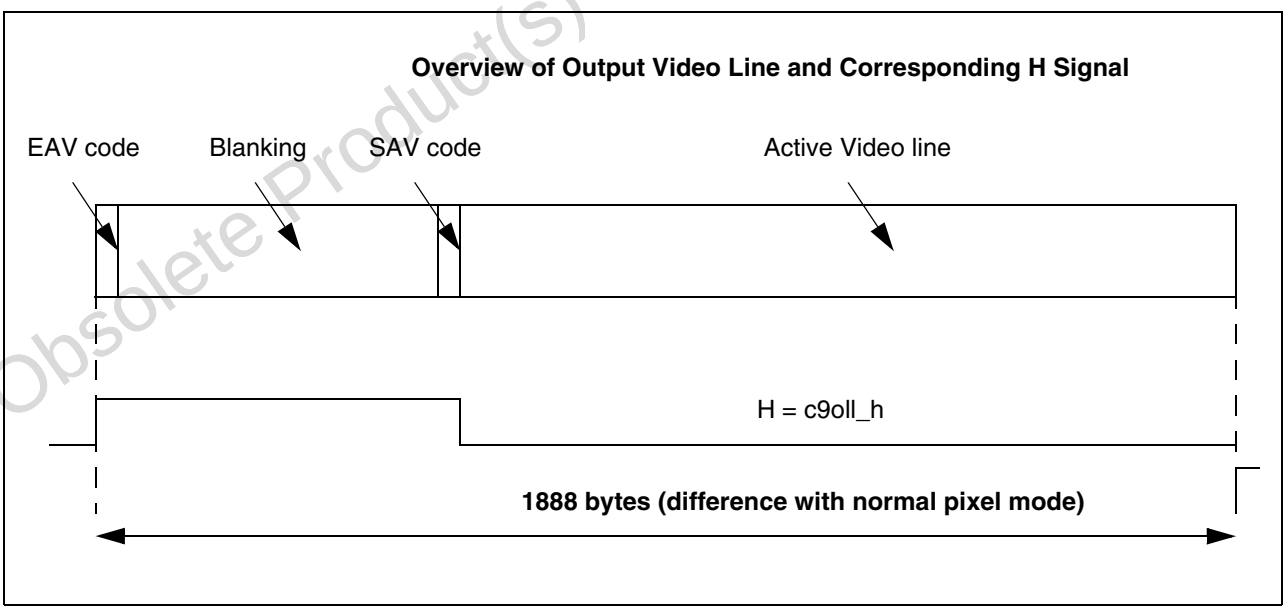


Note that the vertical blanking interval has been extended from line 1 to line 22 included (transition from Field 2 to Field 1 of next Frame) and from line 311 to line 335 included (transition from Field 1 to Field 2)

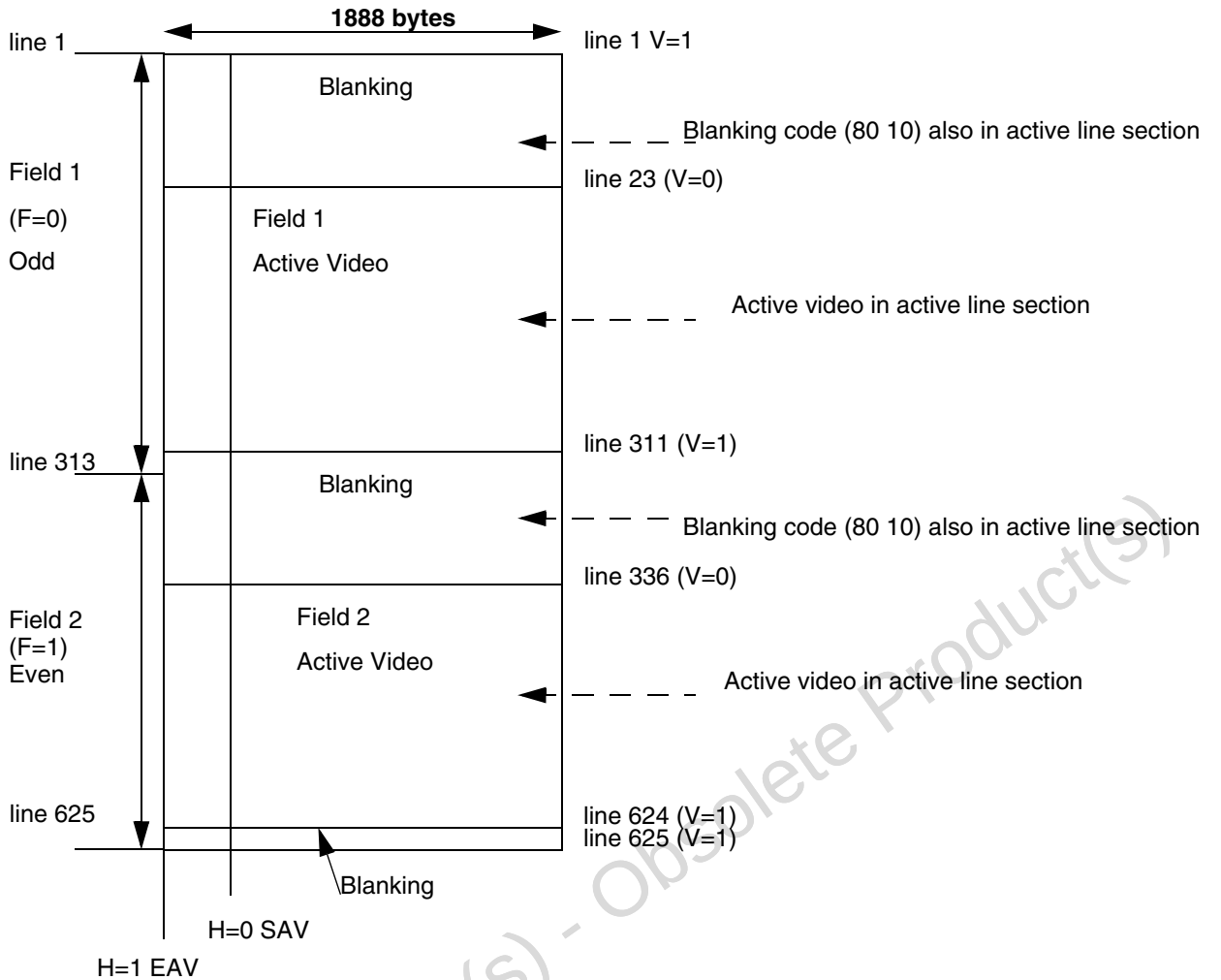
The V and H signals change synchronously with the output pixel clock.
The F signal is given as an indication. It is not output

4.12.2.6 Output Standard 3: square pixel / 625 lines / 50Hz (PAL SECAM)





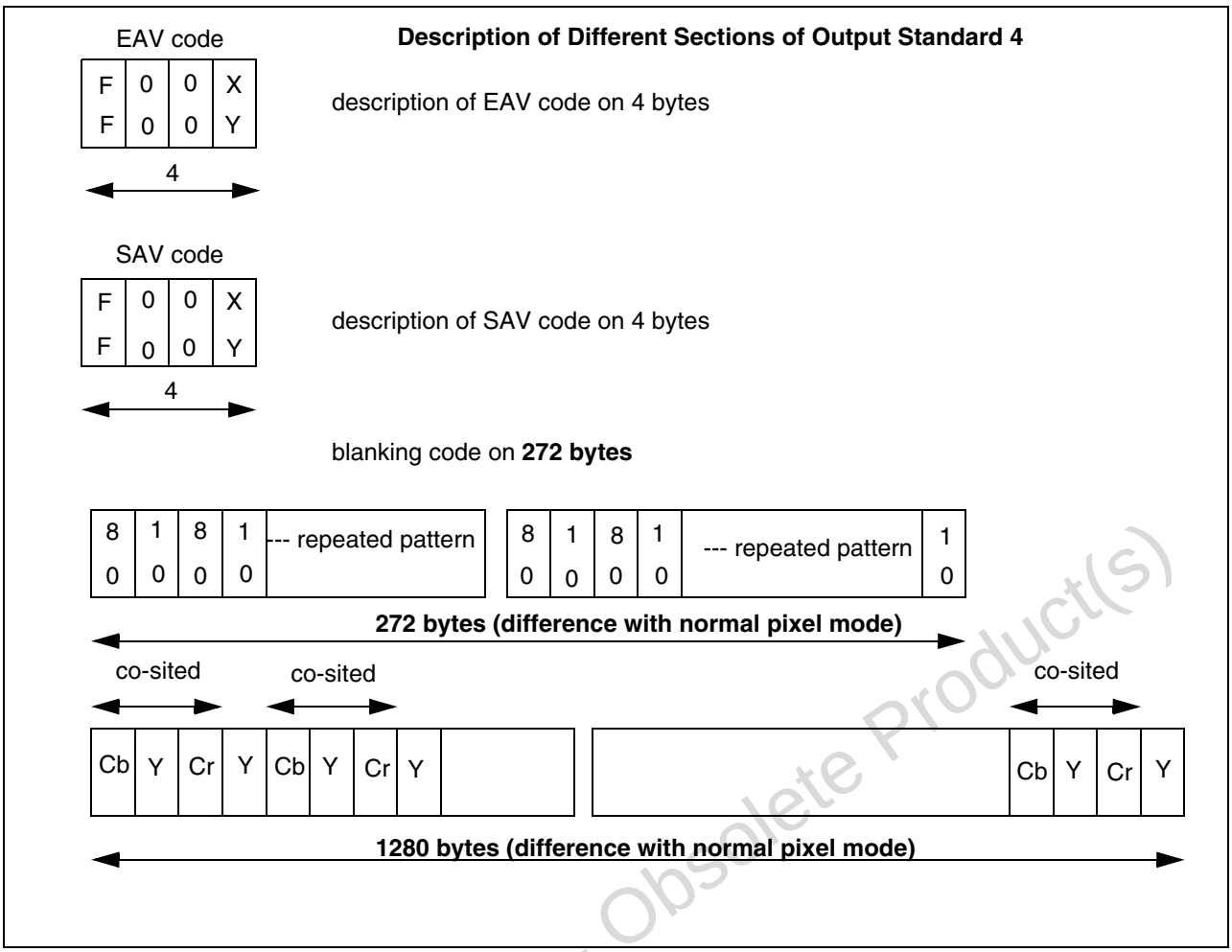
Digital Output Frame Overview for Output Standard 3

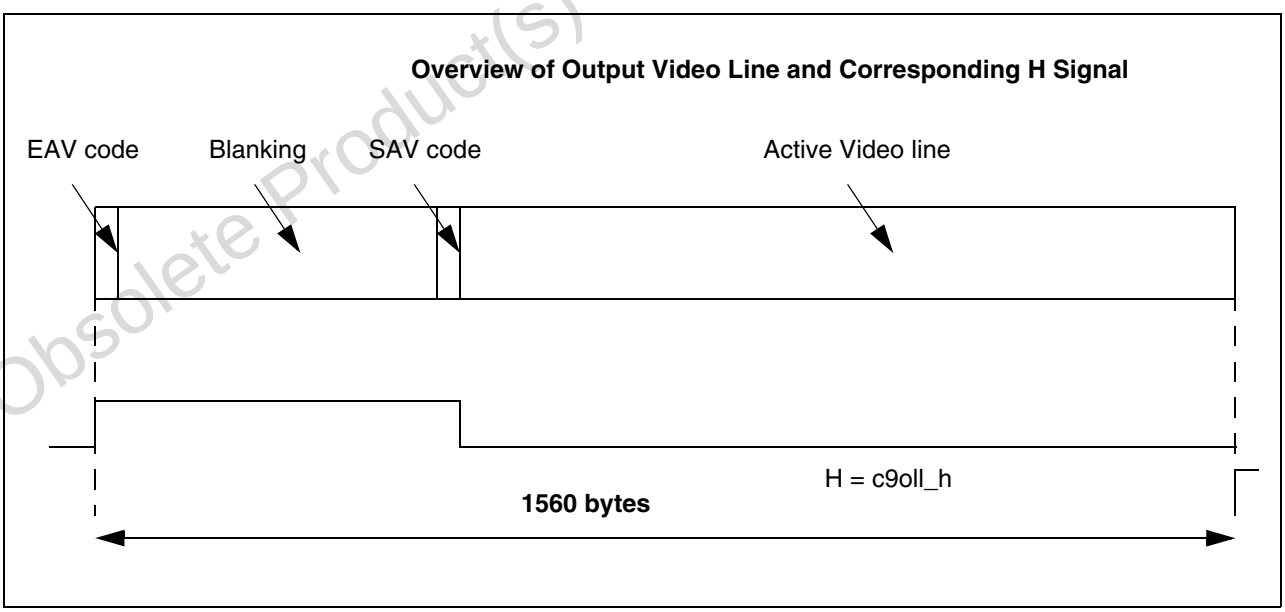


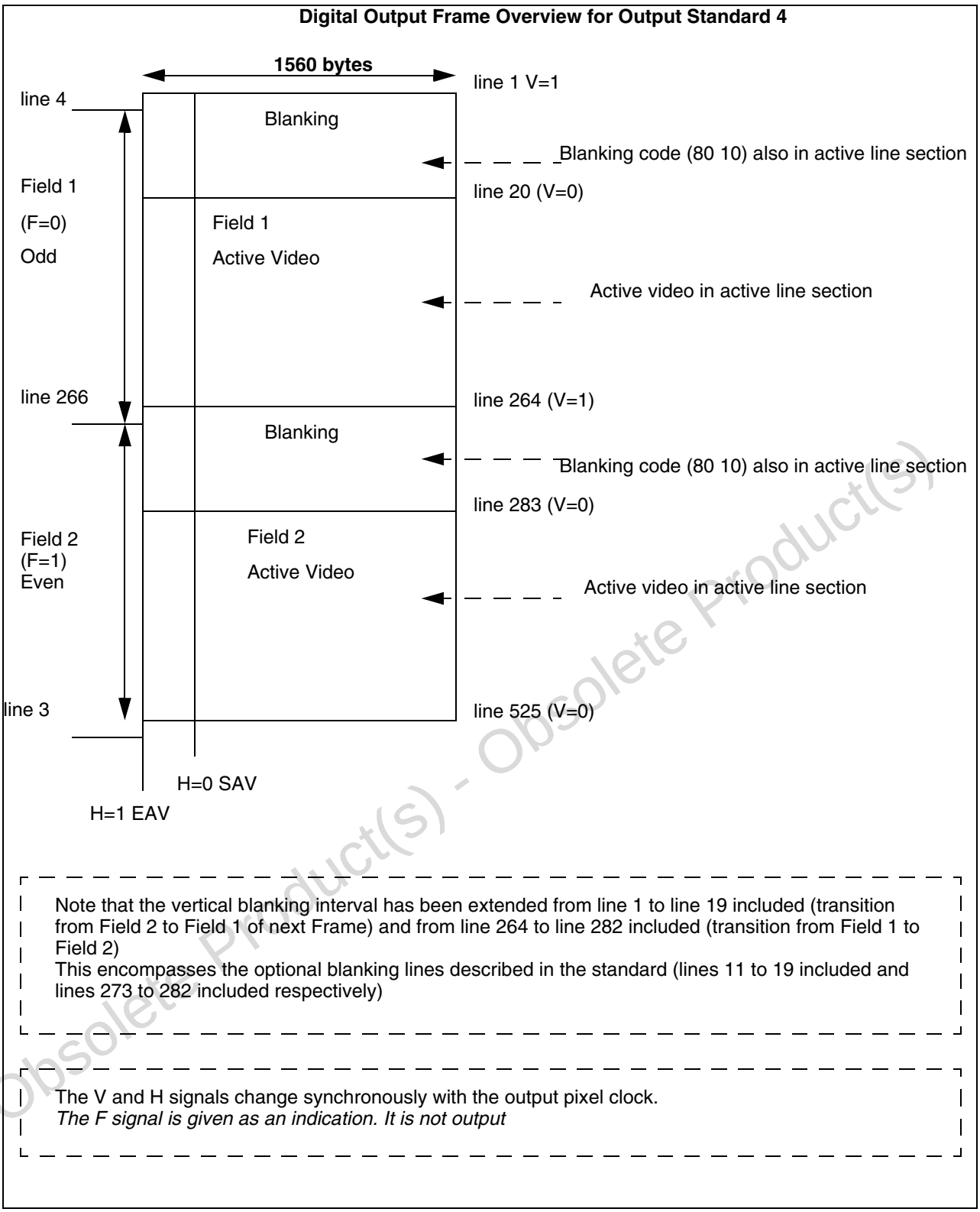
Note that the vertical blanking interval has been extended from line 1 to line 22 included (transition from Field 2 to Field 1 of next Frame) and from line 311 to line 335 included (transition from Field 1 to Field 2)

The V and H signals change synchronously with the output pixel clock.
The F signal is given as an indication. It is not output

4.12.2.7 Output Standard 4: Square Pixel / 525 lines / 60Hz (NTSC)







4.12.3 Insertion of Ancillary Data

Ancillary data is inserted in the output flow as it is received from the VBI slicer. No operation/ modification is performed on this data. No fixed prefix or suffix is added.

The ancillary data is always inserted between the EAV and SAV codes of each line.

The line number is provided by the VBI slicer.VBI data is inserted on the next possible output line. The only lines where insertion cannot take place are the forbidden lines. The list of forbidden lines depend on the standard:

- for the 525 lines (60 Hz): 9,10,11,272,273,274
- for the 625 lines (50 Hz): 5,6,7,318,319,320

Ancillary data is inserted starting just after the EAV code. Ancillary data will replace the blanking data codes. Ancillary data is inserted in the same order as it is received from the VBI slicer.

VBI data belonging to the same line at reception is inserted in a single line.The maximum number of ancillary data bytes to be inserted is 84.

4.12.4 Line-Locked Output Pixel Clock Generation

A phase-locked loop (PLL) generates a clock signal (CLK_DATA) that is used to read the output FIFO and to output the YCrCb data in synchronization. This output pixel clock frequency is a multiple of the input line frequency. Its value (1716, 1728, 1560 or 1888) depends on the input TV standard and the programmable Normal Pixel or Square Pixel mode.

Note that phase jumps detected in the input video are replicated in the output PLL. This is equivalent to a temporary change of the number of samples per line, but no change in the output clock frequency. This feature can be disabled. In this case, the output PLL then corrects the input phase step by frequency modulation.

4.12.5 Alternate Functions: Bus Extensions

Output data is issued synchronously to the CLK_DATA clock active edge. Either the rising or falling edge of the CLK_DATA signal can be programmed as the active edge.

The following pins can be used for bus extension purposes as programmable output pins: PLLLOCK, HSYNC, VSYNC and FIELD.

PLLLOCK has a second alternate function IRQ (Interrrupt Request). Interrupt can be generated by several functions described in registers DDECCONT36 and DDECCONT3C.

4.12.6 Output Code Clipping

To allow compatibility with other devices, output codes can be clipped to remain inside 0 to 100% of luminance (16 to 235) and chrominance (16 to 240) components.

4.12.7 Programming

The Vsync Insertion mode for the output flow is selected in the VSYNCTYPE bit in the DDECCONT0 register.

The PHSHFT_DIS bit in the DDECCONT5 register is used to disable the phase jump mechanism in the output PLL. By default, phase jumps are allowed when a phase shift in the video input is transmitted in the data flow to the output PLL.

The active edge for the CLK_DATA signal is selected by the ACTEDGE bit in the DDECCONT0 register.

Data is output from the STV2310 on the FIELD, VSYNC, HSYNC, PLLLOCK and YCRCB[7:0] pins which are synchronous to the CLK_DATA output clock on either the rising or falling edge (depending on the selected option).

To force the Interlaced output mode, use the NONINTERLACED_EN bit in the DDECCONT18 register.

To force the pass through mode, use the PASSTHROUGH_EN bit in the DDECCONT38 register.

To shift the external Hsync pulse, use the HSYNCSHIFT_DEL[1:0] and HSYNCSHIFT_EN bits in the DDECCONT22 register.

Cr Cb attenuation are controlled by the DDECCONT37 and the DDECCONT38 registers.
The output blanking modes are controlled by the OUTBEHAV_BLANK2 and OUTBEHAV_BLANK1 bits in the DDECCONT38 register.

Output clipping is controlled by the DDECCONT18 register bit [2].

The PLLLOCK, HSYNC, VSYNC and FIELD pins may have bus extension functions. This is done by programming the OUTBUS [7:0] bits in the DDECCONT7 register.

Table 13: Output PLL Alternate Functions

Bitfield	Description
OUTBUS[0]	0: Standard function. 1: PLLLOCK = OUTBUS[1]
OUTBUS[6]	0: Standard function. 1: FIELD = OUTBUS[7]
OUTBUS[4]	0: Standard function. 1: VSYNC = OUTBUS[5]
OUTBUS[2]	0: Standard function. 1: HSYNC = OUTBUS[3]

The PLLLOCK pin has a second alternate IRQ (Interrupt Request) function, selected by the PLLLOCKIT_EN bit in the DDECCONT35 register.

Note: By default, the PLLLOCK, HSYNC, VSYNC, and FIELD pins are used for their primary functions.

4.13 VBI Data Slicing and Insertion

The following standards are supported by the VBI Data Slicer (see Table 14). After slicing, VBI data is embedded in the output stream, using the intervals between the End of Active Video (EAV) and the Start of Active Video (SAV) codes of each line and formatted according to the ancillary sequences in compliance with specification ITU-R BT.656. VBI data is inserted in the Output FIFO.

Table 14: VBI Slicing Standards

VBI Standards	TV Systems (lines/freq.)	TV Lines[1]	Bit Rate (Mbit/s)	Modulation	Bytes per Line
Teletext B WST	625/50	6 to 22	6.9375	NRZ	45
VPS	625/50	16	2.5000	Bi-phase	15
WSS	625/50	23	0.8333	Bi-phase	14 bits of data
Closed Caption	625/50	21/22	0.5035	NRZ	3
Teletext B-WST[1]	525/60	10 to 21	5.727272	NRZ	37
Closed Caption	525/60	21	0.5035	NRZ	3
Gemstar	525/60	21	1.007	NRZ	5

1. Lines are numbered in compliance with specification ITU-R BT.470.

Note: The WST - Teletext C and D (525 lines /60 Hz) formats (NATBS - MOJI) may be covered by the WST - Teletext B (525 lines -60 Hz) format.

4.13.1 VBI Formatting Features

4.13.1.1 VPS Features

Video Programming System (VPS) data complies with ETSI specifications.

- Search of VPS data on TV line 16 of each field
- Optional Extended VPS data on three TV lines (15,16 and 17) of each field
- Search of VPS data regardless of the field information
- Recognition of Start code
- Sampling and decoding of bytes 5 and 11 to 14
- Bi-phase code check
- Generation of bi-phase correctness flags

4.13.1.2 WSS Features

Wide Screen Signaling (WSS) data complies with ETSI specifications.

- Search of WSS data on TV line 23 of each field
- Optional Extended WSS data on four TV lines (21, 22, 23 and 24) of each field
- Search of WSS data regardless of the field information
- Recognition of Start code
- Sampling and decoding of relevant 14 bits
- Bi-phase code check
- Generation of bi-phase correctness flags

4.13.1.3 WST Features

World System Teletext (WST) data complies with ETSI specifications. The searched WST format is unique at a given time and is programmed by software through register-based control bits (50 Hz or 60 Hz, etc.).

- Search of WST data starting at TV line 6 for 525-line broadcasts, or TV line 318 for 625-line broadcasts.
- Optional Extended WST data search starting at 2nd TV line (register-based control bit).
- Recognition and check of usual WST frame code (27h).
- Optional recognition and check of programmable extended frame code (register-based value - but the three LSBs must be kept at ‘1’).
- Recognition of all packets or recognition of only Service Packets X/30 and X/31 (register-based control bit).
- Hamming decode & check of Magazine and Page bytes for usual frame code.
- Split of Magazine & Page data in two separate bytes (1st byte is for Magazine, 2nd for Page).

4.13.1.4 Closed Caption Features

- Search of CC data during line 21 (NTSC) or line 22 (PAL), regardless of the field information.
- Optional Extended slicing during all the VBI (line 5 to 25 /NTSC or 2 to 25 /PAL), regardless of the field information.
- Recognition and check of usual CC Frame code (11000b).
- Recognition and check of tighter CC Frame code (C2h).

- Generation of Per-byte Parity check flags.

4.13.1.5 Gemstar Features

- Search of Gemstar data during the line 21 (NTSC) or line 22 (PAL), regardless of the field information.
- Optional Extended slicing during all the VBI (line 5 to 25 /NTSC or 2 to 25 /PAL), regardless of the field information.
- Recognition and check of usual Gemstar Frame code (x011x1x1b)
- Recognition and check of tighter Gemstar Frame code (10110111b)

4.13.2 Data Output Format (DOF)

The Data Output Format stage will add the following data items to those received from the VBI Formatting unit:

- An ancillary preamble
- A User Data Word Count
- Filler Words
- A User Data Word checksum

It will then perform the following operations:

- Byte-to-nibble Data conversion operations
- Calculation of word-wise parity control bits
- User Data Word checksum calculation

The data output flow issued by the Data Output Format is inserted into an ITU-R BT.656-type digitized stream which complies with specifications ITU-R BT.656, ITU-R BT.1364 and SMPTE 291M.

In particular, the data flow follows the 8-bit data coding convention. Ancillary data is coded as “Type 2" 8-bit data items (as defined in both ITU.1364 and SMPTE 291M specifications).

EAV	Blanking Interval	SAV	Video Digitalized Stream

A maximum of 100 bytes are used in the Blanking Interval for ancillary data. For more information, refer to Table 12: Frame Output Standards.

The Data Output Format unit provides the following data on a TV line base:

- The Transport layer which consists of the Ancillary Data Flag (ADF), Data ID (DID), Secondary Data ID (SDID), Data Count (DC) and Checksum Word (CS).
- The entire data flow generated by the Hardware Filtering, after having split each byte into nibble format.
- The current TV Line value, from which the data was extracted.

Ancillary Data Flow

For each TV line, the following sequence is generated immediately after the EAV code:

ADF	DID	SDID	DC	UDWi	CS
3 Bytes	1 Byte	1 Byte	1 Byte	User Data Words	1 Byte
00h - FFh - FFh	41h	Format ID	UDW Count	Sliced Data in nibble	Checksum

DID & SDID Coding Convention

All VBI data formats recognized by the Slicer use the same Data ID value. This Data ID value is programmed in the SLDID[5:0] bits in the VBICONT1 register. The default value of the DID register is "000001" respecting an 8-bit format and coding for 8-bit applications, in compliance with SMPTE 291M specifications (the full default code is 41h when parity control bits are added). Bits 6 and 7 of the DID value are hardware calculated (bit 6 is the even parity of bits 5 to 0, bit 7 is the binary complement of bit 6).

Note: All possible DID values are coded using a Type 2 ancillary data coding format.

The Secondary Data ID codes (SDID) identify the recognized data formats as follows:

Table 15: Secondary ID Codes

SDID[1]	SDID Byte		Comments
01	41h	WSS (No field link)	
02	42h		(Not used)
03	83h	VPS (No field link)	
04	44h	Closed Caption - Field 2	
05	85h	Closed Caption - Field 1	
06	86h	Gemstar - Field 2	
07	47h	Gemstar - Field 1	
08	48h	Teletext B - 625 lines/50 Hz - Field 2	Frame Code: 27h - F = 6.9375 MHz
09	89h	Teletext B - 625 lines/50 Hz - Field 1	Frame Code: 27h - F = 6.9375 MHz
0A	8Ah	Teletext B - 625 lines/50 Hz - Field 2	Frame Code: XXh[2] - F = 6.9375 MHz
0B	4Bh	Teletext B - 625 lines/50 Hz - Field 1	Frame Codecode: XXh[2] - F = 6.9375 MHz
10	50h	Teletext B - 525 lines/60 Hz - Field 2	Frame Code: 27h - F = 5.727272 MHz
11	91h	Teletext B - 525 lines/60 Hz - Field 1	Frame Code: 27h - F = 5.727272 MHz
12	92h	Teletext B - 525 lines/60 Hz - Field 2	Frame Code: XXh[2] - F = 5.727272 MHz
13	53h	Teletext B - 525 lines/60 Hz - Field 1	Frame Code: XXh[2] - F = 5.727272 MHz

1. 8-bit Format
2. A different Frame Code (from the usual one) has been validated for this data. The field information can be recovered from the Data ID value.

Data Count (DC) Coding

The Data Count (DC) byte is coded according to the parity protection scheme defined in SMPTE 291M or ITU-R BT.1364 specifications, as applied to 8-bit coded data (i.e. bit 6 is the even parity check of bits 0 to 5, bit 7 is bit 6 complement to 1). In 8-bit applications, the DC byte gives a value as a 4-byte group.

The number of the group of 4 User Data Words (UDW) transferred for the corresponding TV line is given in the DC byte using 6 bits.

Checksum (CS) Coding

The Checksum (CS) byte is coded according to the parity protection scheme defined in SMPTE 291M or ITU-R BT.1364 specifications, as applied to 8-bit coded data.

Bits 6 to 0 are the LSB bits of the result of the sum of the seven LSB bits of DID, SDID, DC and all UDW bytes (any carry is dropped). Bit 7 is the complement of Bit 6.

User Data Word (UDW) Coding

As 00h and FFh codes are prohibited in ITU-R BT.656 specifications, each data byte is substituted by a pair of bytes; these two bytes are respectively built with:

- The lower data nibble for the lower nibble of the 1st byte.
- The upper data nibble for the lower nibble of the 2nd byte.

Data is transmitted in the same temporal order as for the Hardware Filtering.

The TV line value is also provided to the DOF block to prevent scrambling errors when the ancillary data flow is re-mixed with the video flow.

User Data Word Filler

As data is coded according to the 8-bit application protocol described in SMPTE 291M and ITU-R BT.1364 specifications, some extra bytes may be inserted into the User Data Word sequence. These bytes code the value 80h which is meaningless and is used only to maintain a 4-byte UDW modularity (in compliance with the above specifications). These meaningless bytes are also used to maintain the most adequate 4-byte wise data storing format handled by the microcontroller.

When an application is running, it is important that these filler bytes are not processed as valid data items.

UDW Coding for WST - Teletext B

For World System Teletext (WST) standards, the UDW coding scheme depends on the searched frame code.

When the searched frame code is the usual code (27h), the two first UDW words code the Magazine (3 bits) and the Page (5 bits) values. In this case, there is no need to perform a nibble split on these two words.When the searched frame code is validated with a programmable value, a split of the two first words is applied (as they may not be necessarily Hamming 8/4 coded).

The above bytes are followed by 80 bytes (respectively 64 bytes in 525/60Hz) resulting of the nibble split of the 40 bytes (respectively 32 bytes in 525/60Hz) decoded from the current TV ancillary data.

Table 16: Magazine and Page Coding

Bit	7	6	5	4	3	2	1	0
Magazine Byte Coding	Bit 6 1's complement	Even parity check for bits [5:0]	Always 0			Magazine value		

Table 16: Magazine and Page Coding

Bit	7	6	5	4	3	2	1	0
Page Byte Coding	Bit 6 1's complement	Even parity check for bits [5:0]	Always 0	Page value				

In both cases, two filler bytes are added immediately after the last meaningful User Data Word in order to maintain a Data Count value that is a multiple of 4 bytes.

All UDW bytes are coded according to the parity protection scheme defined in SMPTE 291M or ITU-R BT.1364 specifications, as applied to 8-bit coded data (i.e. bit 6 is the even parity check of bits 0 to 5 and bit 7 is bit 6 complement to1).

Table 17: UDW Coding for WST

Frame Code			ADF	DID	SDID	DC	MAG	PAGE	Other UDW Bytes	FIL1	FIL2	CS
WST - 625 lines/50 Hz	27h	Byte.count	3	1	1	1	1	1	80	1	1	1
WST - 625 lines/50 Hz	xxh	Byte.count	3	1	1	1	0	0	84	0	0	1
WST - 525 lines/60 Hz	27h	Byte.count	3	1	1	1	1	1	64	1	1	1
WST - 525 lines/60 Hz	xxh	Byte.count	3	1	1	1	0	0	68	0	0	1

Note: "FIL1" and "FIL2" stand for Filler Bytes 1 and 2.

Table 18: UDW Byte Contents

Byte	625 lines / 50 Hz Content (Framing = 27h)	625 lines / 50 Hz Content (Custom Framing)	Byte	525 lines / 60 Hz Content (Framing = 27h)	525 lines / 60 Hz Content (Custom Framing)
1	Decoded Magazine value	LSB of Raw sliced 1st byte	1	Decoded Magazine value	LSB of Raw sliced 1st byte
2	Decoded Page value	MSB of Raw sliced 1st byte	2	Decoded Page value	MSB of Raw sliced 1st byte
3	LSB of 1st data byte	LSB of Raw sliced 2nd byte	3	LSB of 1st data byte	LSB of Raw sliced 2nd byte
4	MSB of 1st data byte	MSB of Raw sliced 2nd byte	4	MSB of 1st data byte	MSB of Raw sliced 2nd byte
5	LSB of 2nd data byte	LSB of Next raw byte	5	LSB of 2nd data byte	LSB of Next raw byte
6	MSB of 2nd data byte	MSB of Next raw byte	6	MSB of 2nd data byte	MSB of Next raw byte
…	…	…	…	…	…
…	…	…	67	LSB of 32nd data byte	LSB of Last raw byte
83	LSB of 40th data byte	LSB of Last raw byte	68	MSB of 32nd data byte	MSB of Last raw byte
84	MSB of 40th data byte	MSB of Last raw byte	…	…	…

UDW Coding for VPS

In Video Programming Systems (VPS), a nibble split algorithm is applied. In all bytes, bit 6 is the even parity check of bits 5 to 0. Bit 7 is the complement of bit 6.

Table 19: UDW Coding for VPS

ADF	DID	SDID	DC	VPUD 00	VPUD 01	VPUD 10	VPUD 11	VPUD 20	VPUD 21	VPUD 30	VPUD 31	VPUD 40	VPUD 41	VPUD S0	VPUD S1	CS

The result of the VPS sliced information is providing 12 bytes of data, which are generated in the following order:

- **VPUD00:** This byte provides the LSB contents of VPS byte 5.

bit	7	6	5	4	3	2	1	0
			0	0	RX3	RX2	RX1	RX0

- **VPUD01:** This byte provides the MSB contents of VPS byte 5.

bit	7	6	5	4	3	2	1	0
			0	0	SD1	SD0	RR1	RR0

SD[1:0]Sound bits

RR[1:0]R-Rating bits for flagging material not suitable for children.

RX[3:0]Reserved bits for future applications. Presently not defined.

- **VPUD10:** This byte provides the LSB contents of VPS byte 11.

bit	7	6	5	4	3	2	1	0
			0	0	ADT2	ADT1	ADT0	AMT3

- **VPUD11:** This byte provides the MSB contents of VPS byte 11.

bit	7	6	5	4	3	2	1	0
			0	0	ID1	ID0	ADT4	ADT3

ID[1:0]Identification of the address for this VPS line.

ADT[4:0]Announced day of transmission.

AMT[3]Announced month of transmission.

- **VPUD20:** This byte provides the LSB contents of VPS byte 12.

bit	7	6	5	4	3	2	1	0
			0	0	ASH3	ASH2	ASH1	ASH0

- **VPUD21:** This byte provides the MSB contents of VPS byte 12.

bit	7	6	5	4	3	2	1	0
			0	0	AMT2	AMT1	AMT0	ASH4

AMT[2:0]Announced month of transmission.

ASH[4]Announced start hour.

- **VPUD30:** This byte provides the LSB contents of VPS byte 13.

bit	7	6	5	4	3	2	1	0
			0	0	ASM1	ASM0	NC3	NC2

- **VPUD31:** This byte provides the MSB contents of VPS byte 13.

bit	7	6	5	4	3	2	1	0
			0	0	ASM5	ASM4	ASM3	ASM2

ASM[5:0]Announced start minute.

NC[3:0]Nationality code which is used to identify the source of the item.

- **VPUD40:** This byte provides the LSB contents of VPS byte 14.

bit	7	6	5	4	3	2	1	0
			0	0	PSC3	PSC2	PSC1	PSC0

- **VPUD41:** This byte provides the MSB contents of VPS byte 14.

bit	7	6	5	4	3	2	1	0
			0	0	NC1	NC0	PSC5	PSC4

NC[3:0]Nationality code which is used to identify the source of the item.

PSC[5:0]Program source code used to identify the source of the item inside the country identified in the nationality code.

- **VPUDS0:** This byte provides the result of data coding checks.

bit	7	6	5	4	3	2	1	0
			0	0	VPSER4	VPSER3	VPSER2	VPSER1

- **VPUDS1**: This byte provides the result of data coding checks.

bit	7	6	5	4	3	2	1	0
			0	0	0	0	VPSVDA	VPSER5

VPSVDA:Valid VPS Data. This bit is set when the VPS Start code has been matched and a full VPS data flow has been sliced. When this bit is reset, it indicates that at least part of the VPS data flow has not been received (in case of a too short TV line, for example).

VPSER1:Bi-phase error in the 1st VPS Byte. Data is written but there was a bi-phase error.

VPSER2:Bi-phase error in the 2nd VPS Byte. Data is written but there was a bi-phase error.

VPSER3:Bi-phase error in the 3rd VPS Byte. Data is written but there was a bi-phase error.

VPSER4:Bi-phase error in the 4th VPS Byte. Data is written but there was a bi-phase error.

VPSER5:Bi-phase error in the 5th VPS Byte. Data is written but there was a bi-phase error.

UDW Coding for WSS

In Wide Screen Signaling (WSS), a nibble split algorithm is applied. In all bytes, bit 6 is the even parity check of bits 5 to 0. Bit 7 is the complement of bit 6.

Table 20: UDW Coding for WSS

ADF	DID	SDID	DC	WSUD 00	WSUD 01	WSUD 10	WSUD 11	WSUD 20	WSUD 21	WSUD 30	WSUD 31	CS

- **WSUD00**: This byte provides the LSB contents of the WSS 1st group of data.

bit	7	6	5	4	3	2	1	0
			0	0	WSS3	WSS2	WSS1	WSS0

- **WSUD01**: This byte provides the MSB contents of the WSS 1st group of data.

bit	7	6	5	4	3	2	1	0
			0	0	0	0	0	WSSER1

WSSER1:WSS data group 1 error flag. This bit is set when any of the Group 1 bits (WSS[3:0]) is received with a bi-phase error.

WSS[3:0]:WSS Aspect Ratio Bits.

- **WSUD10**: This byte provides the LSB contents of the WSS 2nd group of data.

bit	7	6	5	4	3	2	1	0
			0	0	WSS7	WSS6	WSS5	WSS4

- **WSUD11**: This byte provides the MSB contents of the WSS 2nd group of data.

bit	7	6	5	4	3	2	1	0
			0	0	0	0	0	WSSER2

WSSER2:WSS data group 2 error flag. This bit is set when any of the Group 2 bits (WSS[7:4]) is received with a bi-phase error.

WSS[7:4]: WSS Enhanced Services Bits.

- **WSUD20**: This byte provides the LSB contents of the WSS 3rd group of data.

bit	7	6	5	4	3	2	1	0
			0	0	WSSER3	WSS10	WSS9	WSS8

- **WSUD21**: This byte is static and provides no information.

bit	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	0	0

WSSER3:WSS data group 3 error flag. This bit is set when any of the Group 3 bits (WSS[10:8]) is received with a bi-phase error.

WSS[10:8]: WSS Subtitle Bits.

- **WSUD30**: This byte provides the LSB contents of the WSS 4th group of data.

bit	7	6	5	4	3	2	1	0
			0	0	WSSER4	WSS13	WSS12	WSS11

- **WSUD31**: This byte provides the MSB contents of the WSS 4th group of data.

bit	7	6	5	4	3	2	1	0
			0	0	0	0	0	WSSVDA

WSSVDA:Valid WSS Data. This bit is set when the WSS Start code has been matched and a full WSS data flow has been sliced. When this bit is reset, it indicates that at least part of the WSS data flow has not been received (in case of a too short TV line, for example).

WSSER4:WSS Data Group 4 Error Flag. This bit is set when any of the Group 4 bits (WSS[13:11]) is received with a bi-phase error.

WSS[13:11]: WSS reserved Bits.

UDW Coding for CC

In Closed Caption (CC) systems, a nibble split algorithm is applied. In all bytes, bit 6 is the even parity check of bits 5 to 0. Bit 7 is the complement of bit 6.

Table 21: UDW Coding for CC

ADF	DID	SDID	DC	CCUD 00	CCUD 01	CCUD 10	CCUD 11	CCUD L0	CCUD L1	FIL0	FIL1	CS

- **CCUD00**: This byte provides the LSB contents of the CC 1st byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	CC3	CC2	CC1	CC0

- **CCUD01**: This byte provides the MSB contents of the CC 1st byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	CC7	CC6	CC5	CC4

- **CCUD10**: This byte provides the LSB contents of the CC 2nd byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	CC11	CC10	CC9	CC8

- **CCUD11**: This byte provides the MSB contents of the CC 2nd byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	CC15	CC14	CC13	CC12

- **CCUDL0**: This byte provides the contents of the CC bytes parity check.

bit	7	6	5	4	3	2	1	0
			0	0	0	0	CCP1	CCP0

- **CCUDL1**: This byte is static and provide no information.

bit	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	0	0

CCP0:Closed Caption parity flag of the first byte

CCP1:Closed Caption parity flag of the second byte

UDW Coding for Gemstar

In US Gemstar systems, a nibble split algorithm is applied. In all bytes, bit 6 is the even parity check of bits 5 to 0. Bit 7 is the complement of bit 6.

Table 22: UDW Coding for Gemstar

ADF	DID	SDID	DC	GMU D00	GMU D01	GMU D10	GMU D11	GMU D20	GMU D21	GMU D30	GMU D31	GMPF L0	GMPF L1	FIL0	FIL1	CS

- **GMUD00**: This byte provides the LSB contents of the Gemstar 1st byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	GM3	GM2	GM1	GM0

- **GMUD01**: This byte provides the MSB contents of the Gemstar 1st byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	GM7	GM6	GM5	GM4

- **GMUD10**: This byte provides the LSB contents of the Gemstar 2nd byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	GM11	GM10	GM9	GM8

- **GMUD11**: This byte provides the MSB contents of the Gemstar 2nd byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	GM15	GM14	GM13	GM12

- **GMUD20**: This byte provides the LSB contents of the Gemstar 3rd byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	GM19	GM18	GM71	GM16

- **GMUD21**: This byte provides the MSB contents of the Gemstar 3rd byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	GM23	GM22	GM21	GM20

- **GMUD30**: This byte provides the LSB contents of the Gemstar 4th byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	GM27	GM26	GM25	GM24

- **GMUD31**: This byte provides the MSB contents of the Gemstar 4th byte of data.

bit	7	6	5	4	3	2	1	0
			0	0	GM31	GM30	GM29	GM28

- **GMUDL0**: This byte provides the contents of the Gemstar bytes parity check.

bit	7	6	5	4	3	2	1	0
			0	0	GMP3	GMP2	GMP1	GMP0

- **GMUDL1**: This byte is static and provide no information.

bit	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	0	0

GMP0: Gemstar parity flag of the first byte
GMP1: Gemstar parity flag of the second byte
GMP2: Gemstar parity flag of the third byte
GMP3: Gemstar parity flag of the fourth byte

4.14 I²C Bus Specifications

Data transfers follow the usual I²C format: after the start condition (S), a 7-bit slave address is sent, followed by an eight-bit which is a data direction bit (W). An 8-bit sub-address is sent to select a register, followed by an 8-bit data word to be included in the register. The circuit operates at clock frequencies of up to 400 kHz. The IC's I²C bus decoder allows the automatic incrementation mode in write mode.

String Format

Write Only mode (S = Start Condition, P = Stop Condition, A = Acknowledge)

S	SLAVE ADDRESS	0	A	REGISTER N	A	DATA N	A	P

Read Only mode

S	SLAVE ADDRESS	0	A	REGISTER N	A	P

S	SLAVE ADDRESS	1	A	DATA N	A	DATA N+1	A	P

Slave Address

Address	A7	A6	A5	A4	A3	A2	A1	A0
Value	1	0	0	0	I2CADD	1	1	R/W

Table 23: Alternate I²C Addresses

I2CADD = 0		I2CADD = 1	
Write Address	86h	Write Address	8Eh
Read Address	87h	Read Address	8Fh

For the exact numerical values of the I²C timing characteristics, please refer to the I²C Bus Characteristics on page 106.

5 Register List

This section lists the Control and Status registers for the I²C interface. Registers are called as output ports and are named as follows:

- DDECCONT[n][7:0] for non-VBI Control registers
- DDECSTAT[n][7:0] for Status registers (Read Only)
- VBICONT[n][7:0] for VBI Control registers

5.1 Register Map

Name	Add. (h)	Reset Value (Bin)	Register Function and Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DDECCONT0	00h	0000 0100	VSYNC TYPE	PIXMODE	ACT EDGE	CVBS MUX	OUTTRI STATE	SVIDEO SEL	5060MODE[1:0]	
DDECCONT1	01h	0011 1111	BLANKMODE[1:0]		AUTOSTD[5:0]					
DDECCONT2	02h	0100 1001		PEDESTAL _REMOVE	AUTOSTD[11:6]					
DDECCONT3	03h	0001 0111			AUTOSTD[17:12]					
DDECCONT4	04h	0000 0001			AUTOSTD[23:18]					
DDECCONT5	05h	0010 0000			CRCBOVER_EN	FBLANKMODE[2:0]			YCRCB_ MODE	PHSHFT_ DIS
DDECCONT6	06h	0000 0001	MIX_SLOPE[7:0]							
DDECCONT7	07h	0000 0000	OUTBUS[7:0]							
DDECCONT8	08h	1111 1111	ZOOMIN_FACT[9:2]							
DDECCONT9	09h	0100 0000	ZOOMOUT_FACT[9:2]							
DDECCONTA	0Ah	0000 0000	ZOOMIN_OFFSET[9:2]							
DDECCONTB	0Bh	1100 0000	ZOOMIN_FACT[1:0]		ZOOMOUT_FACT [1:0]		ZOOMIN_OFFSET [1:0]		ZOOMOUT _EN	ZOOMIN_ EN
DDECCONTC	0Ch	0000 0000	SPC_CORING[1:0]		ALL_NTSC_HUE_VALUE[5:0]					
DDECCONTD	0Dh	0011 0100		STI_NB_FIELDS_FALSE [1:0]			STI_OK_ONCE_OR_ MORE		DEM_CKILL_CTRL[1:0]	
DDECCONTE	0Eh	0010 0110								
DDECCONTF	0Fh	0000 0000	DEM_CKILL_LVL[2:0]			DEM_CKILL_LVL[4:0]				
DDECCONT10	10h	0001 0000	SPC_NTSC_FLESH_PH	SPC_NTSC_FLESH_EN						
DDECCONT11	11h	1000 1000	SYNC_SLICE_LEVEL[3:0]							
DDECCONT12	12h	0000 0000			SPC_NTSC_GREEN_EN	TINTANGLE[4:0]				

Name	Add. (h)	Reset Value (Bin)	Register Function and Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DDECCONT13	13h	0000 0000								
DDECCONT14	14h	0000 0000								
DDECCONT15	15h	0001 0000					DEM_YC_DELAY[3:0]			
DDECCONT16	16h	0111 1010	SATLMTLN[1:0]		SATLMTPT[1:0]		SMHITH[1:0]		ACTITH[1:0]	
DDECCONT17	17h	0110 0100			STI_50_60 HZ_EN	STI_NB_FIELDS_CONFIRM[2:0]			SPC_OVE RLOAD_O FF	SPC_ACC _OFF
DDECCONT18	18h	0101 1001		BW_SEL[2:0]			NONINTE RLACED_ EN	SATCODE _EN		COMB_MO DE[1:0]
DDECCONT19	19h	0100 0100								
DDECCONT1A	1Ah	0010 0000								
DDECCONT1B	1Bh	1000 0100								
DDECCONT1C	1Ch	1000 0100								
DDECCONT1D	1Dh	1000 1000								
DDECCONT1E	1Eh	1001 1001								
DDECCONT1F	1Fh	0001 1000	DIRECTPA RITY							
DDECCONT20	20h	0000 0100								
DDECCONT21	21h	0010 1011			BLKLINE[1:0]					
DDECCONT22	22h	1110 1000					HTIMECST SEL	HSYNCSHIFT_DEL[1:0]		HSYNCSHI FT_EN
DDECCONT23	23h	1010 1010								
DDECCONT24	24h	1000 0111								
DDECCONT25	25h	1001 0100					HSYNC_ SAV	NOISE_THRESHOLD[2:0]		

Name	Add. (h)	Reset Value (Bin)	Register Function and Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DDECCONT26	26h	0100 0100								
DDECCONT27	27h	0110 0110								
DDECCONT28	28h	1000 0010	HUNLOCK_LINE_NUM[3:0]				HLOCK_LINE_NUM[3:0]			
DDECCONT29	29h	0101 0101					HLOCK_PH_ER_TH[3:0]			
DDECCONT2A	2Ah	1000 0010	CLAM_PROP[1:0]		CLAM_DER[1:0]			CLAMP_INT[2:0]		
DDECCONT2B	2Bh	0110 0011								
DDECCONT2C	2Ch	1000 0010								
DDECCONT2D	2Dh	0000 1010								
DDECCONT2E	2Eh	0000 0000								
DDECCONT2F	2Fh	0000 0000				OVERDRIVE_MODE	OVERDRIVE_SEL[1:0]			
DDECCONT30	30h	0000 0000								
DDECCONT31	31h	0010 0000		AGC_DIS	CVBSAGCGAIN[5:0]					
DDECCONT32	32h	0000 0000								
DDECCONT33	33h	0000 0000								
DDECCONT34	34h	0000 0000								
DDECCONT35	35h	0000 0000	PLLLOCKIT_EN	RGBADJUST_EN	RGBADJUST[5:0]					
DDECCONT36	36h	1111 0000	PLLLOCK_MASK	VLOCK_MASK	HLOCK_MASK	TVSTDID_MASK	FBDEL[3:0]			
DDECCONT37	37h	1111 1111	CB_SCALING[1:0]		CR_SCALING[5:0]					
DDECCONT38	38h	0010 1111					CB_SCALING[5:2]			

Name	Add. (h)	Reset Value (Bin)	Register Function and Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DDECCONT39	39h	0101 0101								
DDECCONT3A	3Ah	0101 0101								
DDECCONT3B	3Bh	0011 0101								
DDECCONT3C	3Ch	1111 1100	VSYNCNSTD_MASK	TRICKDET_MASK	INTERDET_MASK	VCRDET_MASK	INSERDET_MASK	FBDET_MASK		
VBICONT1	3Dh	xx00 0001			SLDID[5:0]					
VBICONT2	3Eh	xx00 0000			SLFIL[5:0]					
VBICONT3	3Fh	1000 0001		SLICECOMP_EN	RAWFILTOFF_EN	WSTSLICING_EN		WSTCUSTOMFRAM	WSTEXTLINES	WSTALLPACKETS
VBICONT4	40h	0010 0111	FRAMINGCODE[7:0]							
VBICONT5	41h	1100 0101	WSSF1ONLY_EN	VPS1ONLY_EN			VPSSLICING_EN	VPSEXTLINES	WSSSLICING_EN	WSSEXTLINES
VBICONT6	42h	0000 0000		GMVBILINES	GMRELAX_EN	GMSLICING_EN		CCVBILINES	CCRELAX_EN	CCSLICING_EN
VBICONT7	43h	0000 1101								
VBICONT8	44h	0000 1000								
VBICONT9	45h	0110 0011								
VBICONT0A	46h	0001 1100								
VBICONT0B	47h	0100 0110								
VBICONT0C	48h	0000 0000								
VBICONT0D	49h	0000 0000								
VBICONT0E	4Ah	0000 0000								
VBICONT0F	4Bh	1011 0011	CGSEW[2:0]			CGNBS[1:0]		CGNBI[2:0]		
VBICONT10	4Ch	0000 1000	CGESPF2	CGESPF1	CGVS[5:0]					
VBICONT11	4Dh	0111 0001								
VBICONT12	4Eh	0000 1100								
VBICONT13	4Fh	0000 0000	WSTH[7:0]							
VBICONT14	50h	0000 0000							WSTH[9:8]	
VBICONT15	51h	0001 0101								
VBICONT16	52h	1010 0000		EQZPRGMODE	EQZORDERSEL	EQZFLTMOD[4:0]				
VBICONT17	53h	0101 0000	VBI_EQUALCOEFF[2:0]							
VBICONT18	54h	0001 0010								

Name	Add. (h)	Reset Value (Bin)	Register Function and Description							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DDECCONTFE	7Eh	0000 0000	INTERDET_ACK	VCRDET_ACK	INSERDET_ACK	FBDET_ACK	PLLLOCK_ACK	VLOCK_ACK	HLOCK_ACK	TVSTDID_ACK
DDECCONTFF	7Fh	0000 0000							VSYNCNSTD_ACK	TRICKDET_ACK
DDECSTAT1	80h	0001 0000	STVDDECVERS[7:0]							
DDECSTAT2	81h	READ ONLY	VLOCK	HLOCK	PLLLOCK	5060ID	TVSTDID	TVSTD[2:0]		
DDECSTAT3	82h	READ ONLY	VSYNCLOC_NSTD	BLANKLVL_SHIFT_DETECTED	INTERLACED_DETECTED	DVD_DETECTED	VCR_DETECTED	INSER_DETECTED	FB_DETECTED	TRICKMOD_DETECTED
DDECSTAT4	83h	READ ONLY	NOISELVL[7:0]							
DDECSTAT5	84h	READ ONLY	SLDID[7:0]							
DDECSTAT6	85h	READ ONLY	SLFIL[7:0]							
DDECSTAT7	86h	READ ONLY		VBIERR_DETECTED	GEM_DETECTED	CC_DETECTED	VPS_DETECTED	WST_DETECTED	WSS_DETECTED	OPENLOOP
DDECSTAT8										

5.2 Non-VBI Control Register Descriptions

DDECCONT0 Register Description

Address: 00h

Reset Value (bin): 0000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VSYNCTYPE	PIXMODE	ACTEDGE	CVBSMUX	OUTTRISTATE	SVIDEOSEL	5060MODE[1:0]	

Bit Name	Function
VSYNCTYPE	Vsync Insertion in Output Flow The VSYNC output signal is always synchronous to the output clock (CLK_DATA). It will toggle twice per frame either in Digital or Analog mode according to this option. 0: Analog mode (Interlaced): depends on the standard: for Output Standard 1: start of line 1 and middle of line 263 for Output Standard 2: start of line 1 and middle of line 313 for Output Standard 3: start of line 1 and middle of line 313 (same as Standard 2) for Output Standard 4: start of line 1 and middle of line 263 (Default) 1: Digital mode: start of line 1/624 or start of line 264/624 (Vsync at beginning of line) Note that the analog mode is now split between an "analog output as input" mode and an "analog output with forced interlaced" output mode. For more information, see bit 3 of register DDECCONT18.

Bit Name	Function
PIXMODE	Pixel Mode Selection In Square Pixel mode, the number of Y, Cr and Cb components depends on the standard as shown in Table 12. The output line locked frequency (CLK_DATA) will also change according to the standard. 0: Normal Pixel mode (Default) 1: Square Pixel mode
ACTEDGE	Data is output from the STV2310 on the following pads: FIELD, VSYNC, HSYNC, PLLLOCK and YCRCB[7:0]. It is synchronous to the CLK_DATA output clock either on the rising or falling edge depending on this option. 0: Clock falling edge is active edge (Default) 1: Clock rising edge is active edge
CVBSMUX	Y/CVBS Input Selection 0: Y/CVBS1 input (Default) 1: Y/CVBS2 input
OUTTRISTATE	Pad Tristate Mode The pad tristate mode depends on the chip I2C address. If the I2C default chip address is chosen: 0: Output digital pads in Output mode (Default) 1: Output digital pads in Tristate mode If the I2C spare chip address is chosen: 0: Output digital pads in Tristate mode (Default) 1: Output digital pads in Output mode Note that only the following pads can be in Tristate mode: FIELD, VSYNC, HSYNC, PLLLOCK, CLK_DATA and YCRCB[7:0]. The I2C pads are never in Tristate mode.
SVIDEOSEL	CVSB/S-Video Selection The S-video mode notifies the STV2310 that the chroma and luma signals are already separated. 0: S-Video Input 1: CVBS Input (Default)
5060MODE[1:0]	Vsync Search Mode and initial Free-running Mode These bits provide the starting point for the Vsync extraction mechanism. 50-Hz or 60-Hz input standards are expected. The options are to look exclusively for 50-Hz or 60-Hz standards (Forced 50 or 60) or to search for all standards with a priority in the search mechanism (Auto 50 or 60). 00: Auto 50: Automatic search mode starting with 50-Hz standards. (Default) 01: Forced 60: Search mode forced to 60-Hz standards only. 10: Forced 50: Search mode forced to 50-Hz standards only. 11: Auto 60: Automatic search mode starting with 60-Hz standards.

DDECCONT1 Register Description

Address (hex): 01h

Reset Value (bin): 0011 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BLANKMODE[1:0]		AUTOSTD[5:0]					

Bit Name	Function
BLANKMODE [1:0]	Blanking Mode The blanking mode defines how the clamp mechanism will perform. The blanking code is the ADC output code used by the clamp mechanism as target In the Auto mode and depends on the vertical sync identification result (50 or 60 Hz). The blanking code is determined in the 2 other modes. 00: Auto (50 Hz = Code 256, 60 Hz = Code 244) (Default) 01: Blanking code 256 (Sync tip 43 IRE) 10: Blanking code 244 (Sync tip 40 IRE) 11: Auto (Same as 00)
AUTOSTD[5:0]	Auto Identification Table (Seventh and Eighth Standards) The STV2310 can search for one of the TV standards programmed in the Automatic Standard Identification Table (split over several registers). The Automatic Standard Identification Table has 8 entries with an order of priority for the search. Note that in the default configuration, "No Standard" is programmed in the seventh and eigth entries. 000: PAL BGDHI100: PAL N 001: SECAM 101 NTSC 4.43 010: NTSC M110 or 111: No Standard 011: PAL M

DDECCONT2 Register Description

Address (hex): 02h

Reset Value (bin): 0100 1001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	PEDESTAL_ REMOVE	AUTOSTD[11:6]					

Bit Name	Function
Bit 7	Reserved: Must be set to 0.
PEDESTAL_ REMOVE	Pedestal Remove in Input signal The PEDESTAL_REMOVE bit describes the input signal (whether a pedestal is present in the input signal or not). This information is entered by the user. Gain and offset on the Y processing will be different according to that bit. The pedestal remove function is active for all 50- and 60-Hz input standards. Note that by default, it is considered that there is no pedestal in NTSC M inputs. The pedestal remove function operates both on the CVBS and RGB flows. 0: Pedestal is present in input signal. 1: Pedestal is not present in input signal. (Default)
AUTOSTD[11:6]	Auto Identification Table (Fifth and Sixth Standards) Fifth and Sixth Standards of the Automatic Standard Identification Table. See register DDECCONT1. 001 001: SECAM (Default)

DDECCONT3 Register Description

Address (hex): 03h

Reset Value (bin): 0001 0111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		AUTOSTD[17:12]					

Bit Name	Function
Bits[7:6]	Reserved: Must be set to 0.
AUTOSTD[17:12]	Auto Identification Table (Third and Fourth Standards) Third and Fourth Standards of the Automatic Standard Identification Table. See register DDECCONT1. 010 111: NTSC M and No Standard (Default)

DDECCONT4 Register Description

Address (hex): 04h

Reset Value (bin): 0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		AUTOSTD[23:18]					

Bit Name	Function
Bits[7:6]	Reserved: must be set to 0.
AUTOSTD[23:18]	Auto Identification Table (First and Second Standards) First and Second Standards of the Automatic Standard Identification Table. See register DDECCONT1. 000 001: PAL BGDHI and SECAM (Default)

DDECCONT5 Register Description

Address (hex): 05h

Reset Value (bin): 0010 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SECAM_CHRTUNING[1:0]		CRCBOVER_EN	FBLANKMODE[2:0]			YCRCB_MODE	PHSHFT_DIS

Bit Name	Function
SECAM_CHRTUNING[1:0]	Reserved: must be set to 0.

Bit Name	Function
CRCBOVER_EN	RGB enables the CRCB overload algorithm This bit enables the RGB CrCb overload mechanism. This mechanism is used to prevent clipping on YCrCb (when the input RGB signals are too large). The CrCb overload mechanism performs chroma measurement during the video line to compute the correcting scale factor. 0: CRCB overload algorithm not active 1: CRCB overload algorithm active
FBLANKMODE [2:0]	Fast Blanking Mode Selection The Fast Blanking mode is only operational when the STV2310 is not in Analog YCrCb mode. It also depends on the programmed mode and the FB input value. See register DDECCONT6. 00x: Normal mixing mode between CVBS and RGB (Default) (FB active during active line; soft mixing between 0 and 1) 01x: Saturated mode (mixing mode between CVBS and RGB) (FB active and soft mixing from 0 to MIXSLOPE[7:0]) 100: Static Mixer or Alpha Blending Mode 1 (FB inactive) Y_{OUT} = alpha x Y_{RGB} + (1-alpha) x Y_{CVBS} 101: Static Mixer or Alpha Blending Mode 2 (FB inactive) Y_{OUT} = alpha x Y_{CVBS} + (1- alpha) x Y_{RGB} with alpha = MIXSLOPE[7:0] (Same relationship for Cr and Cb) 110: Forced CVBS (FB inactive) Y_{OUT} = Y_{CVBS} (idem for Cb, Cr) 111: Forced RGB (FB inactive) Y_{OUT} = Y_{RGB} (idem for Cb,Cr)
YCRCB_MODE	YCrCb Mode Selection When the STV2310 is in Analog YCrCb mode, Fast Blanking Mode is disabled. 0: YCrCb signals all either from CVBS or RGB. (Default) 1: YCrCb mode: Y from CVBS signal, Cr and Cb from RGB signal with priority over FB mode.
PHSHFT_DIS	Phase Shift Option Disabled in Output PLL This bit disables the phase jumps mechanism in the output PLL. Phase jumps are allowed when a phase shift in the video input is transmitted in the data flow to the output PLL. 0: Phase shifts are enabled. (Default) 1: Phase shifts are disabled.

DDECCONT6 Register Description

Address (hex): 06h

Reset Value (bin): 0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIX_SLOPE[7:0]							

Bit Name	Function
MIX_SLOPE[7:0]	Soft Mixing Slope, Alpha Blending or Saturated Value This bitfield provides the soft mixing slope or the alpha blending value depending on Fast Blanking mode. When the blanking mode is in Forced RGB or Forced CVBS mode, this bitfield is irrelevant. When the blanking mode is in one of the alpha blending modes, the MIX_SLOPE[7:0] register provides the alpha value (an FF entry means full scale). When the blanking mode is in the normal mixing mode between RGB and CVBS, the MIX_SLOPE[1:0] bits indicate the mixing slope. The MIX_SLOPE[7:2] bits must be set to 000000. The MIX_SLOPE[1:0] register codes the soft mixing slope from 00 to 11 with 00 corresponding to a slope of 1 clock cycle (4 x f_{SC} clock domain) and 11 corresponding to a slope of 4 clock cycles. The default entry is 01, corresponding to a slope of 2 clock cycles.

DDECCONT7 Register Description

Address (hex): 07h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OUTBUS[7:0]							

Bit Name	Function
OUTBUS[7:2]	Alternative values driven by OUTBUS The OUTBUS[7:2] bits are linked to the HSYNC, VSYNC and FIELD pad control. When OUTBUS[2] = 0: standard function on HSYNC; when = 1: HSYNC = OUTBUS[3] When OUTBUS[4] = 0: standard function on VSYNC; when = 1: VSYNC = OUTBUS[5] When OUTBUS[6] = 0: standard function on FIELD; when = 1: FIELD = OUTBUS[7]
OUTBUS[1:0]	Alternative values driven by OUTBUS The OUTBUS[1:0] bits are linked to the PLLLOCK pad control. When OUTBUS[0] = 0: standard function; when = 1: PLLLOCK = OUTBUS[1]

DDECCONT8 Register Description

Address (hex): 08h

Reset Value (bin): 1111 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZOOMIN_FACT[9:2]							

Bit Name	Function
ZOOMIN_FACT [9:2]	Zoom-in Factor from 1 to 4 (MSBs) The Zoom-in factor operates from 4 to 1 (No zoom). The LSBs of this value are in the DDECCONTB register. This value must be between 256 (x4) and 1023 (x1). 3FFh: Zoom-in factor of 1 (No zoom) (Default value) 200h: Zoom-in factor of 2 100h: Zoom-in factor of 4 (Enlarged picture)

DDECCONT9 Register Description

Address (hex): 09h

Reset Value (bin): 0100 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZOOMOUT_FACT[9:2]							

Bit Name	Function
ZOOMOUT_ FACT [9:2]	Zoom-out Factor from 1 to 0.25 (MSBs) The Zoom-out factor operates from 1 (no zoom) to 0.25 (large zoom). The Zoom-out factor must be between 256 (x1) and 1023 (x0.25). The LSBs of this value are in the DDECCONTB register. 3FFh: Zoom-out factor of 0.25 (Reduced picture) 100h: Zoom-out factor of 1.0 (No zoom) (Default value)

DDECCONTA Register Description

Address (hex): 0Ah

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZOOMIN_OFFSET[9:2]							

Bit Name	Function
ZOOMIN_ OFFSET[9:2]	Zoom-in Offset (Cropping) (MSBs) The Zoom-in offset determines the section of input line used for zooming in. The Zoom-in offset value must be between 0 and the maximum number of Y pixels per line. Note that the number of pixels per line will depend on the standard and the pixel mode. Note that the Zoom-out factor is coded on 10 bits in 2 registers. The Default value is 0 = first left pixel of the active line is the first pixel of zoom.

DDECCONTB Register Description

Address (hex): 0Bh

Reset Value (bin): 1100 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ZOOMIN_FACT[1:0]		ZOOMOUT_FACT[1:0]		ZOOMIN_OFFSET[1:0]		ZOOMOUT_ EN	ZOOMIN_EN

Bit Name	Function
ZOOMIN_FACT [1:0]	Zoom-in Factor (LSBs). See register DDECCONT8.

Bit Name	Function
ZOOMOUT_FACT [1:0]	Zoom-out Factor (LSBs). See register DDECCONT9.
ZOOMIN_OFFSET[1:0]	Zoom-in Offset (LSBs). See register DDECCONTA.
ZOOMOUT_EN	Zoom-out Function Enable When both Zoom-in and Zoom-out functions are enabled, the STV2310 is in Panorama mode. In Panorama mode, the ZOOMIN_FACT, the ZOOMOUT_FACT and the ZOOMIN_OFFSET are used. The ZOOMIN_FACT determines the zoom-in factor at the left and right edges of the picture. The ZOOMOUT_FACT determines the zoom-out factor at the center of the picture. The ZOOMIN_OFFSET determines the border width where the zoom factor increases from the zoom-in factor to the zoom-out factor, starting from the left edge (respectively, the border width finishing on the right edge where the zoom factor decreases from the zoom-out factor to the zoom-in factor). Correct programming is left to the user without hardware check. For programming verification, the following formula must be checked: Zt x (Zout - Zin) = N x (Zout -1) where Zin = ZOOMIN_FACT; Zout = ZOOMOUT_FACT; Zt = ZOOMIN_OFFSET; N = Number of Y pixels per line (720 in Normal Pixel mode, 640 or 768 in Square Pixel mode) 0: Zoom-out function is disabled. (Default) 1: Zoom-out function is enabled.
ZOOMIN_EN	Zoom-in Function Enable 0: Zoom-in function is disabled. (Default) 1: Zoom-in function is enabled.

DDECCONTC Register Description

Address (hex): 0Ch

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPC_CORING[1:0]				ALL_NTSC_HUE_VALUE[5:0]			

Bit Name	Function
SPC_CORING [1:0]	Coring Function for all standards The Coring function is operational for all standards. When activated, the demodulated color components (Cr and Cb) close to 128 are replaced by 128. 00: No action. (Default) 01: 127 to 129 rounded to 128 (dynamic range of ± 1 LSB) 10: 125 to 131 rounded to 128 (dynamic range of ± 3 LSBs) 11: 123 to 133 rounded to 128 (dynamic range of ± 5 LSBs)
ALL_NTSC_HUE_VALUE[5:0]	NTSC Hue Control Function The Hue Control mechanism is only operational when the NTSC or NTSC M standard has been detected (or being tried by the standard identification algorithm). The hue is a fixed offset in a demodulation angle. The offset is only operational in the active line. There are 63 steps of approximately 1.4 degrees each, allowing an offset of between -45° and +43.6°. Coded in 2's complement (0 = No Hue)

DDECCONTD Register Description

Address (hex): 0Dh

Reset Value (bin): 0011 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	STI_NB_FIELDS_FALSE [1:0]			STI_OK_ONCE_OR_MORE		DEM_CKILL_CTRL[1:0]	

Bit Name	Function
Bit 7	Reserved: Must be set to 0.
STI_NB_FIELDS_FALSE[1:0]	Number of Fields where Identification is lost before declaring Loss of Identification The STI_NB_FIELDS_FALSE bits are related to the standard identification algorithm. These bits are operational on all standards. They operate in the tracking phase when a standard has been recognized. They determine the number of successive fields to reach when at least one of the criteria associated with the standard is no longer met: the standard is then considered as lost. 00: 1 field10: 7 fields 01: 3 fields11: 15 fields
Bit 4	Reserved. Must be set to 1.
STI_OK_ONCE_OR_MORE	Number of trials before standard is officially recognized The STI_OK_ONCE_OR_MORE bit is related to the internal standard identification algorithm and provides some flexibility in the standard identification. This bit is operational for all standards. As previously described, up to 8 standards can be entered in the Automatic Standard Identification table. One (or more) standard can be written more than once in that table (e.g. 4 times SECAM and 4 times PAL BGDHI). The complete standard identification table is screened and tried before a decision can be made on identification (one trial per table entry, succesful or not). When a standard has been programmed more than once and when this bit is set, all trials for all entries of that standard in the Automatic Standard Identification table must be successful before the standard is declared identified. When a standard has been programmed more than once and when this bit is reset, the standard is declared identified when at least one trial was successful. (Note that the information presented here only refers to the STI_OK_ONCE_OR_MORE bit. It does not represent the entire standard identification algorithm.)
Bit 2	Reserved. Must be set to 1.
DEM_CKILL_CTRL[1:0]	Color Kill Control The Color Kill Control mode is operational for all TV standards. In Automatic mode, the color is killed until the standard is identified. 00: Automatic (Default)10: Color always killed 01: Color never killed 11: Automatic (Same as 00) with Burst Amplitude control (see DDECCONT0F)

DDECCONTE Register Description

Address (hex): 0Eh

Reset Value (bin): 0010 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [5:0]	Reserved. Must be set to 0.
Bit 6	Reserved. Must be set to 0.
Bit 7	Reserved. Must be set to 0.

DDECCONTF Register Description

Address (hex): 0Fh

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DEM_CKILL_LVL[2:0]			DEM_CKILL_LVL[4:0]				

Bit Name	Function
DEM_CKILL_LVL [2:0]	Reserved. Must be set to 000. Chroma Killer Hysteresis Level The chroma kill mechanism is by default in automatic mode (see ddeccontd[7:0] register). The color is killed on the output when no chroma standard is recognised. This register offers an additional killer feature when in automatic mode. The chroma is killed when the burst amplitude is under the chroma killer automatic level. The chroma is restaured when the chroma burst amplitude is above the threshold plus the programmed hysteresis. When the chroma burst amplitude < dem_ckill_lvl[4:0], the chroma is killed. When the chroma is killed and the chroma burst amplitude > dem_ckill_lvl[4:0] + dem_ckill_lvl[7:5], the chroma is no longer killed.
DEM_CKILL_LVL [4:0]	Reserved. Must be set to 00000. Chroma Killer Automatic Threshold. See above.

DDECCONT10 Register Description

Address (hex): 10h

Reset Value (bin): 0001 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPC_NTSC _FLESH_PH	SPC_NTSC _FLESH_EN						

Bit Name	Function
SPC_NTSC_FLESH_PH	Automatic Flesh Control Phase Reference Selection The Flesh Tone Reference Angle in the [B-Y, R-Y] axis system is either 123° or 117°. 0: Reference Phase is 117° (Default) 1: Reference Phase is 123°
SPC_NTSC_FLESH_EN	Automatic Flesh Control Mode Enable 0: Automatic Flesh Control is disabled. (Default) 1: Automatic Flesh Control is enabled.
Bits [5:0]	Reserved/ Must be set to 01 0000

DDECCONT11 Register Description

Address (hex): 11h

Reset Value (bin): 1000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SYNC_SLICE_LEVEL[3:0]							

Bit Name	Function
SYNC_SLICE_LEVEL[3:0]	Slicing Level Value The horizontal PLL requires a slicing level . This bitfield indicates the slicing level as a fraction between the blanking and the sync tip level. The blanking level is used as the reference level for the clamp mechanism. (See also bit BLANKMODE[1:0] in register DDECCONT1). The sync tip level is computed from the input video signal by the synchronization mechanism. 0000: Slicing Level = Blank Level 1111: Slicing Level = (Blank – sync tip)/16 + sync tip
Bits[3:0]	Reserved. Must be set to 0000.

DDECCONT12 Register Description

Address (hex): 12h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		SPC_NTSC_GREEN_EN	TINTANGLE[4:0]				

Bit Name	Function
Bits[7:6]	Reserved. Must be set to 00.
SPC_NTSC_GREEN_EN	Green Enhancement Mode Enable The Green Enhancement mechanism is applied to the CVBS flow only and is only valid for the NTSC M and the NTSC 4.43 standards. The green tone axis has been defined as flesh tone axis + 90 degrees in the vectorscope representation (i.e. 213 or 207 degrees). Green enhancement is only performed during the active line. Green enhancement operates through saturation increase. Saturation increase factor k is a linear function of the color phase distance to green axis. k = 1 for color phase - green axis = ± 22.5 degrees (minimum value) k = 1.2 for color phase = green axis (maximum value) (k always 1 when color phase not at 22.5 degrees of green axis) 0: Green Enhancement mode is disabled. 1: Green Enhancement mode is enabled.
TINTANGLE[4:0]	Tint Angle The Tint Angle is applied to the Cr and Cb values of the RGB data flow after the RGB to YCrCb conversion. The Tint Angle is coded from -20° to +20° in steps of 1.33°. The bitfield is coded in 2's complement.

DDECCONT13 Register Description

Address (hex): 13h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits[7:0]	Reserved: Must be set to 0000 0000.

DDECCONT14 Register Description

Address (hex): 14h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved: Must be set to 0000 0000.

DDECCONT15 Register Description

Address (hex): 15h

Reset Value (bin): 0001 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				DEM_YC_DELAY[3:0]			

Bit Name	Function
Bits[7:6]	Reserved. Must be set to 00.
Bits[5:4]	Reserved. Must be set to 01.
DEM_YC_DELAY [3:0]	Y vs. C Delay in Chroma Demodulator This bitfield provides a programmable Y path vs. C path delay in the Chroma Demodulator. The unit delay is a quarter of the chroma sub-carrier period. Negative values mean that the luma is in advance compared to the chroma. Bits are coded in 2's complement. 1000: -8 0000: No shift between Chroma and Luma (Default) 0111: +7

DDECCONT16 Register Description

Address (hex): 16h

Reset Value (bin): 0111 1010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SATLMTLN[1:0]		SATLMTPT[1:0]		SMHITH[1:0]		ACTITH[1:0]	

Bit Name	Function
SATLMTLN[1:0] SATLMTPT[1:0]	AGC Saturation Limit (Points/Lines) The SATLMTPT[1:0] and SATLMTLN[1:0] bits are used to program the CVBS Saturation Threshold. It is expressed as a number of samples per field (when, according to the algorithm, the number of samples is reached, the gain is decreased). The formula for the threshold computation is the following: Threshold = 1 + 4 x SATLMTPT[1:0] +16 x SATLMTLN[1:0]
SMHITH[1:0]	AGC SMHI Threshold Value This bitfield defines the Luma Low Signal Detection Threshold (when, according to the algorithm, the luma signal remains under that threshold, the gain is increased). The threshold is defined as an ADC (10 bit) code output according to the following formula: Threshold = 772 + 8 x SMHITH[1:0] (Default = 772 + 8 x 2)
ACTITH[1:0]	AGC ACTI Threshold Value This bitfield defines the Luma Saturation Threshold (when, according to the algorithm, the luma signal overtakes that threshold, the gain is decreased). The threshold is defined as an ADC (10 bit) code output according to the following formula: Threshold = 807 + 8 x ACTITH[1:0] (Default = 807 + 8 x 2)

DDECCONT17 Register Description

Address (hex): 17h

Reset Value (bin): 0010 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			STI_NB_FIELDS_CONFIRM[2:0]				

Bit Name	Function
Bit 7	Reserved. Must be set to 1. Recommended value: 1 (instead of 0 at reset).
Bit 6	Reserved. Must be set to 1.
STI_50_60HZ_ EN	Standard ID Enable This bit modifies the standard identification algorithm. When this bit is set (default), the standard identification algorithm disregards the auto identification table entries not corresponding to the 50 or 60Hz detection performed by the synchronization block.

Bit Name	Function
STI_NB_FIELDS _CONFIRM[2:0]	Number of Fields to be Confirmed This bitfield operates on the second stage of the standard identification algorithm: the confirmation stage. It gives the number of consecutive fields where the standard criteria must be OK before the standard identification is confirmed. 000: 1 field 100: 8 fields 001: 3 fields (default) 101: 32 fields 010: 7 fields 110: 45 fields 011: 10 fields 111: 63 fields
SPC_OVERLOA D_OFF	Cover coefficient forced to 1 The SPC_ACC_OFF and SPC_OVERLOAD_OFF bits are related to the ACC and ACC Overload mechanisms operating on the CVBS flow. These regulating algorithms are a complement to the AGC operating on the CVBS and the Y amplitudes). The ACC and ACC Overload mechanisms operate on the chroma (C) amplitude in the CVBS flow. The ACC (automatic chroma control) operates with the Cburst burst scale factor. The ACC overload mechanism operates with the Cover chroma correction factor. Both Cburst and Cover values are internal variables. The Cover variable carries the maximum chroma value measured during the video line. 0: Cover coefficient is not forced to 1 (Overload mechanism). 1: Cover coefficient is forced to 1.
SPC_ACC_OFF	Cburst coefficient forced to 1 The Cburst variable carries the input video burst amplitude. When that amplitude is different from the standard, demodulated chroma components are scaled with Cburst. Cburst change rate and change steps are also programmable. See registers DDECCONT20[1:0] = SPC_ACC_KTHBURST[1:0] , DDECCONT20[5:4] = SPC_ACC_NB_LINEUP[1:0] , DDECCONT20[7:6] = SPC_ACC_NB_LINEDW[1:0]. 0: Cburst coefficient is not forced to 1 (ACC. mechanism). 1: Cburst coefficient is forced to 1.

DDECCONT18 Register Description

Address (hex): 18h

Reset Value (bin): 0101 1001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	BW_SEL[2:0]			NONINTER LACED_EN	OUT_ RANGE		COMB_ MODE

Bit Name	Function
Bit 7	Reserved. Must be set to 0.
BW_SEL[2:0]	Notch Width Select This register offers the possibility to select the notch width: 000: Notch filter the narrowest 111: Notch filter the widest

Bit Name	Function
NONINTERLACED_EN	Analog Output as Input Bit This bit enables the "analog output as input" mode. It is only operational when the o_vsynctype is set to the analog mode (see register o_ddeccont0[7] bit) When the o_vsynctype is set to the digital mode, that bit is irrelevant. 0: Analog Forced Interlaced Mode. The output is interlaced even if the video input is not. This is equivalent to cut 1.0. It is required by TMM. 1: Analog Output as Input Mode. The output is interlaced when the input is interlaced. The output is not interlaced when the input is not interlaced. (Default)
OUT_RANGE	Output Range Control 0: Output code range is 1 to 254 on Y, Cr and Cb outputs (Default) 1: Output code range is 16 to 235 on Y; and 16 to 240 on Cr and Cb outputs
COMB_MODE	Adaptive Comb or Notch Forced Mode This register selects the Luma Chroma Separation mode. Luma Chroma Separation can be performed by comb filtering or notch filtering. 0: Notch separation mode forced 1: Adaptive comb filter (Default)

DDECCONT19 Register Description

Address (hex): 19h

Reset Value (bin): 0100 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved: Must be set to 0100 0100

DDECCONT1A Register Description

Address (hex): 1Ah

Reset Value (bin): 0010 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits[7:6]	Unused. Must be set to 00.
Bits [5:0]	Reserved: Must be set to 10 0000

DDECCONT1B Register Description

Address (hex): 1Bh

Reset Value (bin): 1000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits[7:4]	Reserved: Must be set to 1000
Bits[3:0]	Reserved: Must be set to 0100

DDECCONT1C Register Description

Address (hex): 1Ch

Reset Value (bin): 1000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits[7:4]	Reserved: Must be set to 1000
Bits[3:0]	Reserved: Must be set to 0100

DDECCONT1D Register Description

Address (hex): 1Dh

Reset Value (bin): 1000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits[7:4]	Reserved: Must be set to 1000
Bits[3:0]	Reserved: Must be set to 1000

DDECCONT1E Register Description

Address (hex): 1Eh

Reset Value (bin): 1001 1001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits[7:4]	Reserved: Must be set to 1001
Bits[3:0]	Reserved: Must be set to 1001

DDECCONT1F Register Description

Address (hex): 1Fh

Reset Value (bin): 0001 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DIRECTPARITY							

Bit Name	Function
DIRECTPARITY	Direct Parity Option This bit selects the option of the direct parity on the F pad. This option is only operational when the stvddec is in the analog output mode (see register DDECCONT0[[7]). The input video parity is detected on every field. The parity issued on the FSYNC pad is normally not this direct parity but is filtered on several fields. 0: Normal parity is issued on the FSYNC pad (Default) 1: Direct parity is issued on the FSYNC pad
Bit 6	Reserved: Must be set to 0.
Bit 5	Reserved: Must be set to 0.
Bit 4	Reserved: Must be set to 1.
Bit 3	Reserved: Must be set to 1.
Bits [2:1]	Reserved: Must be set to 00.
Bit 0	Reserved: Must be set to 0.

DDECCONT20 Register Description

Address (hex): 20h

Reset Value (bin): 0000 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:6]	Reserved: Must be set to 00.
Bits [5:4]	Reserved: Must be set to 00.
Bits [3:2]	Reserved: Must be set to 01.
Bits [1:0]	Reserved: Must be set to 00.

DDECCONT21 Register Description

Address (hex): 21h

Reset Value (bin): 0010 1011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		BLKLINE[1:0]					

Bit Name	Function
Bits[7:6]	Reserved. Must be set to 00.
BLKLINE[1:0]	Optional output blanking lines This register provides additional blanking on lines just before or just after the vertical blanking interval. 00: no additional blanking 01: one line additional blanking 10: 2 lines additional blanking (Default) 11: 3 lines additional blanking
Bits[3:0]	Reserved: Must be set to 1011.

DDECCONT22 Register Description

Address (hex): 22h

Reset Value (bin): 1110 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				HTIMECSTSEL	HSYNCSHIFT_DEL[1:0]		HSYNCSHIFT_EN

Bit Name	Function
Bit 7	Reserved. Must be set to 1.
Bits[6:5]	Reserved. Must be set to 11.
Bit 4	Reserved. Must be set to 0.
HTIMECSTSEL	HPLL Mode Selection 0: Fixed Time Constant mode 1: Automatic mode

Bit Name	Function
HSYNCSHIFT_DEL[1:0]	This register allows a programmable delay of HSYNC output signal. This register is only active when o_hsyncshift_en is active (see register DDECCONT22[0]). 00: (no details yet)
HSYNCSHIFT_EN	Output Synchronisation shift enable 0: No delay (Default) 1: HSYNC is delayed with respect to the digital ouput. Note that this feature has not been decided yet.

DDECCONT23 Register Description

Address (hex): 23h

Reset Value (bin): 1010 1010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:4]	Reserved. Must be set to 1010.
Bits [3:0]	Reserved. Must be set to 1010.

DDECCONT24 Register Description

Address (hex): 24h

Reset Value (bin): 1000 0111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MAX_PJ_AMP[3:0]				ERR_THRESHOLD[2:0]			PJ_EN

Bit Name	Function
Bits [7:4]	Reserved. Must be set to 1000.
Bits [3:1]	Reserved. Must be set to 011.
Bit 0	Reserved. Must be set to 1.

DDECCONT25 Register Description

Address (hex): 25h

Reset Value (bin): 1001 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				HSYNC_SAV	NOISE_THRESHOLD[2:0]		

Bit Name	Function
Bits [7:4]	Reserved. Must be set to 1001.
HSYNC_SAV	HSYNC / SAV This option bit is active when set AND the output mode is an analog mode (see DDECCONT0[7] register). 0: the hsync signal is issued according to the analog mode description 1: the hsync signal coincidates with the SAV code in the digital flow (falling edge on SAV first byte and rising edge on SAV last byte).
NOISE_THRESHOLD[2:0]	HPLL Noise Threshold Selection This bitfield provides a tuning mechanism for HPLL behavior using the detected level of noise as a parameter. This bitfield defines a high noise level. When that high noise level is reached some HPLL features are disabled (phase jumps, copy protection detection). The bitfield can be considered as a cursor where an entry of 000 means that the input signal is above the high noise level, whatever the noise level detected internally. Conversely an entry of 111 means that the input signal is under the high noise level in all circumstances. Between these 2 extremes, a proportion of the detected level of noise (register DDECSTAT3) is the reference for the high noise level.

DDECCONT26 Register Description

Address (hex): 26h

Reset Value (bin): 0100 0100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved. Must be set to 0100 0100.

DDECCONT27 Register Description

Address (hex): 1Eh

Reset Value (bin): 0110 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved. Must be set to 0110 0110.

DDECCONT28 Register Description

Address (hex): 28h

Reset Value (bin): 1000 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HUNLOCK_LINE_NUM[3:0]				HLOCK_LINE_NUM[3:0]			

Bit Name	Function
HUNLOCK_LINE_NUM[3:0]	HPLL number/4 of successive err>thresh for hunlock This register is used by the HPLL. It provides the number of successive lines divided by 4 where the phase error must be above the required threshold to consider the hlock to be lost. The default value is 8 x 4 lines.
HLOCK_LINE_NUM [3:0]	HPLL number/4 of successive err<thresh for hlock This register is used by the HPLL. Its entry is the number of successive lines divided by 4 where the phase error must be below the required threshold before the hlock is acquired (a value of 0001 h = 1 means 4 lines). The default value is 2 x 4 lines.

DDECCONT29 Register Description

Address (hex): 29h

Reset Value (bin): 0101 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
				HLOCK_PH_ER_TH[3:0]			

Bit Name	Function
Bit 7	Reserved. Must be set to 0.
Bit 7	Reserved. Must be set to 1.
Bits [5:4]	Reserved. Must be set to 01.
HLOCK_PH_ER_TH[3:0]	HPLL phase error threshold / 8 for hlock / hunlock This register provides the phase error threshold for the HPLL. The same value is used for the lock and unlock mechanism. The entry value is the number of samples multiplied by 8. The default value is 5 x 8 samples.

DDECCONT2A Register Description

Address (hex): 2Ah

Reset Value (bin): 1000 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLAMP_PROP[1:0]		CLAMP_DER[1:0]			CLAMP_INT[2:0]		

Bit Name	Function
CLAMP_PROP[1:0]	Proportional Gain Selection This register is related to the CVBS clamp regulation algorithm where a PID filter is used. CLAMP_PROP defines the Proportional Gain selection. 00: Proportional Gain divided by 64 01: Proportional Gain divided by 32 10: Proportional Gain divided by 16 11: Proportional Gain divided by 8
CLAMP_DER[1:0]	Defines the Clamp Derivate selection. 00 : 1 01 : 1/2 10 : 1/4 11 : 0
Bit 3	Reserved. Must be set to 0.
CLAMP_INT[2:0]	Clamp Integral Gain Configuration This bitfield is related to the CVBS clamp regulation algorithm where a PID filter is used. This bitfield provides the integral gain selection. The entry is coded as follows: 000: Divided by 64 111: Divided by 5192

DDECCONT2B Register Description

Address (hex): 2Bh

Reset Value (bin): 0110 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved. Must be set to 0110 0011.

DDECCONT2C Register Description

Address (hex): 2Ch

Reset Value (bin): 1000 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved. Must be set to 1000 0010.

DDECCONT2D Register Description

Address (hex): 2Dh

Reset Value (bin): 0000 1010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bit 7	Reserved: Must be set to 0.
Bit 6	Reserved: Must be set to 0.
Bits [5:0]	Reserved: Must be set to 00 1010.

DDECCONT2E Register Description

Address (hex): 2Eh

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bit 7	Reserved: Must be set to 0.
Bit 6	Reserved: Must be set to 0.
Bit 5	Reserved: Must be set to 0.
Bit 4	Reserved: Must be set to 0.
Bit 3	Reserved: Must be set to 0.
Bit 2	Reserved: Must be set to 0.
Bit 1	Reserved: Must be set to 0.
Bit 0	Reserved: Must be set to 0.

DDECCONT2F Register Description

Address (hex): 2Fh

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			OVERDRIVE_MODE	OVERDRIVE_SEL[1:0]			

Bit Name	Function
Bit 7	Reserved: Must be set to 0.
Bits [6:5]	Reserved: Must be set to 00.
OVERDRIVE_MODE	This bit is used for a special proprietary mode between the STV2310 and the STV3500. It is called overdrive mode. Additional VBI data is stuffed between the EAV and the SAV to raise the output clock data. 0: Overdrive output mode disabled 1: Overdrive output mode enabled
OVERDRIVE_SEL[1:0]	Selection of frequency shift in the overdrive mode It is only active when the overdrive mode has been selected. The n value provided by the OVERDRIVE_SEL[1:0] register will determine the number of bytes added in each preamble according to: number of bytes added = n x 32 bytes.
Bit 1	Reserved: Must be set to 0.
Bit 0	Reserved: Must be set to 0.

DDECCONT30 Register Description

Address (hex): 30h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bit 7	Reserved: Must be set to 0.
Bits [6:0]	Reserved: Must be set to 000 0000.

DDECCONT31 Register Description

Address (hex): 31h

Reset Value (bin): 0010 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	AGC_DIS	CVBSAGCGAIN[5:0]					

Bit Name	Function
Bit 7	Reserved: Must be set to 0
AGC_DIS	Disabling AGC 0: Normal mode (AGC is not disabled) 1: Test mode (AGC is disabled) Forced DAC command as specified by CVBSAGCGAIN.
CVBSAGCGAIN [5:0]	Forced value of CVBS AGC when in Forced Mode

DDECCONT32 Register Description

Address (hex): 32h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:4]	Reserved. Must be set to 0000.
Bits [3:0]	Reserved. Must be set to 0000.

DDECCONT33 Register Description

Address (hex): 33h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bit 7	Reserved. Must be set to 0.
Bit [6:0]	Reserved. Must be set to 0000 0000.

DDECCONT34 Register Description

Address (hex): 34h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bit [6:0]	Reserved. Must be set to 0000 0000.

DDECCONT35 Register Description

Address (hex): 35h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLLOCKIT_EN	RGBADJUST_EN	RGBADJUST[5:0]					

Bit Name	Function
PLLLOCKIT_EN	PLLLOCK Pad IT Enable 0: The PLLLOCK pad use is determined by the DDECCONT7 register 1: The PLLLOCK pad is used as the IT pad (in this case, register DDECCONT7 is irrelevant)
RGBADJUST_EN	RGB Gain Adjustment Enable 0: RGB Gain Adjustment mechanism is disabled (Default) 1: RGB Gain Adjustment enabled
RGBADJUST[5:0]	RGB Gain Adjustment Value This adjusts the RGB channel with the CVBS channel. The adjustment gain is expressed as [1 + RGBADJUST]. It is applied on Y, Cr and Cb when in RGB mode. It is applied on Cr and Cb in YCrCb mode. RGBADJUST is coded in 2's complement (+31 to -32). 011111: Maximum positive value of approx. +0.25 000000: RGBADJUST = 0 (Default) 100000: Maximum negative value of approx. -0.25

DDECCONT36 Register Description

Address (hex): 36h

Reset Value (bin): 1111 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLLLOCK_MASK	VLOCK_MASK	HLOCK_MASK	TVSTDID_MASK	FBDEL[3:0]			

Bit Name	Function
PLLLOCK_MASK	Mask for interruption on change of PLLLOCK status
VLOCK_MASK	Mask for interruption on change of VLOCK status
HLOCK_MASK	Mask for interruption on change of HLOCK status
TVSTDID_MASK	Mask for interruption on change of TVSTDID status 0: Interrupt is not masked 1: Interrupt is masked
FBDEL[3:0]	delays the FB signal wrt the RGB flow The delay is coded in 2's complement (from -16 to 15) The Default value is 0, expressed in 4 x f_{SC} clock periods.

DDECCONT37 Register Description

Address (hex): 37h

Reset Value (bin): 1111 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CB_SCALING[1:0]		CR_SCALING[5:0]					

Bit Name	Function
CB_SCALING [1:0]	2 LSB for Scaling Factor for Cb data flow The Cb data flow in the COR block is multiplied by the CB_SCALING factor. (Each LSB of scaling factor = 1/64) when CB_SCALING = 11 1111, the scaling factor = 1 when CB_SCALING = 00 0000, the scaling factor = 1/64
CR_SCALING [5:0]	Scaling Factor for Cr data flow The Cr data flow in the COR block is multiplied by the CR_SCALING factor. (Each LSB of scaling factor = 1/64) when CR_SCALING = 11 1111, the scaling factor = 1 when CR_SCALING = 00 0000, the scaling factor = 1/64

DDECCONT38 Register Description

Address (hex): 38h

Reset Value (bin): 0010 1111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PASSTHROUGH_EN	OUTBEHAV_MOD1	OUTBEHAV_BLANK2	OUTBEHAV_BLANK1	CB_SCALING[5:2]			

Bit Name	Function
PASSTHROUGH_EN	Enable for the pass-through mode The pass-through mode allows (test) lines that are sent during the Vertical Blanking interval to be sent captured by the line memory and reissued.
OUTBEHAV_MOD1	The OUTBEHAV_MOD1 selection bit is used to block the free run mode on the output clock when there is no input video (HLOCK = 0). 0: Free run mode on the output clock when hlock = 0 (Default). The output data is blanked or not during the no video state or the transient state according to the bits OUTBEHAV_BLANK1 and OUTBEHAV_BLANK2. (See above) 1: The output clock follows the search performed by the input PLL. (This mode is mainly used for debug reasons.)
OUTBEHAV_BLANK2 OUTBEHAV_BLANK1	The OUTBEHAV_BLANK1 and OUTBEHAV_BLANK2 selection bits are used to program the STV2310 behaviour when there is no input video (HLOCK = 0) or when there is an input video (HLOCK = 1) but the vertical synchronisation is not yet acquired (VLOCK = 0). They are only operational when OUTBEHAV_MOD1 = 0. This is the normal default mode. OUTBEHAV_BLANK1 = 0, the output FIFO is read when HLOCK = 0 OUTBEHAV_BLANK1 = 1, the output data is blanked when HLOCK = 0 OUTBEHAV_BLANK2 = 0, the output FIFO is read when HLOCK = 1 and VLOCK = 0 OUTBEHAV_BLANK2 = 1, the output data is blanked when HLOCK = 1 and VLOCK = 0

Bit Name	Function
CB_SCALING [5:2]	4 MSBs for Scaling Factor for Cb data flow

DDECCONT39 Register Description

Address (hex): 39h

Reset Value (bin): 0101 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved. Must be set to 0101 0101.

DDECCONT3A Register Description

Address (hex): 3Ah

Reset Value (bin): 0101 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRC_CLK_GEN[15:8]							

Bit Name	Function
Bits [7:0]	Reserved. Must be set to 0101 0101.

DDECCONT3B Register Description

Address (hex): 3Bh

Reset Value (bin): 0011 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved. Must be set to 0011 0101.

DDECCONT3C Register Description

Address (hex): 3Ch

Reset Value (bin): 1111 1100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VSYNCNSTD_MASK	TRICKDET_MASK	INTERDET_MASK	VCRDET_MASK	INSERDET_MASK	FBDET_MASK		

Bit Name	Function
VSYNCNSTD_MASK	Mask for interruption on change of status on VSYNCLOC_NSTD. 0: Interrupt is not masked 1: Interrupt is masked
TRICKDET_MASK	Mask for interruption on change of status on TRICKMODE_DETECTED. 0: Interrupt is not masked 1: Interrupt is masked
INTERDET_MASK	Mask for interruption on change of status on INTERLACED_DETECTED. 0: Interrupt is not masked 1: Interrupt is masked
VCRDET_MASK	Mask for interruption on change of status on VCR_DETECTED. 0: Interrupt is not masked 1: Interrupt is masked
INSERDET_MASK	Mask for interruption on change of status on INSER_DETECTED. 0: Interrupt is not masked 1: Interrupt is masked
FBDET_MASK	Mask for interruption on change of status on FB_DETECTED. 0: Interrupt is not masked 1: Interrupt is masked
Bits [1:0]	Reserved. Must be set to 00.

5.3 VBI Control Register Descriptions

VBICONT1 Register Description

Address (hex): 3Dh

Reset Value (bin): 0000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		SLDID[5:0]					

Bit Name	Function
Bits[7:6]	Reserved. Must be set to 00.
SLDID[5:0]	Bitfield Description DID value used by the STV2310 for coding ancillary packets. (The default value is type 2, first code reserved for 8-bit applications).

VBICONT2 Register Description

Address (hex): 3Eh

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		SLFIL[5:0]					

Bit Name	Function
Bits[7:6]	Reserved. Must be set to 00.
SLFIL[5:0]	Bitfield Description Filler value used by the STV2310 for coding the filler byte in the ancillary packets. The default value is 80.

VBICONT3 Register Description

Address (hex): 3Fh

Reset Value (bin): 1000 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	SLICECOMP_EN	RAWFILTOFF_EN	WSTSLICING_EN		WSTCUSTOMFRAM	WSTEXTLINES	WSTALLPACKETS

Bit Name	Function
Bit 7	Reserved. Must be set to 1.
SLICECOMP_EN	On the fly slicing level computation enable (only for TXT decoding)
RAWFILTOFF_EN	Hamming filtering bypass in raw mode for TXT reception 0: The filtering is active in raw mode (Default) 1: The filtering is bypassed in raw mode
WSTSLICING_EN	WST Slicing Enable 0: (WST) data slicing is disabled 1: (WST) data slicing is authorised Note that this bit is used at the top level to control the equalizer
WSTCUSTOMFRAM	WST search with new framing code enable 0: The new framing code is not enabled 1: The new framing code (provided in register VBICONT4[7:0] = SLCORE[15:8]) is enabled
WSTEXTLINES	WST extended slicing window enable 0: 1: The WST search starts at line 2
WSTALLPACKETS	WST slicing of all packets enable 0: Only service packets X/30 and X/31 are sampled 1: all packets are sampled

VBICONT4 Register Description

Address (hex): 40h

Reset Value (bin): 0010 0111

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRAMINGCODE[7:0]							

Bit Name	Function
FRAMINGCODE[7:0]	New Frame Code Value

VBICONT5 Register Description

Address (hex): 41h

Reset Value (bin): 1100 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WSSF1ONLY_EN	VPS1ONLY_EN			VPSSLICING_EN	VPSEXTLINES	WSSSLICING_EN	WSSEXTLINES

Bit Name	Function
WSSF1ONLY_EN	
VPS1ONLY_EN	
Bit 5	Reserved. Must be set to 0
Bit 4	Reserved. Must be set to 0
VPSSLICING_EN	VPS Slicing Enable 0: (VPS) data slicing is disabled 1: (VPS) data slicing is enabled
VPSEXTLINES	VPS Extended Line 0: VPS data is expected only in line 16 1: VPS data is expected in lines 15, 16, 17 (not necessarily all of them)
WSSSLICING_EN	WSS Slicing Enable 0: (WSS) data slicing is disabled 1: (WSS) data slicing is enabled
WSSEXTLINES	WSS Extended Line 0: WSS data is expected only in line 23 1: WSS data is expected in lines 21, 22, 23, 24 (not necessarily all of them)

VBICONT6 Register Description

Address (hex): 42h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	GMVBILINES	GMRELAX_EN	GMSLICING_EN		CCVBILINES	CCRELAX_EN	CCSLICING_EN

Bit Name	Function
GMVBILINES	GM VBI Slicing Enable 0: Data slicing is active on line 21 in 60Hz and line 22 in 50Hz 1: Data slicing is authorised during the whole VBI
GMRELAX_EN	GEM-US Relaxed Frame Check Enable 0: Relaxed frame check is disabled 1: Relaxed frame check is enabled
GMSLICING_EN	GEM-US Slicing Enable 0: Data slicing is disabled (Gem = Gemstar) 1: Data slicing is enabled
CCVBILINES	CC VBI Slicing Enable 0: Data slicing is running only during the line 21 in 60Hz and line 22 in 50Hz. 1: Data slicing is authorised during the entire VBI
CCRELAX_EN	CC Relaxed Frame Check Enable 0: Relaxed Framecheck is disabled 1: Relaxed Framecheck is enabled
CCSLICING_EN	CC Slicing Enable 0: Data slicing is disabled 1: Data slicing is enabled

VBICONT7 Register Description

Address (hex): 43h

Reset Value (bin): 0000 1101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved. Must be set to 0000 1101.

VBICONT8 Register Description

Address (hex): 44h

Reset Value (bin): 0000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						SLHY[9:8]	

Bit Name	Function
Bits [1:0]	Reserved. Must be set to 00.
Bits [4:2]	Reserved. Must be set to 010.
Bits [7:5]	Reserved. Must be set to 000.

VBICONT9 Register Description

Address (hex): 45h

Reset Value (bin): 0110 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:5]	Reserved. Must be set to 011.
Bits [4:0]	Reserved. Must be set to 0 0011.

VBICONT0A Register Description

Address (hex): 46h

Reset Value (bin): 0001 1100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved. Must be set to 0001 1100.

VBICONT0B Register Description

Address (hex): 47h

Reset Value (bin): 0100 0110

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bit 7	Reserved. Must be set to 0.
Bit 6	Reserved. Must be set to 1.
Bit 5	Reserved. Must be set to 0.

Bit Name	Function
Bits[4:3]	Reserved. Must be set to 00.
Bit 2	Reserved. Must be set to 1.
Bit 1	Reserved. Must be set to 1.
Bit 0	Reserved. Must be set to 0.

VBICONT0C Register Description

Address (hex): 48h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits[7:0]	Reserved. Must be set to 0001 1011.

VBICONT0D Register Description

Address (hex): 49h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved: Must be set to 0001 1011.

VBICONT0E Register Description

Address (hex): 4Ah

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved: Must be set to 0001 1011.

VBICONT0F Register Description

Address (hex): 4Bh

Reset Value (bin): 1011 0011

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CGSEW[2:0]			CGNBS[1:0]		CGNBI[2:0]		

Bit Name	Function
CGSEW[2:0]	Interval width for the shift compansation
CGNBS[1:0]	Number of sample rate for a bit "10" for 1 sample keep every 3
CGNBI[2:0]	Number of Run-in Bytes before to start CCP/GEM slice states machine

VBICONT10 Register Description

Address (hex): 4Ch

Reset Value (bin): 0000 1000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CGESPF2	CGESPF1	CGVS[5:0]					

Bit Name	Function
CGESPF2	Enable the two pulse spike filter
CGESPF1	Enable the one pulse spike filter
CGVS[5:0]	Number of sample for a bit

VBICONT11 Register Description

Address (hex): 4Dh

Reset Value (bin): 0111 0001

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:4]	Reserved. Must be set to 0111.
Bits [3:0]	Reserved. Must be set to 0001.

VBICONT12 Register Description

Address (hex): 4Eh

Reset Value (bin): 0000 1100

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bit 7	Reserved. Must be set to 0.
Bit 6	Reserved. Must be set to 0.
Bits [5:0]	Reserved. Must be set to 1100.

VBICONT13 Register Description

Address (hex): 4Fh

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WSTH[7:0]							

Bit Name	Function
WSTH[7:0]	Hysteresis value for Teletext Slicer

VBICONT14 Register Description

Address (hex): 50h

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						WSTH[9:8]	

Bit Name	Function
Bits[7:2]	Reserved. Must be set to 00 0011.
WSTH[9:8]	Hysteresis value for Teletext Slicer

VBICONT15 Register Description

Address (hex): 51h

Reset Value (bin): 0001 0101

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bits [7:0]	Reserved. Must be set to 0001 0101.

VBICONT16 Register Description

Address (hex): 52h

Reset Value (bin): 1010 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	EQZPRGMODE	EQZORDERSEL					

Bit Name	Function
Bit 7	Reserved. Must be set to 0.
EQZPRGMODE	0: Coefficients set not programmable 1: Coefficients set programmable. When set, the table of coefficients can be programmed. The selection of each coefficients is done with VBI_EQUALCOEFF[2:0]
EQZORDERSEL	0: Second order filter is used 1: First order filter is used
Bits [4:0]	Reserved. Must be set to 0 0000.

VBICONT17 Register Description

Address (hex): 53h

Reset Value (bin): 0101 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VBI_EQUALCOEFF[2:0]							

Bit Name	Function
VBI_EQUALCOEFF[2:0]	These bits select precomputed coefficients for the equaliser or let the equaliser select automatically the best set of coefficients or impose to the equaliser the sets of coefficients programmed 000: use set 1 of coefficients 001: use set 2 of coefficients 010: use set 3 of coefficients (central or no equaliser) 011: use set 4 of coefficients 100: equaliser in automatic mode 101: use set 5 of ceofficients 110: use programmed registers (see registers VBICONT0D and VBICONT0E) for the equaliser coefficients.
Bit 4	Reserved. Must be set to 1.
Bits [3:0]	Reserved. Must be set to 0000.

VBICONT18 Register Description

Address (hex): 54h

Reset Value (bin): 0001 0010

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Bit Name	Function
Bit 7	Reserved. Must be set to 0.
Bit 6	Reserved. Must be set to 0.
Bit 5	Reserved. Must be set to 0.
Bit 4	Reserved. Must be set to 1.
Bits [3:0]	Reserved. Must be set to 0010.

5.4 Acknowledge Registers

The acknowledge registers are used to acknowledge the interruption source. When ACK = 1, the I²C master acknowledges the corresponding interrupt.

Warning : These 2 registers can be written by the I2C but can't be read. Each bit is reset by the I2C slave (stv2310) one clock period after an high level has been detected.

DDECCONTFE Register Description

Address (hex): 7Eh - Write Only

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTERDET_ACK	VCRDET_ACK	INSERDET_ACK	FBDET_ACK	PLLLOCK_ACK	VLOCK_ACK	HLOCK_ACK	TVSTDID_ACK

Bit Name	Function
INTERDET_ACK	Acknowledge for interrupt on INTERLACED_DETECTED status change
VCRDET_ACK	Acknowledge for interrupt on VCR_DETECTED status change
INSERDET_ACK	Acknowledge for interrupt on INSER_DETECTED status change
FBDET_ACK	Acknowledge for interrupt on FB_DETECTED status change
PLLLOCK_ACK	Acknowledge for interrupt on PLLLOCK status change
VLOCK_ACK	Acknowledge for interrupt on VLOCK status change
HLOCK_ACK	Acknowledge for interrupt on HLOCK status change
TVSTDID_ACK	Acknowledge for interrupt on TVSTDID status change

DDECCONTFF Register Description

Address (hex): 7Eh - Write Only

Reset Value (bin): 0000 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
						VSYNCNSTD_ACK	TRICKDET_ACK

Bit Name	Function
Bits[7:3]	Reserved.
Bit 2	Reserved
VSYNCNSTD_ACK	Acknowledge for interrupt on VSYNCLOCK_NOSTD status change
TRICKDET_ACK	Acknowledge for interrupt on TRICKMODE_DETECTED status change

5.5 Status Registers

DDECSTAT1 Register Description

Address (hex): 80h - Read Only

Reset Value (bin): 0001 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STVDDECVERS[7:0]							

Bit Name	Function
STVDDECVERS [7:0]	This block is hardwired in every STV2310 cut. [7:4]: for Full Layer cuts (0001 is Cut 1.0, 0010 is Cut 2.0) [3:0]: for Metal Fix cuts

DDECSTAT2 Register Description

Address (hex): 81h - Read Only

Reset Value (bin): Undefined

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VLOCK	HLOCK	PLLLOCK	5060ID	TVSTDID	TVSTD[2:0]		

Bit Name	Function
VLOCK	Flag used to signal Vertical Synchronization Signal Capture 0: Vsync is not captured 1: Vsync is captured
HLOCK	Flag used to signal Horizontal PLL (detection) lock status 0: HPLL is out of lock 1: HPLL is in lock
PLLLOCK	Flag used to signal Output PLL (line-locked) status 0: Output PLL is out of lock 1: Output PLL is in lock
5060ID	Flag used to signal detection of either 50 Hz or 60 Hz signal 0: 60 Hz signal is detected. 1: 50 Hz signal is detected.
TVSTDID	Flag used to signal that standard is identified 0: Standard is not identified. 1: Standard is identified.
TVSTD[2:0]	Identification (code) of Identified Standard See the AUTOSTD[5:0] bits in the DDECCONT1 register.

DDECSTAT3 Register Description

Address (hex): 82h - Read Only

Reset Value (bin): Undefined

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VSYNCLOC_NSTD	BLANKLVL_SHIFT_DETECTED	INTERLACED_DETECTED	DVD_DETECTED	VCR_DETECTED	INSER_DETECTED	FB_DETECTED	TRICKMOD_DETECTED

Bit Name	Function
VSYNCLOC_NSTD	The synchronisation block normally detects the input video parity by detecting the Vsync position with respect to the Hsync. The Vsync position is normally at the beginning of line (0%) or middle of line (50%). The built-in thresholds for Vsync position are 25% and 75%. When the Vysnc is actually close to these limits, a bad parity detection may take place. This is the reason for this status bit. When set, the Vsync is positioned between 20% - 30% OR 70%-80% of input video line.
BLANKLVL_SHIFT_DETECTED	When set, this bit indicates that the input video blank level is shifted during the VBI. This detection only takes place when the shift is above a determined threshold and there is a low level of noise.
INTERLACED_DETECTED	When set, this bit indicates that the input video is interlaced. When reset the input video is non interlaced. This bit can potentially change value at each input video field
DVD_DETECTED	When set, this bit indicates that a DVD has been detected on the input.
VCR_DETECTED	When set, this bit indicates that a VCR has been detected on the input.

Bit Name	Function
INSER_ DETECTED	When set, this bit indicates that a transition on the FB signal has been detected inside an active line at least once in the field. This flag remains set for the next field.
FB_DETECTED	When set, this bit indicates that the FB signal has been detected to 1 (level detection) at least once in the field. This flag remains set for the next field.
TRICKMOD_ DETECTED	This status bit purpose is to detect special VCR playback modes where the number of lines is non standard. (note that it is not limited to VCR inputs). The standard number of lines depend on the 50Hz/60Hz detection: When in 50Hz mode, the number of lines is standard when >= 310 and <= 314 When in 60Hz mode, the number of lines is standard when >= 260 and <= 264 When this bit is set, the number of lines is non-standard.

DDECSTAT4 Register Description

Address (hex): 83h - Read Only

Reset Value (bin): Undefined

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
NOISELVL[7:0]							

Bit Name	Function
NOISELVL[7:0]	Noise level computed by sync and monitoring block

DDECSTAT5 Register Description

Address (hex): 84h - Read Only

Reset Value (bin): Undefined

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLDID[7:0]							

Bit Name	Function
SLDID[7:0]	Replica (read only) of bits SLDID[5:0] in register VBICONT1 with parity and checksum

DDECSTAT6 Register Description

Address (hex): 85h - Read Only

Reset Value (bin): Undefined

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SLFIL[7:0]							

Bit Name	Function
SLFIL[7:0]	Reserved.

DDECSTAT7 Register Description

Address (hex): 86h - Read Only

Reset Value (bin): Undefined

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		GEM_DETECTED	CC_DETECTED	VPS_DETECTED	WST_DETECTED	WSS_DETECTED	OPENLOOP

Bit Name	Function
Bit 7	Reserved.
Bit 6	Reserved.
GEM_DETECTED	Detection of gemstar ancillary data
CC_DETECTED	Detection of close caption ancillary data
VPS_DETECTED	Detection of VPS ancillary data
WST_DETECTED	Detection of WST ancillary data
WSS_DETECTED	Detection of WSS ancillary data
OPENLOOP	This flag indicates that the output PLL uses phase jumps for phase error correction. 0: Phase jump inactive 1: Phase jump active

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{3.3V}$	3.3 V Supply Voltage			3.8	V
$V_{1.8V}$	1.8 V Supply Voltage			2.2	V
V_{ESD}	Capacitor 100 pF discharged via 1.5 kΩ serial resistance (Human Body Model)			±4	kV
T_{OPER}	Operating Temperature	0		+70	°C
T_{STG}	Storage Temperature	-55		+150	°C

6.2 Thermal Data

Symbol	Parameter	Min.	Typ.	Max.	Unit
R_{thJA}	Junction-ambient Thermal Resistance (TQFP64, 14x14x1.4mm) two layer PCB, one copper ground layer		50		°C/W
R_{thJA}	Junction-ambient Thermal Resistance (TQFP64, 10x10x1.4mm) two layer PCB, one copper ground layer		60		°C/W

6.3 Operating Conditions

Symbol	Parameter	Min.	Typ.	Max	Unit
$V_{1.8V}$	1.8 V Supply Voltage	1.6	1.8	2.0	V
$V_{3.3V}$	3.3 V Supply Voltage	3.0	3.3	3.6	V
f_{MC}	Master Clock Frequency		27		MHz
$I_{CC1.8V}$	1.8V Supply Current		235		mA
$I_{CC3.3V}$	3.3V Supply Current		40		mA

6.4 CVBS/Y/C Analog Inputs

T_{AMB} = 25 °C, V_{CC33} = 3.3 V, V_{CC18} = 1.8 V

Symbol	Parameter	Min.	Typ.	Max	Unit
$V_{IN\_CVBS/Y}$	Y/CVBS Sync to Peak Chroma Input Voltage (Anti-Aliasing Filter with Attenuation = 0.75, Standard Color bar 100%); AGC active	.74	1.24	2.08	V_{PP}
AGC	AGC Range on Y/CVBS inputs		±6		dB
G_Step	AGC Step		0.19		dB

Symbol	Parameter	Min.	Typ.	Max	Unit
V_{IN_Chroma}	C Full Scale Input Voltage (before external Anti-Aliasing Filter with Attenuation = 0.55)	0.6	0.88	1.25	V_{PP}
C_{IN_CVBS}	Input Coupling Capacitor for CVBS		22		nF
C_{IN_C}	Input Coupling Capacitor for C		1		nF
BW_{CVBS}	Input Bandwidth Analog Input		6		MHz
CL_{CVBS}	CVBS/Y Input Black Clamping Level		1.0		V
C_{BIAS}	C Input Bias Level		560		mV
I_{SOURCE}	Positive Clamp Current (CVBS/Y)	+200		+400	µA
I_{SINK}	Negative Clamp Current (CVBS/Y)	-400		-200	µA
I_Step	I Step Clamp		±5		µA
Z_{IN}	C Input Impedance		10		kOhm
Crosstalk	Channel Crosstalk		50		dB

6.5 R/G/B and Cr/Cb Inputs

Symbol	Parameter	Min.	Typ.	Max	Unit
V_{IN_RGB}	R/G/B Full Scale Input Voltage (before external Anti-Aliasing Filter with Attenuation = 0.65)	0.5	0.7	1.0	V_{PP}
CL_{RGB}	R/G/B Input Clamp Level		1.0		V
C_{IN_RGB}	Input Coupling Capacitor		22		nF
BW_{RGB_L}	Channel Bandwidth on Luma Component		6		MHz
BW_{RGB_Chr}	Channel Bandwidth on CrCb Component		3		MHz
V_{IN_CrCb}	Cr/Cb Full Scale Input Voltage (before external Anti-Aliasing Filter with Attenuation = 0.65)	0.5	0.7	1.0	V_{PP}
CL_{CrCb}	Cr/Cb Clamp Level		1.3		V
I_{SOURCE}	Positive Clamp Current (RGB)	+200		+400	µA
I_{SINK}	Negative Clamp Current (RGB)	-400		-200	µA
	I Step Clamp		±5		µA
Crosstalk	Crosstalk between Analog Inputs		50		dB

6.6 FB Input

Symbol	Parameter	Min.	Typ.	Max	Unit
V_{IL}	FB Input Voltage Low Level			0.4	V
V_{IH}	FB Input Voltage High Level	1.0			V
I_L	FB Input Leakage Current			1	µA

6.7 Analog-to-Digital Converter (ADC)

Symbol	Parameter	Min.	Typ.	Max	Unit
10-bit ADC for CVBS Input					
B	Analog Bandwidth		15		MHz
f_{CLK}	ADC Clock Frequency		27		MHz
E_D	Differential Linearity Error (DLE)		1		LSB
E_L	Integral Linearity Error (ILE)		2		LSB
8-bit ADCs for RGB/C Inputs					
B	Analog Bandwidth		15		MHz
f_{CLK}	ADC Clock Frequency		27		MHz
E_D	Differential Linearity Error (DLE)		1		LSB
E_L	Integral Linearity Error (ILE)		2		LSB
G_{match}	RGB Gain Matching		0.5	1.5	%

6.8 Analog Reference Levels

Symbol	Parameter	Min.	Typ.	Max	Unit
REFP_CVBS	REFP_CVBS Pin Level		750		mV
Videocomm	Videocomm Pin Level		1.2		V
REFP_RGB	REFP_RGB Pin Level		750		mV
REFM_RGB	REFM_RGB Pin Level		375		mV

6.9 YCrCb, Hsync, Vsync, Field and PLL Lock Outputs

Symbol	Parameter	Min.	Typ.	Max	Unit
V_{OL}	Low Level Output Voltage (I_{OUT} = 2 mA)			0.4	V
V_{OH}	High Level Output Voltage (I_{OUT} = 2 mA)	2.4			V
t_r	Rise Time		3		ns

Symbol	Parameter	Min.	Typ.	Max	Unit
t_f	Fall Time		3		ns
	Maximum Capacitive Load			30	pf

6.10 Clock Data Output

Symbol	Parameter	Min.	Typ.	Max	Unit
V_{OL}	Low Level Output Voltage (I_{OUT} = 4 mA)			0.4	V
V_{OH}	High Level Output Voltage (I_{OUT} = 4 mA)	2.4			V
t_r	Rise Time		3		ns
t_f	Fall Time		3		ns
	Maximum Capacitive Load			30	pf

6.11 CLKSEL, TST_MODE, $\overline{\text{NRESET}}$ and I2CADD Inputs

Symbol	Parameter	Min.	Typ.	Max	Unit
CLKSEL Input					
V_{IL}	CLKSEL Input Voltage Low Level			0.6	V
V_{IH}	CLKSEL Input Voltage High Level	1.2			V
I_L	CLKSEL Input Leakage Current			1	µA
TST_MODE, $\overline{\text{NRESET}}$ and I2CADD Inputs					
V_{IL}	Input Low Level			0.8	V
V_{IH}	Input High Level	2.0			V
I_L	Input Leakage Current	-1.0		1.0	µA

6.12 Main Clock Characteristics

Symbol	Parameter	Min.	Typ.	Max	Unit
Differential Clock Input (CLKXTM, CLKXTP)					
F_S	Nominal Frequency		27		MHz
F_{S_TOL}	Tolerance (including Temp. shift)		±50		ppm
Duty_cycle	Clock Duty Cycle	45		50	%
V_{IL}	Input Voltage Low Level			0.6	
V_{IH}	Input Voltage High Level	1.2			
I_L	Input Leakage Current			1	µA
External Crystal Characteristics					

Symbol	Parameter	Min.	Typ.	Max	Unit
f_{XTAL}	Crystal Frequency, Fundamental Mode		27		MHz
R_{BIAS}	Internal Bias Resistance		1.5		MΩ
	Tolerance (including Temp. shift)			±60	ppm

6.13 Horizontal/Vertical Synchronization Block

Symbol	Parameter	Min.	Typ.	Max	Unit
	Output Luma/Sync Misalignment			±2.5	ns
	Output Chroma/Sync Misalignment			±20	ns
	Line PLL Capture Range			±8	%

6.14 Chroma Block

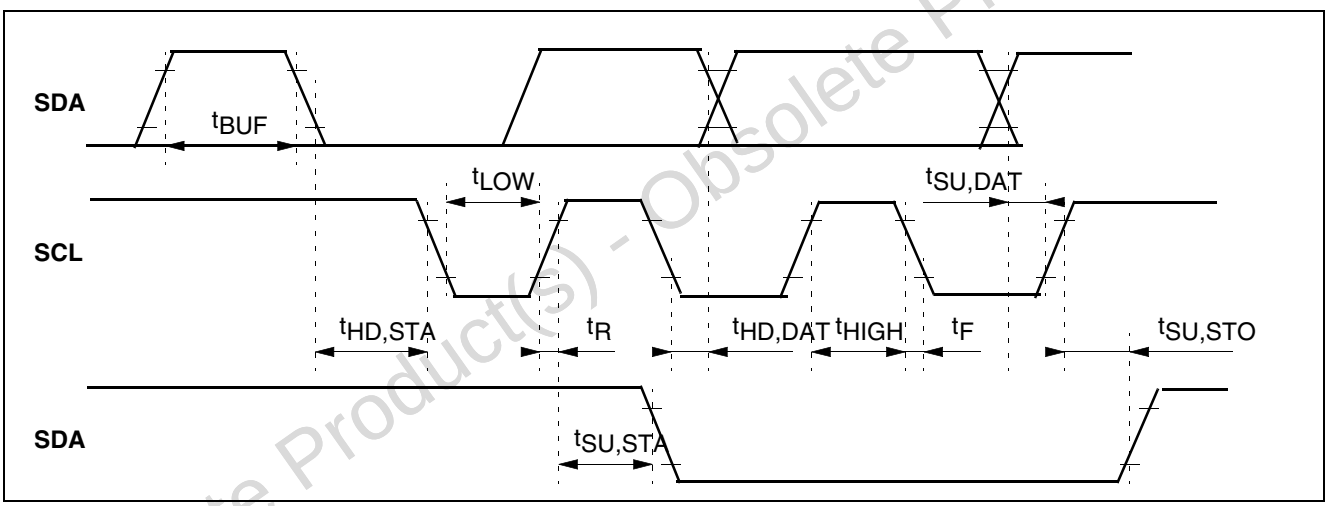
Symbol	Parameter	Min.	Typ.	Max	Unit
	ACC Control Range	-6		+30	dB
	Chroma PLL Capture Range	0.8		1	kHz
	Total Chroma Phase Tracking Error		±0.5	±1	deg.
	Quadrature Error		±0.5	±1	deg.
	Hue Control Range			±40	deg
	Hue Control Step		1.5		deg.

6.15 I²C Bus Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
SCL						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		2.3		5.5	V
I_{IL}	Input Leakage Current	V_{IN} = 0 to 5.0 V	-10		10	µA
f_{SCL}	Clock Frequency				400	kHz
t_R	Input Rise Time	1 V to 2 V			300	ns
t_F	Input Fall Time	2 V to 1 V			300	ns
C_I	Input Capacitance				10	pF
SDA						
V_{IL}	Low Level Input Voltage		-0.3		1.5	V
V_{IH}	High Level Input Voltage		2.3		5.5	V
I_{IL}	Input Leakage Current	V_{IN} = 0 to 5.0 V	-10		10	µA
t_R	Input Rise Time	1 V to 2 V			300	ns
t_F	Input Fall Time	2 V to 1 V			300	ns
V_{OL}	Low Level Output Voltage	I_{OL} = 3 mA			0.4	V
t_F	Output Fall Time	2 V to 1 V			250	ns

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
C_L	Load Capacitance				400	pF
C_I	Input Capacitance				10	pF
I²C Timing						
t_{LOW}	Clock Low period		1.3			µs
t_{HIGH}	Clock High period		0.6			µs
$t_{SU,DAT}$	Data Set-up Time		100			ns
$t_{HD,DAT}$	Data Hold Time		0		900	ns
$t_{SU,STO}$	Set-up Time from Clock High to Stop		0.6			µs
t_{BUF}	Start Set-up Time following a Stop		1.3			µs
$t_{HD,STA}$	Start Hold Time		0.6			µs
$t_{SU,STA}$	Start Set-up Time following Clock Low to High Transition		0.6			µs

Figure 19: I²C Bus Timing



Note: The STV2310 device can be interfaced with +3.3 V or +5.0 V logic levels.

7 Package Mechanical Data

7.1 TQFP64 14x14 Package

Figure 20: TQFP64 14x14 Package

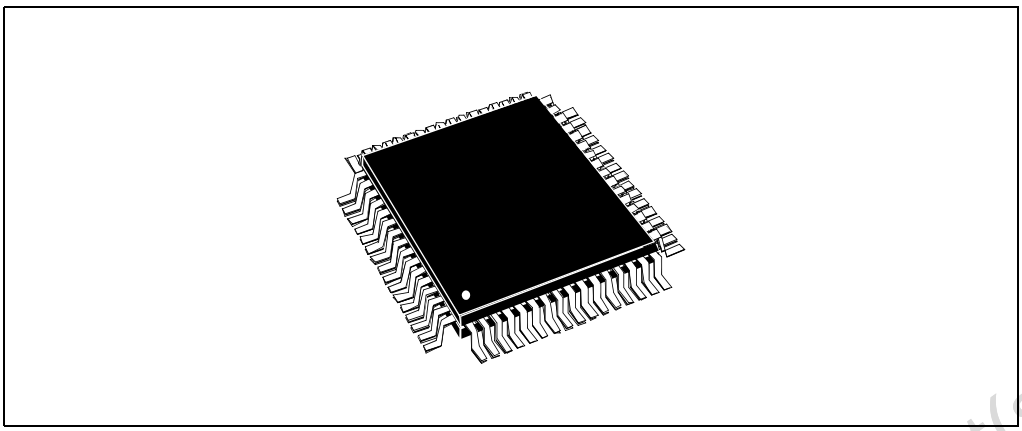
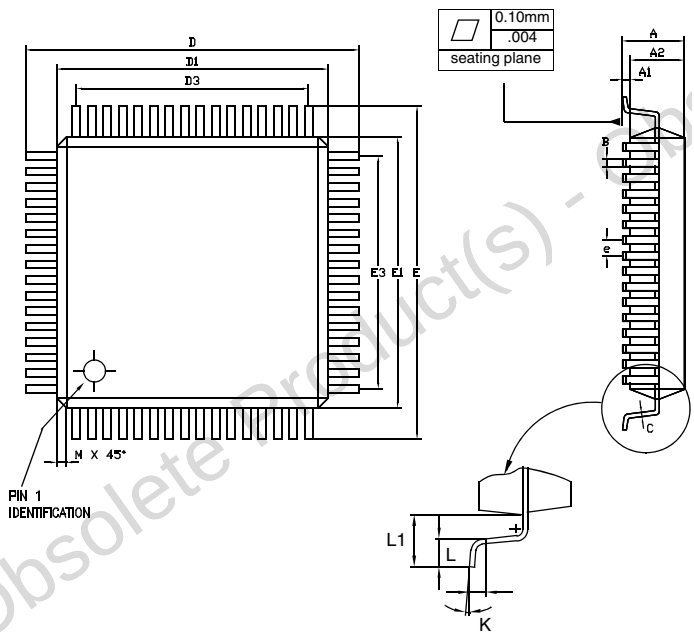


Figure 21: 64-Pin Thin Quad Flat Package



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
e		0.80			0.031	
K	0°	3.5°	7°			
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64		ND	16	NE	16

7.2 TQFP64 10x10 Package

Figure 22: TQFP64 10x10 Package

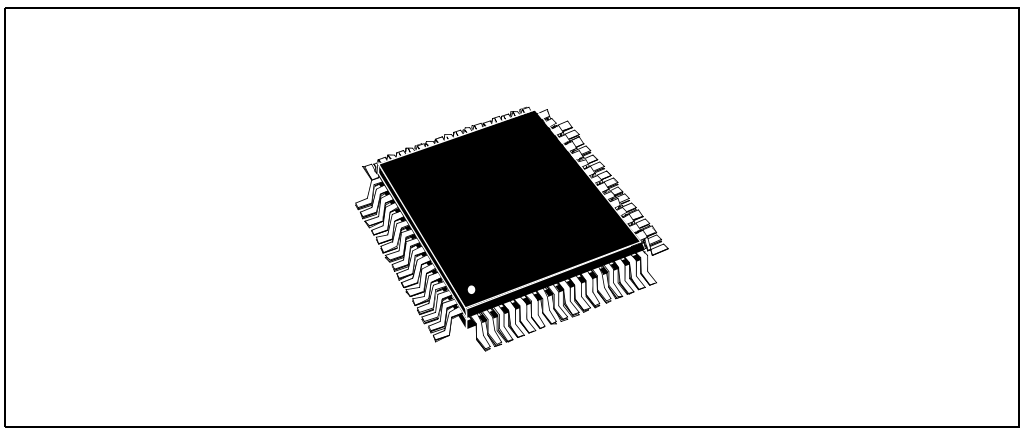
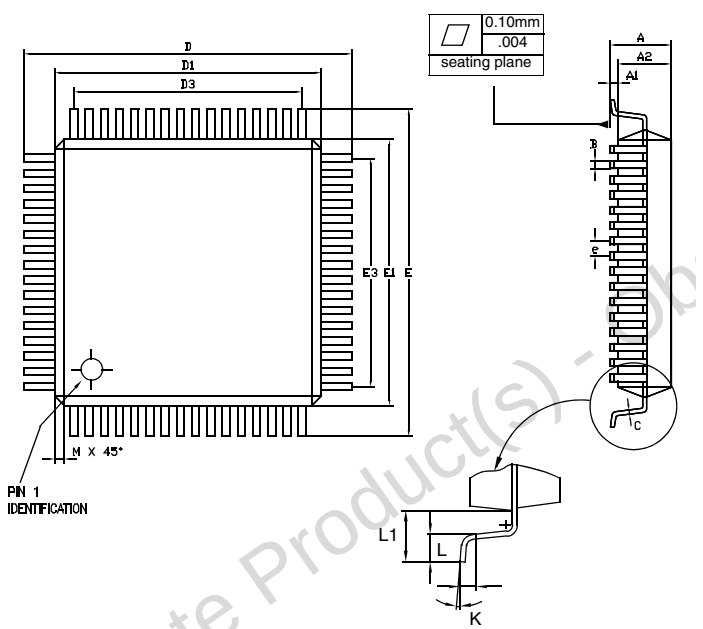


Figure 23: 64-Pin Thin Quad Flat Package



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of Pins					
N	64		ND	16	NE	16

7.3 Lead-free Packaging

To meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com.*

8 Revision History

The following table summarizes the modifications applied to this document.

Revision	Description	Date
1.0	First Issue	N/A
1.1	Addition of Section 5.3: VBI Control Register Descriptions on page 87.	March 2001
1.2	Addition of Chapter 7: Package Mechanical Data on page 108.	March 2001
1.3	Addition of Section 4.5: Standard Research Sequence Programming on page 21, Section 4.9: Output Scaler and Format Converter on page 25, Section 4.3: Input Sample Rate Conversion on page 18 and Section 6: Electrical Characteristics on page 101	9 May 2001
1.4	Update of all register descriptions, general descriptions and programming information. Pin description section reformatted. Addition of Anti-Aliasing Filter Diagrams.	June 2001
1.5	Update of all register descriptions, general descriptions and programming information.	July 2001
1.6	Update of Figure 9 and Analog Input Stage programming data.	July 2001
1.7	Reset values corrected in Register Descriptions and register DDECCONT35 updated with Cut 2 information. Section 6: Electrical Characteristics on page 101 updated. Figure 35 updated. Moved to Datasheet template 2.1 and converted from single file to book format.	November 2001
1.8	Updated Figure 18 on page 31 and Figure 3 on page 8, Zoom in/out function characteristics clarified. Addition of ESD PERFORMANCES on page 80.	
1.9	SECAM filter is removed. Registers DDECCONT2A, DDECCONT17 and DDECCONTE modified.	12 February 2002
2.0	Update of Section 6: Electrical Characteristics on page 101.	25 March 2002
2.1	ESD Section removed.	10 July 2002
2.2	Pin NRESET changed to $\overline{\text{NRESET}}$. Updated register information for cut 3.0.	21 Nov 2002
2.3	Updated Figure 3 on page 8 and Figure 6 on page 15.	
2.4	Updated Figure 3 on page 8 and Figure 4 on page 9. Update to VCC33OUT in Section 2.2: Pin Descriptions. Update of Figure 6 on page 15. Ouput Sync Pulse information added to Section 4.2: Synchronization and Monitoring Unit on page 16. Update of Section 4.4: Luminance and Chrominance Separation on page 19. Update of Table 8: Confirmation Codes on page 22. New section added: Section 4.6: Standard Identification on page 23. Update of Section 4.7: Chroma Demodulation on page 23. Update of Section 4.8: Soft Mixer on page 24.Update of Section 4.12: Output FIFO and Line-locked Ouput Pixel Clock Generator on page 29. G_{DIFF} added to Section 6.7: Analog-to-Digital Converter (ADC) on page 103. Updated Figure 35 and Figure 36.	20 January 2003
3.0	Re-organisation and update of page 1 and page 2. Modification of text in Section 1: General Description on page 6. Updated Figure 2 on page 7, Figure 3 on page 8 and Figure 4 on page 9. Modification of pin descriptions in Section 2: Pin Allocation and Description on page 9. Addition of Section 3: Default Setup At Reset on page 13. Major updates to Chapter 5: Register List on page 80. Major change to Figure 6 on page 15. Various modifications to Chapter 6: Electrical Characteristics on page 134. Addition of TQFP64 10x10 package in Chapter 8: Package Mechanical Data on page 143.	July 2004

Revision	Description	Date
3.1	Minor updates to Register Description	December 2004
4.0	Section 7.3 added, disclaimer updated. Technical content unaffected.	07-Nov-2008

Index

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

STMicroelectronics:

STV2310D