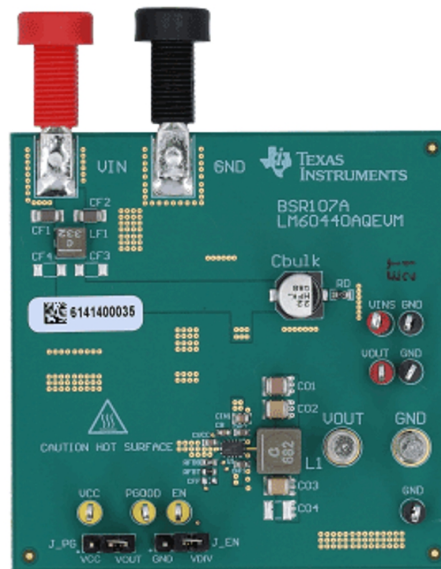


## LM60440AQEVM User's Guide

The Texas Instruments LM60440AQEVM evaluation module helps designers evaluate the operation and performance of the LM60440-Q1 wide-input buck converters. The LM60440-Q1 is an easy-to-use synchronous step-down DC/DC converter capable of driving up to 4.0 A of load current from an input voltage of up to 36 V. The LM60440AQEVM features an adjustable output voltage of 5 V and a switching frequency of 400 kHz. See the [LMR60440-Q1 3.8-V to 36-V, 4-A Synchronous Step-down Voltage Converter Data Sheet](#) data sheets for additional features, detailed descriptions, and available options.

**Table 1. Device and Package Configurations**

EVM	U1	FREQUENCY	CURRENT
LM60440AQEVM	LM60440AQRPKRQ1	400 kHz	4.0 A



**Figure 1. LM60440AQEVM Board**

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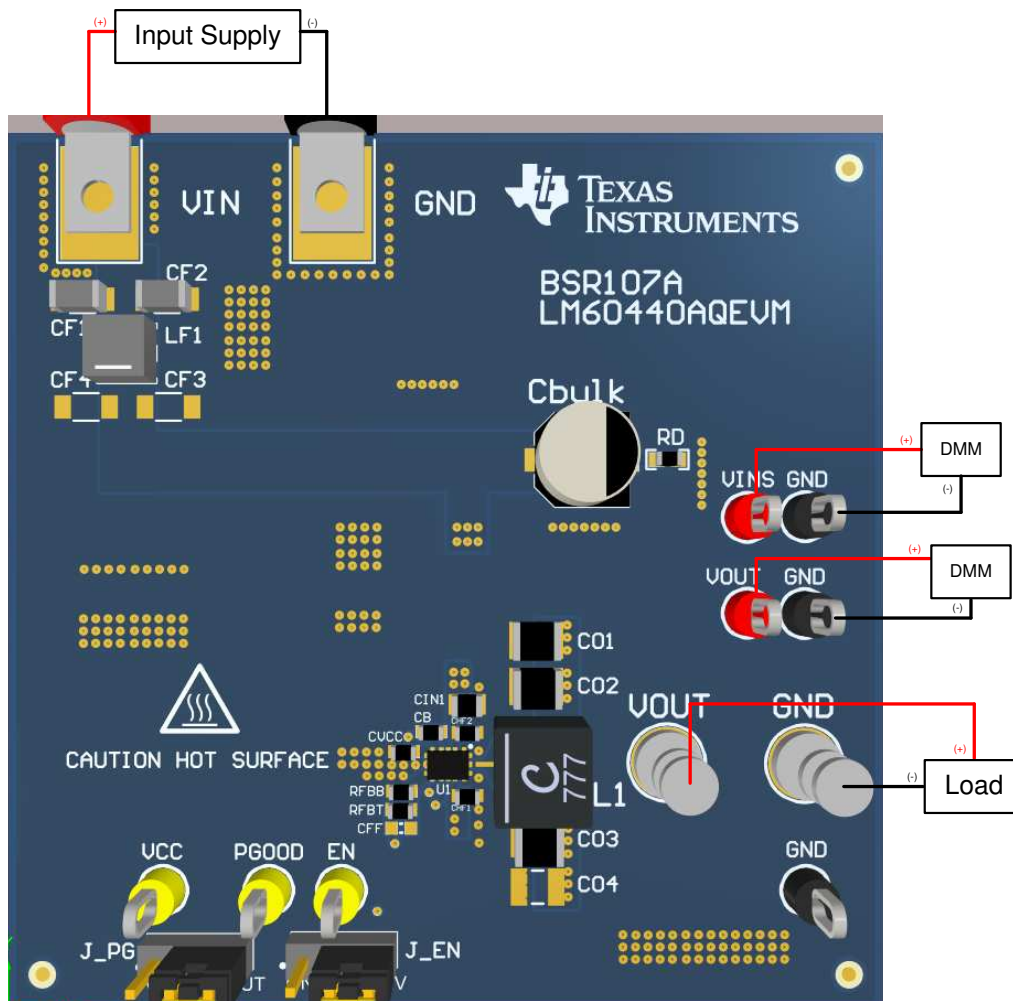
## 1 Setup

This section describes the test points and connectors on the EVM and how to properly connect, set up, and use the LM60440AQEVM.

### 1.1 Test Points

The test points on the top of the board can be used for connecting to the input and output of the EVM. See [Figure 2](#) for typical test setup. The functions of the test points connections are:

- **VIN** -- Input supply to EVM including an EMI filter. Connect to a suitable input supply. Connect at this point for conducted EMI test.
- **VINS** -- Input voltage sense to the IC. Connect to a DMM to measure input voltage after EMI filter.
- **VOUT** -- Output voltage of EVM. Connect to a desired load.
- **VOUTS** -- Output voltage sense test point. This test point is a direct short to VOUT. Connect to a DMM to measure the output voltage.
- **GND** -- Ground connections for the input supply, desired load, or test points.
- **VCC** -- This test point is connected to the VCC pin. Connect to a DMM to monitor VCC regulation.
- **EN** -- This test point is connected to the EN pin. By default, a resistor divider (REN1 and REN2) from VIN is used to enable the IC.
- **PGOOD** -- This test point is connected to the PGOOD pin from the IC. It is an open-drain output of the PGOOD pin. Can be tied to external supply through a pullup resistor or left open.

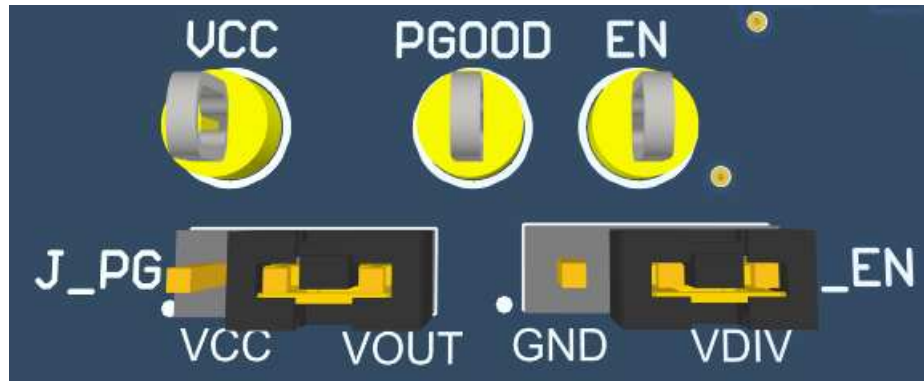


**Figure 2. EVM Board Connections**

## 1.2 Jumpers and Test Points

See [Figure 3](#) for jumper locations.

- **J\_EN** - This jumper allows the ENABLE input to be connected to GND in order to disable the IC. By default, a resistor divider (REN1 and REN2) from VIN is used to enable the IC.
- **J\_PG** - Use this jumper to select how the PGOOD pin can be connected. By default, a jumper connects the pin with a pullup resistor to the output voltage.



**Figure 3. Jumper Locations**

## 2 Operation

### 2.1 Quick Start

1. Connect the voltage supply between VIN and GND banana jacks inputs.
2. Connect the load between VOUT and GND test points.
3. Set the supply voltage at an appropriate level between 4.8 V to 36 V. Set the current limit of the supply to an appropriate level.
4. Turn on the power supply. With the default configuration, the EVM powers up and provides  $V_{OUT} = 5\text{ V}$ .
5. Monitor the output voltage. The maximum load current must be 4.0 A with the LM60440-Q1 device.

### 3 Schematic

VIN: 3.8V to 36V

5 VOUT @ 4A

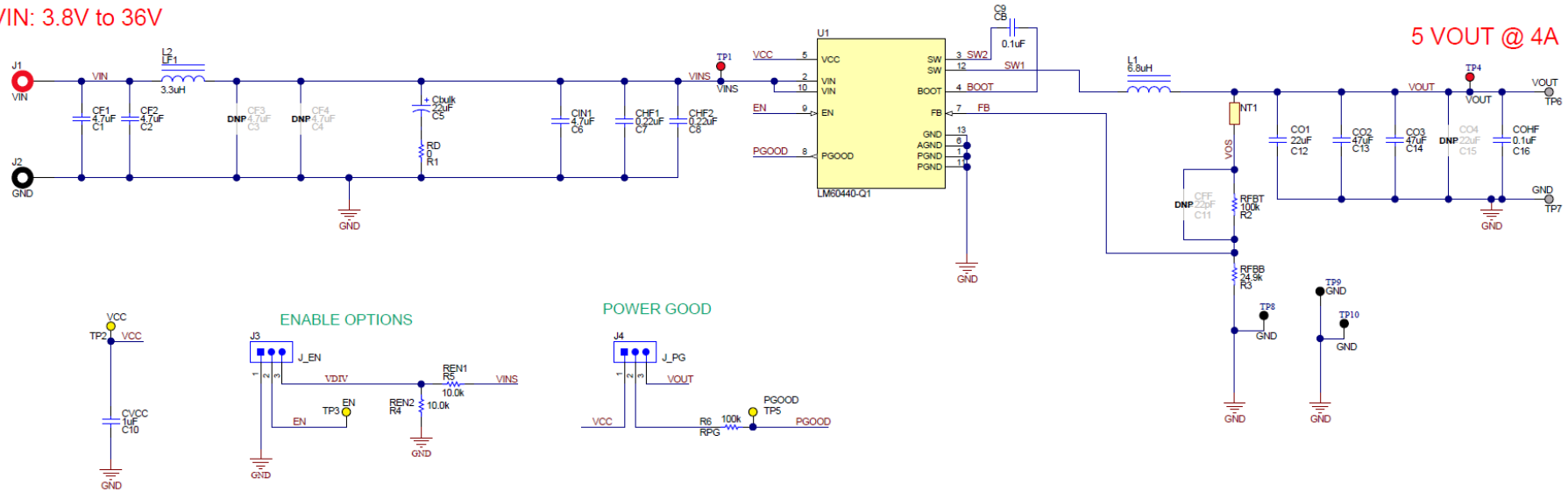


Figure 4. LM60440AQEVM Schematic

## 4 Board Layout

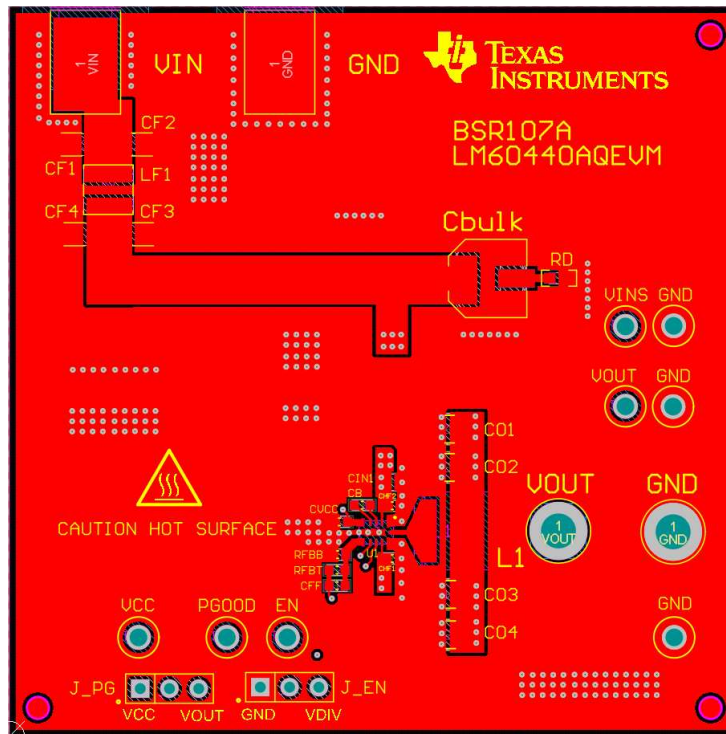


Figure 5. Top View of EVM

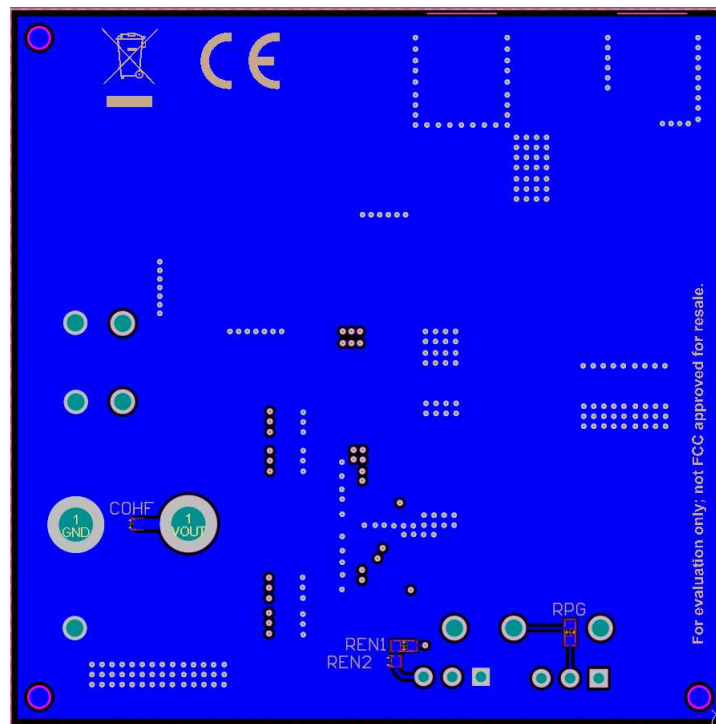
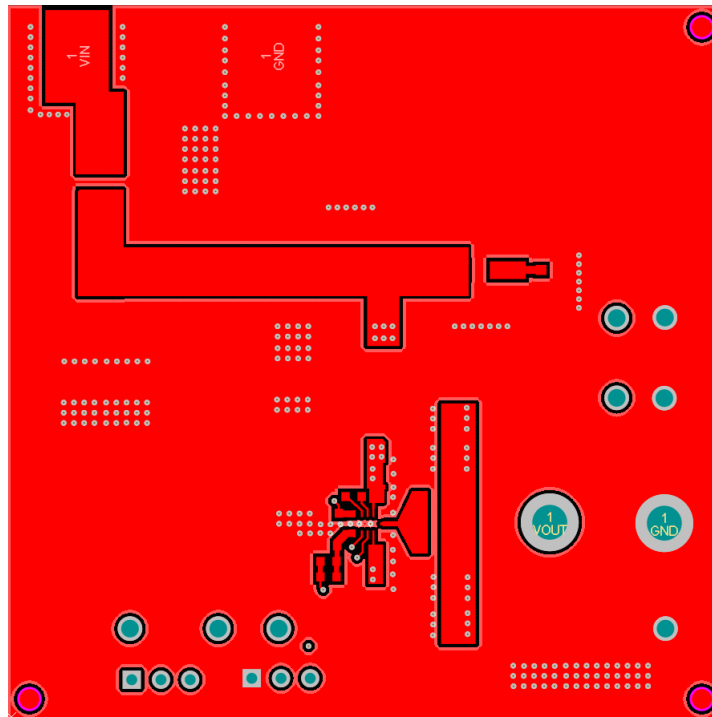
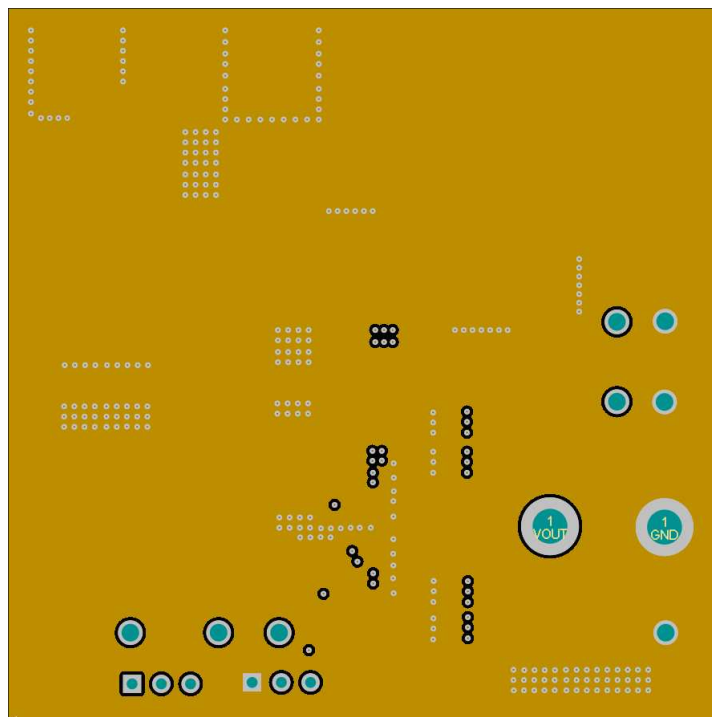


Figure 6. Bottom View of EVM



**Figure 7. EVM Top Copper Layer**



**Figure 8. EVM Mid Layer One**

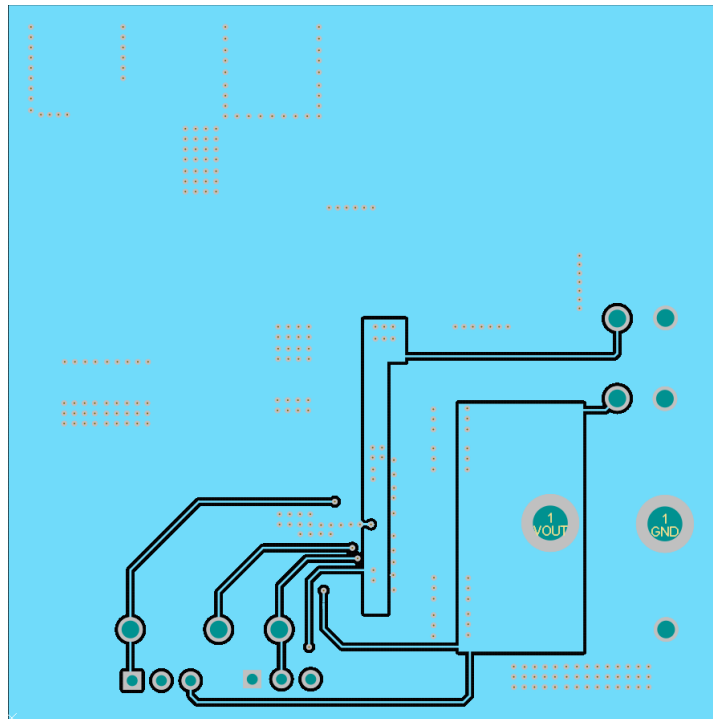


Figure 9. EVM Mid Layer Two

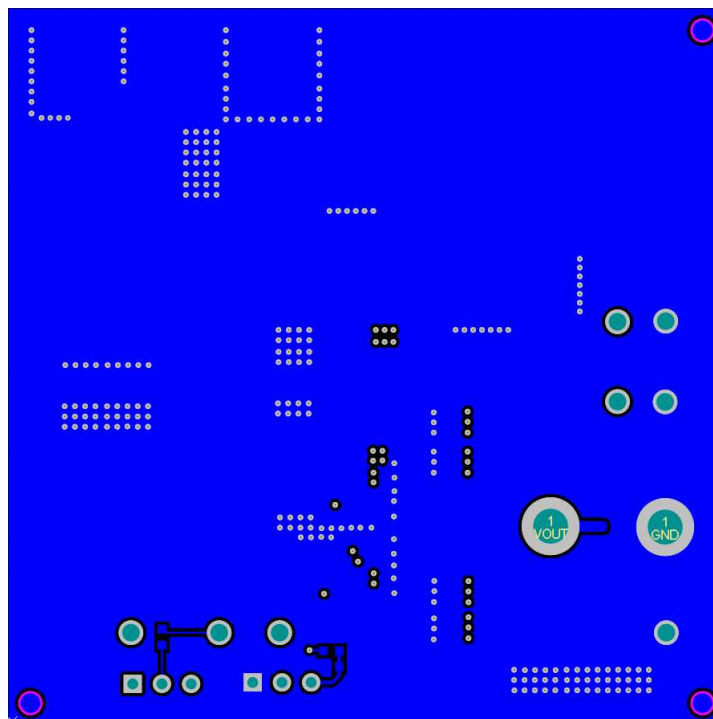


Figure 10. EVM Bottom Copper Layer



## 5 Bill of Materials

**Table 2. Bill of Materials**

DESIGNATOR	COMMENT	DESCRIPTION	PART NUMBER	MANUFACTURER	QUANTITY
C1, C2	CF1, CF2	CAP, CERM, 4.7 $\mu$ F, 50 V, $\pm$ 10%, X7R, 1206	GRM31CR71H475K A12L	MuRata	2
C5	Cbulk	CAP, AL, 22 $\mu$ F, 50 V, $\pm$ 20%, 0.88 $\Omega$ , AEC-Q200 Grade 2, SMD	EEE-FK1H220P	Panasonic	1
C6	CIN1	CAP, CERM, 4.7 $\mu$ F, 50 V, $\pm$ 10%, X5R, 0805	C2012X5R1H475K1 25AB	TDK	1
C7, C8	CHF1, CHF2	CAP, CERM, 0.22 $\mu$ F, 50 V, $\pm$ 10%, X7R, 0603	C1608X7R1H224K0 80AB	TDK	2
C9, C16	CB, COHF	CAP, CERM, 0.1 $\mu$ F, 25 V, $\pm$ 10%, X7R, 0603	06033C104KAT2A	AVX	2
C10	CVCC	CAP, CERM, 1 $\mu$ F, 25 V, $\pm$ 10%, X7R, 0603	885012206076	Wurth Elektronik	1
C12	CO1	CAP, CERM, 22 $\mu$ F, 25 V, $\pm$ 10%, X5R, 1210	CL32A226KAJNNN E	Samsung Electro-Mechanics	1
C13, C14	CO2, CO3	CAP, CERM, 47 $\mu$ F, 16 V, $\pm$ 10%, X5R, 1210	GRM32ER61C476K E15L	MuRata	2
J1	VIN	Standard Banana Jack, Insulated, Red	6091	Keystone	1
J2	VOUT	Standard Banana Jack, Insulated, Black	6092	Keystone	1
J3, J4	J_EN, J_PG	Header, 100 mil, 3x1, Gold, TH	HTSW-103-07-G-S	Samtec	2
L1	L1	Inductor, Shielded, Composite, 6.8 $\mu$ H, 9 A, 0.0208 $\Omega$ , AEC-Q200 Grade 1, SMD	XAL6060-682MEB	Coilcraft	1
L2	LF1	Inductor, Shielded, Composite, 3.3 $\mu$ H, 5.5 A, 0.026 $\Omega$ , SMD	XAL4030-332MEB	Coilcraft	1
R1	RD	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	RMCF0603ZT0R00	Stackpole Electronics Inc	1
R2	RFBT	RES, 100 k, 1%, 0.1 W, 0603	RC0603FR-07100KL	Yageo	1
R3	RFBB	RES, 24.9 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060324K9FK EA	Vishay-Dale	1
R4, R5	REN1, REN2	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0FK EA	Vishay-Dale	2
R6	RPG	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603100KFK EA	Vishay-Dale	1
SH-J1, SH-J2	SNT-100-BK-G	Shunt, 100 mil, Gold plated, Black	SNT-100-BK-G	Samtec	2

**Table 2. Bill of Materials (continued)**

DESIGNATOR	COMMENT	DESCRIPTION	PART NUMBER	MANUFACTURER	QUANTITY
TP1, TP4	VINS, VOULTS	Test Point, Multipurpose, Red, TH	5010	Keystone	2
TP2, TP3, TP5	VCC, EN, PGOOD	Test Point, Multipurpose, Yellow, TH	5014	Keystone	3
TP6, TP7	VOULT, GND	Terminal, Turret, TH, Double	1503-2	Keystone	2
TP8, TP9, TP10	GND	Test Point, Multipurpose, Black, TH	5011	Keystone	3
U1	LM60440AQRPKR Q1	LM60440-Q1, RPK0013A (VQFN- 12)	LM60440AQRPKR Q1	Texas Instruments	1
C3, C4	CF3, CF4	CAP, CERM, 4.7 $\mu$ F, 50 V, $\pm$ 10%, X7R, 1206	GRM31CR71H475K A12L	MuRata	0
C11	CFF	CAP, CERM, 22 pF, 50 V, $\pm$ 5%, C0G/NP0, 0603	GRM1885C1H220J A01D	MuRata	0
C15	CO4	CAP, CERM, 22 $\mu$ F, 25 V, $\pm$ 10%, X5R, 1210	CL32A226KAJNNN E	Samsung Electro- Mechanics	0
FID1, FID2, FID3, FID4, FID5, FID6	Fiducial	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	0

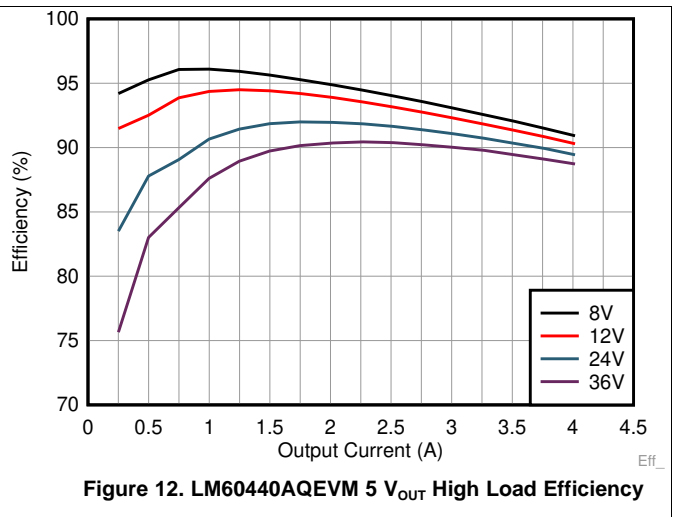
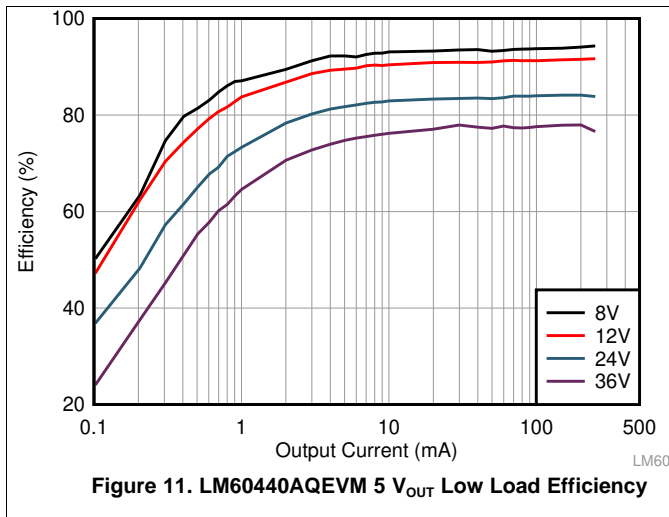
## 6 Test Results (Preliminary)

Section 6.1 details the test results from the LM60440AQEVM variant.

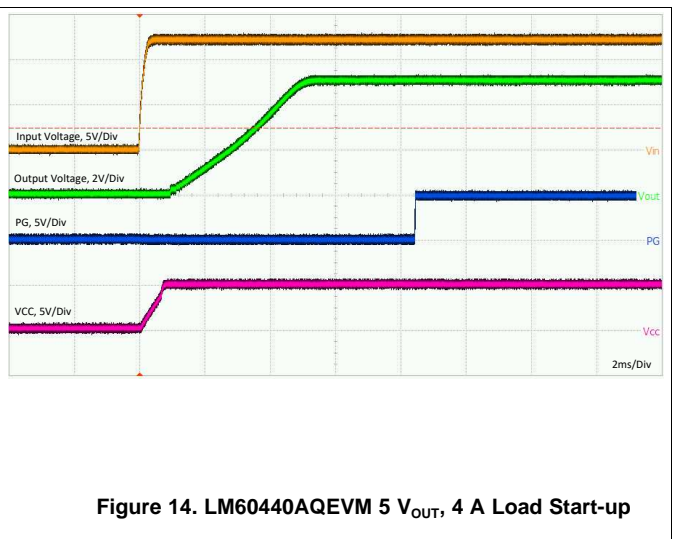
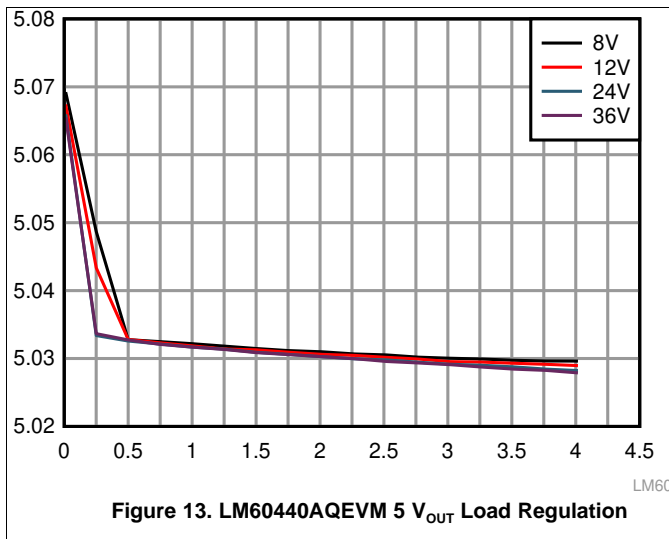
### 6.1 LM60440AQEVM Test Results

The LM60440AQEVM variant is used for all figures from Figure 12 to Figure 20.

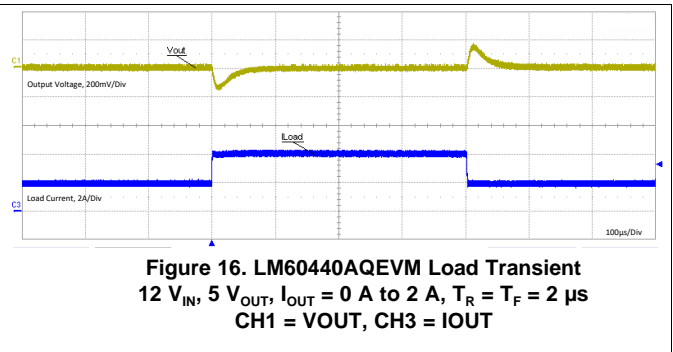
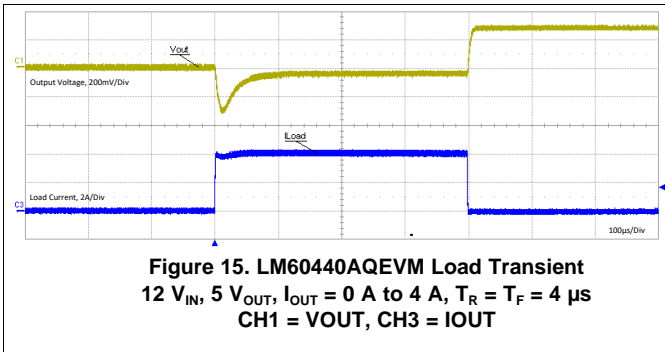
#### 6.1.1 Efficiency and Load Regulation



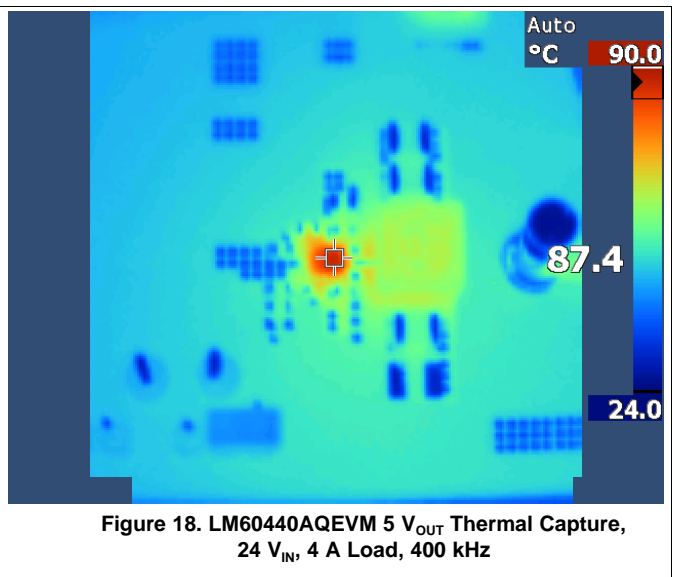
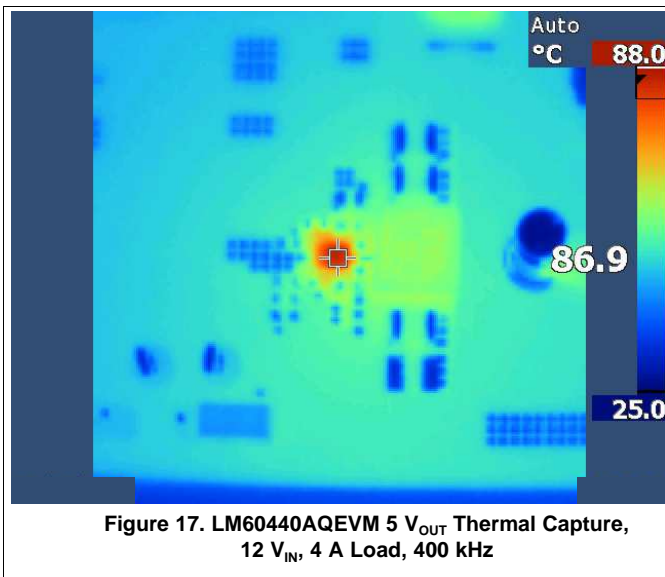
#### 6.1.2 Start-up and Load Regulation



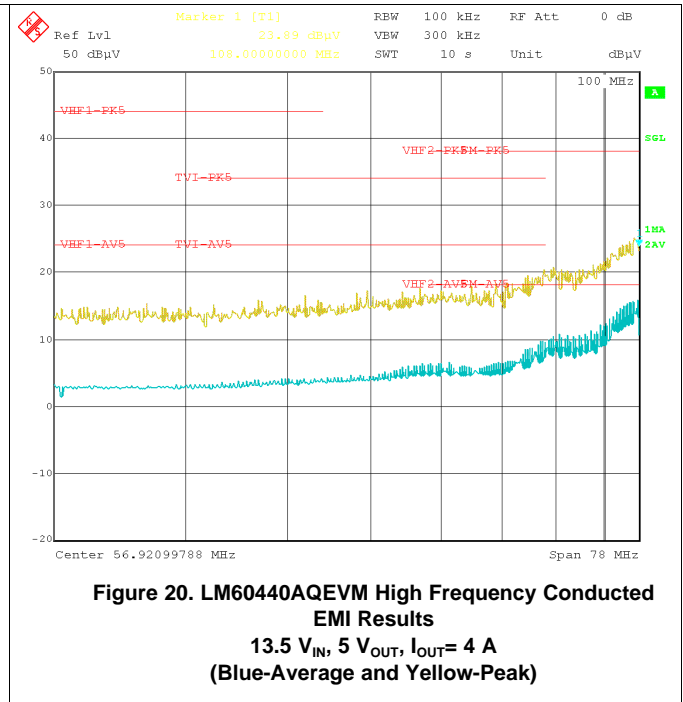
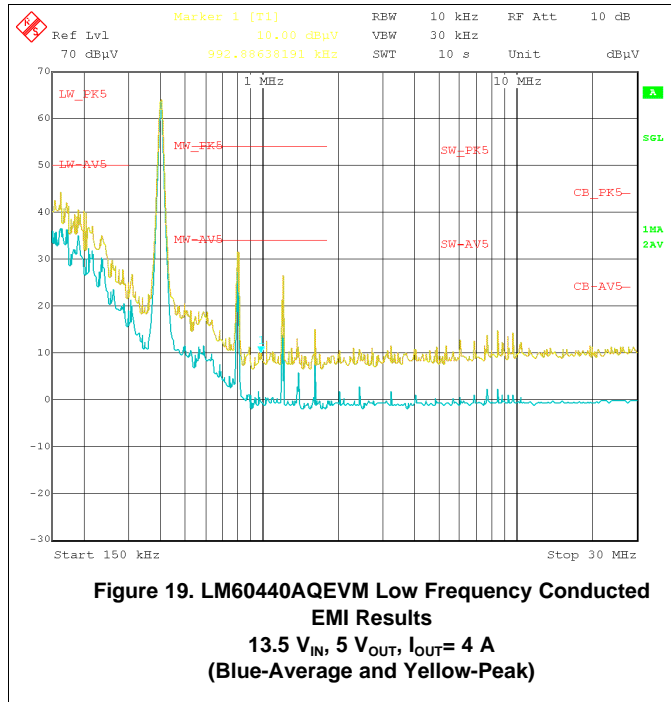
### 6.1.3 Load Transients



### 6.1.4 Thermal Picture



### 6.1.5 Conducted EMI



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