



FEATURES

Ultrawideband frequency range: 9 kHz to 40 GHz

Attenuation range: 2 dB steps to 30 dB

Low insertion loss

1.6 dB to 18 GHz

2.0 dB to 26 GHz

3.4 dB to 40 GHz

Attenuation accuracy

±(0.1 + 1.0%) of attenuation state up to 18 GHz

±(0.1 + 2.5%) of attenuation state up to 26 GHz

±(0.6 + 10.0%) of attenuation state up to 40 GHz

Typical step error

±0.15 dB to 18 GHz

±0.20 dB to 26 GHz

±0.60 dB to 40 GHz

High input linearity

P0.1dB insertion loss state: 30 dBm

P0.1dB other attenuation states: 26 dBm

IP3: 50 dBm typical

High RF input power handling: 26 dBm average, 30 dBm peak

Tight distribution in relative phase

No low frequency switching spurs

SPI and parallel mode control, CMOS/LVTTL compatible

RF amplitude settling time (0.1 dB of final RF output): 8.5 μs

2.5 mm × 2.5 mm, 16-terminal LGA package

Pin compatible with [ADRF5731](#), fast switching version

APPLICATIONS

Industrial scanners

Test and instrumentation

Cellular infrastructure: 5G millimeter wave

Military radios, radars, electronic counter measures (ECMs)

Microwave radios and very small aperture terminals (VSATs)

GENERAL DESCRIPTION

The ADRF5721 is a silicon, 4-bit digital attenuator with a 30 dB attenuation control range in 2 dB steps.

This device operates from 9 kHz to 40 GHz with better than 3.4 dB of insertion loss. The ATTIN port of the ADRF5721 has a radio frequency (RF) input power handling capability of 26 dBm average and 30 dBm peak for all states.

The ADRF5721 requires a dual supply voltage of +3.3 V and -3.3 V. The device features serial peripheral interface (SPI), parallel mode control, and complementary metal-oxide

FUNCTIONAL BLOCK DIAGRAM

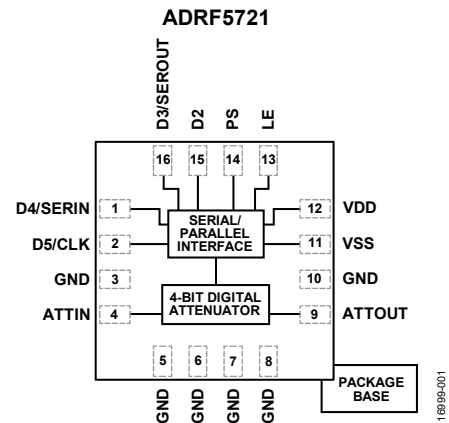


Figure 1.

semiconductor (CMOS)-/low voltage transistor to transistor logic (LVTTL)-compatible controls.

The ADRF5721 is pin compatible with the [ADRF5731](#), the fast switching version, which operates from 100 MHz to 40 GHz.

The ADRF5721 RF ports are designed to match a characteristic impedance of 50 Ω.

The ADRF5721 comes in a 16-terminal, 2.5 mm × 2.5 mm, RoHS compliant, land grid array (LGA) package and operates from -40°C to +105°C.

Rev. A

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REVISION HISTORY

3/2020—Rev. 0 to Rev. A

| | |
|---|----|
| Changes to RF Power Parameter, Table 1 | 4 |
| Changes to Table 3..... | 6 |
| Changes to Power Supply Section | 11 |
| Added Power-Up State Section..... | 11 |
| Moved Serial or Parallel Mode Selection Section and Table 7; Renumbered Sequentially | 12 |

9/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

VDD = 3.3 V, VSS = -3.3 V, digital voltages = 0 V or VDD, case temperature (T_{CASE}) = 25°C, and a 50 Ω system, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit | |
|---------------------------|---|---|-------------------|--------------------|---------|----|
| FREQUENCY RANGE | | 0.009 | | 40,000 | MHz | |
| INSERTION LOSS (IL) | 9 kHz to 10 GHz | | 1.3 | | dB | |
| | 10 GHz to 18 GHz | | 1.6 | | dB | |
| | 18 GHz to 26 GHz | | 2.0 | | dB | |
| | 26 GHz to 35 GHz | | 2.7 | | dB | |
| | 35 GHz to 40 GHz | | 3.4 | | dB | |
| RETURN LOSS | ATTIN and ATTOUT, all attenuation states | | | | | |
| | 9 kHz to 10 GHz | | 20 | | dB | |
| | 10 GHz to 18 GHz | | 19 | | dB | |
| | 18 GHz to 26 GHz | | 17 | | dB | |
| | 26 GHz to 35 GHz | | 17 | | dB | |
| 35 GHz to 40 GHz | | 16 | | dB | | |
| ATTENUATION | Range | Between minimum and maximum attenuation states | 30 | | dB | |
| | Step Size | Between any successive attenuation states | 2 | | dB | |
| | Accuracy | Referenced to insertion loss | | | | |
| | | 9 kHz to 10 GHz | | $\pm(0.1 + 1.0\%)$ | | dB |
| | | 10 GHz to 18 GHz | | $\pm(0.1 + 1.0\%)$ | | dB |
| | | 18 GHz to 26 GHz | | $\pm(0.1 + 2.5\%)$ | | dB |
| | | 26 GHz to 35 GHz | | $\pm(0.2 + 6.0\%)$ | | dB |
| | 35 GHz to 40 GHz | | $\pm(0.6 + 10\%)$ | | dB | |
| | Step Error | Between any successive attenuation states | | | | |
| | | 9 kHz to 10 GHz | | ± 0.05 | | dB |
| | | 10 GHz to 18 GHz | | ± 0.15 | | dB |
| | | 18 GHz to 26 GHz | | ± 0.20 | | dB |
| | | 26 GHz to 35 GHz | | ± 0.35 | | dB |
| 35 GHz to 40 GHz | | ± 0.60 | | dB | | |
| RELATIVE PHASE | Referenced to insertion loss | | | | | |
| | 9 kHz to 10 GHz | | 17 | | Degrees | |
| | 10 GHz to 18 GHz | | 26 | | Degrees | |
| | 18 GHz to 26 GHz | | 37 | | Degrees | |
| | 26 GHz to 35 GHz | | 53 | | Degrees | |
| 35 GHz to 40 GHz | | 77 | | Degrees | | |
| SWITCHING CHARACTERISTICS | All attenuation states at input power (P_{IN}) = 10 dBm | | | | | |
| | Rise and Fall Time (t_{RISE} and t_{FALL}) | 10% to 90% of RF output | 1.3 | | μs | |
| | On and Off Time (t_{ON} and t_{OFF}) | 50% triggered control (CTL) to 90% of RF output | 3.8 | | μs | |
| | RF Amplitude Settling Time | 50% triggered CTL to 0.1 dB of final RF output | 8.5 | | μs | |
| | | 50% triggered CTL to 0.05 dB of final RF output | 11 | | μs | |
| | Overshoot | | 1.5 | | dB | |
| | Undershoot | | -1.0 | | dB | |
| | RF Phase Settling Time | f = 5 GHz | | | | |
| | | 50% triggered CTL to 5° of final RF output | 2.2 | | μs | |
| | 1° | 50% triggered CTL to 1° of final RF output | 3.5 | | μs | |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|--|-------|------------------|-------|--------------------|
| INPUT LINEARITY ¹ | 500 kHz to 30 GHz | | | | |
| 0.1 dB Power Compression (P0.1dB) | | | 30 | | dBm |
| Insertion Loss State | | | 26 | | dBm |
| Other Attenuation States | | | 50 | | dBm |
| Third-Order Intercept (IP3) | Two-tone input power = 14 dBm per tone, $\Delta f = 1$ MHz, all attenuation states | | | | dBm |
| DIGITAL CONTROL INPUTS | LE, PS, D2, D3/SEROUT, ² D4/SERIN, D5/CLK pins | | | | |
| Voltage | | | | | |
| Low (V_{INL}) | | 0 | | 0.8 | V |
| High (V_{INH}) | | 1.2 | | 3.3 | V |
| Current | | | | | |
| Low (I_{INL}) | | | <1 | | μ A |
| High (I_{INH}) | D2 | | 33 | | μ A |
| | LE, PS, D3/SEROUT, ² D4/SERIN, D5/CLK pins | | <1 | | μ A |
| DIGITAL CONTROL OUTPUT | D3/SEROUT pin ² | | | | |
| Voltage | | | | | |
| Low (V_{OUTL}) | | | 0 ± 0.3 | | V |
| High (V_{OUTH}) | | | $V_{DD} \pm 0.3$ | | V |
| Low and High Current (I_{OUTL} , I_{OUTH}) | | | | 0.5 | mA |
| SUPPLY CURRENT | VDD and VSS pins | | | | |
| Positive | | | 117 | | μ A |
| Negative | | | -117 | | μ A |
| RECOMMENDED OPERATING CONDITIONS | | | | | |
| Supply Voltage | | | | | |
| Positive (V_{DD}) | | 3.15 | | 3.45 | V |
| Negative (V_{SS}) | | -3.45 | | -3.15 | V |
| Digital Control Voltage | | 0 | | VDD | V |
| RF Power ³ | $f = 500$ kHz to 30 GHz, $T_{CASE} = 85^{\circ}\text{C}$, ⁴ all attenuation states | | | | |
| Input at ATTIN | Steady state average | | | 26 | dBm |
| | Steady state peak | | | 30 | dBm |
| | Hot switching average | | | 24 | dBm |
| | Hot switching peak | | | 27 | dBm |
| Input at ATTOUT | Steady state average | | | 18 | dBm |
| | Steady state peak | | | 21 | dBm |
| | Hot switching average | | | 15 | dBm |
| | Hot switching peak | | | 18 | dBm |
| Case Temperature (T_{CASE}) | | -40 | | +105 | $^{\circ}\text{C}$ |

¹ Input linearity performance degrades over frequency (see Figure 20 and Figure 21).

² The D3/SEROUT pin is an input in parallel control mode and an output in serial control mode. See Table 5 for the pin function descriptions.

³ For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

⁴ For 105 $^{\circ}\text{C}$ operation, the power handling degrades from the $T_{CASE} = 85^{\circ}\text{C}$ specifications by 3 dB.

TIMING SPECIFICATIONS

See Figure 24, Figure 25, and Figure 26 for the timing diagrams.

Table 2.

| Parameter | Description | Min | Typ | Max | Unit |
|-----------|---|-----|-----|-----|------|
| t_{SCK} | Minimum serial period, see Figure 24 | 70 | | | ns |
| t_{CS} | Control setup time, see Figure 24 | 15 | | | ns |
| t_{CH} | Control hold time, see Figure 24 | | 20 | | ns |
| t_{LN} | LE setup time, see Figure 24 | 15 | | | ns |
| t_{LEW} | Minimum LE pulse width, see Figure 24 and Figure 26 | | 10 | | ns |
| t_{LES} | Minimum LE pulse spacing, see Figure 24 | | 630 | | ns |
| t_{CKN} | Serial clock hold time from LE, see Figure 24 | | 0 | | ns |
| t_{PH} | Hold time, see Figure 26 | | 10 | | ns |
| t_{PS} | Setup time, see Figure 26 | | 2 | | ns |
| t_{CO} | Clock to output (SEROUT) time, see Figure 25 | | 20 | | ns |

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|--|-----------------------------------|
| Positive Supply Voltage (V _{DD}) | -0.3 V to +3.6 V |
| Negative Supply Voltage (V _{SS}) | -3.6 V to +0.3 V |
| Digital Control Inputs | |
| Voltage | -0.3 V to V _{DD} + 0.3 V |
| Current | 3 mA |
| RF Power ¹ (f = 500 kHz to 30 GHz, T _{CASE} = 85°C ²) | |
| Input at ATTIN | |
| Steady State Average | 27 dBm |
| Steady State Peak | 31 dBm |
| Hot Switching Average | 25 dBm |
| Hot Switching Peak | 28 dBm |
| Input at ATTOUT | |
| Steady State Average | 19 dBm |
| Steady State Peak | 22 dBm |
| Hot Switching Average | 16 dBm |
| Hot Switching Peak | 19 dBm |
| RF Power Under Unbiased Condition (V _{DD} , V _{SS} = 0 V) | |
| Input at ATTIN | 21 dBm |
| Input at ATTOUT | 15 dBm |
| Temperature | |
| Junction (T _J) | 135°C |
| Storage | -65°C to +150°C |
| Reflow | 260°C |
| Continuous Power Dissipation (P _{DISS}) | 0.5 W |
| Electrostatic Discharge (ESD) Sensitivity | |
| Human Body Model (HBM) | |
| ATTIN and ATTOUT Pins | 1500 V |
| Digital Pins | 2000 V |
| Charged Device Model (CDM) | 1250 V |

¹ For power derating over frequency, see Figure 2 and Figure 3. Applicable for all ATTIN and ATTOUT power specifications.

² For 105°C operation, the power handling derates from the T_{CASE} = 85°C specifications by 3 dB.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 4. Thermal Resistance

| Package Type | θ _{JC} | Unit |
|--------------|-----------------|------|
| CC-16-6 | 100 | °C/W |

POWER DERATING CURVES

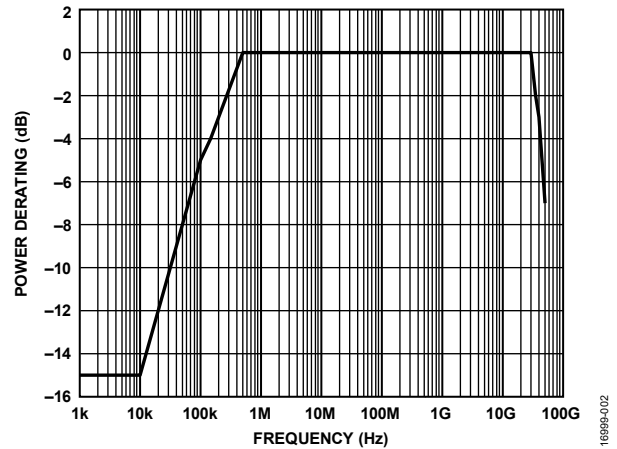


Figure 2. Power Derating vs. Frequency, Low Frequency Detail, T_{CASE} = 85°C

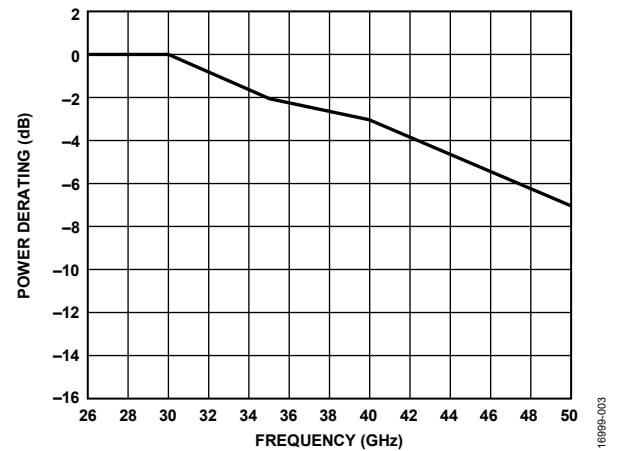


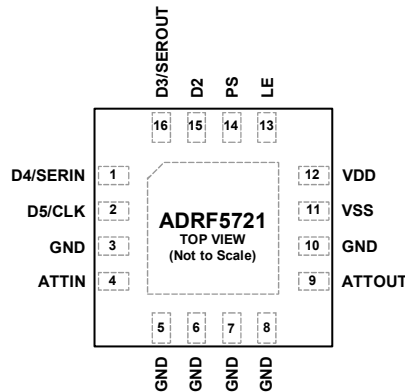
Figure 3. Power Derating vs. Frequency, High Frequency Detail, T_{CASE} = 85°C

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE RF AND DC GROUND OF THE PCB.

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------------|-----------|--|
| 1 | D4/SERIN | Parallel Control Input for 8 dB Attenuator Bit (D4). Serial Data Input (SERIN). See the Theory of Operation section for more information. |
| 2 | D5/CLK | Parallel Control Input for 16 dB Attenuator Bit (D5). Serial Clock Input (CLK). See the Theory of Operation section for more information. |
| 3, 5 to 8, 10 | GND | Ground. These pins must be connected to the RF and dc ground of the PCB. |
| 4 | ATTIN | Attenuator Input. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is needed when the RF line potential is equal to 0 V dc. |
| 9 | ATTOUT | Attenuator Output. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is needed when the RF line potential is equal to 0 V dc. |
| 11 | VSS | Negative Supply Input. |
| 12 | VDD | Positive Supply Input. |
| 13 | LE | Latch Enable Input. See the Theory of Operation section for more information. |
| 14 | PS | Parallel or Serial Control Interface Selection Input. See the Theory of Operation section for more information. |
| 15 | D2 | Parallel Control Input for 2 dB Attenuator Bit. See the Theory of Operation section for more information. |
| 16 | D3/SEROUT | Parallel Control Input for 4 dB Attenuator Bit (D3). Serial Data Output (SEROUT). See the Theory of Operation section for more information. |
| 17 | EPAD | Exposed Pad. The exposed pad must be connected to the RF and dc ground of the PCB. |

INTERFACE SCHEMATICS

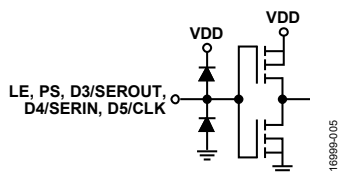


Figure 5. Digital Input Interface Schematic for LE, PS, D3/SEROUT, D4/SERIN, and D5/CLK

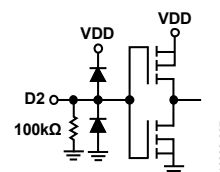


Figure 7. Digital Input Interface Schematic for D2

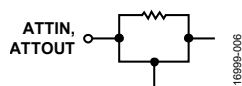


Figure 6. ATTIN and ATTOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

VDD = 3.3 V, VSS = -3.3 V, digital voltages = 0 V or VDD, T_{CASE} = 25°C, and a 50 Ω system, unless otherwise noted. Measured on probe matrix board using ground signal ground (GSG) probes close to the RF pins (ATTIN and ATTOUT). See the Applications Information section for details on evaluation and probe matrix boards.

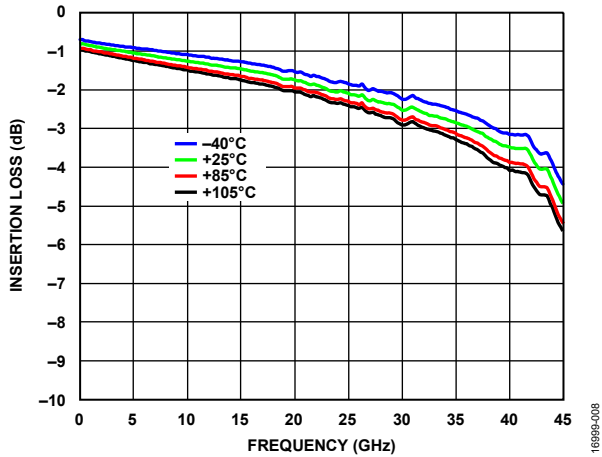


Figure 8. Insertion Loss vs. Frequency over Temperature

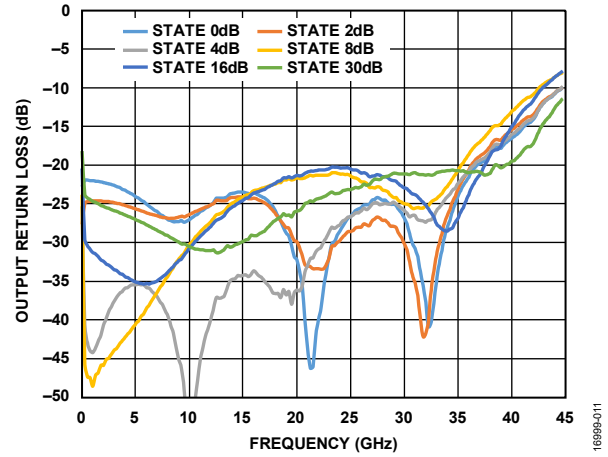


Figure 11. Output Return Loss vs. Frequency (Major States Only)

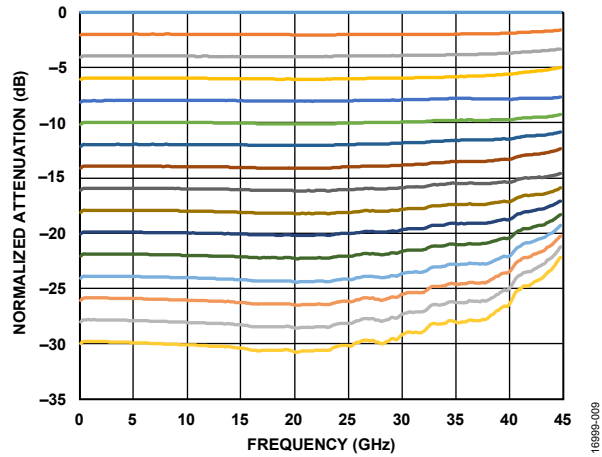


Figure 9. Normalized Attenuation vs. Frequency for All States at Room Temperature

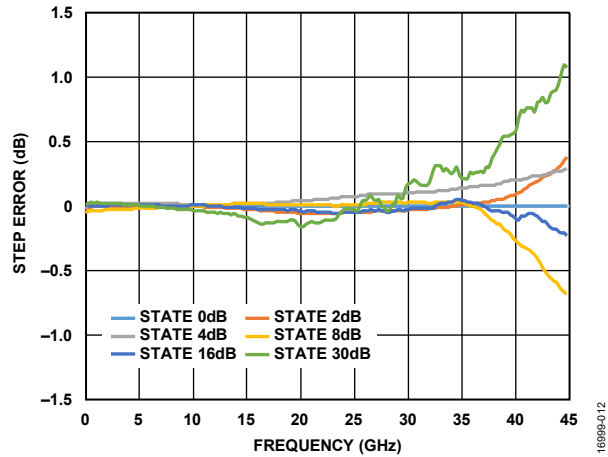


Figure 12. Step Error vs. Frequency (Major States Only)

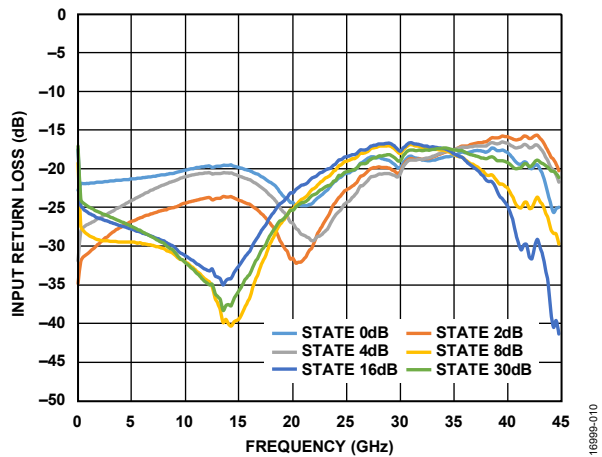


Figure 10. Input Return Loss vs. Frequency (Major States Only)

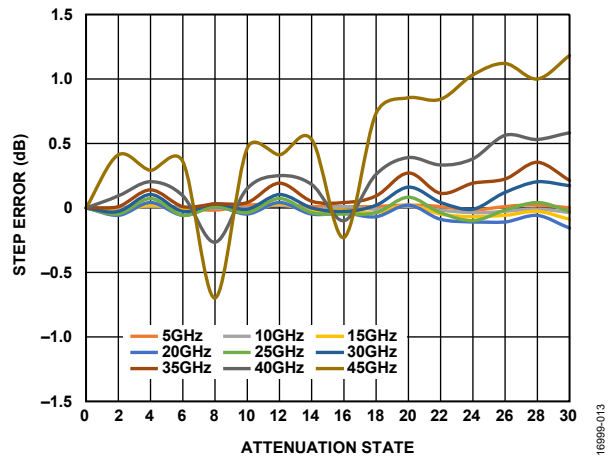


Figure 13. Step Error vs. Attenuation State over Frequency

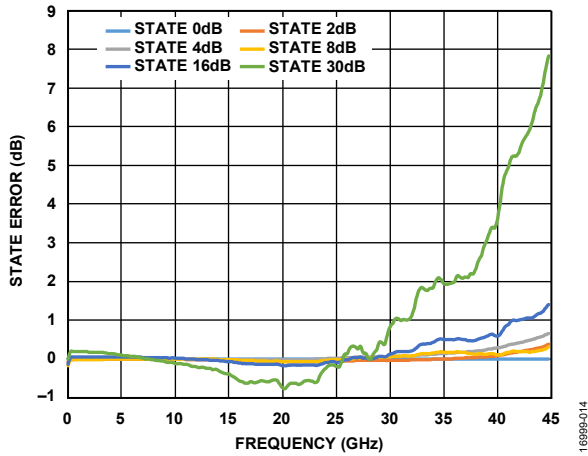


Figure 14. State Error vs. Frequency (Major States Only)

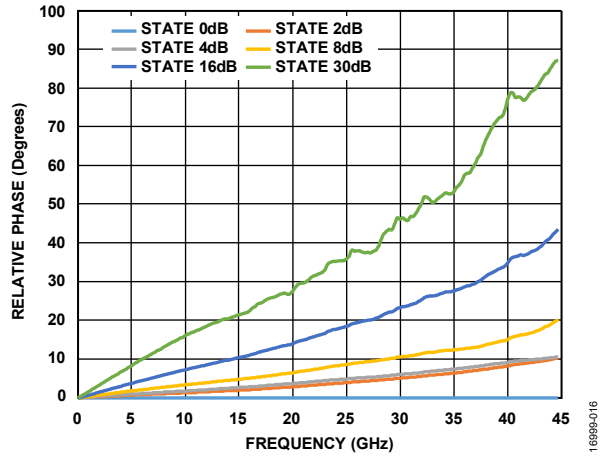


Figure 16. Relative Phase vs. Frequency (Major States Only)

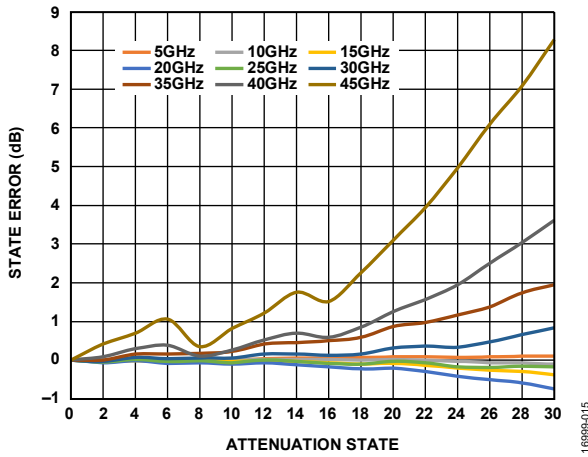


Figure 15. State Error vs. Attenuation State over Frequency

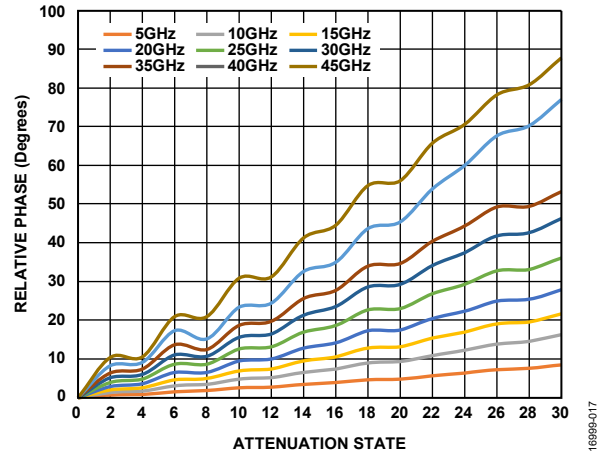


Figure 17. Relative Phase vs. Attenuation State over Frequency

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

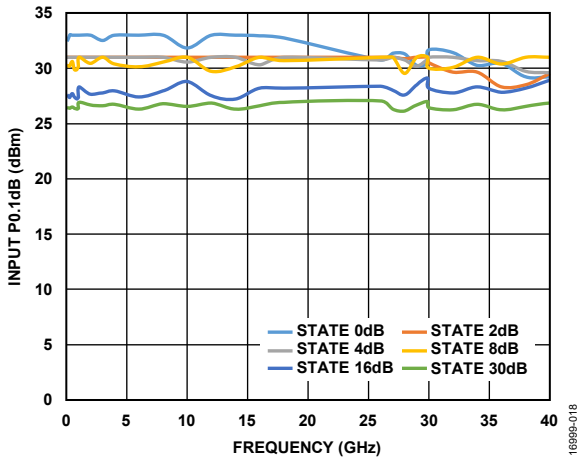


Figure 18. Input P0.1dB vs. Frequency (Major States Only)

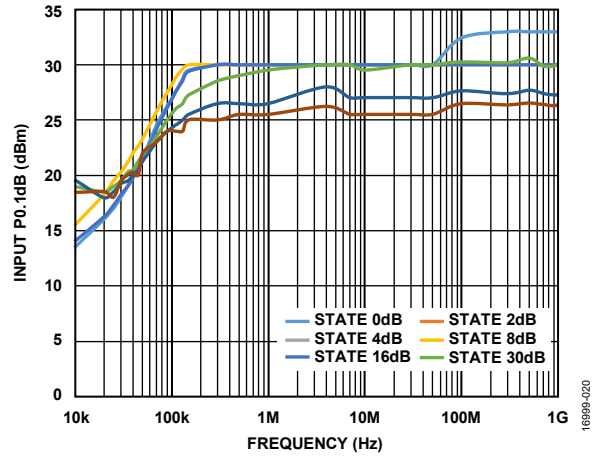


Figure 20. Input P0.1dB vs. Frequency (Major States Only), Low Frequency Detail

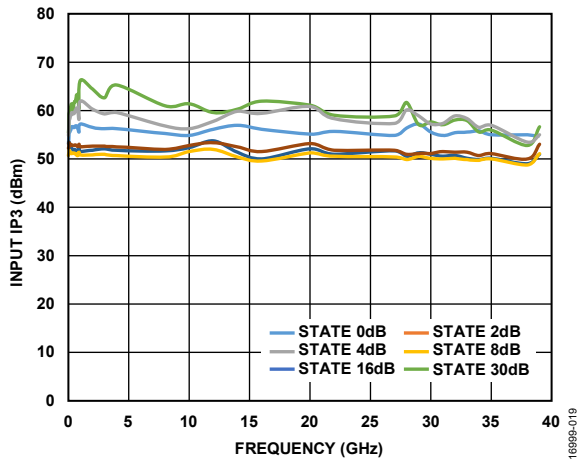


Figure 19. Input IP3 vs. Frequency (Major States Only)

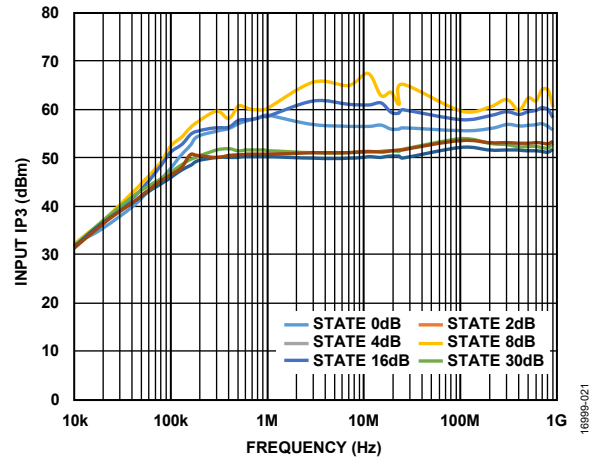


Figure 21. Input IP3 vs. Frequency (Major States Only), Low Frequency Detail

THEORY OF OPERATION

The ADRF5721 incorporates a 4-bit fixed attenuator array that offers an attenuation range of 30 dB in 2 dB steps. An integrated driver provides both serial and parallel mode control of the attenuator array (see Figure 22).

Note that when referring to a single function of a multifunction pin in this section, only the portion of the pin name that is relevant is mentioned. For full pin names of the multifunction pins, refer to the Pin Configuration and Function Descriptions section.

POWER SUPPLY

Bypassing capacitors are recommended on the positive supply voltage line (VDD) and negative supply line (VSS) to filter high frequency noise.

The power-up sequence is as follows:

1. Connect GND.
2. Power up the VDD and VSS voltages. Power up VSS after VDD to avoid current transients on VDD during ramp-up.
3. Power up the digital control inputs. The order of the digital control inputs is not important. However, powering the digital control inputs before the VDD voltage supply may inadvertently forward bias and damage the internal ESD structures. To avoid this damage, use a series 1 kΩ resistor to limit the current flowing in to the control pin. Use pull-up or pull-down resistors if the controller output is in a

high impedance state after the VDD voltage is powered up and the control pins are not driven to a valid logic state.

4. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse order of the power-up sequence.

Power-Up State

The ADRF5721 has internal power-on reset circuitry. This circuitry sets the attenuator to the maximum attenuation state (30 dB) when the VDD and VSS voltages are applied and LE is set to low.

RF INPUT AND OUTPUT

Both RF ports (ATTIN and ATTOUT) are dc-coupled to 0 V. DC blocking is not required at the RF ports when the RF line potential is equal to 0 V.

The RF ports are internally matched to 50 Ω. Therefore, external matching components are not required.

The ADRF5721 supports bidirectional operation at a lower power level. The power handling of the ATTIN and ATTOUT ports are different. Therefore, the bidirectional power handling is defined by the ATTOUT port. Refer to the RF input power specifications in Table 1.

Table 6. Truth Table

| Digital Control Input ¹ | | | | | | Attenuation State (dB) |
|------------------------------------|------|------|------|------------|------------|------------------------|
| D5 | D4 | D3 | D2 | D1 | D0 | |
| Low | Low | Low | Low | Don't care | Don't care | 0 (reference) |
| Low | Low | Low | High | Don't care | Don't care | 2 |
| Low | Low | High | Low | Don't care | Don't care | 4 |
| Low | High | Low | Low | Don't care | Don't care | 8 |
| High | Low | Low | Low | Don't care | Don't care | 16 |
| High | High | High | High | Don't care | Don't care | 30 |

¹ Any combination of the control voltage input states shown in Table 6 provides an attenuation equal to the sum of the bits selected.

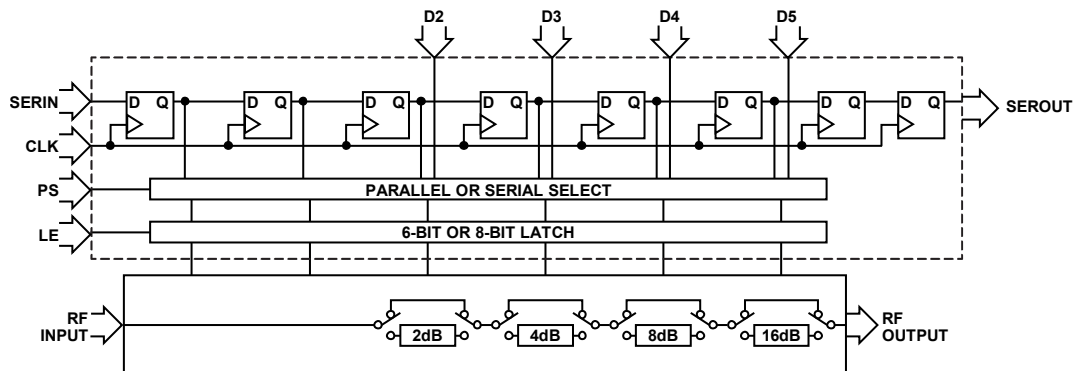


Figure 22. Simplified Circuit Diagram

1699P-022

SERIAL OR PARALLEL MODE SELECTION

The ADRF5721 can be controlled in either serial or parallel mode by setting the PS pin to high or low, respectively (see Table 7).

Table 7. Mode Selection

| PS | Control Mode |
|------|--------------|
| Low | Parallel |
| High | Serial |

SERIAL MODE INTERFACE

The ADRF5721 supports a 3-wire SPI: serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when PS is set to high.

The ADRF5721 attenuation state is controlled by Bits[D5:D2]. Bit D0 and Bit D1 are don't care bits but must be input. Therefore, at least a 6-bit SERIN must be used to control the attenuation states. If using an 8-bit word to control the state of the attenuator, Bits[D7:D6] and Bits[D1:D0] are don't care bits. It does not matter if these bits are held low or high. Refer to Table 6 and Figure 24 for additional information.

In serial mode, the SERIN data is clocked most significant bit (MSB) first on the rising CLK edges into the shift register. Then, LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock new SERIN data into the shift register as CLK is masked to prevent the attenuator value from changing if LE is kept high. See Figure 24 in conjunction with Table 2 and Table 6.

Using SEROUT

The ADRF5721 also features a serial data output, SEROUT. SEROUT outputs the serial input data at the eighth clock cycle, and can control a cascaded attenuator using a single SPI bus. Figure 25 shows the serial output timing diagram.

When using the attenuator in a daisy-chain operation, 8-bit SERIN data must be used due to the 8-clock cycle delay between SERIN and SEROUT.

It is optional to use a 1 kΩ resistor between SEROUT on the first attenuator and SERIN of the next attenuator to filter the signal (see Figure 23).

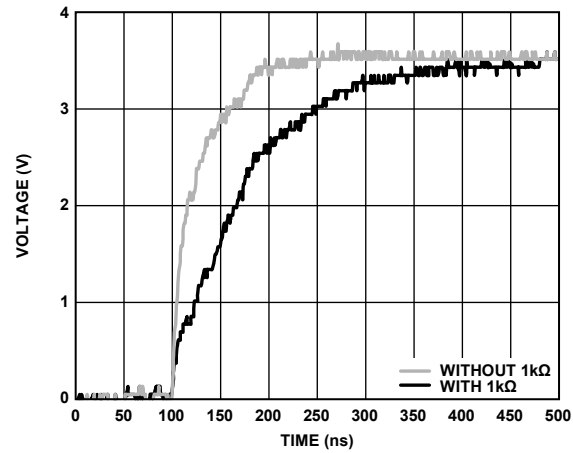


Figure 23. Using a Resistor on SEROUT

16895-023

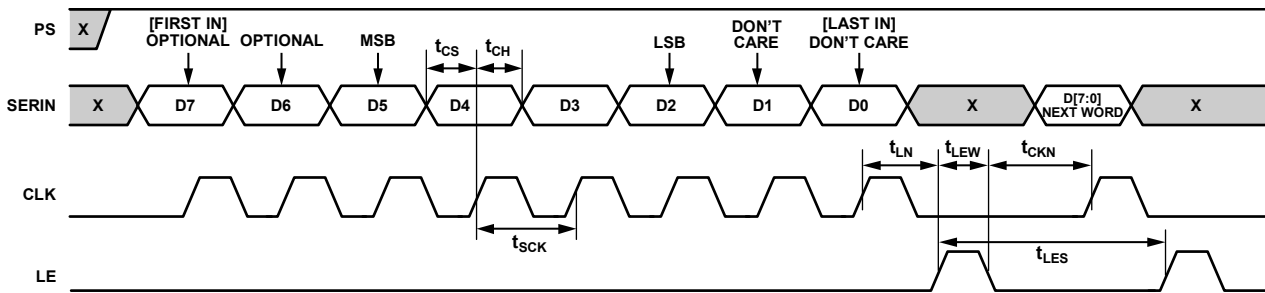


Figure 24. Serial Control Timing Diagram

16895-024

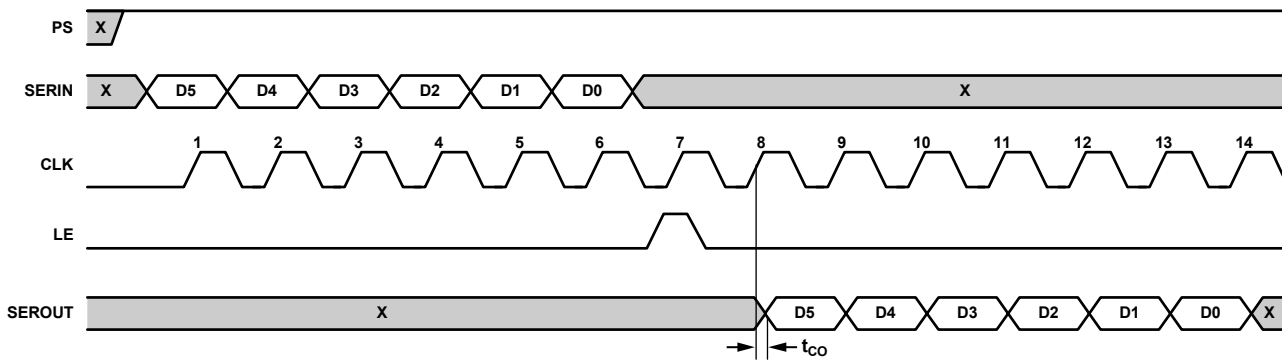


Figure 25. Serial Output Timing Diagram

16895-025

PARALLEL MODE INTERFACE

The ADRF5721 has four digital control inputs, D2 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 6. The parallel control interface is activated when PS is set to low.

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

To enable direct parallel mode, keep the LE pin high. To change the attenuation state, use the control voltage inputs (D2 to D5) directly. This mode is ideal for manual control of the attenuator.

Latched Parallel Mode

To enable latched parallel mode, keep the LE pin low when changing the control voltage inputs (D2 to D5) to set the attenuation state. When the desired state is set, toggle LE high to transfer the 4-bit data to the bypass switches of the attenuator array, and then toggle LE low to latch the change into the device until the next desired attenuation change (see Figure 26 in conjunction with Table 2).

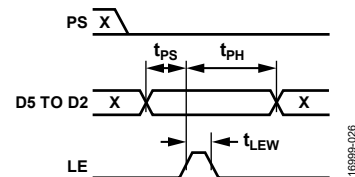


Figure 26. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

EVALUATION BOARD

The [ADRF5721-EVALZ](#) is a 4-layer evaluation board. The top and bottom copper layer are 0.5 oz (0.7 mil) plated to 1.5 oz (2.2 mil) and are separated by dielectric materials. The stackup for this evaluation board is shown in Figure 27.

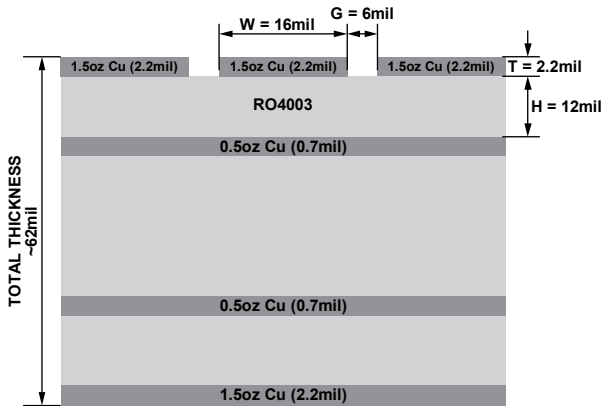


Figure 27. Evaluation Board Stackup, Cross Sectional View

All RF and dc traces are routed on the top copper layer, whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. The top dielectric material is 12 mil Rogers RO4003, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is 62 mil, which allows 2.4 mm RF launchers to be connected at the board edges.

The RF transmission lines are designed using a coplanar waveguide (CPWG) model, with a trace width of 16 mil and ground clearance of 6 mil to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many through vias as possible are arranged around transmission lines and under the exposed pad of the package.

Thru calibration can be used to calibrate out the board loss effects from the [ADRF5721-EVALZ](#) evaluation board measurements to determine the device performance at the pins of the IC. Figure 28 shows the typical board loss (THRU) for the [ADRF5721-EVALZ](#) evaluation board at room temperature, the embedded insertion loss, and the de-embedded insertion loss for the ADRF5721.

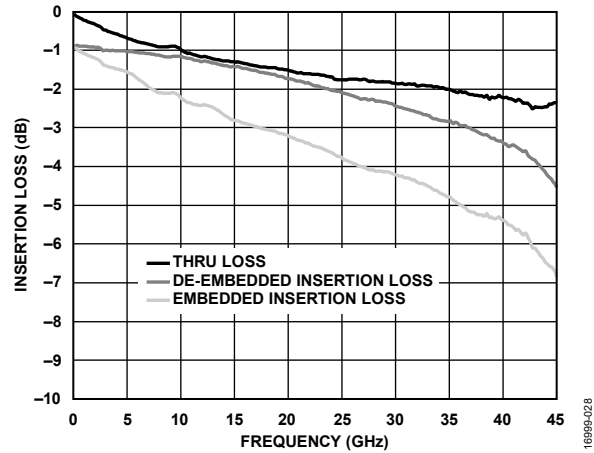


Figure 28. Insertion Loss vs. Frequency

Figure 29 shows the actual [ADRF5721-EVALZ](#) evaluation board with component placement.

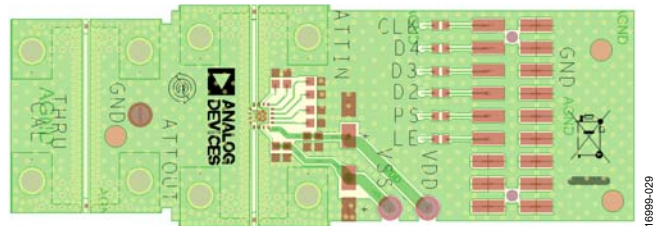


Figure 29. Evaluation Board Layout, Top View

Two power supply ports are connected to the VDD and VSS test points, TP1 and TP2, and the ground reference is connected to the GND test point, TP4. On the supply traces, VDD and VSS, use a 100 pF bypass capacitor to filter high frequency noise. Additionally, unpopulated components positions are available for applying extra bypass capacitors.

All the digital control pins are connected through digital signal traces to the 2 × 9-pin header, P1. There are provisions for a resistor capacitor (RC) filter that helps eliminate dc-coupled noise. The ADRF5721 was evaluated without an external RC filter, the series resistors are 0 Ω, and shunt capacitors are unpopulated on the evaluation board.

The RF input and output ports (ATTIN and ATTOUT) are connected through 50 Ω transmission lines to the 2.4 mm RF launchers, J1 and J2, respectively. These high frequency RF launchers are connected by contact and are not soldered onto the board.

A thru calibration line connects the unpopulated J3 and J4 launchers. This transmission line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

The schematic of the [ADRF5721-EVALZ](#) evaluation board is shown in Figure 30.

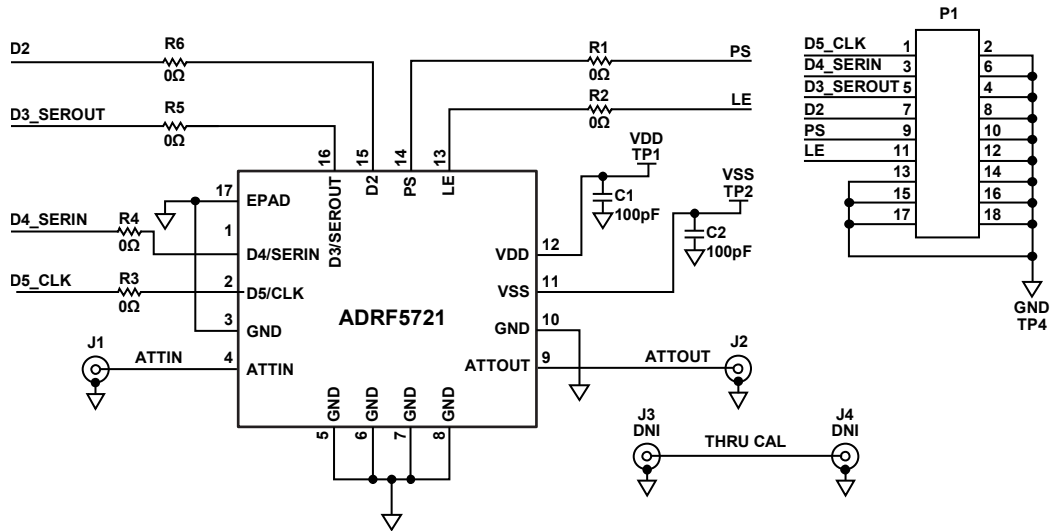


Figure 30. Evaluation Board Schematic

16999-030

Table 8. Evaluation Board Components

| Component | Default Value | Description |
|---------------|----------------|--|
| C1, C2 | 100 pF | Capacitors, C0402 package |
| J1, J2 | Not applicable | 2.4 mm end launch connectors (Southwest Microwave: 1492-04A-6) |
| P1 | Not applicable | 2 × 9-pin header |
| R1 to R6 | 0 Ω | Resistors, 0402 package |
| TP1, TP2, TP4 | Not applicable | Through hole mount test points |
| U1 | ADRF5721 | ADRF5721 digital attenuator, Analog Devices, Inc. |

PROBE MATRIX BOARD

The probe matrix board is a 4-layer board. Similar to the evaluation board, the probe matrix board also uses a 12 mil Rogers RO4003 dielectric. The top and bottom copper layers are 1.5 oz (2.2 mil) plated to 1.5 oz (2.2 mil). The RF transmission lines are designed using a CPWG model with a width of 16 mil and ground spacing of 6 mil to have a characteristic impedance of 50 Ω.

Figure 31 and Figure 32 show the cross sectional view and the top view of the board, respectively. Measurements are made using GSG probes at close proximity to the RF pins (ATTIN and ATTOUT). Unlike the evaluation board, probing reduces reflections caused by mismatch arising from connectors, cables, and board layout, resulting in a more accurate measurement of the device performance.

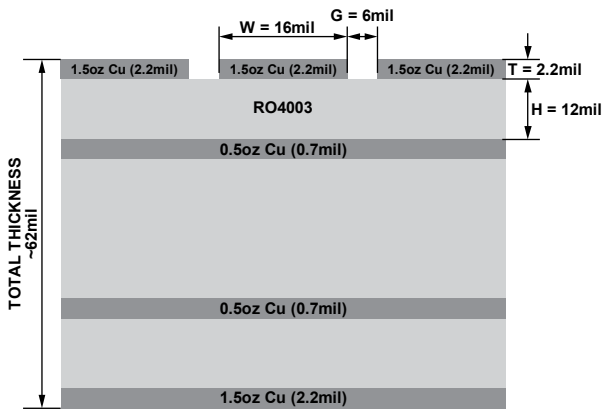


Figure 31. Probe Matrix Board (Cross Sectional View)

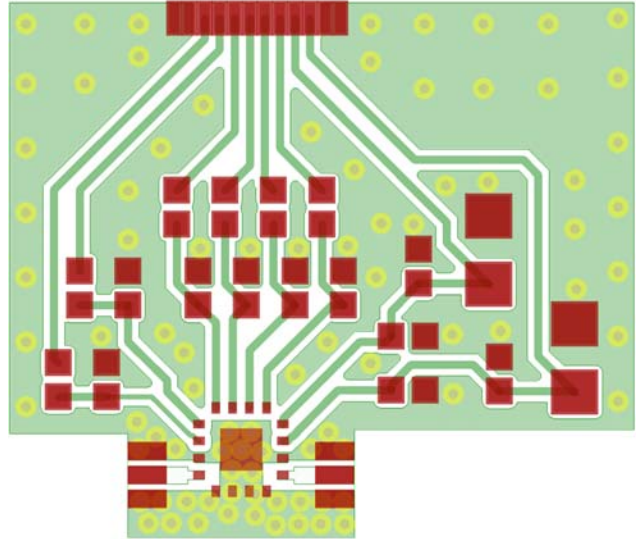


Figure 32. Probe Matrix Board Layout (Top View)

The probe matrix board includes a thru reflect line (TRL) calibration kit, allowing board loss de-embedding. The actual board duplicates the same layout in matrix form to assemble multiple devices at one time. Figure 33 is a detailed image of the trace to pin transition with corresponding dimensions. All S parameters were measured on this board.

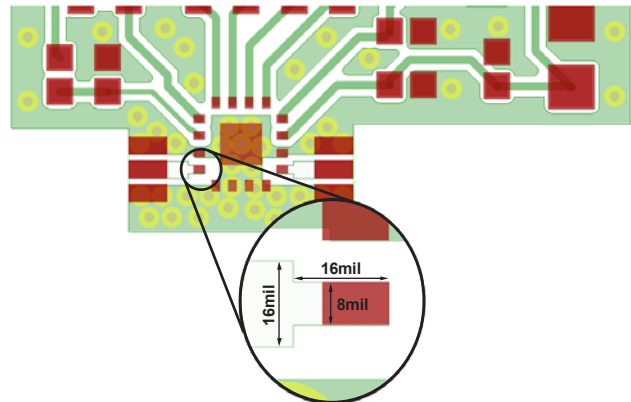


Figure 33. Probe Board Layout Dimensions (Top View)

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

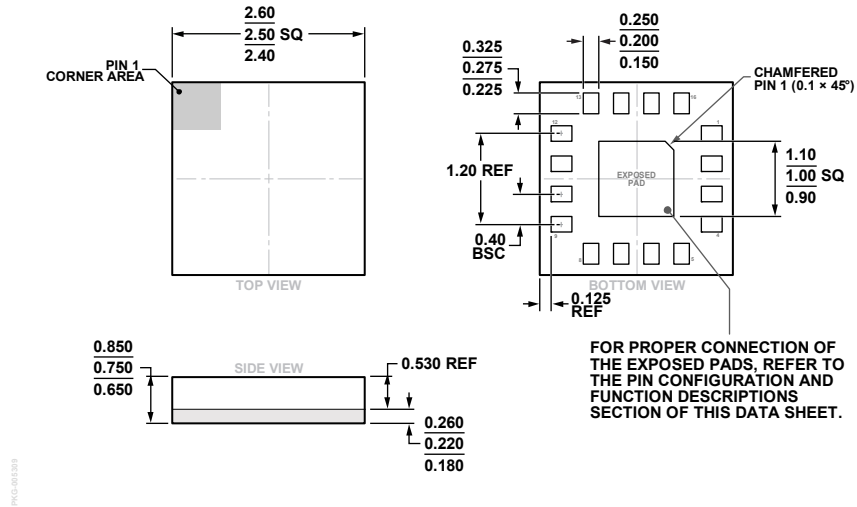


Figure 34. 16-Terminal Land Grid Array [LGA]
 2.5 mm × 2.5 mm Body and 0.75 mm Package Height
 (CC-16-6)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Marking Code |
|--------------------|-------------------|-----------------------------------|----------------|--------------|
| ADRF5721BCCZN | −40°C to +105°C | 16-Terminal Land Grid Array [LGA] | CC-16-6 | 21 |
| ADRF5721BCCZN-R7 | −40°C to +105°C | 16-Terminal Land Grid Array [LGA] | CC-16-6 | 21 |
| ADRF5721-EVALZ | | Evaluation Board | | |

¹ Z = RoHS Compliant Part.