

**PI6C49S1504T**

**High Performance Selectable 1:4 Differential Fanout Buffer**

**Features**

- 4 differential outputs with 2 banks
- User-configurable output signaling standard for each bank: LVDS or LVPECL or HCSL
- LVC MOS reference output up to 200MHz
- Up to 1.5GHz output frequency for differential outputs
- Ultra-low additive phase jitter: < 0.03ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Selectable reference inputs support either single-ended or differential or Xtal
- Low skew between outputs within banks (<40ps)
- Low delay from input to output (Tpd typ. < 1.5ns)
- Separate input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](https://www.diodes.com/quality/product-definitions/) or your local Diodes representative.
- Packaging (Pb-free & Green):
  - 32-pin, TQFN (ZH)

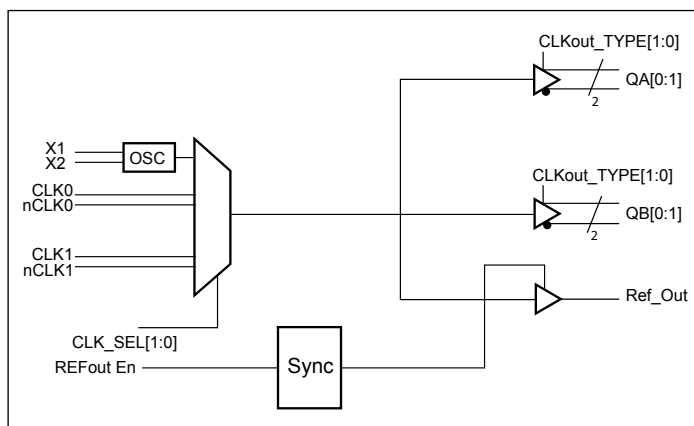
**Description**

The PI6C49S1504T is a high-performance fanout buffer device which supports up to 1.5GHz frequency. This device is ideal for systems that need to distribute low-jitter clock signals to multiple destinations.

**Applications**

- Networking Systems, including Switches and Routers
- High-Frequency Backplane-based Computing and Telecom Platforms

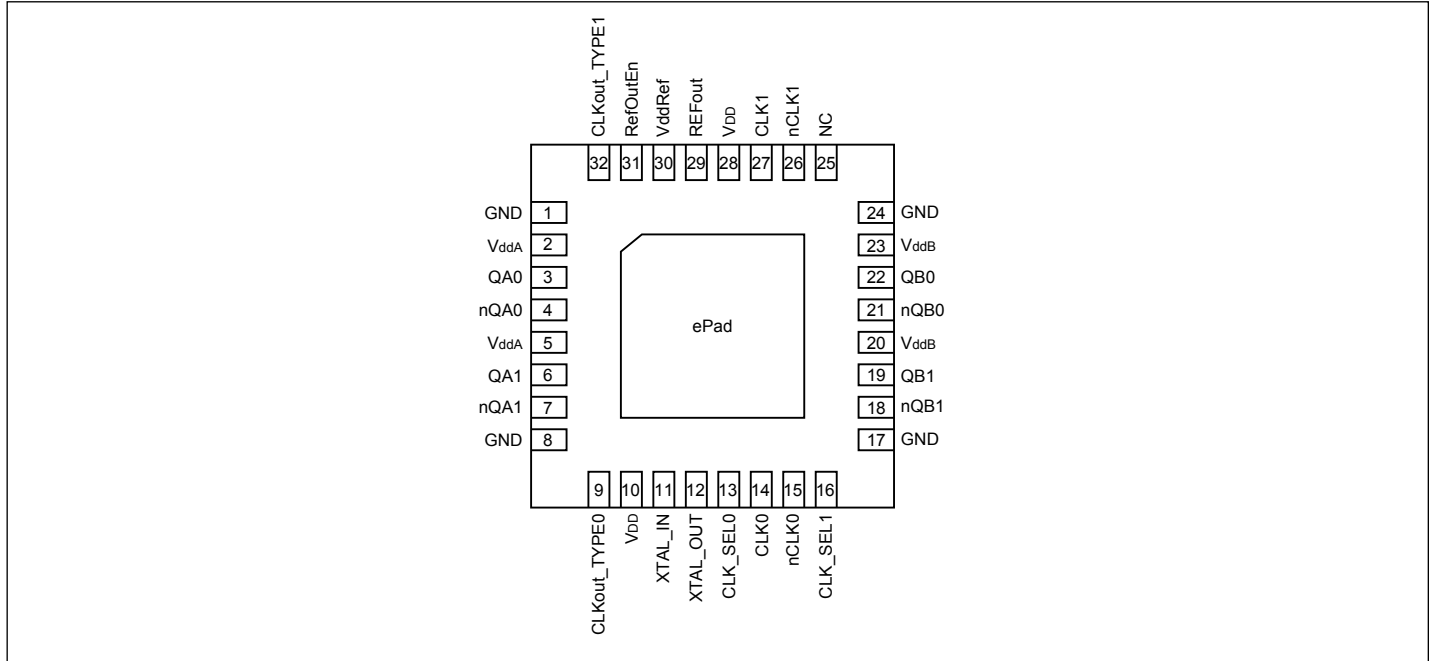
**Block Diagram**



**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Configuration



## Pin Description

Pin #	Pin Name	Type	Description
1, 8, 17, 24	GND	Power	Negative power supply
25	NC	-	Not Connect
2, 5	V <sub>ddA</sub>	Power	Power supply for Bank A Output buffers. V <sub>ddA</sub> operates from 3.3V or 2.5V
13	CLK_SEL0	Input	Clock input source selection pin
16	CLK_SEL1	Input	Clock input source selection pin
14, 15	CLK0 nCLK0	Input	Differential clock input
27, 26	CLK1 nCLK1	Input	Differential clock input
11	XTAL_In	Input	Input for crystal, XO, or single ended clock
12	XTAL_Out	Output	Output for crystal. Leave Xtal_Out floating if Xtal_In is driven by a single ended clock
10, 28	V <sub>DD</sub>	Power	Power supply for core
18, 19	nQB1 QB1	Output	Differential output clock
21, 22	nQB0 QB0	Output	Differential output clock

### Pin Description Cont.

Pin #	Pin Name	Type	Description
29	Ref_Out	Output	Reference output clock
7, 6	nQA1 QA1	Output	Differential output clock
4, 3	nQA0 QA0	Output	Differential output clock
9	CLKout_TYPE0	Input	Bank A and Bank B output buffer type selection pins
32	CLKout_TYPE1	Input	Bank A and Bank B output buffer type selection pins
ePad	ePad	GND	Connect to the PCB ground
20, 23	V <sub>ddB</sub>	Power	Power supply for Bank B Output buffers. V <sub>ddB</sub> operates from 3.3 V or 2.5V
30	VddRef	Power	Power supply for reference clock output
31	RefOutEn	Input	REFout enable input

## Function Table

Table 1: Input Selection

CLK_SEL1	CLK_SEL0	Selected Input
0	0	CLK0, nCLK0
0	1	CLK1, nCLK1
1	X	XTAL_In

Table 2: Differential Output Buffer Type Selection

CLKout_TYPE1	CLKout_TYPE0	CLKoutX Buffer Type (Bank A and B)
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Disabled (Hi-Z)

Table 3: Reference Output Enable

REFout_EN	REFout STATE
0	Disabled (Hi-Z)
1	Enabled

Table 4: CLKx Input vs. Output States

State of Selected Input Clock	State of Enabled Outputs
CLKx and nCLKx Inputs Floating	Logic Low
CLKx and nCLKx Inputs Shorted Together	Not Supported. Output is Undefined
CLKx Logic Low	Logic Low
CLKx Logic High	Logic High

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature.....	-55 to +150°C
Supply Voltage to Ground Potential ( $V_{DD}, V_{DDO}$ )...	-0.5 to +4.6V
Inputs (Referenced to GND) .....	-0.5 to $V_{DD}+0.5V$
Clock Output (Referenced to GND).....	-0.5 to $V_{DD}+0.5V$
Latch up .....	200mA
ESD Protection (Input) .....	2000V min (HBM)
Junction Temperature .....	150 °C max

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Power Supply Characteristics and Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{DD}$	Core Supply Voltage		2.375		3.465	V
$V_{DDO}$	Output Supply Voltage	$V_{DDO} \leq V_{DD}$	2.375		3.465	V
$I_{DD}$	Core Power Supply Current			90	120	mA
$I_{DDO}$	Output Power Supply Current	All LVPECL outputs unloaded		150	190	
		All LVDS outputs loaded		110	130	
		All HCSL outputs loaded		95		
$T_A$	Ambient Operating Temperature <sup>(1)</sup>		-40		85	°C
$T_B$	PCB Operating Temperature <sup>(1)</sup>		-40		105	°C

Note:

1. Either  $T_A$  or  $T_B$  used as operating condition

## DC Electrical Specifications - Differential Inputs

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$I_{IH}$	Input High current	Input = $V_{DD}$			150	uA
$I_{IL}$	Input Low current	Input = GND	-150			uA
$C_{IN}$	Input capacitance			3		PF
$V_{IH}$	Input high voltage				$V_{DD}+0.3$	V
$V_{IL}$	Input low voltage		-0.3			V
$V_{ID}$	Input Differential Amplitude PK-PK		0.15		1.3	V
$V_{CM}$	Common mode input voltage		0.25		$V_{DD}-1.2$	V
$ISO_{MUX}$	MUX isolation			-89		dBc

### DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{IH}$	Input High current	Input = $V_{DD}$			150	$\mu A$
$I_{IL}$	Input Low current	Input = GND	-150			$\mu A$
$V_{IH}$	Input high voltage	$V_{DD}=3.3V$	2.0		$V_{DD}+0.3$	V
$V_{IL}$	Input low voltage	$V_{DD}=3.3V$	-0.3		0.8	V
$V_{IH}$	Input high voltage	$V_{DD}=2.5V$	1.7		$V_{DD}+0.3$	V
$V_{IL}$	Input low voltage	$V_{DD}=2.5V$	-0.3		0.7	V

### DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
$V_{OH}$	Output High voltage		$V_{DDO}-1.4$		$V_{DDO}-0.9$	V
$V_{OL}$	Output Low voltage		$V_{DDO}-2.2$		$V_{DDO}-1.7$	V

### DC Electrical Specifications- LVDS Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
$V_{OH}$	Output High voltage		1.4	1.5	1.6	V
$V_{OL}$	Output Low voltage		1	1.1	1.25	V
$V_{ocm}$	Output commode voltage		1.2	1.3	1.45	V
$DV_{ocm}$	Change in $V_{ocm}$ between completely output states				50	mV
$R_o$	Output impedance		85		140	$\Omega$

### DC Electrical Specifications – HCSL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
$V_{OH}$	Output High voltage	2.5V	660	725	850	mV
		3.3V	700	850	900	mV
$V_{OL}$	Output Low voltage		-150		150	mV

### DC Electrical Specifications – LVCMOS Output

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V <sub>OH</sub>	Output High voltage	V <sub>DDO</sub> =3.3V +/-5%, I <sub>OH</sub> = -8mA	2.3			V
		V <sub>DDO</sub> =2.5V +/- 5%, I <sub>OH</sub> = -8mA	1.5			V
V <sub>OL</sub>	Output Low voltage	V <sub>DDO</sub> =3.3V +/-5%, I <sub>OL</sub> = 8mA			0.5	V
		V <sub>DDO</sub> =2.5V +/- 5%, I <sub>OL</sub> = 8mA			0.4	V
V <sub>OH</sub>	Output High voltage	V <sub>DDO</sub> =3.3V +/-5%, I <sub>OH</sub> = -24mA	2.1			V
		V <sub>DDO</sub> =2.5V +/- 5%, I <sub>OH</sub> = -16mA	1.5			V
V <sub>OL</sub>	Output Low voltage	V <sub>DDO</sub> =3.3V +/-5%, I <sub>OL</sub> = 24mA			1	V
		V <sub>DDO</sub> =2.5V +/- 5%, I <sub>OL</sub> = 16mA			0.8	V

### AC Electrical Specifications – Differential Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units	
F <sub>OUT</sub>	Clock output frequency	LVPECL, LVDS			1500	MHz	
		HCSL			250		
T <sub>r</sub>	Output rise time	From 20% to 80%	LVPECL	100	150	300	ps
			LVDS	100	150	300	
			HCSL	300		700	
T <sub>f</sub>	Output fall time	From 80% to 20%	LVPECL	100	150	300	ps
			LVDS	100	150	300	
			HCSL	300		700	
T <sub>ODC</sub>	Output duty cycle	Frequency<650MHz, V <sub>ID</sub> ≥ 400mV	LVPECL, HCSL (<250MHz)	48		52	%
			LVDS	47		53	
		Frequency<1GHz, V <sub>ID</sub> ≥ 400mV	LVPECL	45		55	
			LVDS	45		55	
		Frequency<1.5GHz, V <sub>ID</sub> ≥ 400mV	LVDS	40		60	
Frequency<1.5GHz, V <sub>ID</sub> ≥ 400mV	LVPECL	40		60			
V <sub>PP</sub>	Output swing Single-ended	LVPECL outputs @ <1GHz		500		1100	mV
		LVPECL outputs @ >1GHz		400		1000	
		LVDS outputs @ <1GHz		250		600	
		LVDS outputs @ >1GHz		250		550	
T <sub>j</sub>	Buffer additive jitter RMS	156.25MHz, 12kHz to 20MHz			0.02	ps	
		156.25MHz, 10kHz to 1MHz			0.01	ps	

**AC Electrical Specifications – Differential Outputs Cont.**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
V <sub>CROSS</sub>	Absolute crossing voltage	HCSL		460		mV
DV <sub>CROSS</sub>	Total variation of crossing voltage	HCSL			140	mV
T <sub>SK</sub>	Output Skew	4 outputs devices, outputs in same bank, with same load, at DUT.		15	40	ps
T <sub>PD</sub>	Propagation Delay	LVPECL, LVDS @ 3.3V, 100MHz		570		ps
		HCSL @ 3.3V, 100MHz		900		ps
T <sub>OD</sub>	Valid to HiZ				200	ns
T <sub>OE</sub>	HiZ to valid				200	ns
T <sub>P2P Skew</sub>	Part to Part Skew <sup>(1)</sup>			80	120	ps

**AC Electrical Specifications – CMOS**

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
F <sub>OUT</sub>	Ref_Out frequency	XTAL input	10		50	MHz
		Reference input			200	MHz
T <sub>j</sub>	Buffer additive jitter RMS	XTAL input		0.3		ps
		Reference input		0.03		ps
t <sub>r</sub> /t <sub>f</sub>	Rise time, Fall time	C <sub>L</sub> = 5pF		0.8		ns
T <sub>ODC</sub>	Output duty cycle	C <sub>L</sub> = 5pF 3.3V, max test freq. 250MHz 2.5V, max test freq. 150MHz	45		55	%
t <sub>PD</sub>	Propagation delay	3.3V, 25MHz		4500		ps
t <sub>s</sub>	Setup time		300			ps
t <sub>SOD</sub>	Clock edge to output disable	Ref_Out	2		4	cycles
t <sub>SOE</sub>	Clock edge to output enable	Ref_Out	2		4	cycles
R <sub>IUT</sub>	Output Impedance	V <sub>DDO</sub> = 3.3V ± 5%		30		Ω
		V <sub>DDO</sub> = 2.5V ± 5%		45		Ω

**Notes:**

- This parameter is guaranteed by design



### Crystal Characteristics

Parameter	Min.	Typ.	Max.	Units
Mode of Oscillation	Fundamental			
Frequency Range	10		50	MHz
Equivalent Series Resistance (ESR)			70	$\Omega$
Shunt Capacitance			7	pF
Load Capacitance	10		18	pF
Drive Level			500	$\mu$ W

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### Recommended Crystals

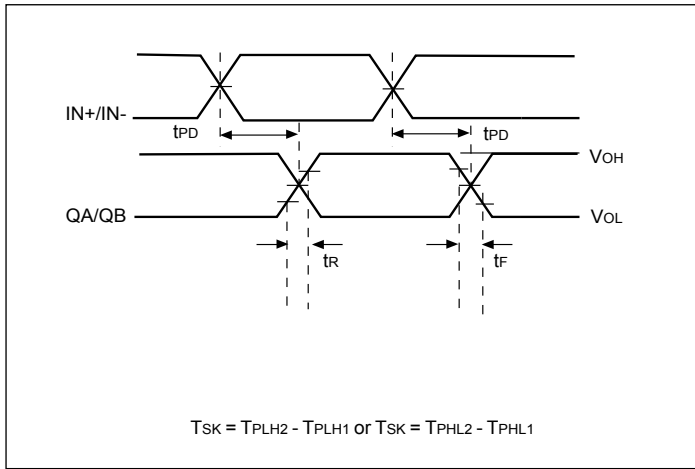
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Diodes Recommends:

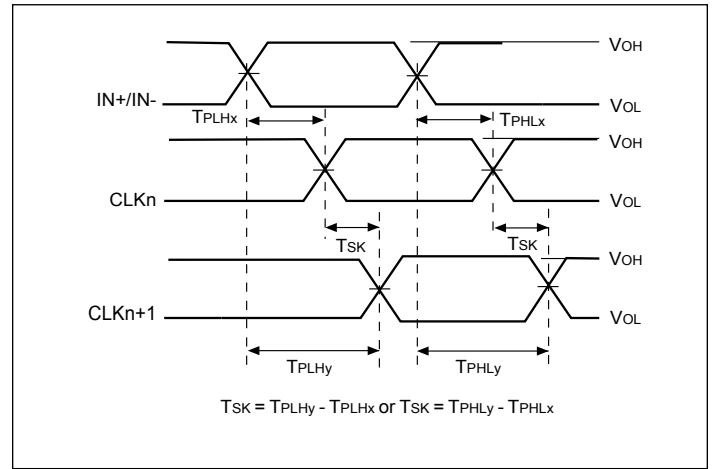
- a) GC2500003 XTAL 49S/SMD(4.0 mm), 25M, CL=18pF, +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/GC\\_GF.pdf](http://www.pericom.com/pdf/datasheets/se/GC_GF.pdf)
- b) FY2500091, SMD 5x3.2(4P), 25M, CL=18pF, +/-30ppm  
[http://www.pericom.com/pdf/datasheets/se/FY\\_F9.pdf](http://www.pericom.com/pdf/datasheets/se/FY_F9.pdf)
- c) FL2500047, SMD 3.2x2.5(4P), 25M, CL=18pF, +/-20ppm  
<http://www.pericom.com/pdf/datasheets/se/FL.pdf>

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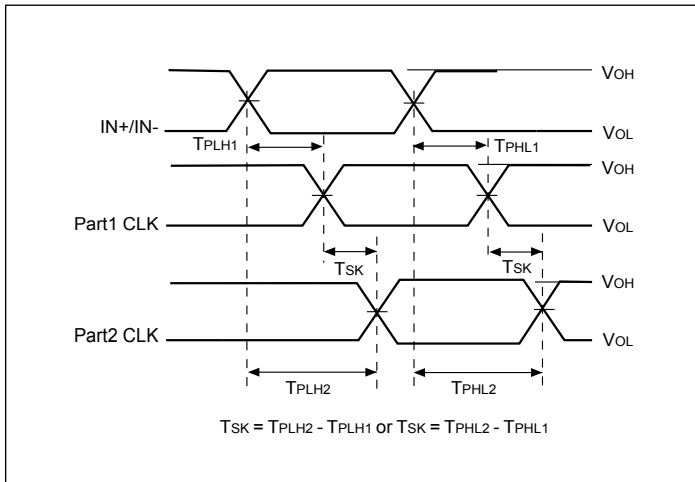
**Propagation Delay (T<sub>PD</sub>)**



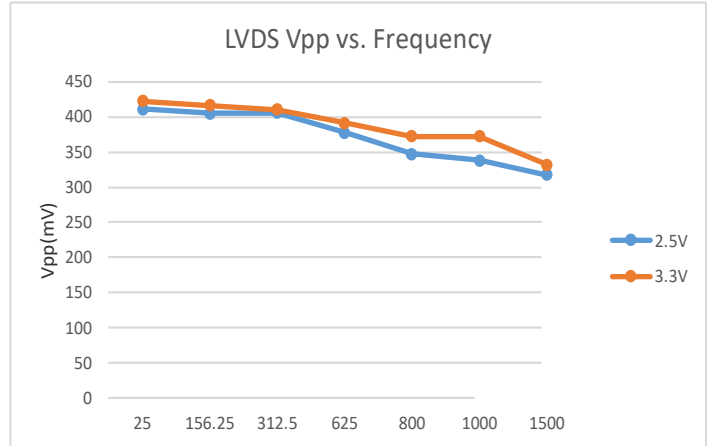
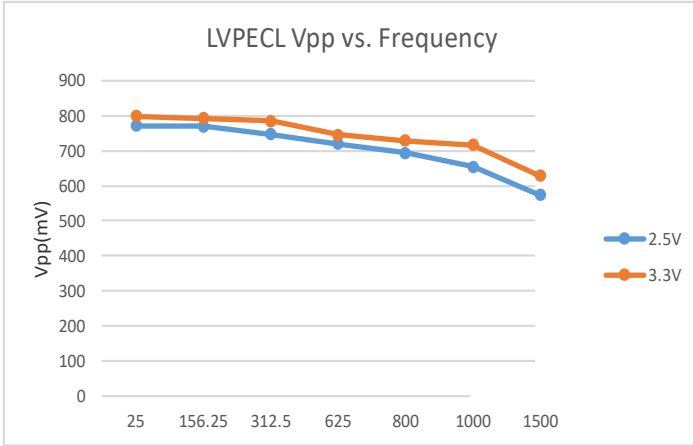
**Output Skew (T<sub>SK</sub>)**



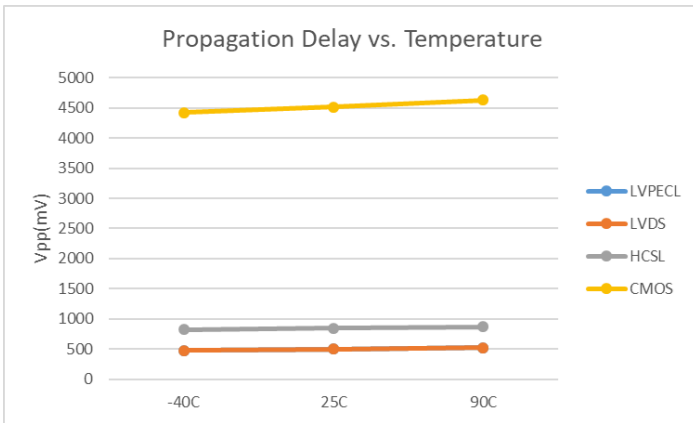
**Part to Part Skew**



**LVPECL/ LVDS Output Swing vs. Frequency**



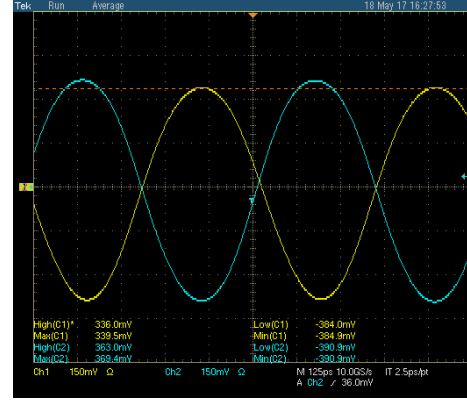
**Propagation Delay vs Temperature**



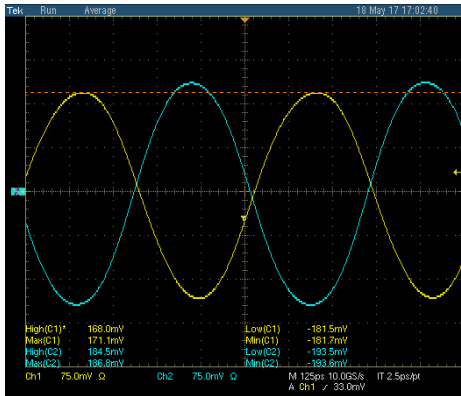
**1.5GHz LVPECL/ LVDS Waveform**



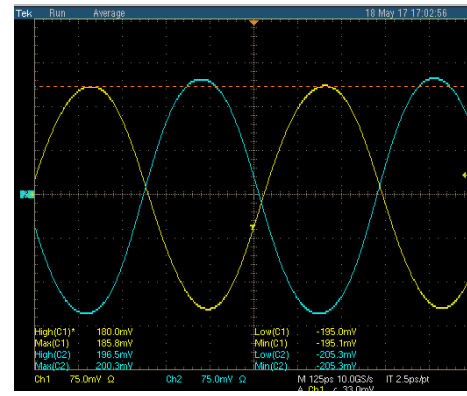
**2.5V LVPECL Waveform**



**3.3V LVPECL Waveform**



**2.5V LVDS Waveform**



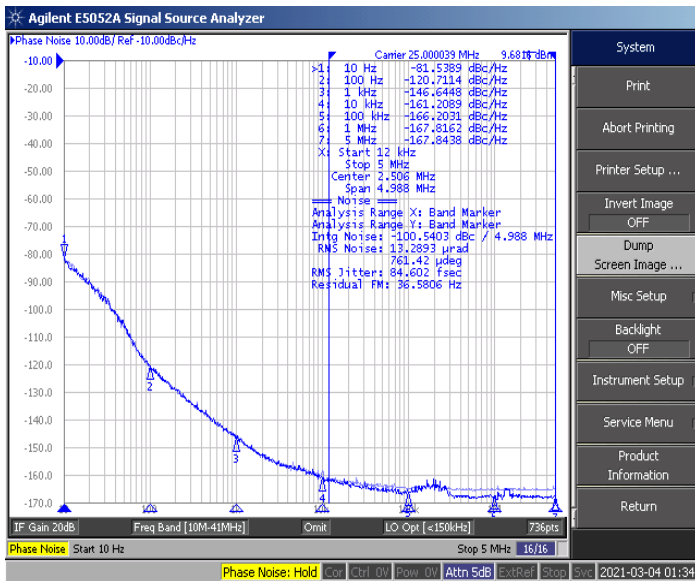
**3.3V LVDS Waveform**

## Phase Noise and Additive Jitter

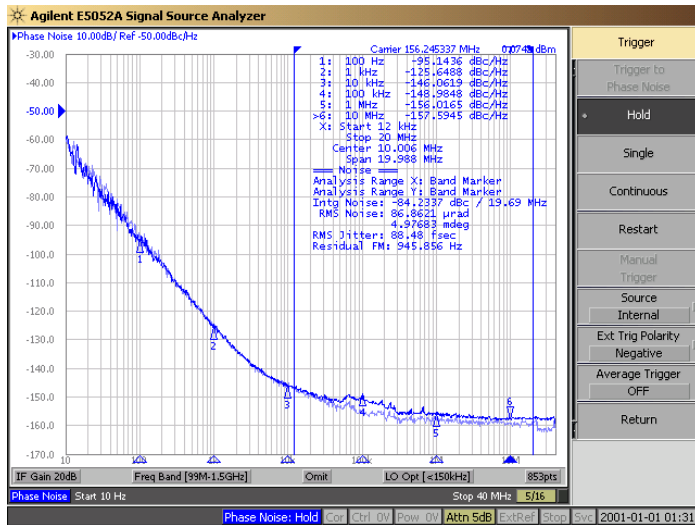
Output phase noise (Dark Blue) vs Input Phase noise (light blue)

Additive jitter is calculated at 25MHz ~71fs RMS (12kHz to 5MHz). Additive jitter =  $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$

Ref\_out 25MHz Phase Noise Plot, VDD=VDDO=3.3V, 25°C, Driven by 25MHz CMOS XO

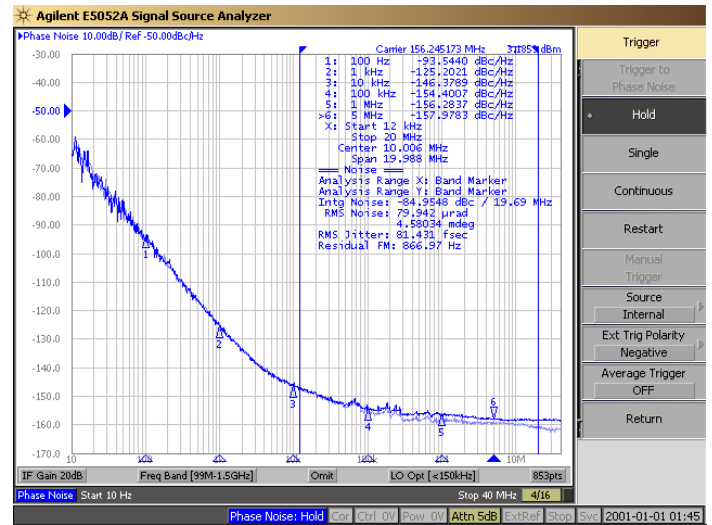


## 156.25M LVDS Output Additive Jitter Noise Plot, 3.3V



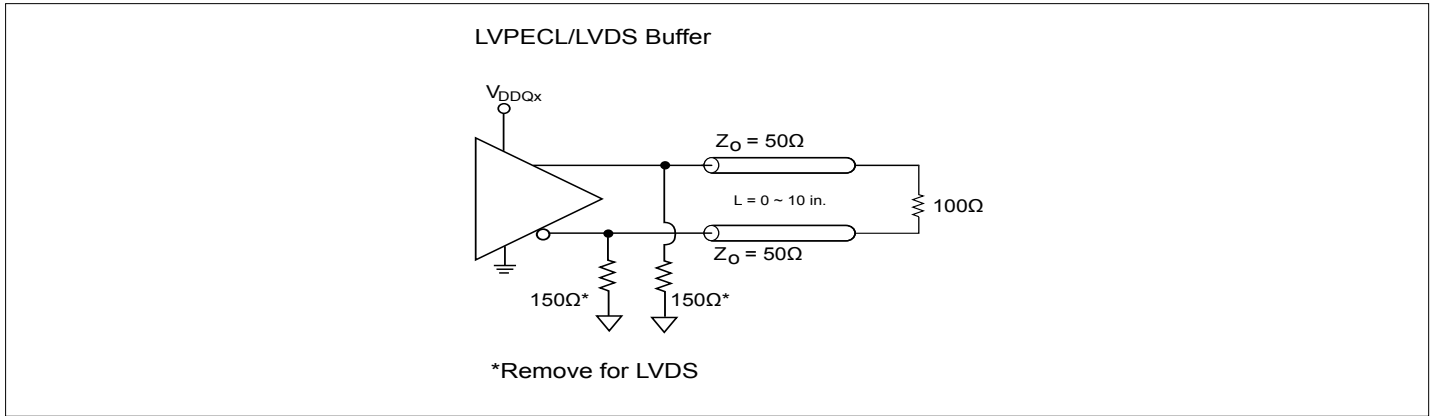
3.3V LVDS Output Jitter 88fs vs. Input 72fs

## 156.25M LVPECL XO Input, LVPECL output Noise, 3.3V

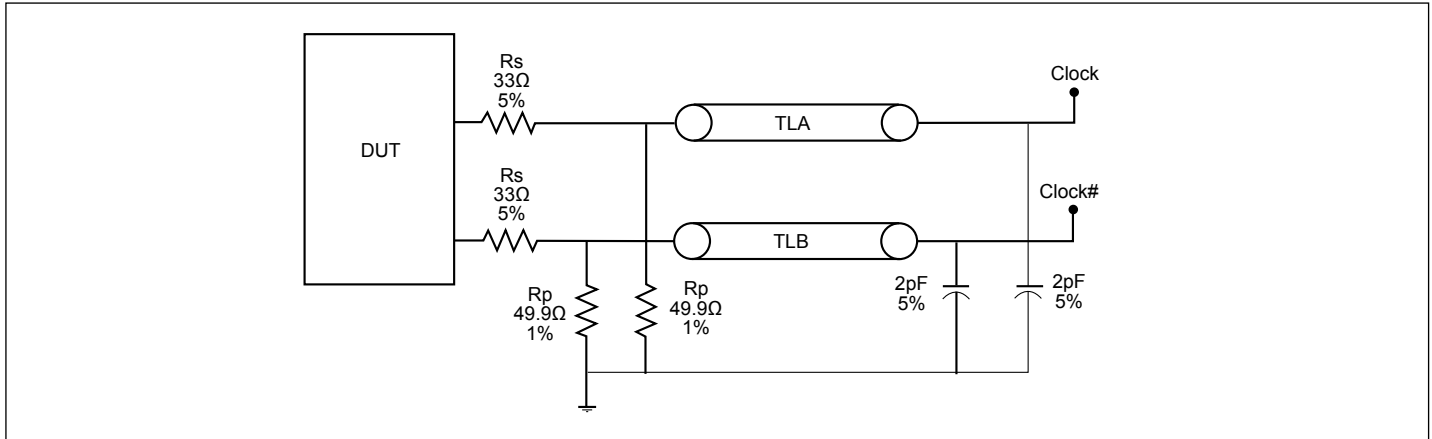


3.3V 156.25M LVPECL Input LVPECL output Jitter 81fs vs. input jitter 75fs

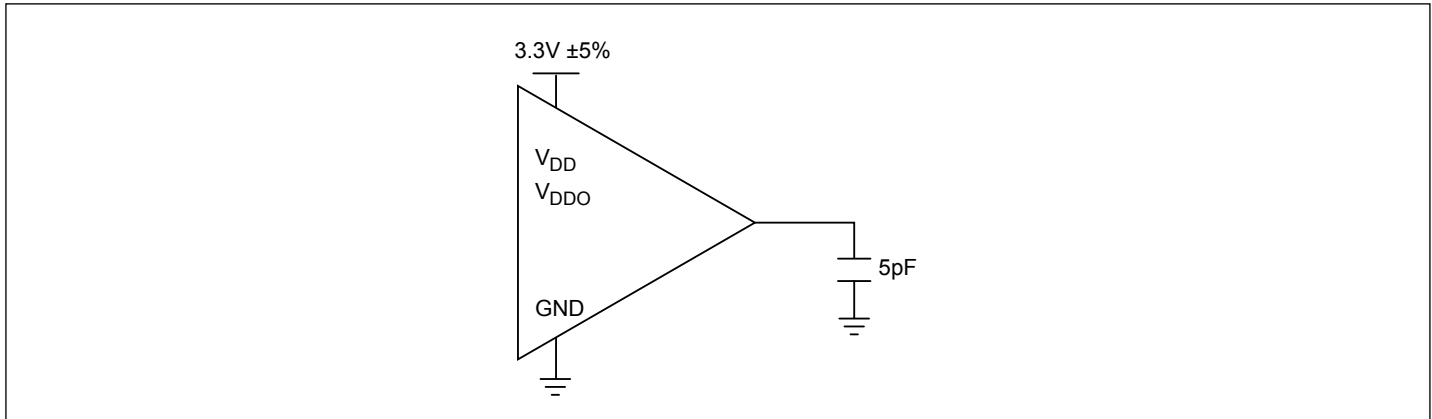
**Configuration Test Load Board Termination for LVPECL/ LVDS Outputs**



**Configuration Test Load Board Termination for HCSL Outputs**



**Configuration Test Load Board Termination for LVCMOS Outputs**



## Application Information

### Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

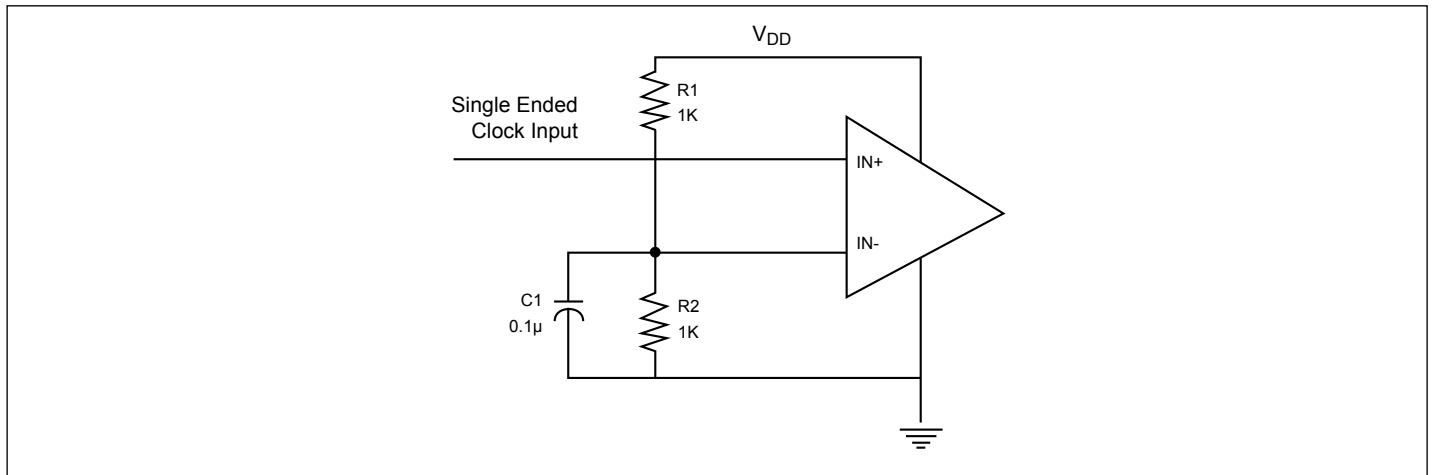
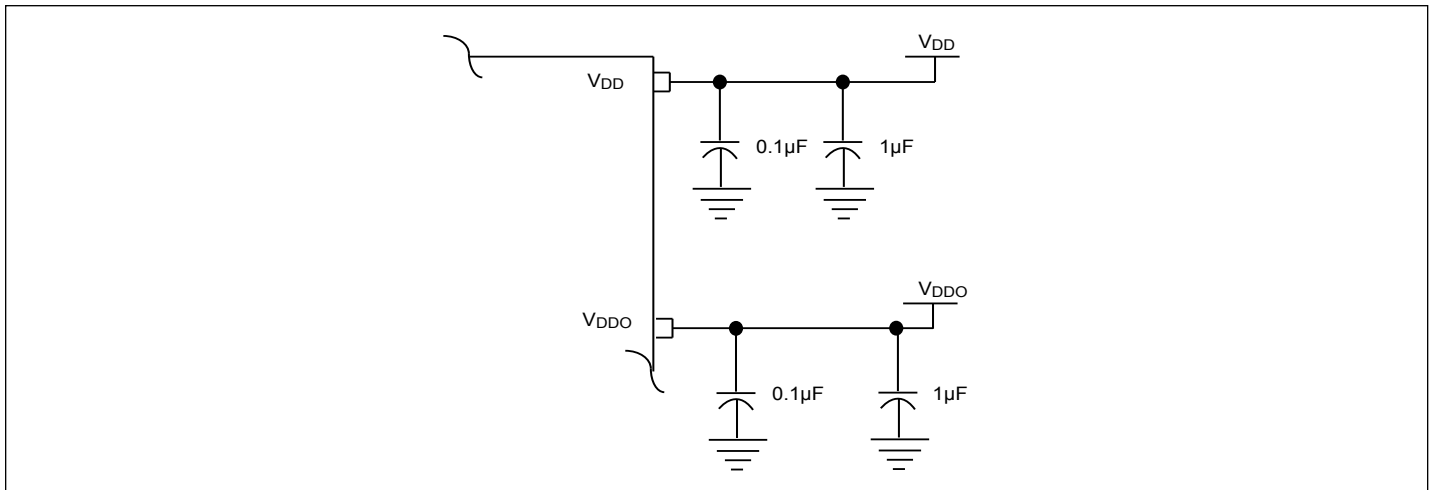


Figure 1. Single-ended Input to Differential Input Device

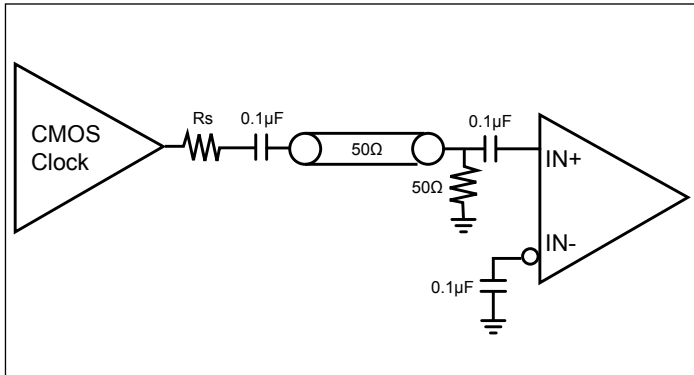
## Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. All power pins should be individually connected to the power supply plane through vias, and  $0.1\mu F$  and  $1\mu F$  bypass capacitors should be used for each pin.

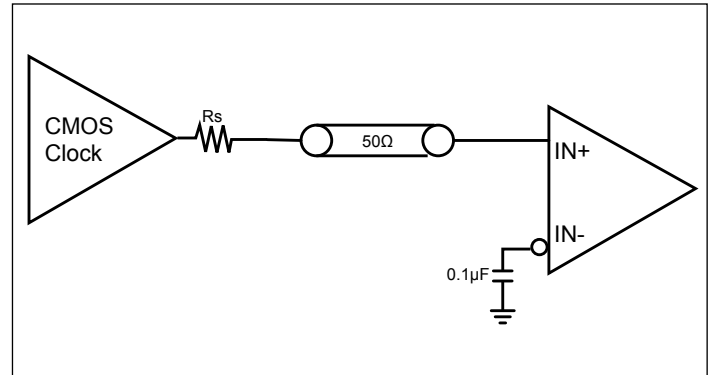


**PI6C49S1504T**

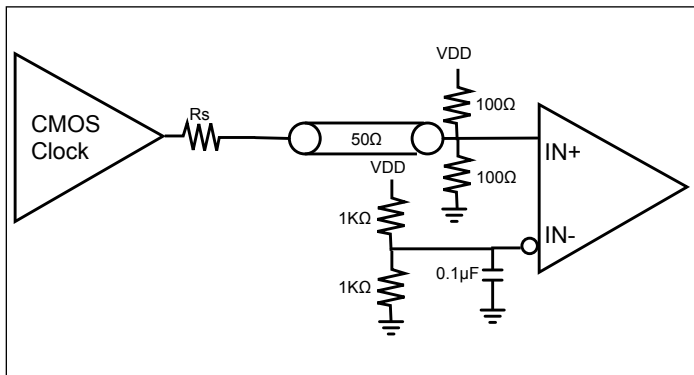
**Single Ended Input, AC Couple**



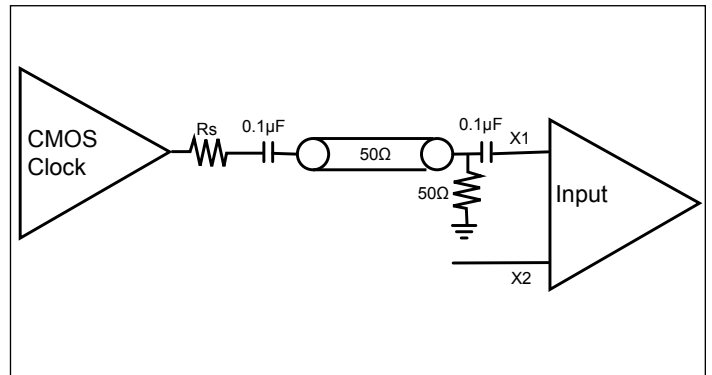
**Single Ended Input, DC Couple**



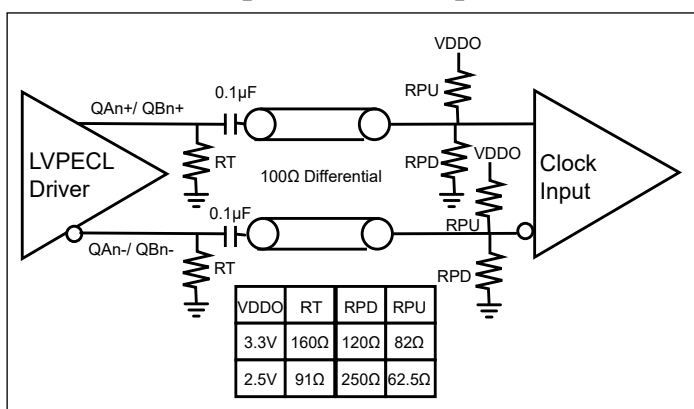
**Single Ended Input, DC Couple**



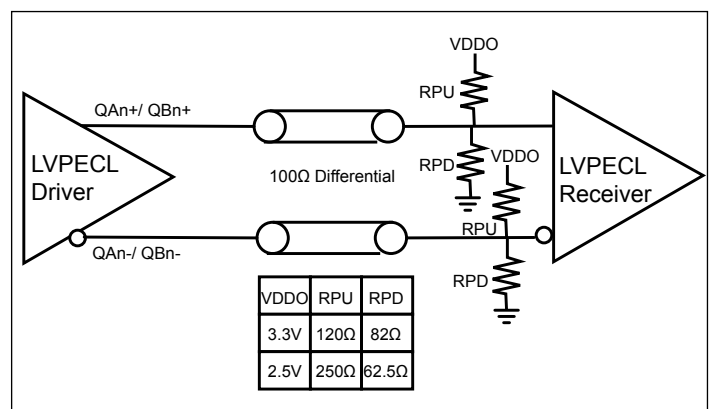
**Driving X1 with a Single Ended Input**



**LVPECL, AC Couple, Thevenin Equivalent**



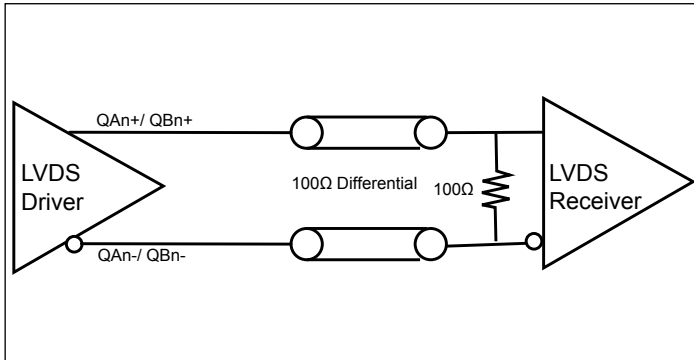
**LVPECL, DC Couple, Thevenin Equivalent**



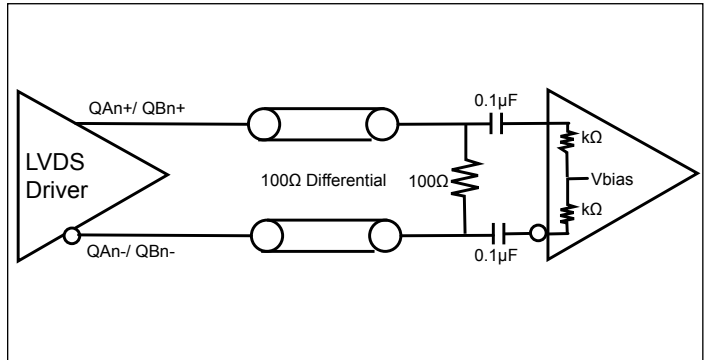


**PI6C49S1504T**

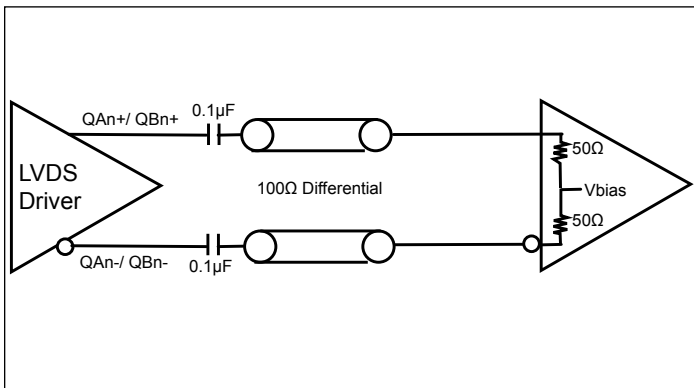
**LVDS DC Couple**



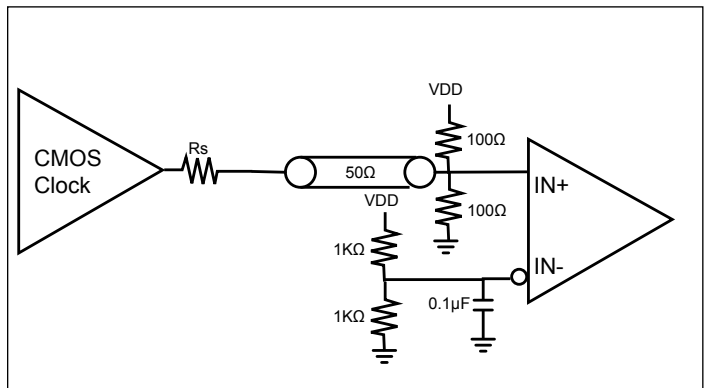
**LVDS AC Couple at Load**



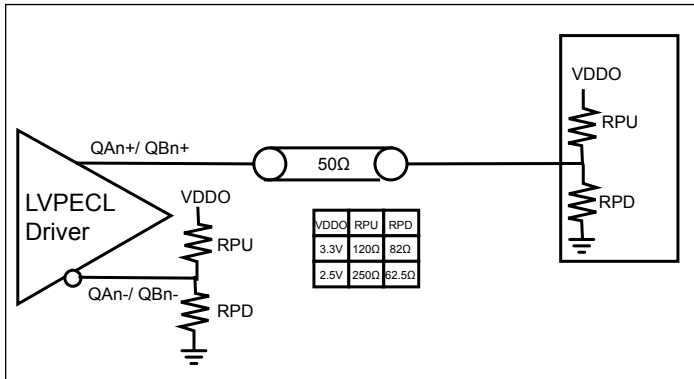
**LVDS AC Couple with Internal Termination**



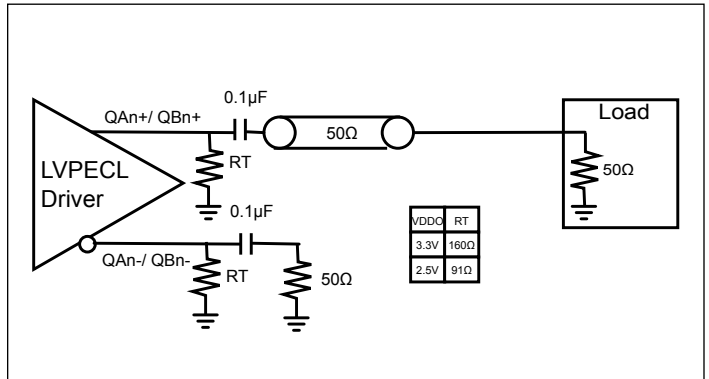
**Single Ended LVPECL, DC Couple**



**Single Ended LVPECL, DC Couple, Thevenin Equivalent**

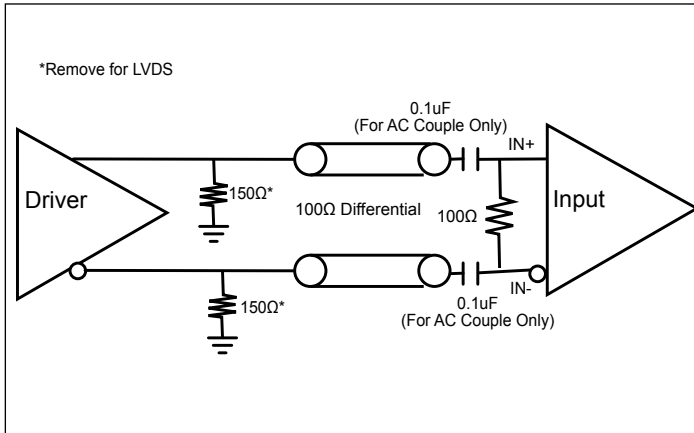


**Single Ended LVPECL, AC Couple, Thevenin Equivalent**

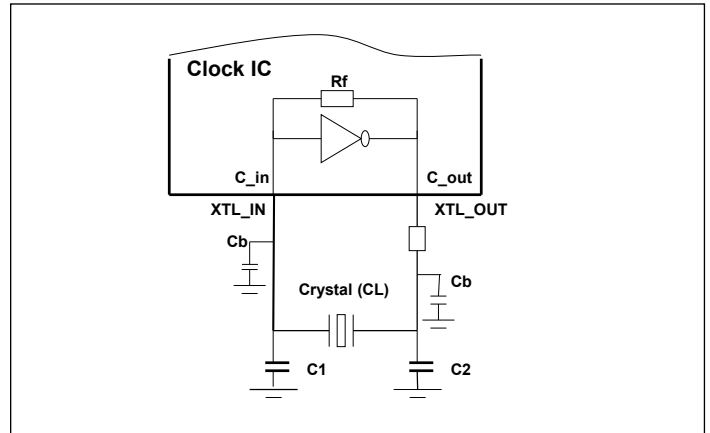


**PI6C49S1504T**

**LVPECL/ LVDS AC and DC input**



**Clock IC Crystal Input Guide**

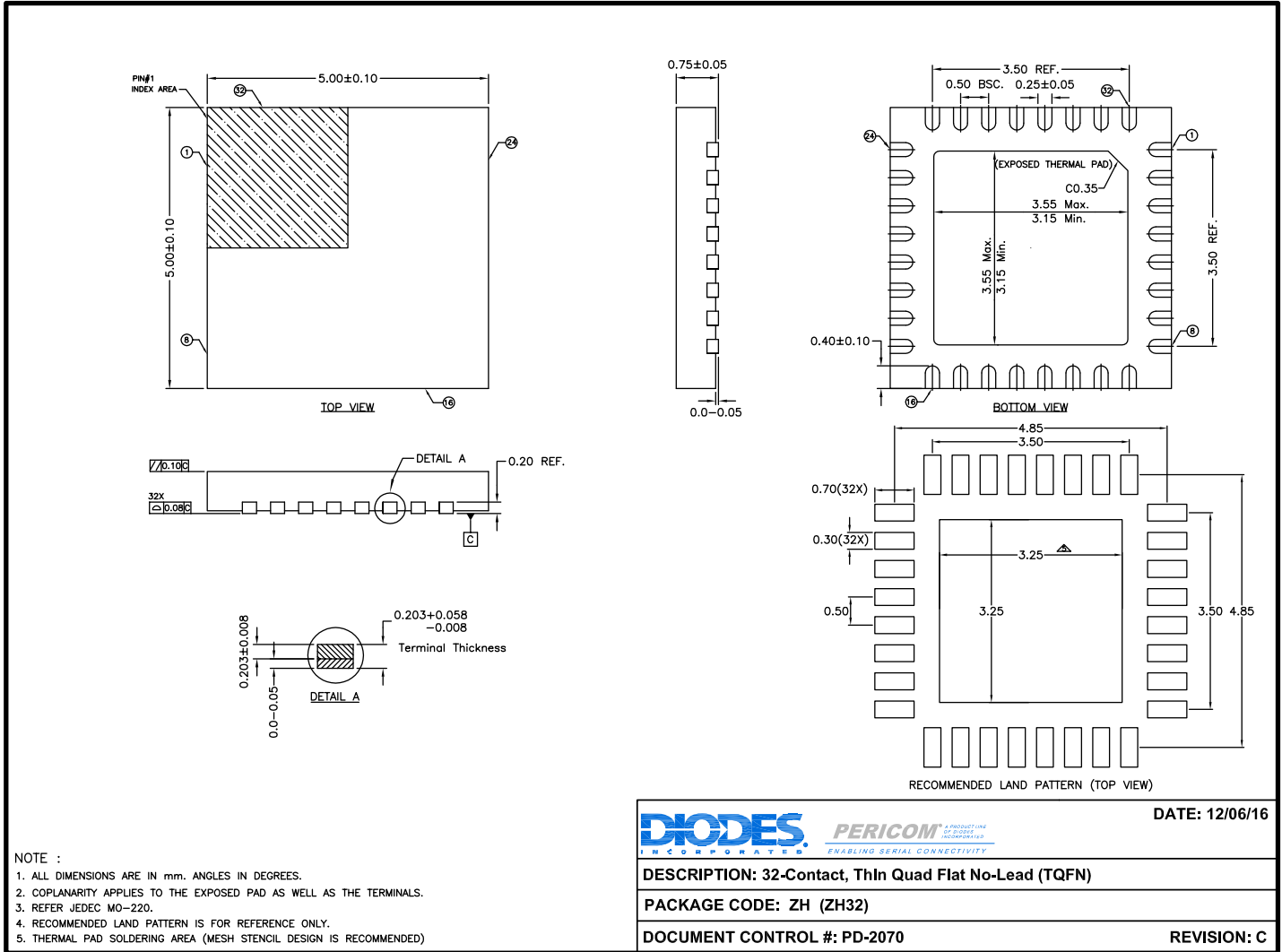


**Part Marking**

Top mark not available at this time. To obtain advance information regarding the top mark, please contact your local sales representative.

**Packaging Mechanical**

**32-TQFN (ZH)**



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

17-0570

For latest package info.  
please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

Ordering Code	Package Code	Package Description	Operating Temperature
PI6C49S1504TZHIEX	ZH	32-contact, Thin Quad Flat No-Lead (TQFN)	-40 °C to 85 °C

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

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