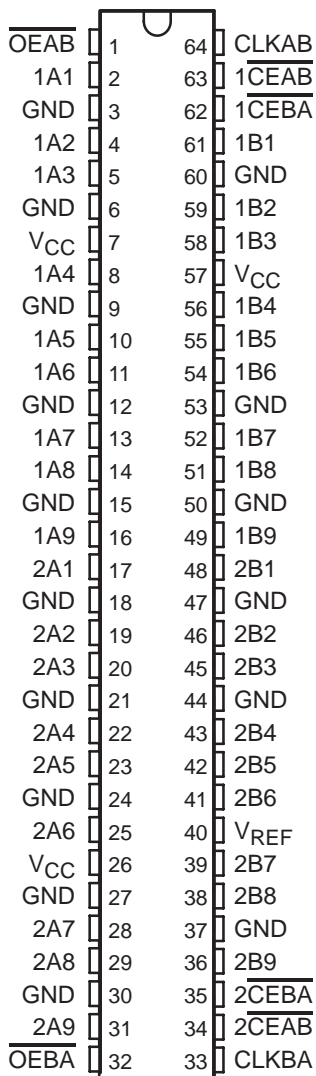


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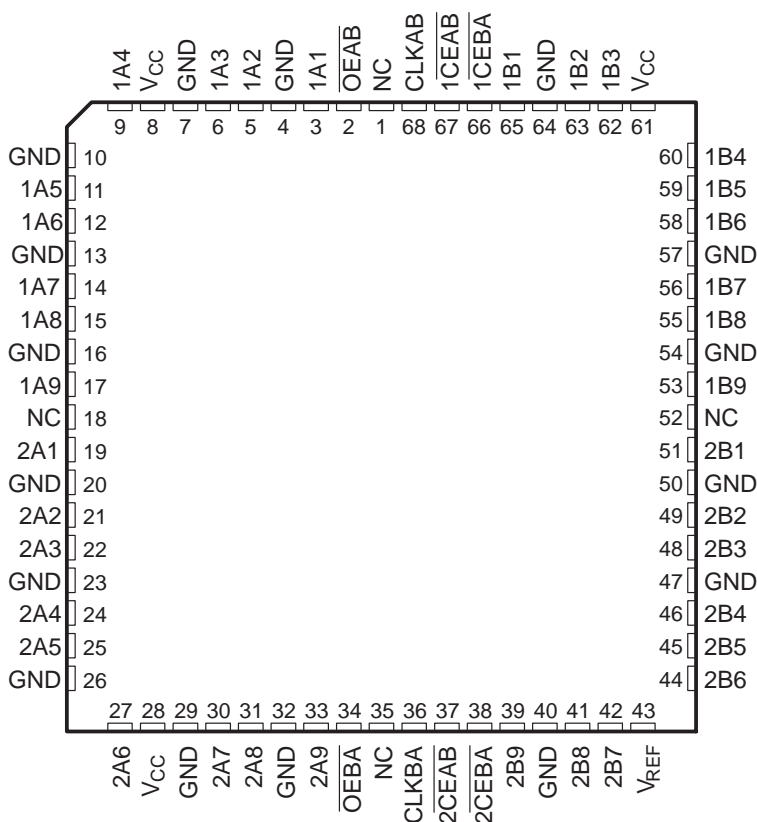
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- Translate Between GTL/GTL+ Signal Levels and LVTTTL
- Members of the Texas Instruments *Widebus™* Family
- Support GTL/GTL+ Signal Operation on B Port
- D-Type Flip-Flops With Qualified Storage Enable
- Bus-Hold Data Inputs Eliminate the Need for External Pullup or Pulldown Resistors on A Port
- Flow-Through Architecture Facilitates Printed-Circuit-Board Layout
- Package Options Include Plastic Thin-Shrink Small-Outline (DGG) and Ceramic Quad Flat (HV) Packages

SN74GTL16622 . . . DGG PACKAGE
(TOP VIEW)



SN54GTL16622 . . . HV PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN54GTL16622, SN74GTL16622 18-BIT LVTTTL-TO-GTL/GTL+ TRANSCEIVERS

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description

These 18-bit registered bus transceivers contain two sets of D-type flip-flops for temporary storage of data flowing in either direction.

The B port operates at GTL ($V_{TT} = 1.2\text{ V}$ and $V_{REF} = 0.8\text{ V}$) and GTL+ ($V_{TT} = 1.5\text{ V}$ and $V_{REF} = 1\text{ V}$) levels, while the A port and control inputs are compatible with LVTTTL logic levels.

Data flow in each direction is controlled by output-enable (\overline{OEAB} and \overline{OEBA}) and clock (CLKAB and CLKBA) inputs. The clock-enable (\overline{CEAB} and \overline{CEBA}) inputs are designed to control each 9-bit transceiver independently, which makes the device more versatile.

For A-to-B data flow, the devices operate on the low-to-high transition of CLKAB if \overline{CEAB} is low. When \overline{OEAB} is low, the outputs are active. When \overline{OEAB} is high, the outputs are in the high-impedance state. Data flow for B to A is similar to that for A to B, but uses \overline{OEBA} , CLKBA, and \overline{CEBA} .

Active bus-hold circuitry is provided to hold unused or floating TTL inputs at a valid logic state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54GTL16622 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74GTL16622 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE†

INPUTS				OUTPUT B	MODE
\overline{CEAB}	\overline{OEAB}	CLKAB	A		
X	H	X	X	Z	
H	L	X	X	B_0^{\ddagger}	Latched storage of A data
X	L	H or L	X	B_0^{\ddagger}	
L	L	↑	L	L	Clocked storage of A data
L	L	↑	H	H	

† A-to-B data flow is shown; B-to-A data flow is similar but uses \overline{OEBA} , CLKBA, and \overline{CEBA} .

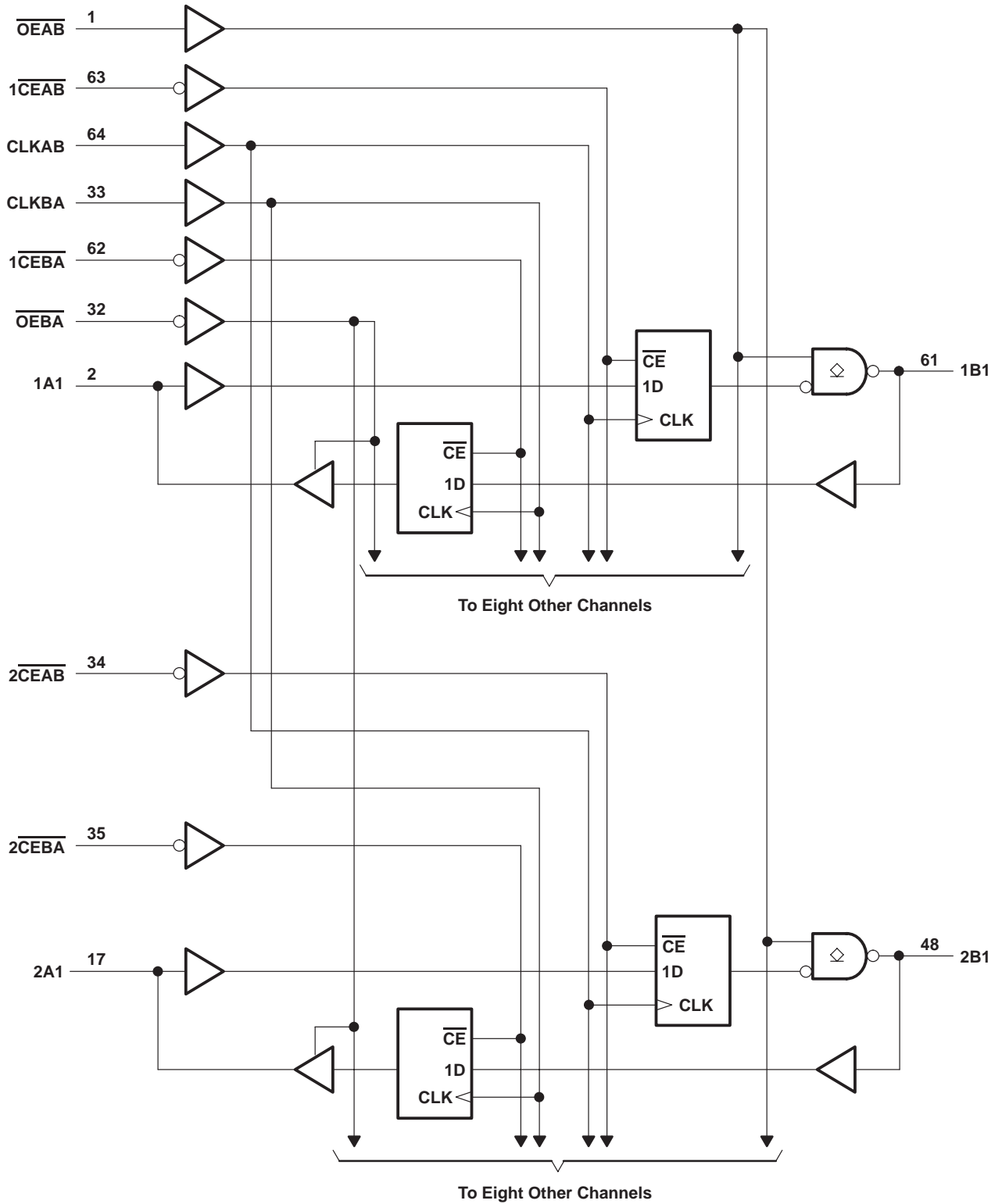
‡ Output level before the indicated steady-state input conditions are established



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logic diagram (positive logic)



Pin numbers shown are for the DGG package.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): A port/B port	–0.5 V to 4.6 V
Voltage range applied to any output in the high or power-off state, V_O (see Note 1): A port/B port	–0.5 V to 4.6 V
Current into any output in the low state, I_O : A port	48 mA
B port	100 mA
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DGG package	1.3 W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 1000 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*.

recommended operating conditions (see Note 3)

		SN54GTL16622			SN74GTL16622			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V_{CC}	Supply voltage	3.15	3.3	3.45	3.15	3.3	3.45	V	
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	1.14	1.2	1.26	V
		GTL+	1.35	1.5	1.65	1.35	1.5	1.65	
V_{REF}	Supply voltage	GTL	0.74	0.8	0.87	0.74	0.8	0.87	V
		GTL+	0.87	1	1.1	0.87	1	1.1	
V_I	Input voltage	B port	0		V_{TT}	0		V_{TT}	V
		Except B port	0		V_{CC}	0		V_{CC}	
V_{IH}	High-level input voltage	B port	$V_{REF}+50\text{ mV}$			$V_{REF}+50\text{ mV}$			V
		Except B port	2			2			
V_{IL}	Low-level input voltage	B port	$V_{REF}-50\text{ mV}$			$V_{REF}-50\text{ mV}$			V
		Except B port	0.8			0.8			
I_{IK}	Input clamp current			–18			–18	mA	
I_{OH}	High-level output current	A port			–24		–24	mA	
I_{OL}	Low-level output current	A port			24		24	mA	
		B port			50		50		
T_A	Operating free-air temperature	–55		125	–40		85	°C	

NOTE 3: Unused control inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range, $V_{REF} = 1\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54GTL16622			SN74GTL16622			UNIT		
		MIN	TYP†	MAX	MIN	TYP†	MAX			
V_{IK}	$V_{CC} = 3.15\text{ V}$, $I_I = -18\text{ mA}$	-1.2			-1.2			V		
V_{OH}	A port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V	
		$V_{CC} = 3.15\text{ V}$	2.4			2.4				
	$I_{OH} = -12\text{ mA}$ $I_{OH} = -24\text{ mA}$	2			2					
V_{OL}	A port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$	0.2			0.2			V	
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 12\text{ mA}$	0.4			0.4			
			$I_{OL} = 24\text{ mA}$	0.5			0.5			
	B port	$V_{CC} = 3.15\text{ V to } 3.45\text{ V}$, $I_{OL} = 100\text{ }\mu\text{A}$	$I_{OL} = 10\text{ mA}$	0.2			0.2			
			$I_{OL} = 40\text{ mA}$	0.4			0.4			
		$V_{CC} = 3.15\text{ V}$	$I_{OL} = 50\text{ mA}$	0.55			0.55			
I_I	Control inputs	$V_{CC} = 3.45\text{ V}$, $V_I = V_{CC}\text{ or GND}$	± 5			± 5			μA	
	B port	$V_{CC} = 3.45\text{ V}$, $V_I = V_{TT}\text{ or GND}$	± 5			± 5				
I_{off}	A port	$V_{CC} = 0$, $V_I\text{ or } V_O = 0\text{ to } 3.45\text{ V}$	100			100			μA	
$I_I(\text{hold})$	A port	$V_{CC} = 3.15\text{ V}$	$V_I = 0.8\text{ V}$	75			75			μA
			$V_I = 2\text{ V}$	-75			-75			
		$V_{CC} = 3.45\text{ V}^\ddagger$, $V_I = 0.8\text{ V to } 2\text{ V}$	± 500			± 500				
I_{OZH}	B port	$V_{CC} = 3.45\text{ V}$, $V_O = 1.5\text{ V}$	10			10			μA	
I_{OZ}^\S	A port	$V_{CC} = 3.45\text{ V}$, $V_O = V_{CC}\text{ or GND}$	± 10			± 10			μA	
I_{CC}	A or B port	$V_{CC} = 3.45\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$	60			60			mA	
ΔI_{CC}^\parallel	A port or control inputs	$V_{CC} = 3.45\text{ V}$, A port or control inputs at $V_{CC}\text{ or GND}$, One input at $V_{CC} - 0.6\text{ V}$	500			500			μA	
C_i	Control inputs	$V_I = 3.15\text{ V or } 0$	3			3			pF	
C_{io}	A port	$V_O = 3.15\text{ V or } 0$	10			10			pF	
	B port	Per IEEE 1194.1	8.5			8.5				

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ This is the bus-hold maximum dynamic current required to switch the input from one state to another.

§ For I/O ports, the parameter I_{OZ} includes the input leakage current.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL (unless otherwise noted)[†]

		SN54GTL16622		SN74GTL16622		UNIT
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	0	200	0	200	MHz
t _w	Pulse duration, CLK high or low	2.5		2.5		ns
t _{su}	Setup time	Data before CLK↑	3.1	3		ns
		\overline{CE} before CLK↑	2.8	2.7		
t _h	Hold time	Data after CLK↑	0.7	0.6		ns
		\overline{CE} after CLK↑	0.4	0.3		

[†] These parameters are warranted but not production tested.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL (see Figure 1)[†]

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16622			SN74GTL16622			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
f _{max}			200			200			MHz
t _{PLH}	CLKAB	B	2.7		6.5	2.8	4.3	6.1	ns
t _{PHL}			1.9		6.2	2	3.6	5.5	
t _{PLH}	\overline{OEAB}	B	2.5		6.4	2.6	4.2	6	ns
t _{PHL}			1.6		5.8	1.7	3.1	5.1	
Slew rate	Both transitions		0.5			0.5			V/ns
t _r	Transition time, B outputs (0.6 V to 1 V)		0.5		2.6	0.6	1.2	2.5	ns
t _f	Transition time, B outputs (1 V to 0.6 V)		0.3		2.3	0.4	0.8	2	ns
t _{PLH}	CLKBA	A	2.1		5.6	2.2	3.7	5.3	ns
t _{PHL}			2.2		5.6	2.3	3.8	5.2	
t _{en}	\overline{OEBA}	A	1.7		5.4	1.8	3.3	5	ns
t _{dis}			2.2		6.2	2.4	4.1	5.7	

[†] These parameters are warranted but not production tested.

[‡] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature for GTL+ (unless otherwise noted)

		SN54GTL16622		SN74GTL16622		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	0	200	0	200	MHz
t_w	Pulse duration, CLK high or low	2.5		2.5		ns
t_{su}	Setup time	Data before CLK \uparrow	2.8	2.5		ns
		$\overline{\text{CE}}$ before CLK \uparrow	2.7	2.6		
t_h	Hold time	Data after CLK \uparrow	0.6	0.5		ns
		$\overline{\text{CE}}$ after CLK \uparrow	0.2	0.1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature for GTL+ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54GTL16622			SN74GTL16622			UNIT
			MIN	TYP \dagger	MAX	MIN	TYP \dagger	MAX	
f_{max}			200			200			MHz
t_{PLH}	CLKAB	B	2.8		6.6	2.9	4.2	6.1	ns
t_{PHL}			2		6.6	2.1	3.7	5.7	
t_{PLH}	$\overline{\text{OEAB}}$	B	2.6		6.4	2.7	4.1	5.9	ns
t_{PHL}			1.7		6.1	1.8	3.3	5.3	
Slew rate	Both transitions		0.5			0.5			V/ns
t_r	Transition time, B outputs (0.6 V to 1.3 V)		0.9		3.1	1	1.6	3	ns
t_f	Transition time, B outputs (1.3 V to 0.6 V)		0.6		4.3	0.7	1.4	3.3	ns
t_{PLH}	CLKBA	A	2.1		5.6	2.2	3.7	5.3	ns
t_{PHL}			2.2		5.6	2.3	3.8	5.2	
t_{en}	$\overline{\text{OEBA}}$	A	1.6		5.4	1.7	3.2	5	ns
t_{dis}			2.2		6.2	2.4	4.1	5.7	

\dagger All typical values are at $V_{\text{CC}} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$.

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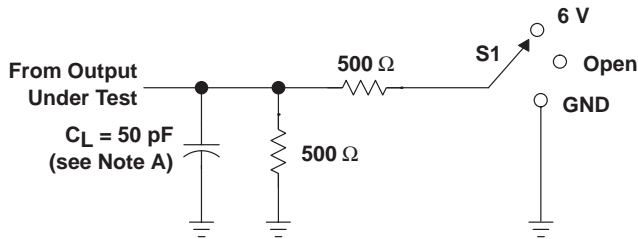


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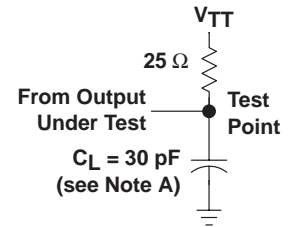
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PARAMETER MEASUREMENT INFORMATION

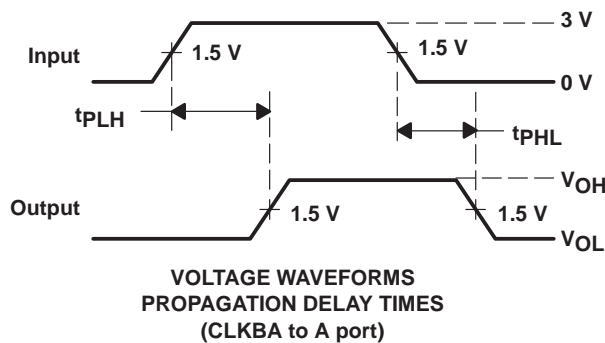
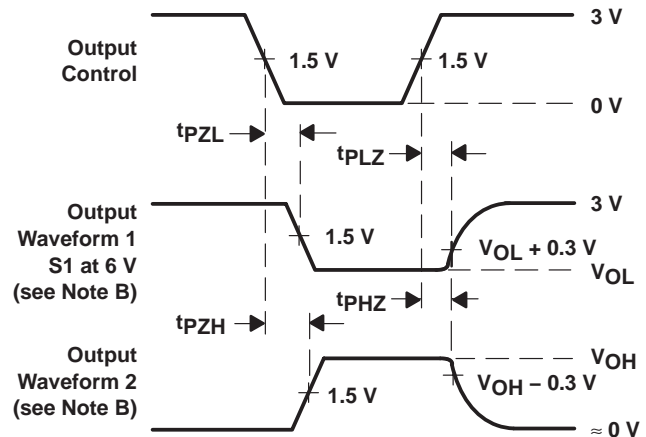
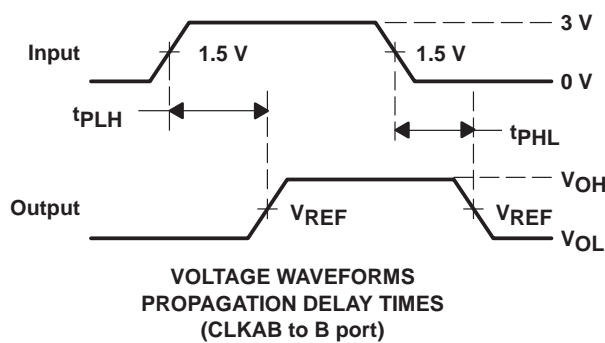
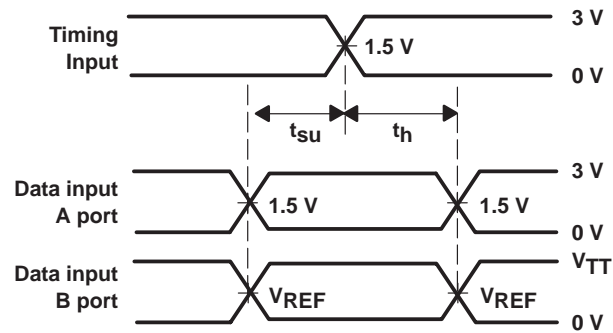
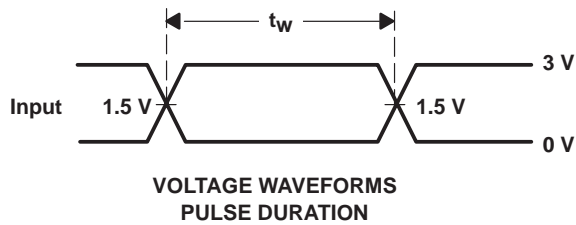


LOAD CIRCUIT FOR A OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



LOAD CIRCUIT FOR B OUTPUTS



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74GTL16622DGGR	OBSOLETE	TSSOP	DGG	64		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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