FAIRCHILD SEMICONDUCTOR®

May 2007

# 74F240, 74F244
# Octal Buffers/Line Drivers with 3-STATE Outputs

## Features

- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 64mA (48mA mil)
- 12mA source current
- Input clamp diodes limit high-speed termination effects

## General Description

The 74F240 and 74F244 are octal buffers and line drivers designed to be employed as memory and address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC and board density.

## Ordering Information

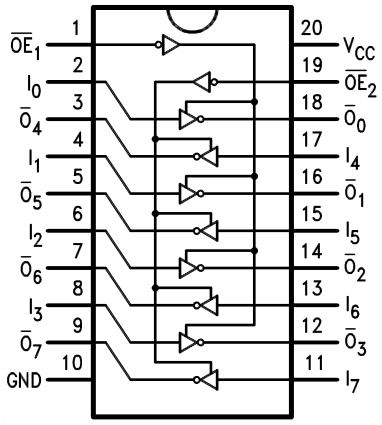
| Order Code | Package Number | Package Description |
|---|---|---|
| 74F240SC(1) | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74F240SJ(1) | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F240PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| 74F244SC(1) | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74F244SJ(1) | M20D | 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F244MSA(1) | MSA20 | 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide |
| 74F244PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

**Note:**

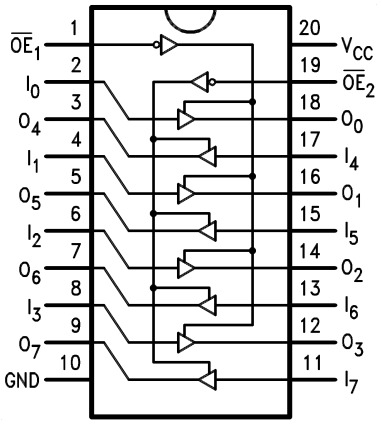
1. Devices also available in Tape and Reel. Specify by appending the suffix letter “X” to the ordering number.

## Connection Diagrams

**74F240**

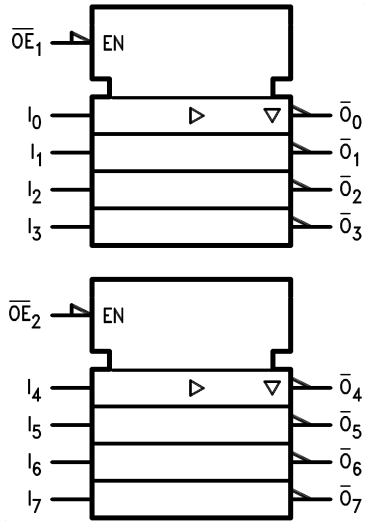



**74F244**

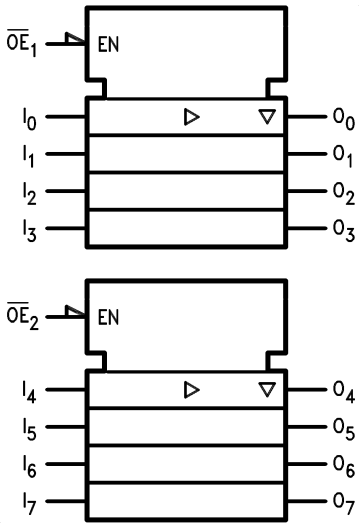


## Logic Symbols

IEEE/IEC
74F240




IEEE/IEC
74F244




## Unit Loading/Fan Out

| Pin Names | Description | U.L. HIGH/LOW | Input $I_{IH}$ / $I_{IL}$, Output $I_{OH}$ / $I_{OL}$ |
|---|---|---|---|
| $\overline{OE}_1$, $\overline{OE}_2$ | 3-STATE Output Enable Input (Active LOW) | 1.0 / 1.667 | 20µA / –1mA |
| $OE_2$ | 3-STATE Output Enable Input (Active HIGH) | 1.0 / 1.667 | 20µA / –1mA |
| $I_0$–$I_7$ | Inputs (74F240) | 1.0 / 1.667(2) | 20µA / –1mA |
| $I_0$–$I_7$ | Inputs (74F244) | 1.0 / 2.667(2) | 20µA / –1.6mA |
| $\overline{O}_0$–$\overline{O}_7$, $O_0$–$O_7$ | Outputs | 600 / 106.6 (80) | –12mA / 64mA (48mA) |

**Note:**

2. Worst-case 74F240 enabled; 74F244 disabled.

## Truth Tables

**74F240**

| $\overline{OE}_1$ | $D_{1n}$ | $O_{1n}$ | $\overline{OE}_2$ | $D_{2n}$ | $O_{2n}$ |
|---|---|---|---|---|---|
| H | X | Z | H | X | Z |
| L | H | L | L | H | L |
| L | L | H | L | L | H |

**74F244**

| $\overline{OE}_1$ | $D_{1n}$ | $O_{1n}$ | $\overline{OE}_2$ | $D_{2n}$ | $O_{2n}$ |
|---|---|---|---|---|---|
| H | X | Z | H | X | Z |
| L | H | H | L | H | H |
| L | L | L | L | L | L |

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Rating |
|---|---|---|
| $T_{STG}$ | Storage Temperature | –65°C to +150°C |
| $T_A$ | Ambient Temperature Under Bias | –55°C to +125°C |
| $T_J$ | Junction Temperature Under Bias | –55°C to +150°C |
| $V_{CC}$ | $V_{CC}$ Pin Potential to Ground Pin | –0.5V to +7.0V |
| $V_{IN}$ | Input Voltage(3) | –0.5V to +7.0V |
| $I_{IN}$ | Input Current(3) | –30mA to +5.0mA |
| $V_O$ | Voltage Applied to Output in HIGH State (with $V_{CC}$ = 0V)<br>Standard Output<br>3-STATE Output | <br>–0.5V to $V_{CC}$<br>–0.5V to 5.5V |
| | Current Applied to Output in LOW State (Max.) | twice the rated $I_{OL}$ (mA) |
| | ESD Last Passing Voltage (Min.) | 4000V |

**Note:**

3. Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

| Symbol | Parameter | Rating |
|---|---|---|
| $T_A$ | Free Air Ambient Temperature | 0°C to +70°C |
| $V_{CC}$ | Supply Voltage | +4.5V to +5.5V |

## DC Electrical Characteristics

| Symbol | Parameter | | $V_{CC}$ | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | | Recognized as a HIGH Signal | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | Recognized as a LOW Signal | | | 0.8 | V |
| $V_{CD}$ | Input Clamp Diode Voltage | | Min. | $I_{IN}$ = –18mA | | | –1.2 | V |
| $V_{OH}$ | Output HIGH Voltage | 10% $V_{CC}$ | Min. | $I_{OH}$ = –3mA | 2.4 | | | V |
| | | 10% $V_{CC}$ | | $I_{OH}$ = –15mA | 2.0 | | | |
| | | 5% $V_{CC}$ | | $I_{OH}$ = –3mA | 2.7 | | | |
| $V_{OL}$ | Output LOW Voltage | 10% $V_{CC}$ | Min. | $I_{OL}$ = 64mA | | | 0.55 | V |
| $I_{IH}$ | Input HIGH Current | | Max. | $V_{IN}$ = 2.7V | | | 5.0 | µA |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | Max. | $V_{IN}$ = 7.0V | | | 7.0 | µA |
| $I_{CEX}$ | Output HIGH Leakage Current | | Max. | $V_{OUT}$ = $V_{CC}$ | | | 50 | µA |
| $V_{ID}$ | Input Leakage Test | | 0.0 | $I_{ID}$ = 1.9µA | 4.75 | | | V |
| | | | | All Other Pins Grounded | | | | |
| $I_{OD}$ | Output Leakage Circuit Current | | 0.0 | $V_{IOD}$ = 150mV | | | 3.75 | µA |
| | | | | All Other Pins Grounded | | | | |
| $I_{IL}$ | Input LOW Current | | Max. | $V_{IN}$ = 0.5V ($\overline{OE}_1$, $\overline{OE}_2$, $OE_2$, $D_n$ (74F240)) | | | –1.0 | mA |
| | | | | $V_{IN}$ = 0.5V ($D_n$ (74F244)) | | | –1.6 | |
| $I_{OZH}$ | Output Leakage Current | | Max. | $V_{OUT}$ = 2.7V | | | 50 | µA |
| $I_{OZL}$ | Output Leakage Current | | Max. | $V_{OUT}$ = 0.5V | | | –50 | µA |
| $I_{OS}$ | Output Short-Circuit Current | | Max. | $V_{OUT}$ = 0V | –100 | | –225 | mA |
| $I_{ZZ}$ | Bus Drainage Test | | 0.0V | $V_{OUT}$ = 5.25V | | | 500 | µA |
| $I_{CCH}$ | Power Supply Current (74F240) | | Max. | $V_O$ = HIGH | | 19 | 29 | mA |
| $I_{CCL}$ | Power Supply Current (74F240) | | Max. | $V_O$ = LOW | | 50 | 75 | mA |
| $I_{CCZ}$ | Power Supply Current (74F240) | | Max. | $V_O$ = HIGH Z | | 42 | 63 | mA |
| $I_{CCH}$ | Power Supply Current (74F244) | | Max. | $V_O$ = HIGH | | 40 | 60 | mA |
| $I_{CCL}$ | Power Supply Current (74F244) | | Max. | $V_O$ = LOW | | 60 | 90 | mA |
| $I_{CCZ}$ | Power Supply Current (74F244) | | Max. | $V_O$ = HIGH Z | | 60 | 90 | mA |

## AC Electrical Characteristics

| Symbol | Parameter | $T_A$ = +25°C, $V_{CC}$ = +5.0V, $C_L$ = 50pF | | | $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V, $C_L$ = 50pF | | $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V, $C_L$ = 50pF | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay Data to Output (74F240) | 3.0 | 5.1 | 7.0 | 3.0 | 9.0 | 3.0 | 8.0 | ns |
| | | 2.0 | 3.5 | 4.7 | 2.0 | 6.0 | 2.0 | 5.7 | |
| $t_{PZH}$, $t_{PZL}$ | Output Enable Time (74F240) | 2.0 | 3.5 | 4.7 | 2.0 | 6.5 | 2.0 | 5.7 | ns |
| | | 4.0 | 6.9 | 9.0 | 4.0 | 10.5 | 4.0 | 10.0 | |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time (74F240) | 2.0 | 4.0 | 5.3 | 2.0 | 6.5 | 2.0 | 6.3 | |
| | | 2.0 | 6.0 | 8.0 | 2.0 | 12.5 | 2.0 | 9.5 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation Delay, Data to Output (74F244) | 2.5 | 4.0 | 5.2 | 2.0 | 6.5 | 2.5 | 6.2 | ns |
| | | 2.5 | 4.0 | 5.2 | 2.0 | 7.0 | 2.5 | 6.5 | |
| $t_{PZH}$, $t_{PZL}$ | Output Enable Time (74F244) | 2.0 | 4.3 | 5.7 | 2.0 | 7.0 | 2.0 | 6.7 | ns |
| | | 2.0 | 5.4 | 7.0 | 2.0 | 8.5 | 2.0 | 8.0 | |
| $t_{PHZ}$, $t_{PLZ}$ | Output Disable Time (74F244) | 2.0 | 4.5 | 6.0 | 2.0 | 7.0 | 2.0 | 7.0 | |
| | | 2.0 | 4.5 | 6.0 | 2.0 | 7.5 | 2.0 | 7.0 | |

## Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

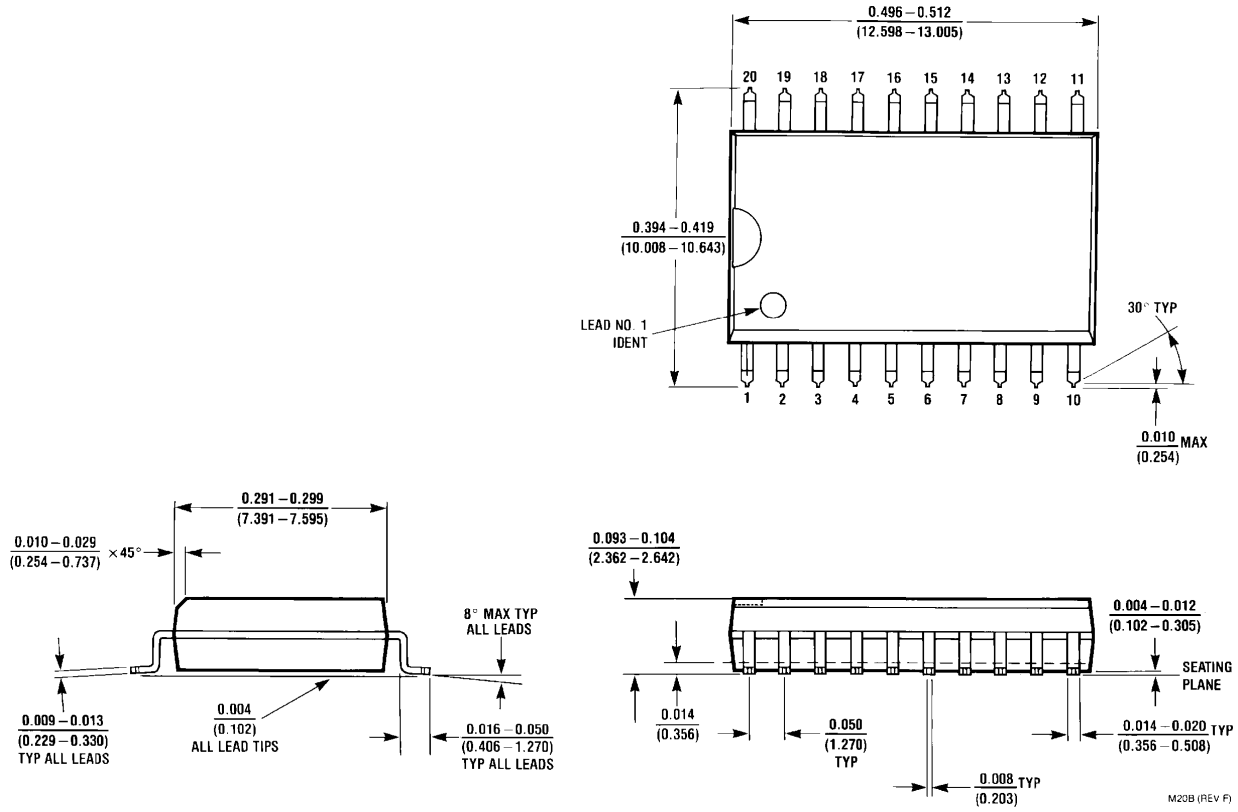
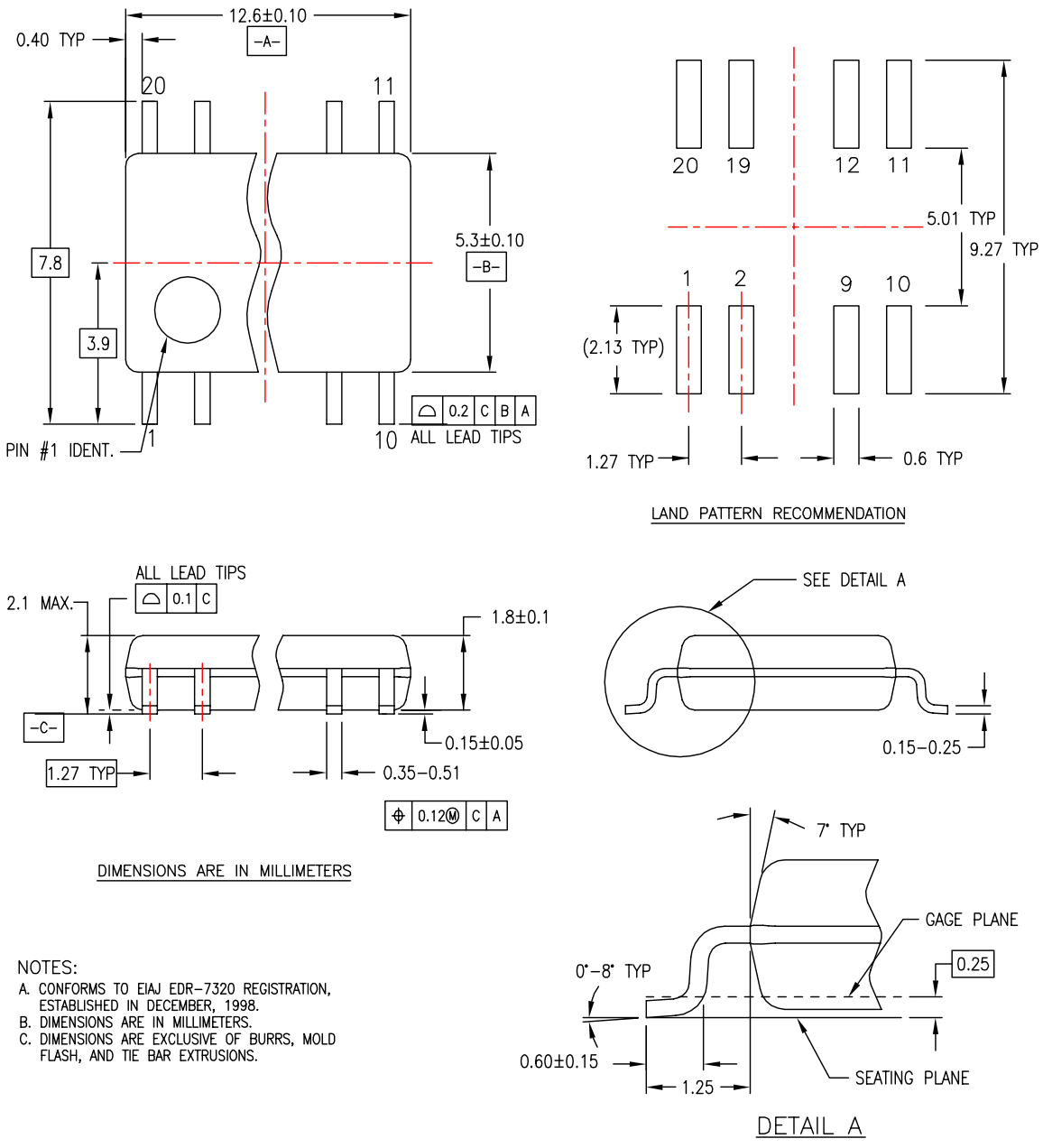



**Figure 1. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide**
**Package Number M20B**

## Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.




NOTES:

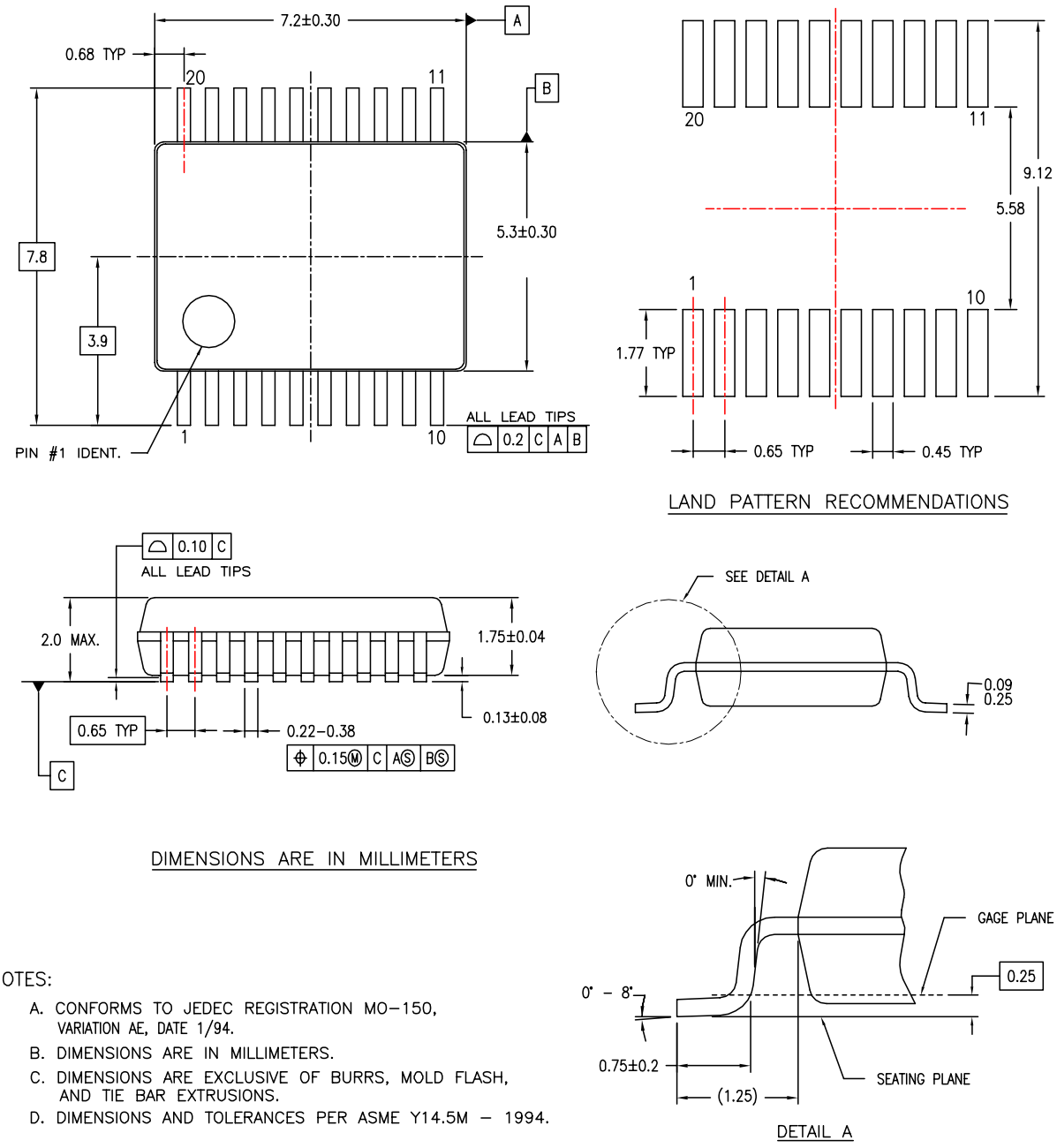
A. CONFORMS TO EIAJ EDR–7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

**Figure 2. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide**
**Package Number M20D**

## Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.




NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO–150, VARIATION AE, DATE 1/94.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M – 1994.

MSA20REVB

**Figure 3. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide**
**Package Number MSA20**

## Physical Dimensions (Continued)

Dimensions are in inches (millimeters) unless otherwise noted.

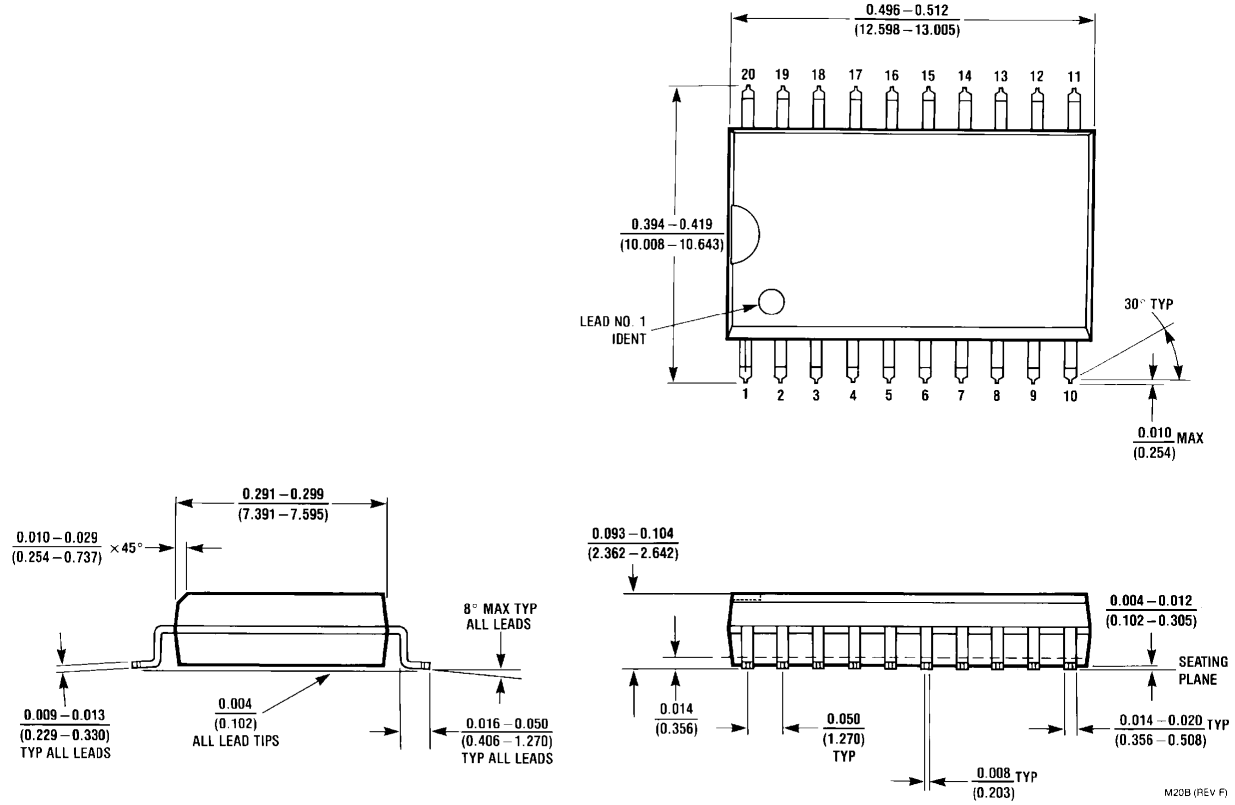



**Figure 4. 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide**
**Package Number N20A**

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