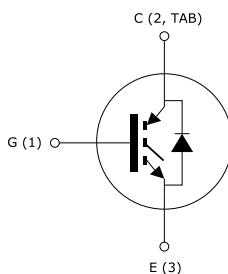


Trench gate field-stop 650 V, 40 A high speed HB series IGBT



TO-247 long leads



Features

- Maximum junction temperature: $T_J = 175\text{ }^\circ\text{C}$
- High speed switching series
- Minimized tail current
- Low saturation voltage: $V_{CE(sat)} = 1.6\text{ V (typ.) @ } I_C = 40\text{ A}$
- Tight parameter distribution
- Safe paralleling
- Positive $V_{CE(sat)}$ temperature coefficient
- Low thermal resistance
- Very fast soft recovery antiparallel diode

Applications

- Photovoltaic inverters
- High frequency converters

Description

This device is an IGBT developed using an advanced proprietary trench gate field-stop structure. The device is part of the new HB series of IGBTs, which represents an optimum compromise between conduction and switching loss to maximize the efficiency of any frequency converter. Furthermore, the slightly positive $V_{CE(sat)}$ temperature coefficient and very tight parameter distribution result in safer paralleling operation.

Product status link

[STGWA40H65DFB](#)

Product summary

Order code	STGWA40H65DFB
Marking	G40H65DFB
Package	TO-247 long leads
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0$ V)	650	V
I_C	Continuous collector current at $T_C = 25$ °C	80	A
	Continuous collector current at $T_C = 100$ °C	40	
$I_{CP}^{(1)}$	Pulsed collector current	160	A
V_{GE}	Gate-emitter voltage	± 20	V
	Transient gate-emitter voltage	± 30	
I_F	Continuous forward current at $T_C = 25$ °C	80	A
	Continuous forward current at $T_C = 100$ °C	40	
$I_{FP}^{(1)}$	Pulsed forward current	160	A
P_{TOT}	Total power dissipation at $T_C = 25$ °C	283	W
T_{STG}	Storage temperature range	- 55 to 150	°C
T_J	Operating junction temperature range	- 55 to 175	

1. Pulse width limited by maximum junction temperature.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case IGBT	0.53	°C/W
R_{thJC}	Thermal resistance junction-case diode	1.14	
R_{thJA}	Thermal resistance junction-ambient	50	

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 3. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	$V_{GE} = 0\text{ V}, I_C = 2\text{ mA}$	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}, I_C = 40\text{ A}$		1.6	2	V
		$V_{GE} = 15\text{ V}, I_C = 40\text{ A}, T_J = 125\text{ °C}$		1.7		
		$V_{GE} = 15\text{ V}, I_C = 40\text{ A}, T_J = 175\text{ °C}$		1.8		
V_F	Forward on-voltage	$I_F = 40\text{ A}$		1.7	2.45	V
		$I_F = 40\text{ A}, T_J = 125\text{ °C}$		1.4		
		$I_F = 40\text{ A}, T_J = 175\text{ °C}$		1.3		
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}, I_C = 1\text{ mA}$	5	6	7	V
I_{CES}	Collector cut-off current	$V_{GE} = 0\text{ V}, V_{CE} = 650\text{ V}$			25	μA
I_{GES}	Gate-emitter leakage current	$V_{CE} = 0\text{ V}, V_{GE} = \pm 20\text{ V}$			± 250	nA

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{ V}, f = 1\text{ MHz}, V_{GE} = 0\text{ V}$	-	5412	-	pF
C_{oes}	Output capacitance		-	198	-	
C_{res}	Reverse transfer capacitance		-	107	-	
Q_g	Total gate charge	$V_{CC} = 520\text{ V}, I_C = 40\text{ A}, V_{GE} = 0\text{ to }15\text{ V}$ (see Figure 28. Gate charge test circuit)	-	210	-	nC
Q_{ge}	Gate-emitter charge		-	39	-	
Q_{gc}	Gate-collector charge		-	82	-	

Table 5. IGBT switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{CE} = 400\text{ V}$, $I_C = 40\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 5\ \Omega$ (see Figure 27. Test circuit for inductive load switching)		40	-	ns	
t_r	Current rise time			13	-		
$(di/dt)_{on}$	Turn-on current slope				2413	-	A/ μ s
$t_{d(off)}$	Turn-off-delay time				142	-	ns
t_f	Current fall time				27	-	
$E_{on}^{(1)}$	Turn-on switching energy				498	-	μ J
$E_{off}^{(2)}$	Turn-off switching energy				363	-	
E_{ts}	Total switching energy			861	-		
$t_{d(on)}$	Turn-on delay time	$V_{CE} = 400\text{ V}$, $I_C = 40\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 5\ \Omega$, $T_J = 175\text{ }^\circ\text{C}$ (see Figure 27. Test circuit for inductive load switching)		38	-	ns	
t_r	Current rise time				14		-
$(di/dt)_{on}$	Turn-on current slope				2186	-	A/ μ s
$t_{d(off)}$	Turn-off-delay time				141	-	ns
t_f	Current fall time				61	-	
$E_{on}^{(1)}$	Turn-on switching energy				1417	-	μ J
$E_{off}^{(2)}$	Turn-off switching energy				764	-	
E_{ts}	Total switching energy			2181	-		

1. Including the reverse recovery of the diode.
2. Including the tail of the collector current.

Table 6. Diode switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
t_{rr}	Reverse recovery time	$I_F = 40\text{ A}$, $V_R = 400\text{ V}$, $V_{GE} = 15\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ (see Figure 27. Test circuit for inductive load switching)	-	62	-	ns	
Q_{rr}	Reverse recovery charge			-	99	-	nC
I_{rrm}	Reverse recovery current			-	3.3	-	A
dI_{rr}/dt	Peak rate of fall of reverse recovery current during t_b			-	187	-	A/ μ s
E_{rr}	Reverse recovery energy			-	68	-	μ J
t_{rr}	Reverse recovery time	$I_F = 40\text{ A}$, $V_R = 400\text{ V}$, $V_{GE} = 15\text{ V}$, $T_J = 175\text{ }^\circ\text{C}$ di/ $dt = 100\text{ A}/\mu\text{s}$ (see Figure 27. Test circuit for inductive load switching)	-	310	-	ns	
Q_{rr}	Reverse recovery charge			-	1550	-	nC
I_{rrm}	Reverse recovery current			-	10	-	A
dI_{rr}/dt	Peak rate of fall of reverse recovery current during t_b			-	70	-	A/ μ s
E_{rr}	Reverse recovery energy			-	674	-	μ J

2.1 Electrical characteristics (curves)

Figure 1. Power dissipation vs case temperature

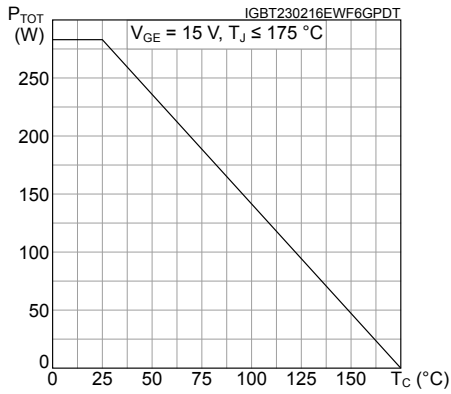


Figure 2. Collector current vs case temperature

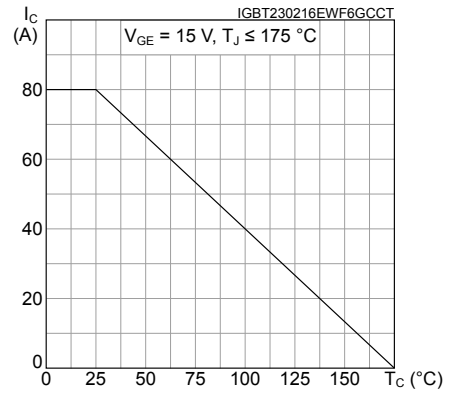


Figure 3. Output characteristics ($T_J = 25\text{ }^\circ\text{C}$)

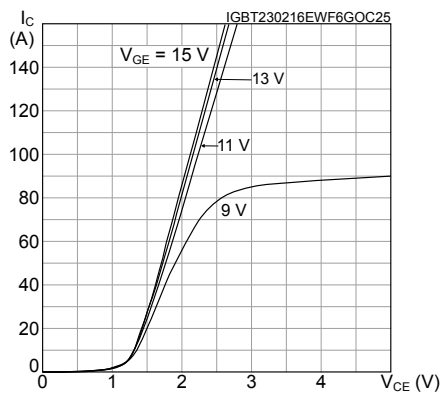


Figure 4. Output characteristics ($T_J = 175\text{ }^\circ\text{C}$)

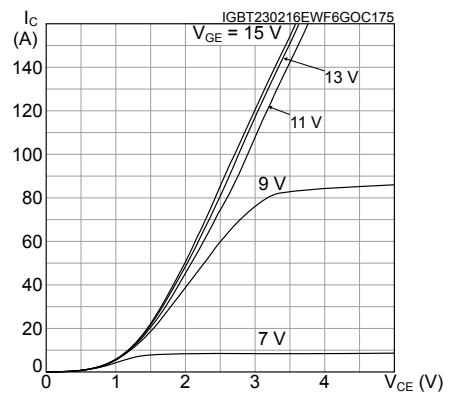


Figure 5. $V_{CE(sat)}$ vs junction temperature

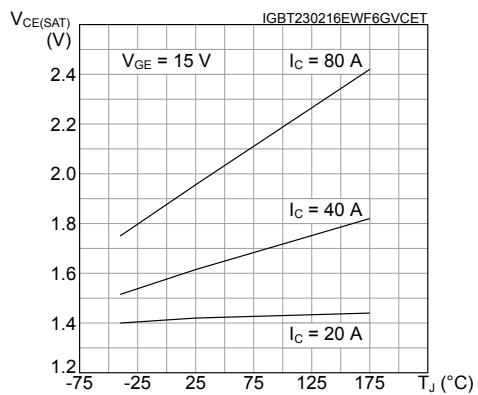


Figure 6. $V_{CE(sat)}$ vs collector current

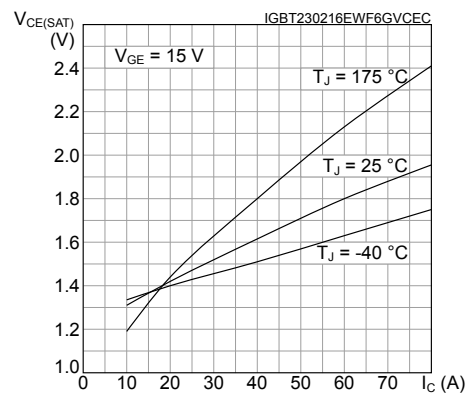


Figure 7. Collector current vs switching frequency

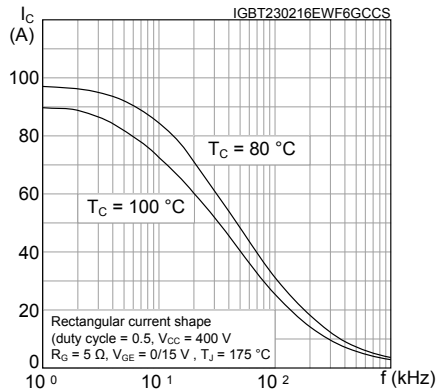


Figure 8. Forward bias safe operating area

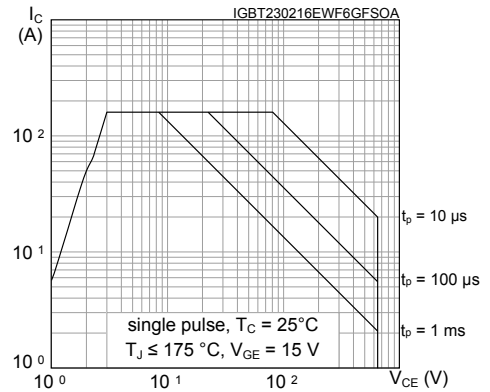


Figure 9. Transfer characteristics

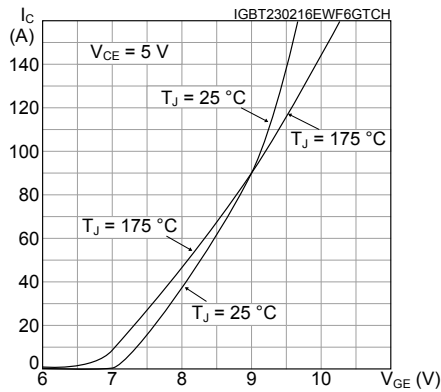


Figure 10. Diode Vf vs forward current

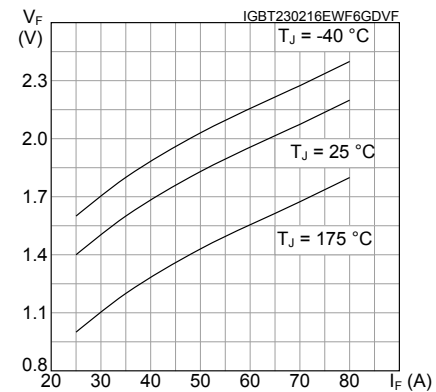


Figure 11. Normalized VGE(th) vs junction temperature

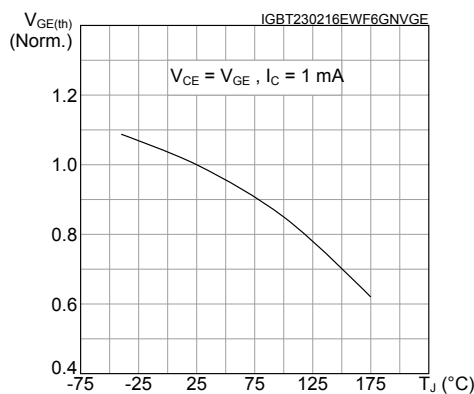


Figure 12. Normalized V(BR)CES vs junction temperature

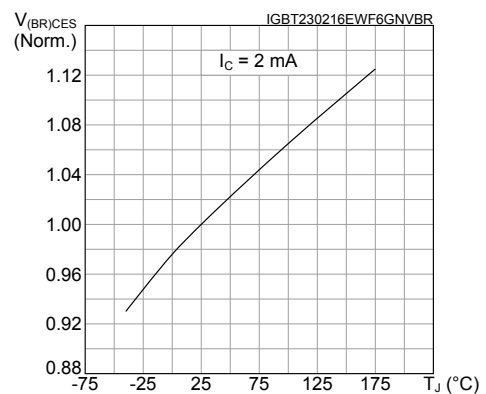


Figure 13. Capacitance variations

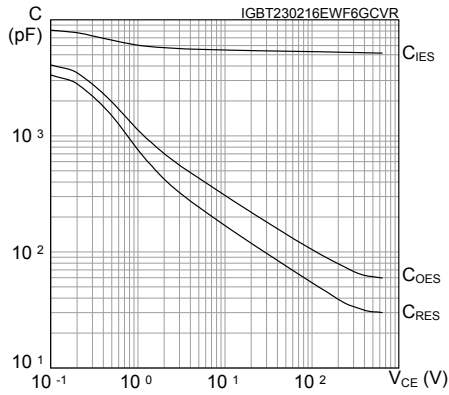


Figure 14. Gate charge vs gate-emitter voltage

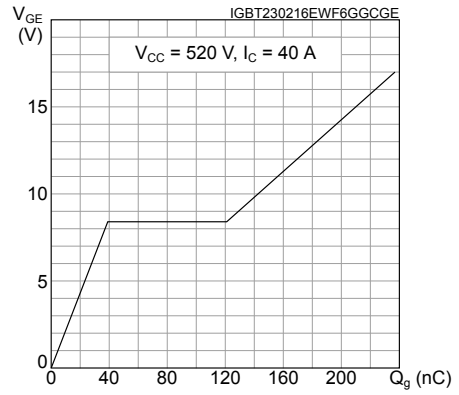


Figure 15. Switching energy vs collector current

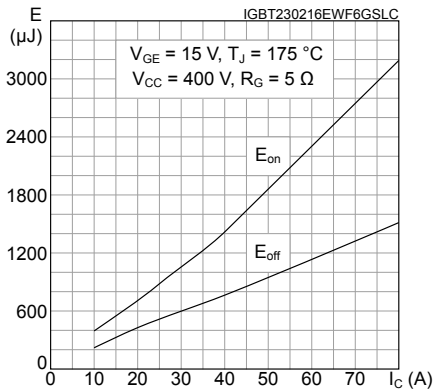


Figure 16. Switching energy vs gate resistance

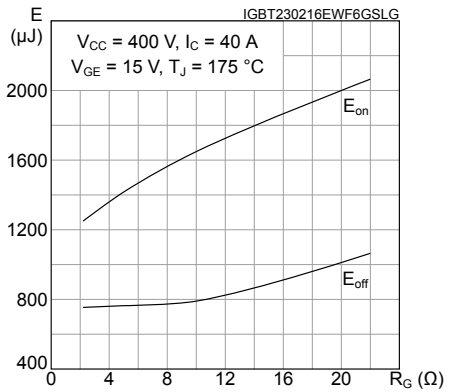


Figure 17. Switching energy vs temperature

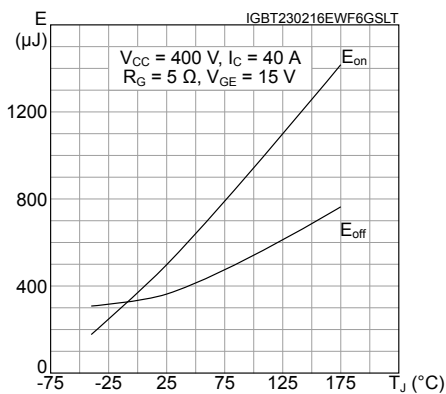


Figure 18. Switching energy vs collector emitter voltage

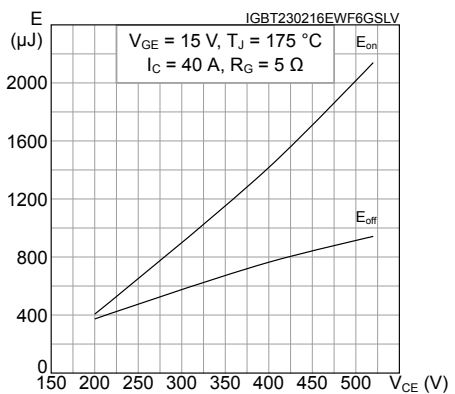


Figure 19. Switching times vs collector current

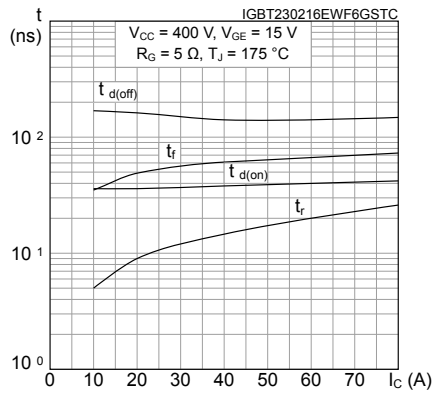


Figure 20. Switching times vs gate resistance

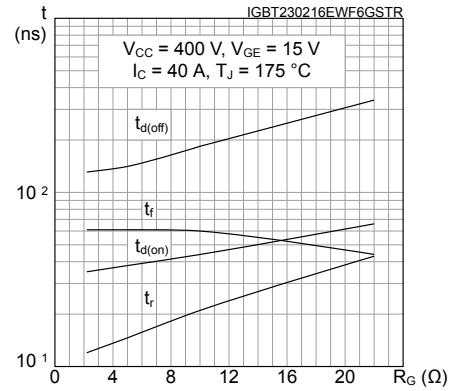


Figure 21. Reverse recovery current vs diode current slope

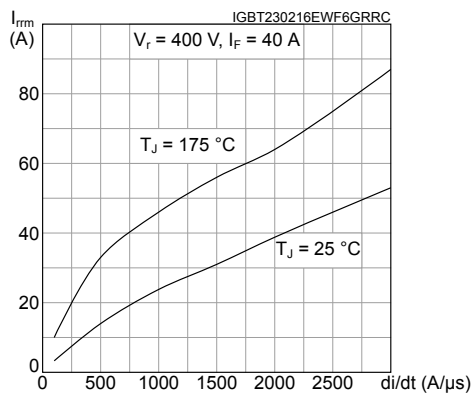


Figure 22. Reverse recovery time vs diode current slope

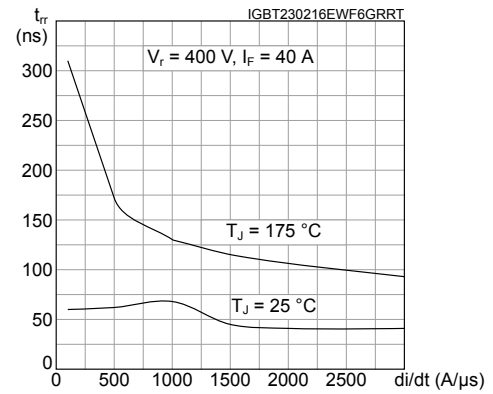


Figure 23. Reverse recovery charge vs diode current slope

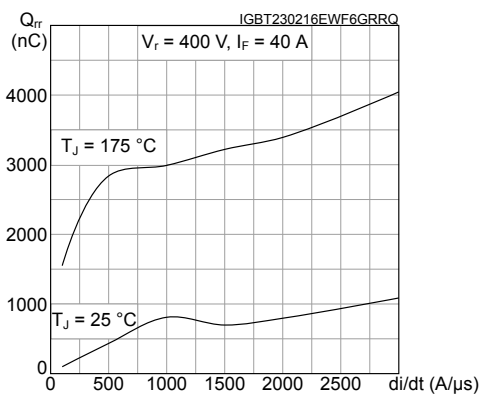


Figure 24. Reverse recovery energy vs diode current slope

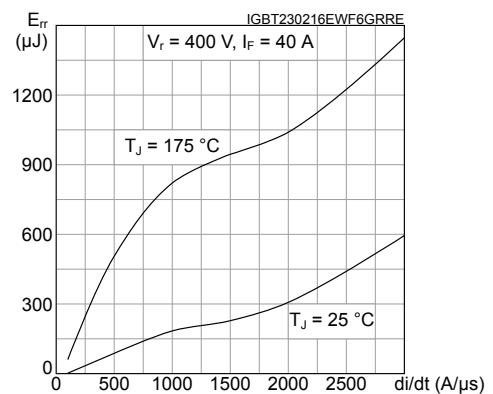


Figure 25. Thermal impedance for IGBT

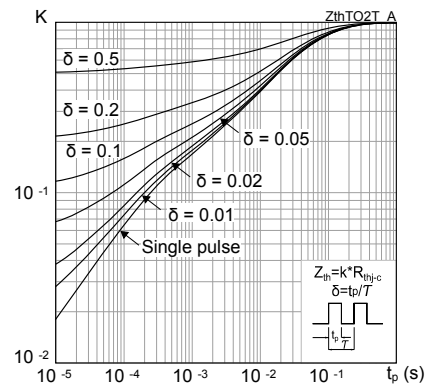
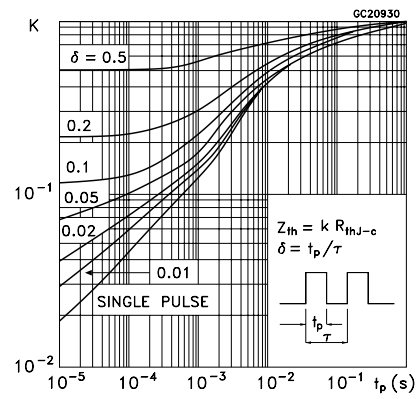
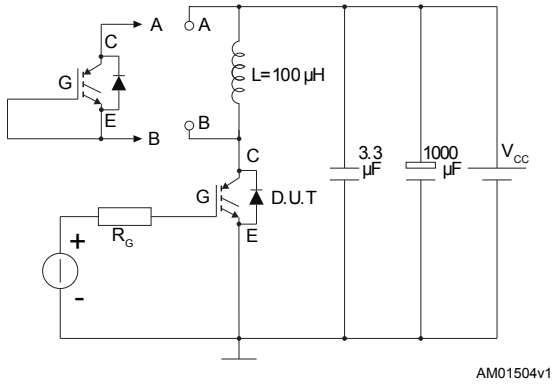
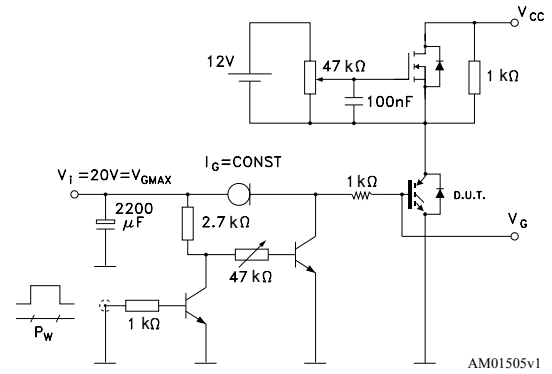
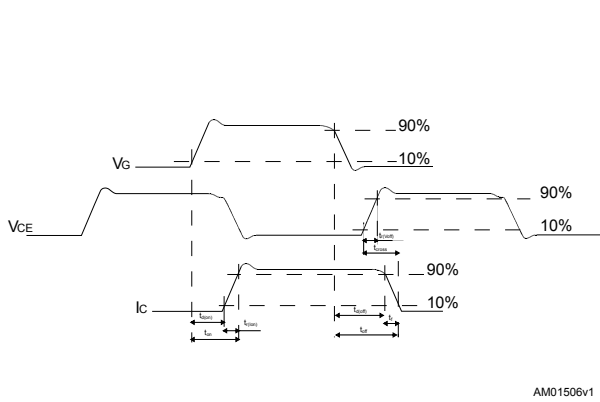
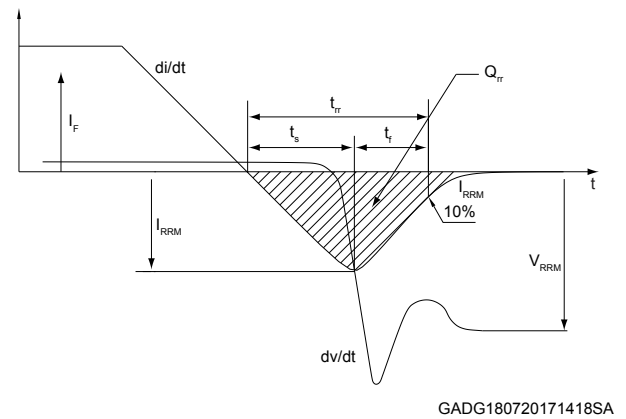


Figure 26. Thermal impedance for diode



3 Test circuits

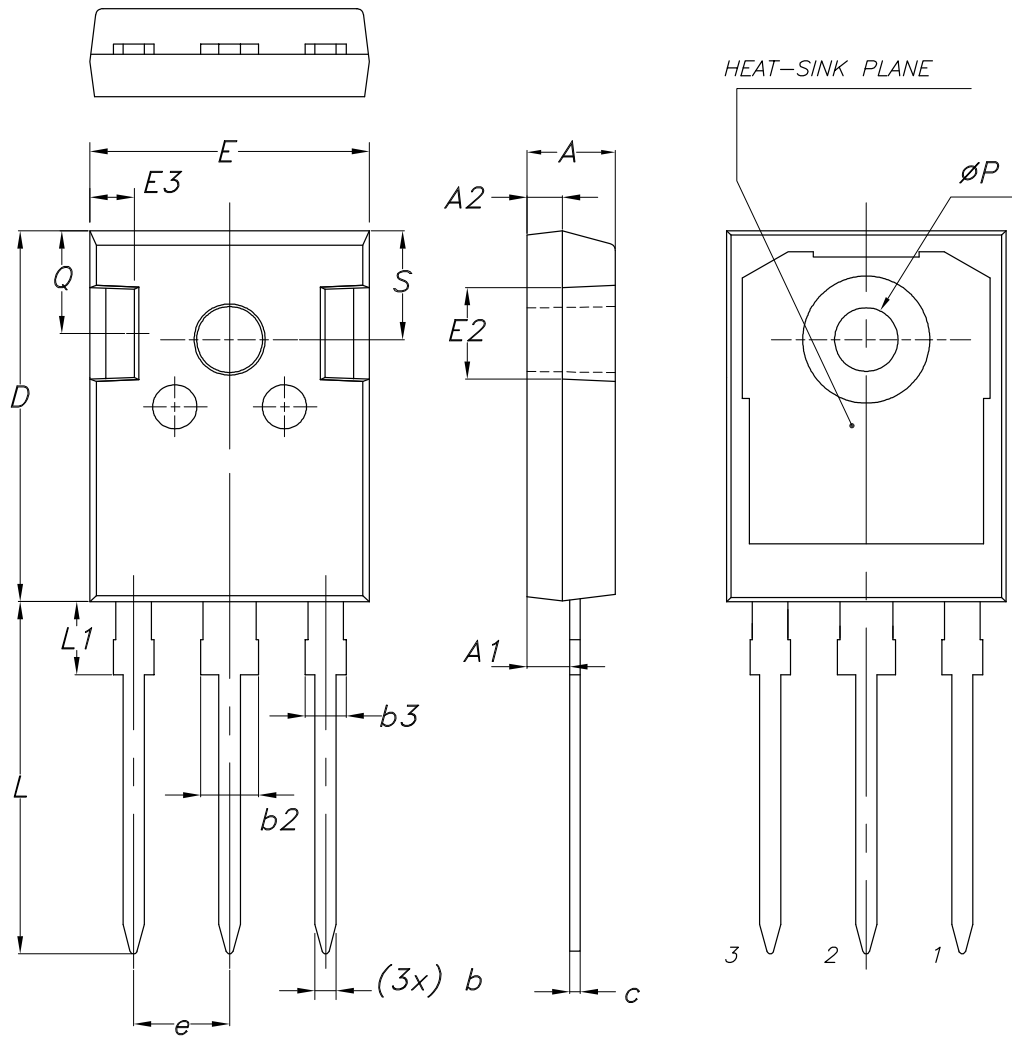
Figure 27. Test circuit for inductive load switching

Figure 28. Gate charge test circuit

Figure 29. Switching waveform

Figure 30. Diode reverse recovery waveform


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 long leads package information

Figure 31. TO-247 long leads package outline



8463846_2_F

Table 7. TO-247 long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

Revision history

Table 8. Document revision history

Date	Revision	Changes
06-Jun-2016	1	Initial version. Part number previously included in datasheet DocID024363.
24-Jun-2019	2	Modified Table 1. Absolute maximum ratings . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	4
3	Test circuits	10
4	Package information	11
4.1	TO-247 long leads package information	11
	Revision history	14

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