DATA SHEET

SKY12343-364LF: 0.01 to 4.0 GHz Seven-Bit Digital Attenuator with Serial and Parallel Drivers

Applications

- Cellular and 3G infrastructure
- WiMAX, LTE, 4G infrastructure

Features

- Broadband operation: 0.01 to 4.0 GHz
- Attenuation range: 31.75 dB with 0.25 dB LSB
- TTL/CMOS-compatible serial, parallel, or latched parallel control interface
- Single supply voltage: +3.3 or +5 V
- Small QFN (32-pin, 5 x 5 mm) Pb-free package (MSL1, 260 °C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

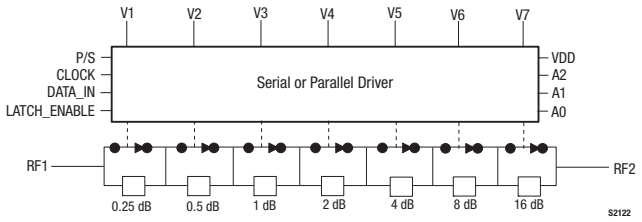


Figure 1. SKY12343-364LF Block Diagram

Description

The SKY12343-364LF is a GaAs broadband seven-bit pHEMT digital attenuator with a 0.25 dB least significant bit (LSB). The programming logic levels are TTL/CMOS-compatible with both a dual mode serial controller and an integrated Serial Peripheral Interface (SPI) controller.

The SKY12343-364LF attenuator features low insertion loss, excellent attenuation accuracy, a 31.75 dB attenuation range, and high-linearity performance. The device is an ideal choice for a wide variety of 3G and 4G cellular infrastructure applications.

A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

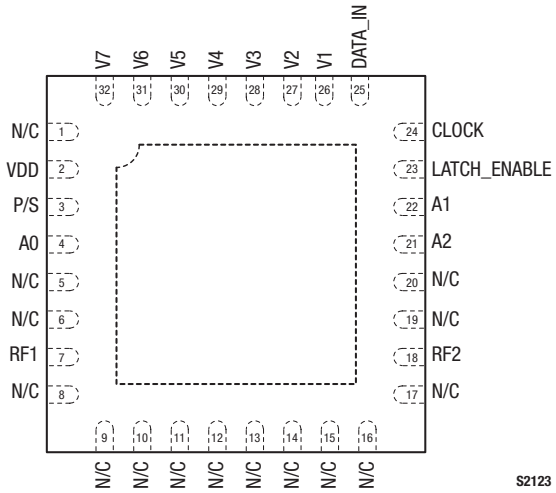


Figure 2. SKY12343-364LF Pinout (Top View)

Table 1. SKY12343-364LF Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	N/C	No connection[1]	17	N/C	No connection[1]
2	VDD	DC power supply	18	RF2	RF input/output to digital attenuator
3	P/S	Serial or parallel operation select. Logic low enables parallel mode.	19	N/C	No connection[1]
4	A0	Address bit A0	20	N/C	No connection[1]
5	N/C	No connection[1]	21	A2	Address bit A2
6	N/C	No connection (Note 1)	22	A1	Address bit A1
7	RF1	RF input/output to digital attenuator	23	LATCH_ENABLE	On rising edge of pulse, shifts the most recent clocked-in data and address bits to set the attenuation state. In parallel mode, if this signal is logic high, changes to the V1 through V7 signals occur directly. If this signal is logic low, the attenuator does not change states until this signal is raised.
8	N/C	No connection[1]	24	CLOCK	Clock input
9	N/C	No connection[1]	25	DATA_IN	Serial data input
10	N/C	No connection[1]	26	V1	Parallel attenuation control input
11	N/C	No connection[1]	27	V2	Parallel attenuation control input
12	N/C	No connection[1]	28	V3	Parallel attenuation control input
13	N/C	No connection[1]	29	V4	Parallel attenuation control input
14	N/C	No connection[1]	30	V5	Parallel attenuation control input
15	N/C	No connection[1]	31	V6	Parallel attenuation control input
16	N/C	No connection[1]	32	V7	Parallel attenuation control input

[1] May be connected to ground with no change in performance.

Functional Description

The SKY12343-364LF is a seven-bit digital attenuator comprised of a GaAs attenuator and a silicon CMOS driver. The attenuation setting is controlled by a serial or parallel interface.

Pin 3 (P/S) selects the input mode of the attenuator. A logic low signal applied to pin 3 enables parallel mode; a logic high enables serial mode. Control logic levels are defined in Table 2.

Serial Data Programming

Parallel Mode Interface

In parallel mode, the desired attenuation state is selected using the seven CMOS-compatible control lines, V1 through V7 (pins 26 through 32). The logic for these pins is presented in Table 3. A logic level low on these pins places the device in the minimum insertion loss state while a logic high places the part in the maximum 31.75 dB insertion loss state. Intermediate levels of attenuation are the total attenuation represented by the major bits selected with logic high.

When the LATCH_ENABLE signal (pin 23) is held high, direct parallel programming through pins 26 through 32 is possible, which is useful for manual control of the device attenuation states.

For latched parallel programming, the LATCH_ENABLE signal should be held low while the inputs to pins 26 through 32 are applied for the desired attenuation state. When the LATCH_ENABLE signal is pulsed high to low, the desired attenuation state is latched.

Serial Mode Interface

In serial mode, the SKY12343-364LF is programmed using an 8-bit attenuation word and an 8-bit address word as shown in Figure 3. The attenuation word controls the attenuation state of the device as shown in Table 4. As with parallel mode programming, intermediate levels of attenuation are the total attenuation represented by the major bits selected with logic high.

For systems that use multiple SKY12343-364LF devices on a single programming bus, up to eight devices can be individually addressed using the address word and the device address signals A0, A1, and A2 (pins 4, 22, and 21, respectively). A device responds to a change in an attenuation setting when its address matches the address defined by the address word. The address word logic is shown in Table 5.

Note that the logic levels of bits A3 to A7 of the address word are “don’t care” bits as shown in Figure 3.

Serial input data (DATA_IN pin) is shifted into the register on the rising edge of the CLOCK signal (pin 24), Least Significant Bit (LSB) first. The attenuator changes states on the rising edge of the LATCH_ENABLE signal (pin 23) according to the most recent seven bits of shifted data accepted since the previous falling edge of the LATCH_ENABLE signal. The shift register must be loaded with LATCH_ENABLE held at logic low to prevent the attenuator from changing attenuation states as data is entered. Once the attenuation data is loaded, the LATCH_ENABLE input should be toggled high and then low to set the new attenuation state.

Refer to the timing diagram in Figure 4 and timing parameters in Table 6.

Power Up and Initialization

Power Up. Voltage in the allowable range from 3.3 to 5.0 V is applied to the VDD signal (pin 2). At power up, LATCH_ENABLE should be logic low. Immediately after power up, wait approximately 400 µs before setting LATCH_ENABLE logic high to allow for internal device voltages to settle. During this period, the device defaults to the maximum insertion loss state of 31.75 dB.

Direct Parallel Mode (P/S pin set to logic low and LATCH_ENABLE pin set to logic high). The SKY12343_364LF should always be powered up with the LATCH_ENABLE signal at logic low. Therefore, powering up in direct parallel mode is not recommended.

The device attenuation state can be preset to any value with the appropriate logic levels on pins 26 to 32 before power up. Immediately after power up and the associated 400 µs delay, LATCH_ENABLE can be toggled to logic high. The device attenuation state changes to the attenuation level that corresponds to the logic levels on pins 26 to 32. If these attenuation logic levels are allowed to float, the device powers up in the minimum insertion loss state when LATCH_ENABLE is set to logic high.

Latched Parallel Mode (P/S pin and LATCH_ENABLE pin set to logic low). The device attenuation state can be preset to any value with the appropriate logic levels on pins 26 to 32 before power up. Immediately after power up and the associated 400 µs delay, the device attenuation changes to the attenuation level that corresponds to the logic levels on pins 26 to 32 on the rising edge of the first LATCH_ENABLE signal.

As noted above, the device attenuation state defaults to the minimum insertion loss if pins 26 to 32 are allowed to float. In latched parallel mode, the attenuation setting on pins 26 to 32 can be latched into the internal register at the falling edge of the LATCH_ENABLE signal.

Serial Addressable Mode (P/S pin set to logic high and LATCH_ENABLE pin set to logic low). For power up in this mode, the parallel control input pins 26 to 32 must be set to logic low. The device powers up in the maximum insertion loss state and remains in that condition until the next programming word is latched after the initial 400 µs delay.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY12343-364LF are provided in Table 7. Electrical specifications are provided in Table 8.

Typical performance characteristics of the SKY12343-364LF are illustrated in Figures 5 through 18.

Table 2. SKY12343-364LF Control Logic Levels

Parameter	Symbol	Test Condition	Min	Max	Units
Logic high	High	Vcc = 3.3 V Vcc = 5.0 V	3.0 3.0	3.3 5.0	V V
Logic low	Low	Vcc = 3.3 V Vcc = 5.0 V	0 0	1.3 1.9	V V

Table 3. SKY12343-364LF Parallel Mode Truth Table (Enabled by Logic Low on Pin 3)

V7 (Pin 32)	V6 (Pin 31)	V5 (Pin 30)	V4 (Pin 29)	V3 (Pin 28)	V2 (Pin 27)	V1 (Pin 26)	Attenuation Setting (RF1 <-> RF2)
Low	Low	Low	Low	Low	Low	Low	Insertion loss
High	Low	Low	Low	Low	Low	Low	0.25 dB
Low	High	Low	Low	Low	Low	Low	0.50 dB
Low	Low	High	Low	Low	Low	Low	1.00 dB
Low	Low	Low	High	Low	Low	Low	2.00 dB
Low	Low	Low	Low	High	Low	Low	4.00 dB
Low	Low	Low	Low	Low	High	Low	8.00 dB
Low	Low	Low	Low	Low	Low	High	16.00 dB
High	High	High	High	High	High	High	31.75 dB
Low	High	Low	High	High	High	Low	14.50 dB (example)

Table 4. SKY12343-364LF Serial Mode Attenuation Word Truth Table (Enabled by Logic High on Pin 3)

Bit D7 (MSB)	Bit D6	Bit D5	Bit D4	Bit D3	Bit D2	Bit D1	Bit D0 (LSB)	Attenuation Word Setting (RF1 <-> RF2)
Low	Low	Low	Low	Low	Low	Low	Low	Insertion loss
Low	Low	Low	Low	Low	Low	Low	High	0.25 dB
Low	Low	Low	Low	Low	Low	High	Low	0.50 dB
Low	Low	Low	Low	Low	High	Low	Low	1.00 dB
Low	Low	Low	Low	High	Low	Low	Low	2.00 dB
Low	Low	Low	High	Low	Low	Low	Low	4.00 dB
Low	Low	High	Low	Low	Low	Low	Low	8.00 dB
Low	High	Low	Low	Low	Low	Low	Low	16.00 dB
Low	High	High	High	High	High	High	High	31.75 dB
Low	Low	High	High	High	Low	High	Low	14.50 dB (example)

Table 5. SKY12343-364LF Serial Mode Address Word Truth Table

Bit A7 (MSB)	Bit A6	Bit A5	Bit A4	Bit A3	Bit A2 (Pin 21)	Bit A1 (Pin 22)	Bit A0 (Pin 4, LSB)	Address Setting
X	X	X	X	X	Low	Low	Low	000
X	X	X	X	X	Low	Low	High	001
X	X	X	X	X	Low	High	Low	010
X	X	X	X	X	Low	High	High	011
X	X	X	X	X	High	Low	Low	100
X	X	X	X	X	High	Low	High	101
X	X	X	X	X	High	High	Low	110
X	X	X	X	X	High	High	High	111

X = Don't care bit

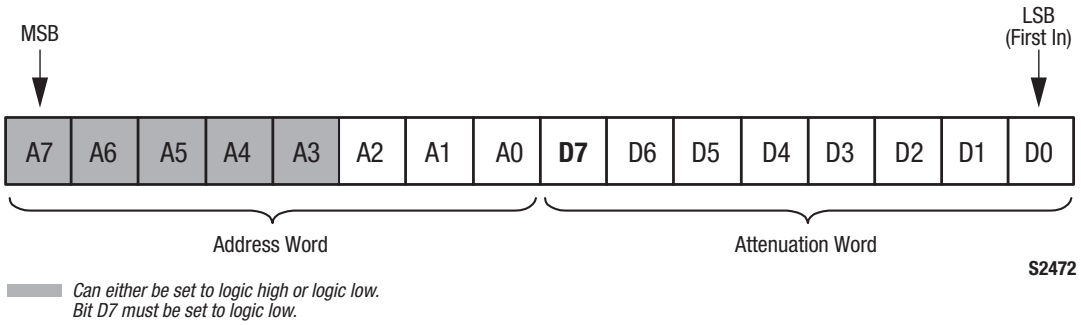


Figure 3. SKY12343-364LF Serial Addressable Register Map

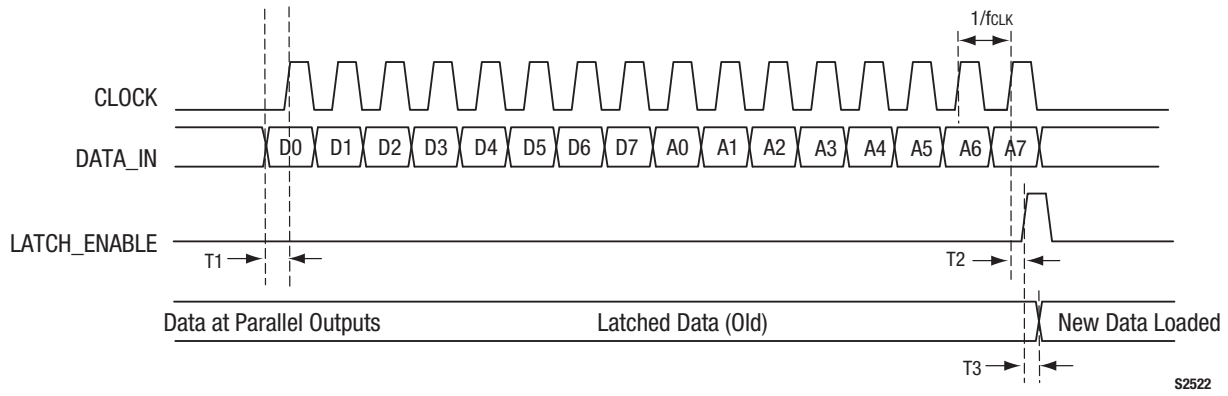


Figure 4. Power-Up/Power-Down Timing

Table 6. Power-Up/Power-Down Timing Parameters (V_{DD} = 3.3 V ~ 5.0 V)

Parameter	Symbol	Minimum	Maximum	Units
Serial input setup time	T1	10		ns
Setup time from shift clock to latch enable	T2	10		ns
Internal propagation delay, latch enable to parallel outputs	T3	10		ns
Serial clock frequency	f_{CLK}		10	MHz

Table 7. SKY12343-364LF Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Typical	Maximum	Units
Supply voltage	V_{DD}	3.0	5.0	+6.0	V
Control voltage	V_{CTL}	0	5	V_{DD}	V
RF input power	P_{IN}			+25	dBm
Storage temperature	T_{STG}	-65		+150	°C
Operating temperature	T_{OP}	-40		+85	°C
Electrostatic discharge: Human Body Model (HBM), Class 1C	ESD	1000		2000	V

1 Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***ESD HANDLING**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 8. SKY12343-364LF Electrical Specifications[1]
(T_{OP} = +25 °C, V_{DD} = 3.3 to 5.0 V, V_{CTL} = 3.3 V to V_{DD}, Characteristic Impedance [Z_0] = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
RF Specifications						
Insertion loss	IL	0.01 to 1.5 GHz 1.5 to 3.0 GHz		1.8 1.9	2.0 3.0	dB dB
Attenuation range	Attn	0.01 to 4.0 GHz		0.25	31.75	dB
Attenuation accuracy		0.01 to 3.0 GHz: 0 dB to 7.75 dB Attn 8 dB to 31.75 dB Attn 3.0 to 4.0 GHz: 0 dB to 31.75 dB Attn			 ±(0.20 + 1.5%) ±(0.15 + 5%) ±(0.25 + 4.5%)	 dB dB dB
Return loss	RL	0.01 to 4.0 GHz		18		dB
Relative phase	PH	0.01 to 4.0 GHz		44		deg
1 dB input compression point	IP1dB	0.5 MHz to 3.0 GHz: IL state, V_{DD} = 5 V Attn states, V_{DD} = 5 V IL state, V_{DD} = 3.3 V Attn states = V_{DD} = 3.3 V		 +35 +27 +30 +24		 dBm dBm dBm dBm
0.1 dB input compression point	IP0.1dB	0.5 MHz to 3.0 GHz: IL state, V_{DD} = 5 V Attn states, V_{DD} = 5 V IL state, V_{DD} = 3.3 V Attn states = V_{DD} = 3.3 V		 +32 +26 +26 +23		 dBm dBm dBm dBm
Third order input intercept point	IIP3	0.5 to 3.0 GHz, two tones @ +18 dBm, 20 MHz spacing: V_{DD} = 5 V V_{DD} = 3.3 V		 +50 +42		 dBm dBm
Typical spurious value		0.01 to 0.1 GHz 0.1 to 4.0 GHz		-120 -125		dBm dBm
Video feedthrough	$V_{\_FD}$	V_{DD} = 3.0 V, Bit= 3.0 V V_{DD} = 3.3 V, Bit= 3.3 V V_{DD} = 5.0 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 5.0 V		23 26 37 37		mVpp mVpp mVpp mVpp
OFF → ON switching time 50% CTRL → 90%	$t_{\_ON}$	V_{DD} = 3.0 V, Bit= 3.0 V V_{DD} = 3.3 V, Bit= 3.3 V V_{DD} = 5.0 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 5.0 V		53 47 52 53		nSec nSec nSec nSec
ON → OFF switching time 50% CTRL → 10%	$t_{\_OFF}$	V_{DD} = 3.0 V, Bit= 3.0 V V_{DD} = 3.3 V, Bit= 3.3 V V_{DD} = 5.0 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 5.0 V		93 71 42 40		nSec nSec nSec nSec
OFF → ON rise time 10% → 90%	$t_{\_RISE}$	V_{DD} = 3.0 V, Bit= 3.0 V V_{DD} = 3.3 V, Bit= 3.3 V V_{DD} = 5.0 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 5.0 V		12 13 24 24		nSec nSec nSec nSec
ON → OFF fall time 90% → 10%	$t_{\_FALL}$	V_{DD} = 3.0 V, Bit= 3.0 V V_{DD} = 3.3 V, Bit= 3.3 V V_{DD} = 5.0 V, Bit = 3.3 V V_{DD} = 5.0 V, Bit = 5.0 V		21 18 13 13		nSec nSec nSec nSec

[1] Performance is guaranteed only under the conditions listed in this table.

Typical Performance Characteristics

(TOP = +25 °C, VDD = 3.3 V, VCTL = 3.3 V, Characteristic Impedance [Zo] = 50 Ω, VDD = 5 V, Unless Otherwise Noted)

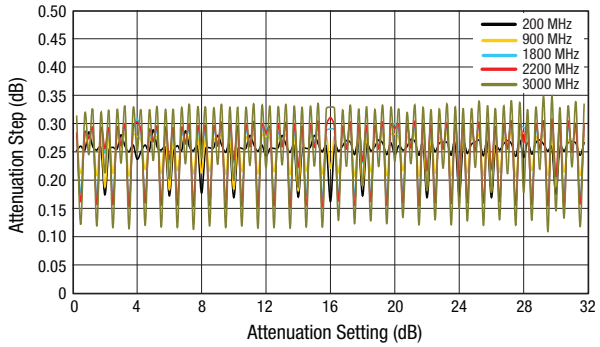


Figure 5. Attenuation Step vs Attenuation Setting

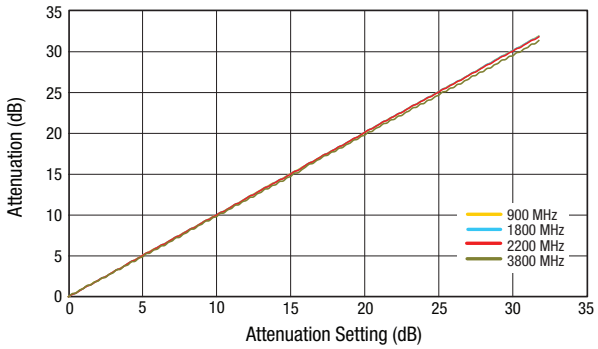


Figure 6. Attenuation vs Attenuation Setting

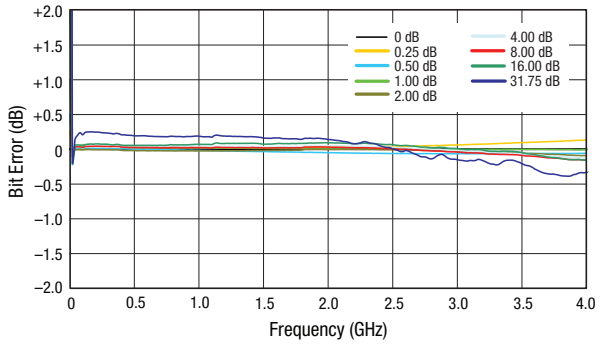


Figure 7. Major State Bit Error vs Frequency

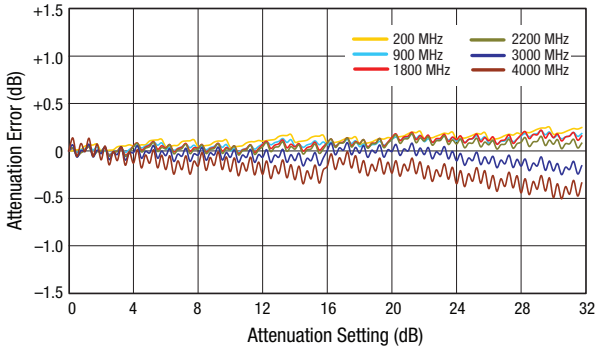


Figure 8. Attenuation Error vs Attenuation Setting

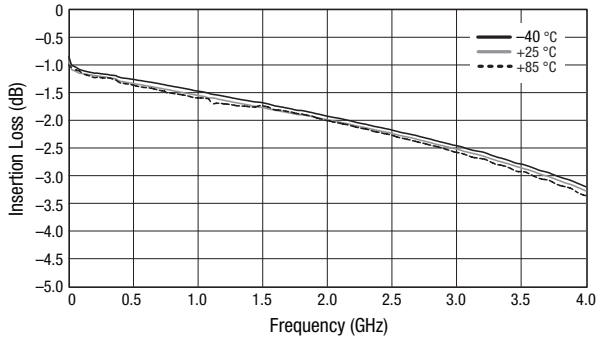


Figure 9. Insertion Loss vs Frequency

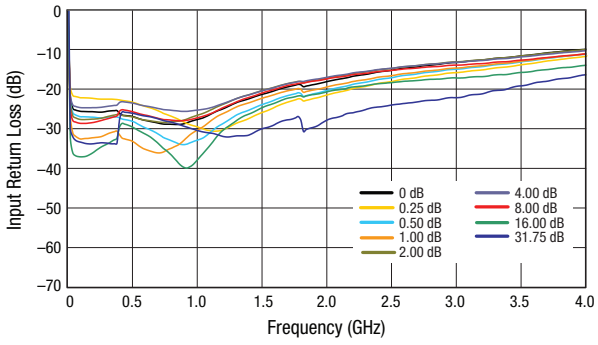


Figure 10. Input Return Loss vs Frequency

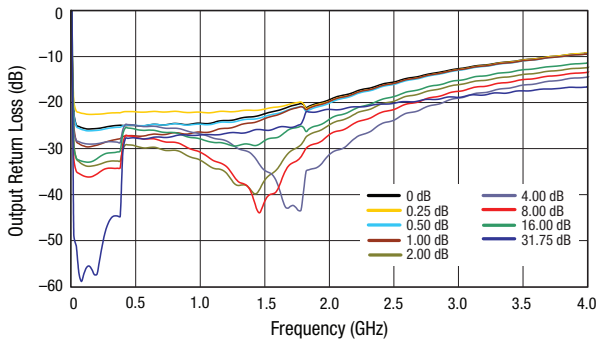


Figure 11. Output Return Loss vs Frequency

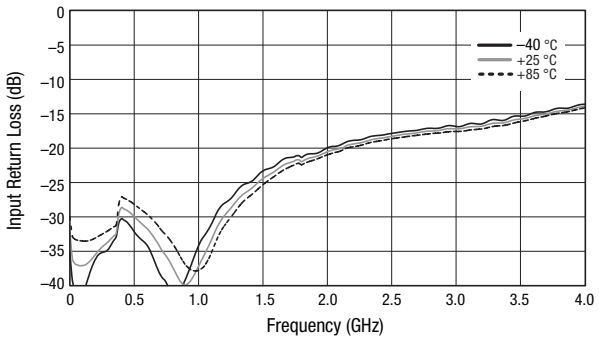


Figure 12. Input Return Loss (16 dB State) vs Frequency

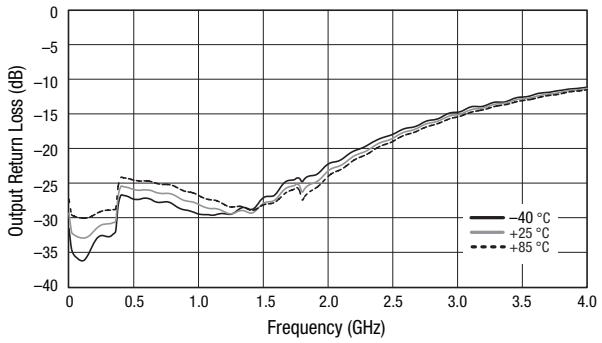


Figure 13. Output Return Loss (16 dB State) vs Frequency

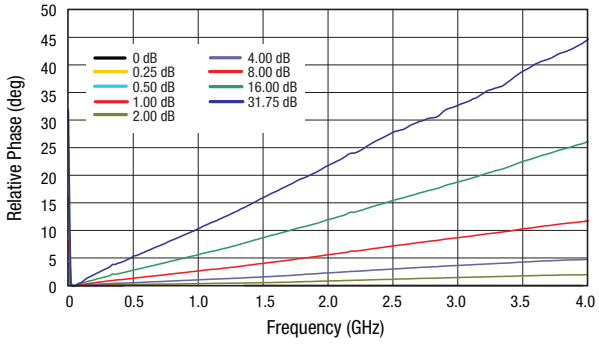


Figure 14. Relative Phase vs Frequency

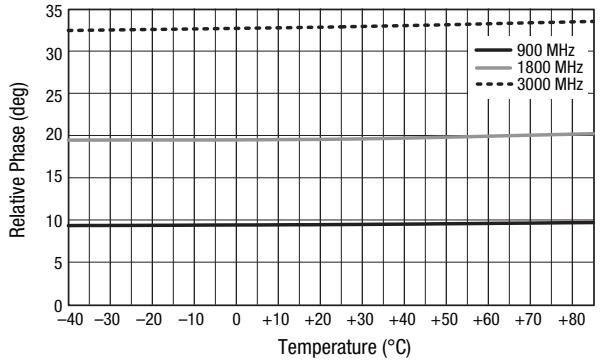


Figure 15. Relative Phase (31.75 dB State) vs Temperature

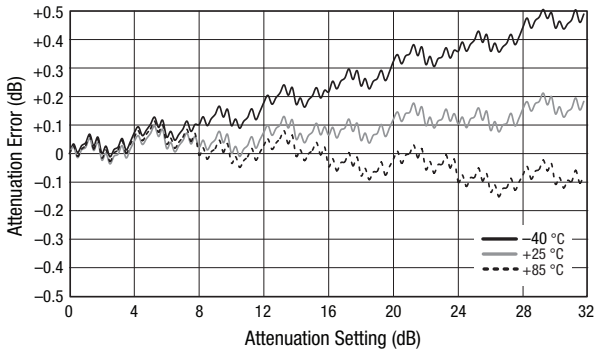


Figure 16. Attenuation Error vs Attenuation Setting @ 900 MHz

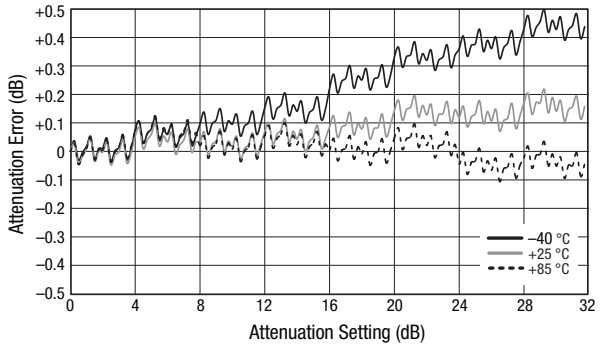


Figure 17. Attenuation Error vs Attenuation Setting @ 1800 MHz

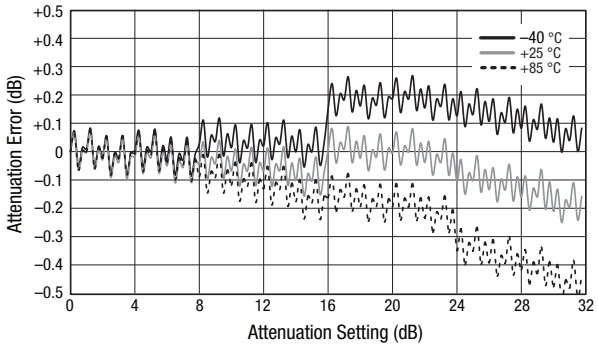


Figure 18. Attenuation Error vs Attenuation Setting @ 3000 MHz

Evaluation Board Description

The SKY12343-364LF Evaluation Board is used to test the performance of the SKY12343-364LF digital attenuator. An assembly drawing for the Evaluation Board is shown in Figure 19 and an Evaluation Board schematic diagram is shown in Figure 20. Table 9 provides the Evaluation Board Bill of Materials (BOM) list.

Package Dimensions

The PCB layout footprint for the SKY12343-364LF is shown in Figure 21. Typical part markings are noted in Figure 22. Package dimensions are shown in Figure 23, and tape and reel dimensions are provided in Figure 24.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY12343-364LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

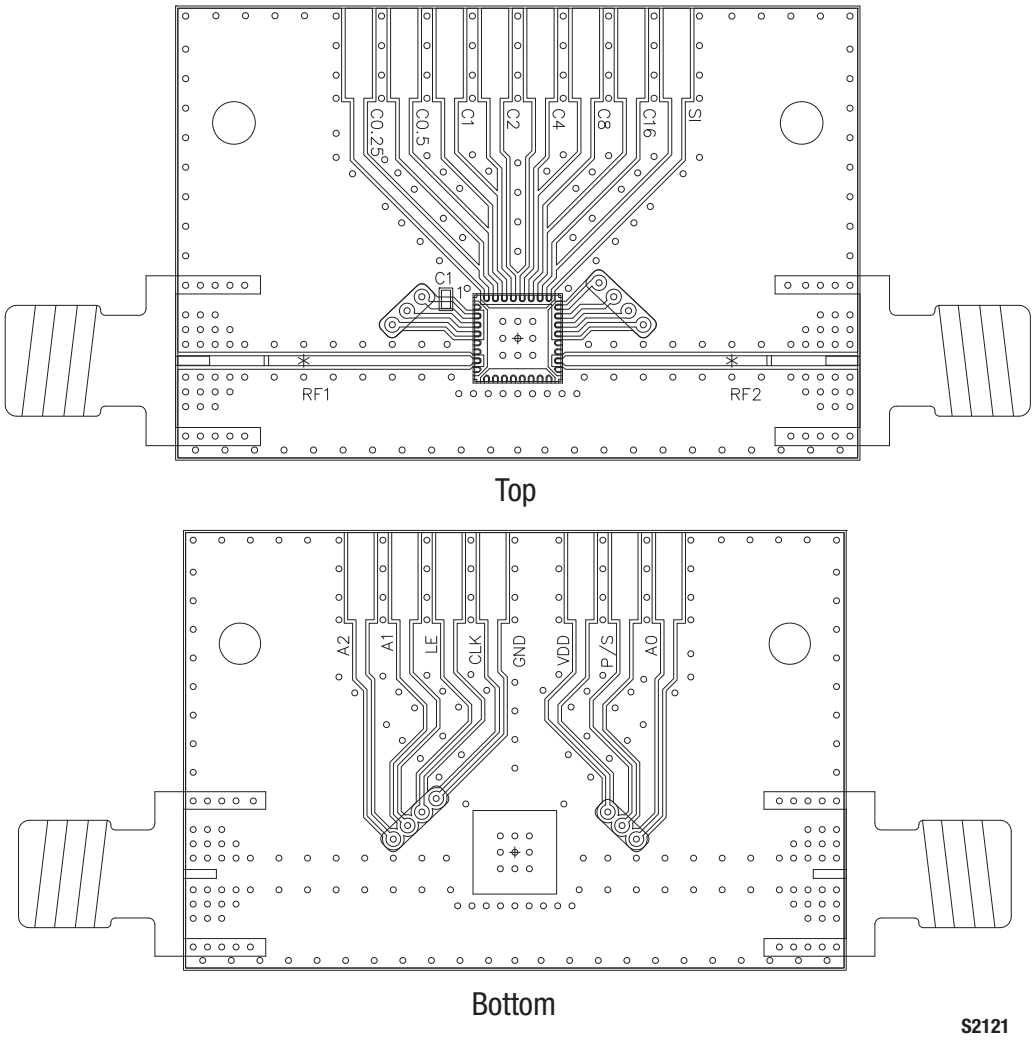


Figure 19. SKY12343-364LF Evaluation Board Assembly Diagram

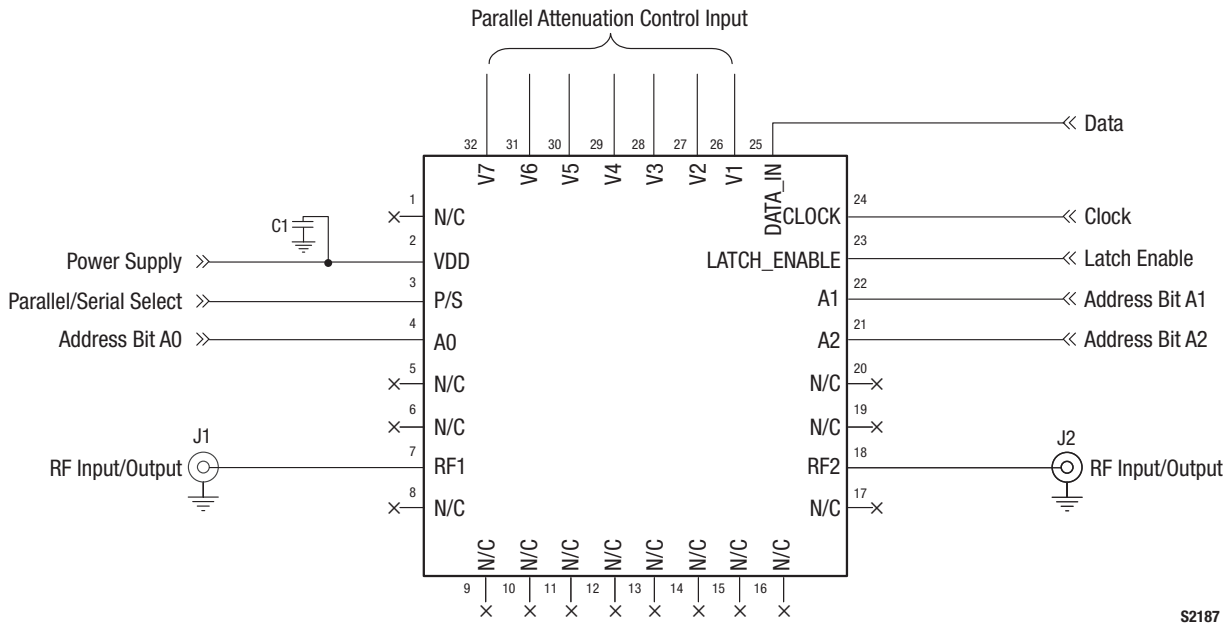


Figure 20. SKY12343-364LF Evaluation Board Schematic Diagram

Table 9. Recommended Evaluation Board Bill of Materials

Component	Value	Size	Manufacturer
C1	0.01 µF	0402	Murata

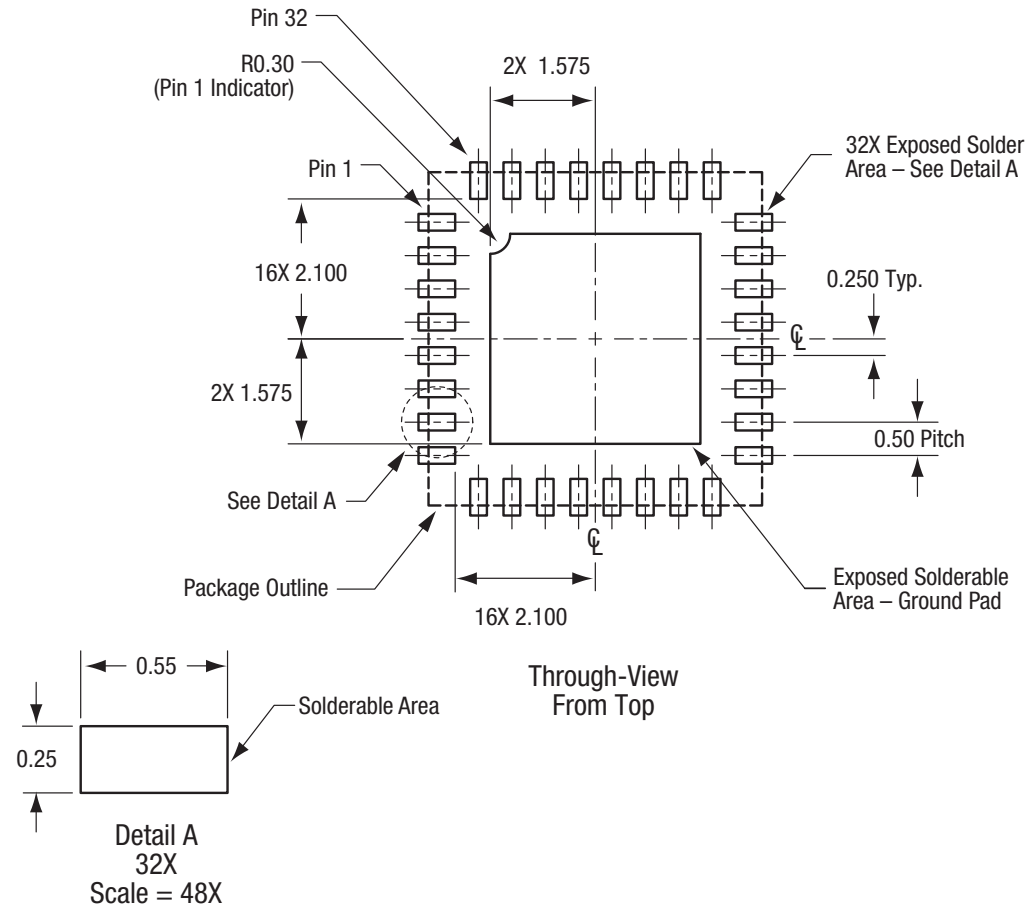


Figure 21. SKY12343-364LF PCB Layout Footprint

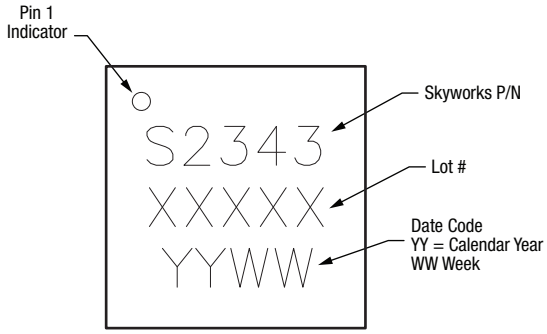
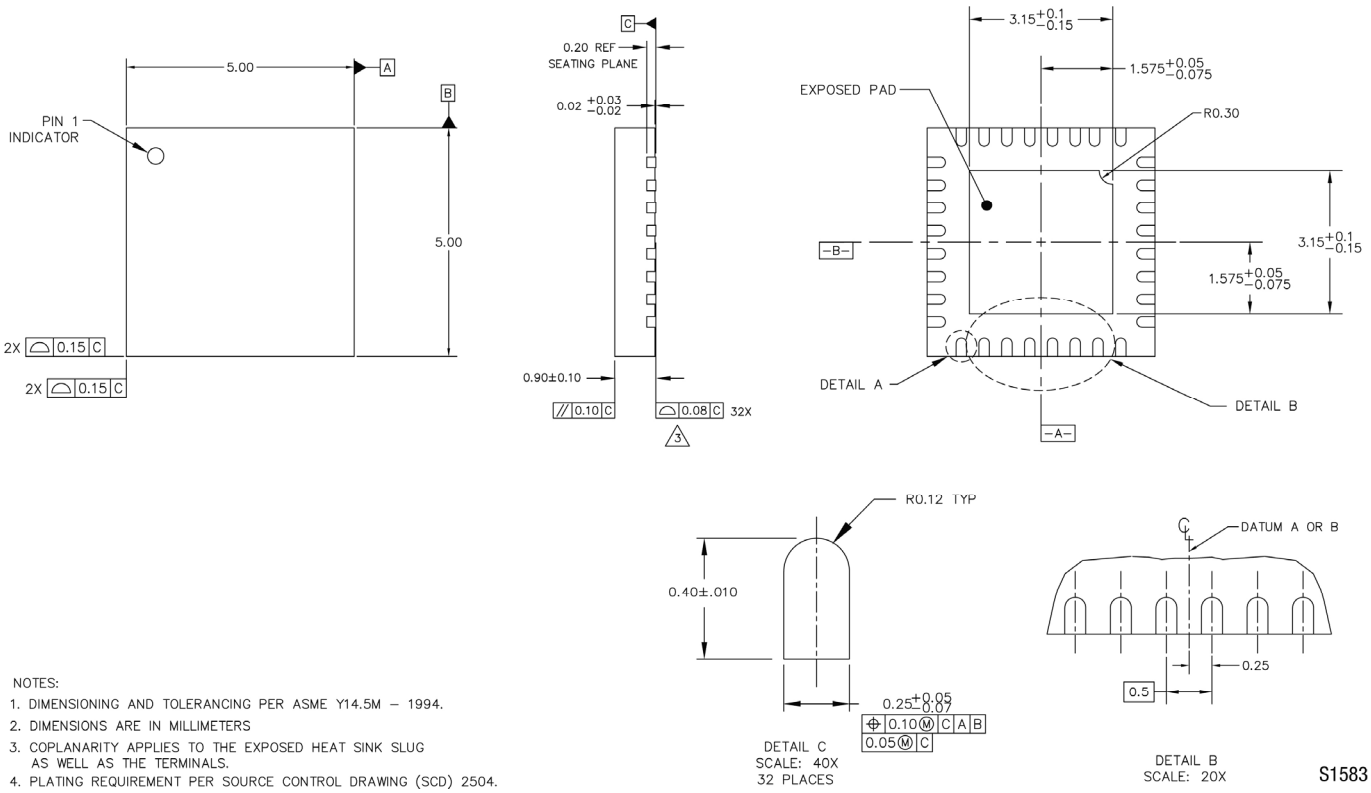
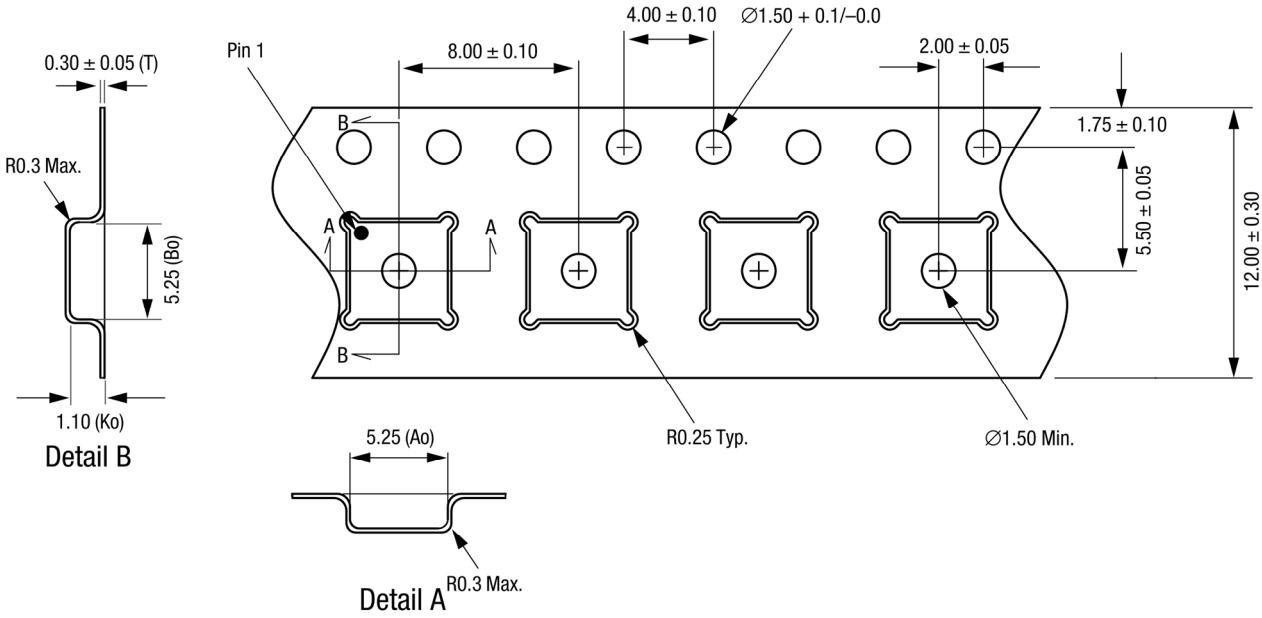


Figure 22. Typical Part Markings



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. DIMENSIONS ARE IN MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
4. PLATING REQUIREMENT PER SOURCE CONTROL DRAWING (SCD) 2504.

Figure 23. SKY12343-364LF Package Dimensions



Notes:
1. *Carrier tape: black conductive polystyrene, non-bakeable material.*
2. *Cover tape material: transparent conductive HSA.*
3. *Cover tape size: 9.20 mm width.*
4. *ESD-surface resistivity is ≥1 x 10^5 ~ ≤1 x 10^{10} Ohms/square per EIA, JEDEC TNR Specification.*
5. *All measurements are in millimeters.*

S1602

Figure 24. SKY12343-364LF Tape and Reel Dimensions

Ordering Information

Part Number	Product Description	Evaluation Board Part Numbers
SKY12343-364LF	0.01 to 4.0 GHz Seven-Bit Digital Attenuator with Serial and Parallel Drivers	SKY12343-364LF-EVB